Water Level Indicator System
(Digital Logic Design)

University of Science and Technology (UST), Zewail City

1 Project Specifications & Objectives

- **Project Goal:** To design and implement a digital logic circuit that functions as a 4-level water indicator.
- **Design Methodology:** The system is built using pure combinational logic and discrete logic gates, demonstrating core hardware design principles without the use of microcontrollers.
- **Core Functionality:** The system uses four conductive sensors (W1, W2, W3, W4) placed at varying heights. As water contacts each sensor, the corresponding LEDs light up cumulatively.
- **Cumulative Logic:** Once an LED turns on, it remains on for all higher water levels, providing a clear visual representation of the tank's volume.

2 System Architecture

The system consists of 4 inputs and 4 outputs:

- **Inputs (W1 - W4):** Water level sensors (Logic HIGH when water is detected).
- **Outputs (L1 - L4):** Three indicator LEDs and one high-level indicator (L4) coupled with a Buzzer.

2.1 Truth Table

The following table illustrates the desired output logic for the sensor states:

W4	W3	W2	W1	L1	L2	L3	L4
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	1	1	1	0	0
0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1

3 Logical Optimization (Karnaugh Maps)

Karnaugh Maps (K-Maps) were used to minimize the logic gate count and derive the most efficient Boolean expressions for the hardware.

3.1 L1 Map

W3W4 \ W1W2	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

3.2 L2 Map

W3W4 \ W1W2	00	01	11	10
00	0	0	1	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

4 Boolean Equations

Based on the K-Map simplifications, the following logic was implemented:

- **Level 1 Output:** $L1 = W1 + W2 + W3 + W4$
- **Level 2 Output:** $L2 = (W1 \cdot W2) + W3 + W4$
- **Level 3 Output:** $L3 = (W1 \cdot W2 \cdot W4) + W3$
- **Level 4 Output (Buzzer):** $L4 = W1 \cdot W2 \cdot W3 \cdot W4$

5 Circuit Implementation

5.1 Logical Schematic

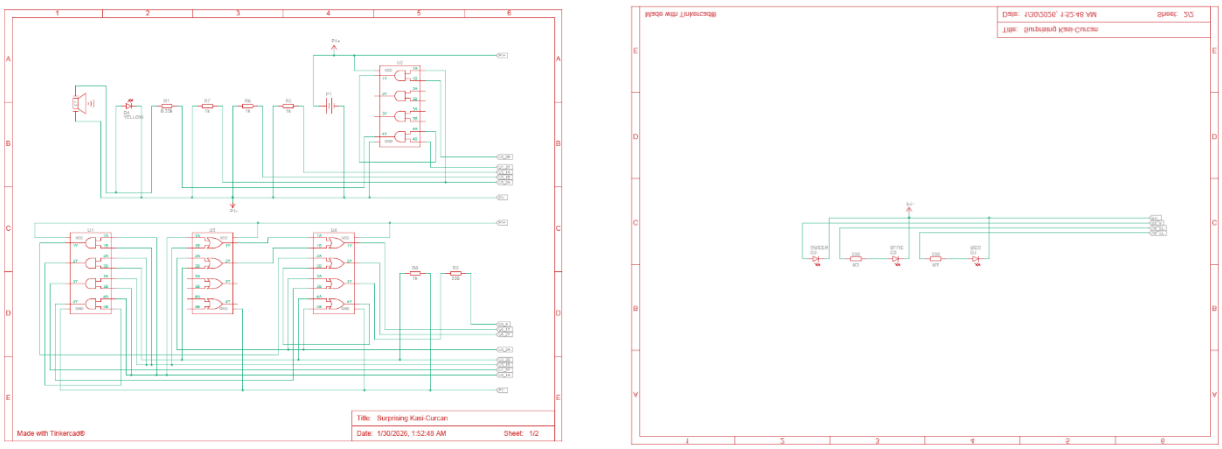

Figure 1&2: Logical Diagram for the 4-level indicator.

5.2 Breadboard Simulation & Hardware

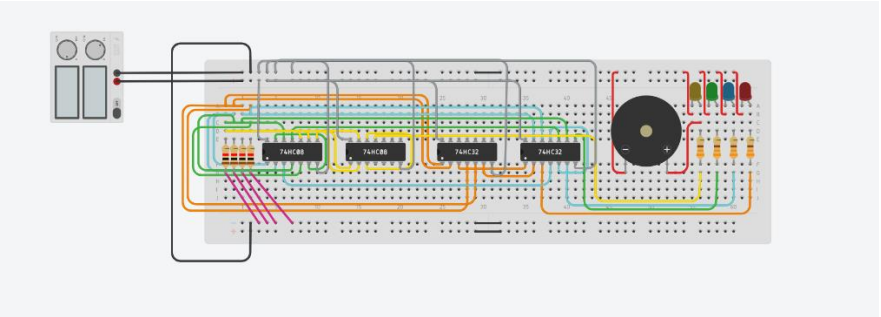

Figure 3: Breadboard Simulation layout.

The physical implementation was modeled using breadboard simulations with the following Integrated Circuits (ICs):

- **74HC08:** Quad 2-input AND gates used for level intersections.
- **74HC32:** Quad 2-input OR gates used for signal summation.
- **Active Buzzer:** Triggered by L4 to provide an audible overflow alarm.