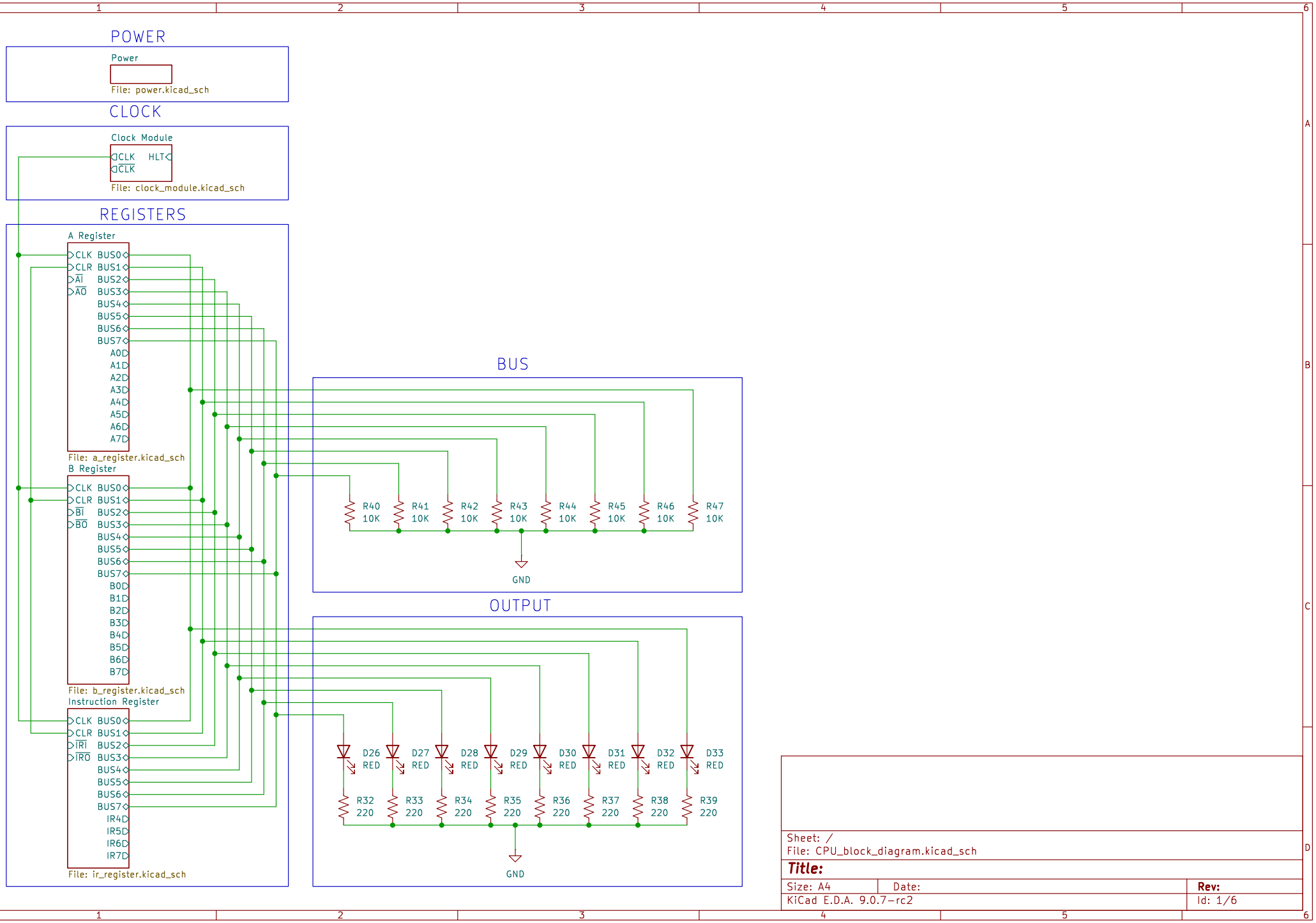
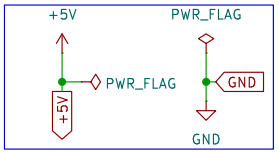

POWER
Power
File: power.kicad_sch
CLOCK
Clock Module
CLK
HLT
CLK
File: clock_module.kicad_sch
REGISTERS
A Register
CLK BUS0
CLR BUS1
AI BUS2
AO BUS3
BUS4
BUS5
BUS6
BUS7
A0D
A1D
A2D
A3D
A4D
A5D
A6D
A7D
File: a_register.kicad_sch
B Register
CLK BUS0
CLR BUS1
BI BUS2
BO BUS3
BUS4
BUS5
BUS6
BUS7
B0D
B1D
B2D
B3D
B4D
B5D
B6D
B7D
File: b_register.kicad_sch
Instruction Register
CLK BUS0
CLR BUS1
IRI BUS2
IRO BUS3
BUS4
BUS5
BUS6
BUS7
IR4D
IR5D
IR6D
IR7D
File: ir_register.kicad_sch
BUS
R40 10K
R41 10K
R42 10K
R43 10K
R44 10K
R45 10K
R46 10K
R47 10K
GND
OUTPUT
D26 RED
D27 RED
D28 RED
D29 RED
D30 RED
D31 RED
D32 RED
D33 RED
R32 220
R33 220
R34 220
R35 220
R36 220
R37 220
R38 220
R39 220
GND
Sheet: /
File: CPU_block_diagram.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 9.0.7-rc2
Id: 1/6



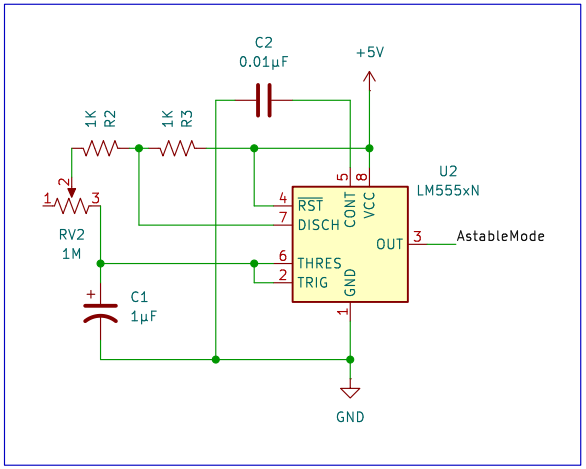
Simple Power Lable

Sheet: /Power/
File: power.kicad_sch

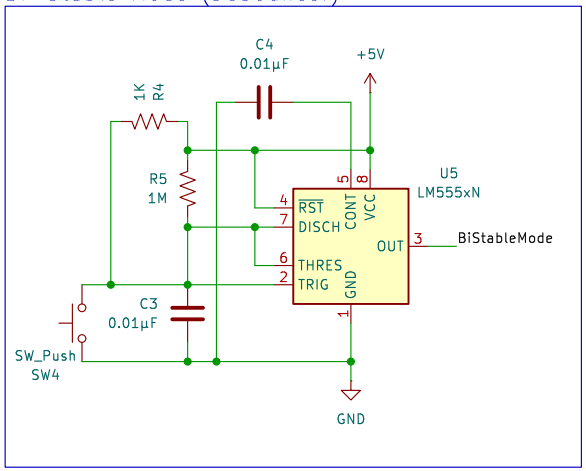
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.7-rc2		Id: 2/6

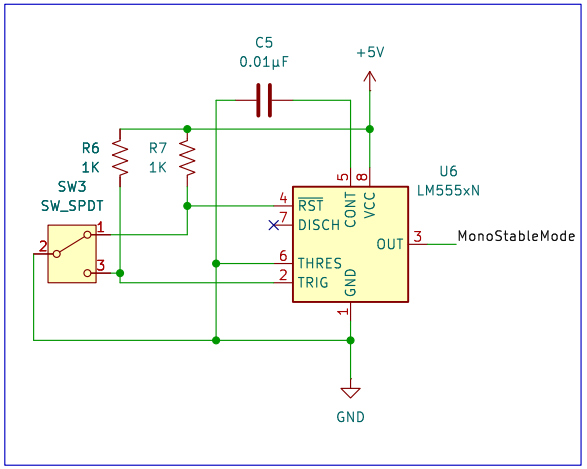
Astable Mode



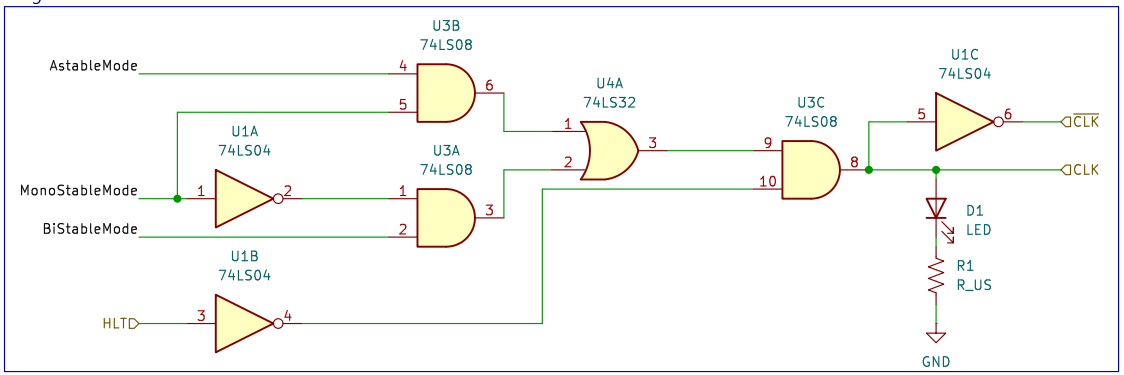
Bi-Stable Mode (Debouncer)



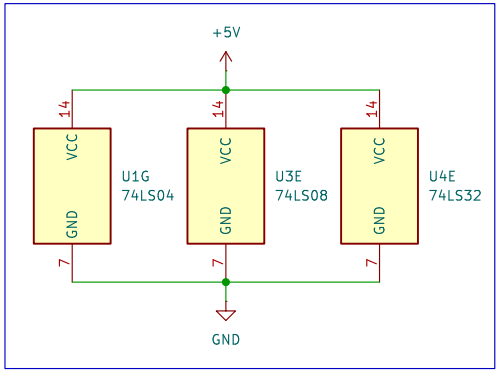
Mono-Stable Mode



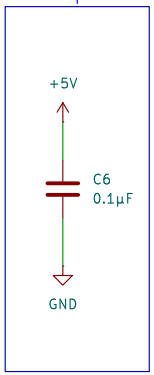
Logic



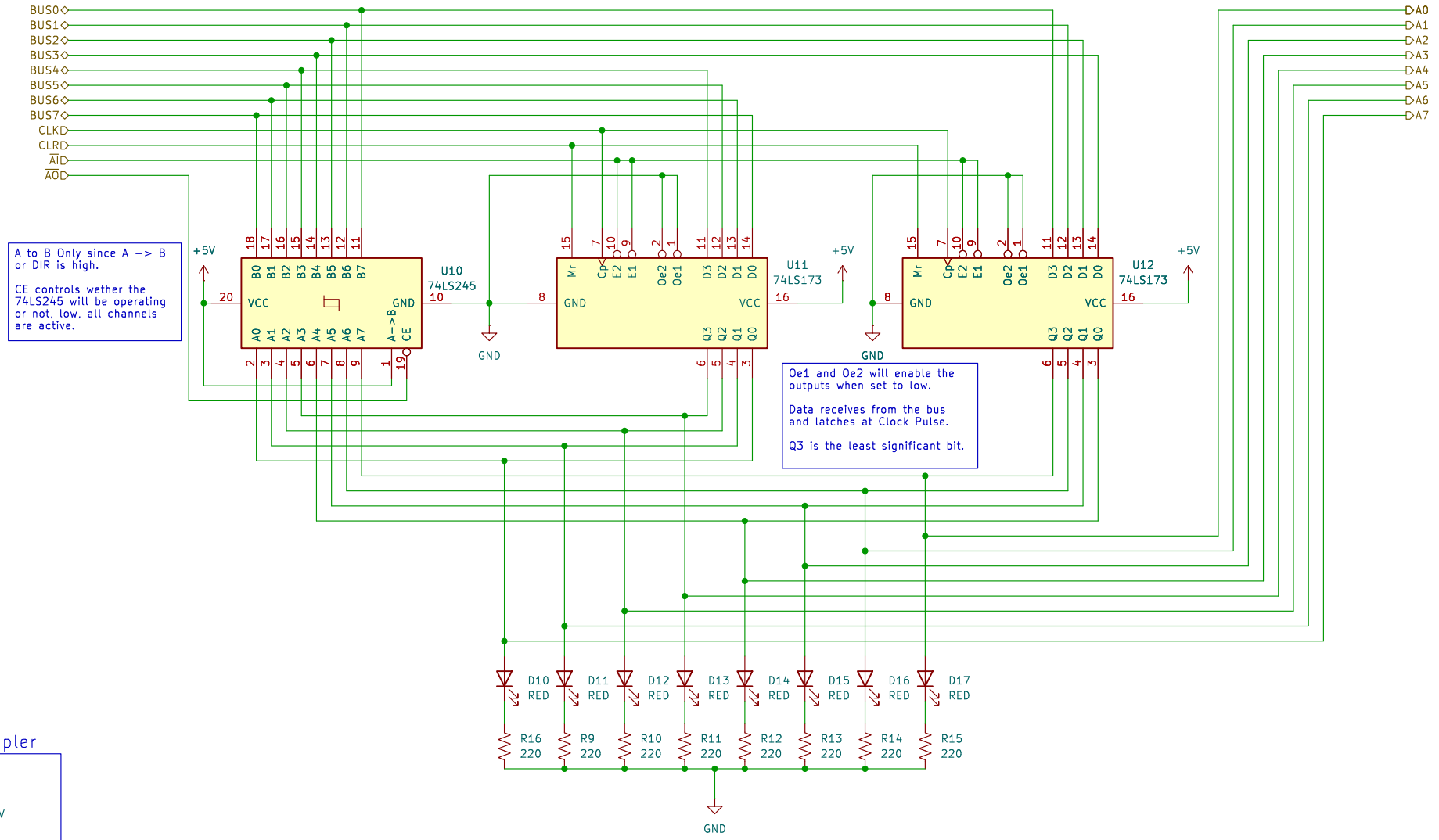
Logic Power



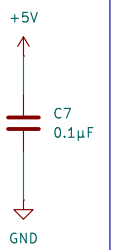
Decoupler



Sheet: /Clock Module/		
File: clock_module.kicad_sch		
Title: Clock_Module		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.7-rc2		Id: 3/6



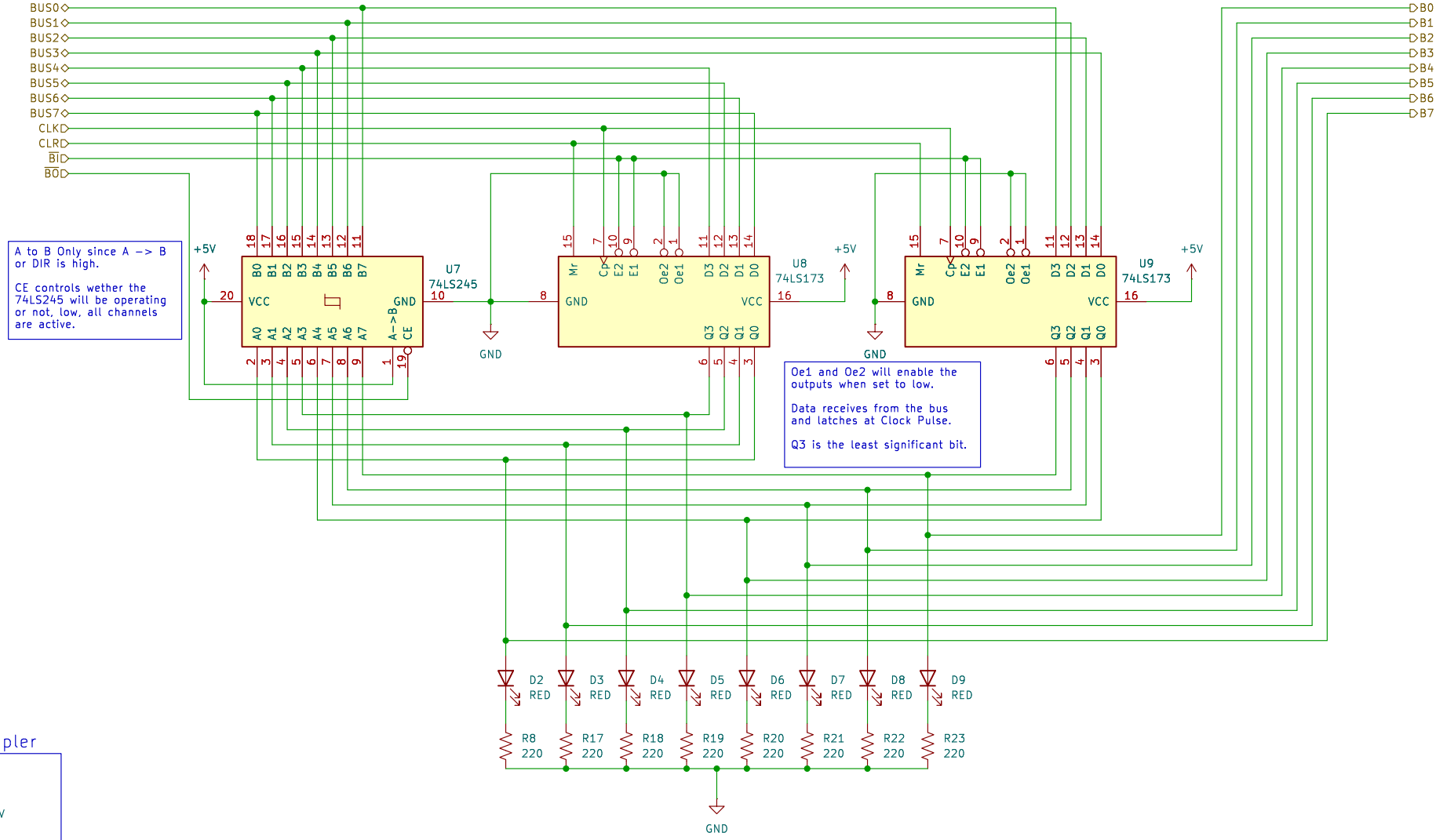
Decoupler



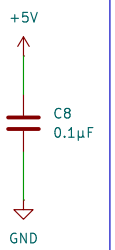
Sheet: /A Register/
File: a_register.kicad_sch

Title: Register_A

Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.7-rc2		Id: 4/6



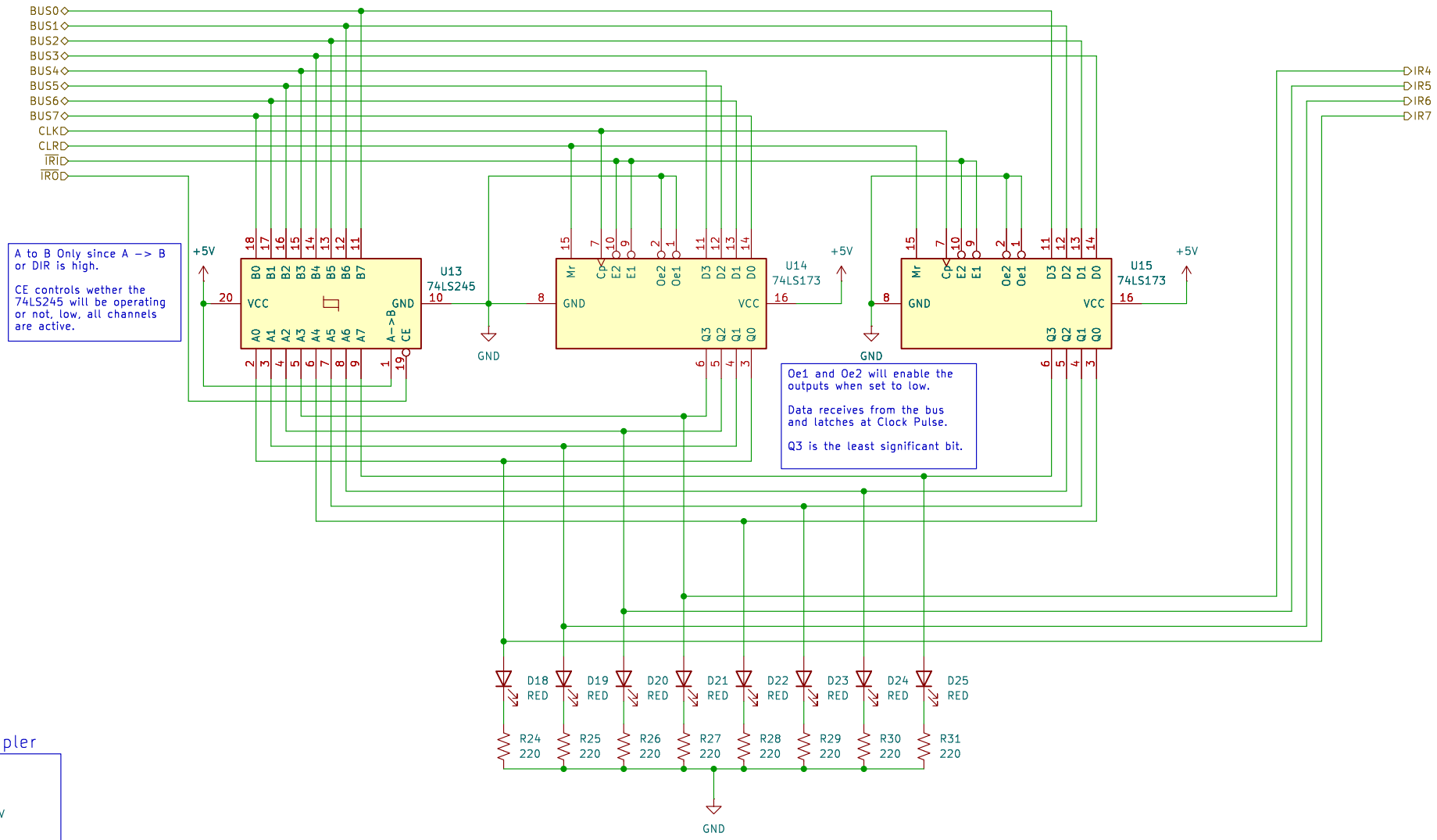
Decoupler



Sheet: /B Register/
File: b_register.kicad_sch

Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. 9.0.7-rc2 | Id: 5/6



Sheet: /Instruction Register/		
File: IR_register.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.7-rc2		Id: 6/6