Lab 3: Full Subtractor Implementation and Testing

Your Name

March 2, 2025

1 Introduction

This lab focuses on the design, implementation, and testing of a 1-bit full subtractor using Verilog HDL. A full subtractor is a combinational circuit that performs subtraction of three binary digits: minuend (A), subtrahend (B), and borrow-in (Bin). The circuit produces two outputs: difference (diff) and borrow-out (Bout).

2 Design Approach

The full subtractor is implemented using a hierarchical design approach with the following components:

- Half Subtractor module
- Full Subtractor module (using two half subtractors)

2.1 Half Subtractor

The half subtractor is the basic building block that subtracts two bits and produces a difference and borrow output. The logic equations for the half subtractor are:

$$\text{diff} = A \oplus B \text{ (XOR)}$$
$$\text{borrow} = \overline{A} \cdot B \text{ (AND with NOT)}$$

2.2 Full Subtractor

The full subtractor is constructed using two half subtractors and an OR gate. The first half subtractor subtracts B from A, and the second half subtractor subtracts the borrow-in (Bin) from the difference of the first stage. The final borrow-out is the OR of the borrows from both half subtractors.

3 Implementation

3.1 Verilog Code

3.1.1 Half Subtractor Module

```
module halfSubtractor(op1, op2, diff, borrow);
    input op1, op2;
    output diff, borrow;

    assign diff = op1 ^ op2;
    assign borrow = op1 & !op2;
endmodule
```

3.1.2 Full Subtractor Module

```
module fullSubtractor(A, B, Bin, diff, Bout);
    input A, B, Bin;
    output diff, Bout;

    wire c, d, e, f;

    halfSubtractor u1(A, B, c, d);
    halfSubtractor u2(c, Bin, diff, f);
    assign Bout = f | d;
endmodule
```

4 Testing Strategy

The testbench implements a comprehensive testing approach by:

- Testing all possible input combinations (8 test cases)

- Using appropriate time delays between test cases
- Generating waveform output for verification

4.1 Test Cases

The following test cases were implemented:

A	B	Bin	diff	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

5 Results and Analysis

[This section will be completed after running the simulation and analyzing the results]

6 Conclusion

[This section will summarize the lab findings and learning outcomes]