# Lab Report CSE4010 Computer Architecture

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Lab: Lab 3 - Full Adder and Full Subtractor Implementation

Score: /10
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## Report

- How can addition and subtraction of large numbers be performed by computers if they are only aware of numbers 0 and 1?
  - Computers perform arithmetic operations on large numbers by breaking them down into binary digits and processing them one bit at a time. For multi-digit numbers:
    - \* Addition is performed using full adders in cascade, where each full adder processes one bit position and handles the carry from the previous stage
    - \* Subtraction is similarly performed using full subtractors in cascade, where each subtractor handles one bit position and processes the borrow from the previous stage
    - \* The carry/borrow propagation between stages allows for handling numbers of any size
  - This binary arithmetic is implemented using combinational circuits that:
    - \* Process bits from least significant to most significant position
    - \* Use carry/borrow propagation for managing digit transitions
    - \* Can be extended to any number of bits by cascading multiple stages

## Source Code

## fullAdder.v

```
module fullAdder(
       input A,
2
       input B,
3
       input Cin,
       output sum,
       output Cout
  );
7
       wire sum1, carry1, carry2;
       // First half adder
11
       assign sum1 = A ^ B;
12
       assign carry1 = A & B;
13
14
       // Second half adder
15
       assign sum = sum1 ^ Cin;
16
       assign carry2 = sum1 & Cin;
17
18
       // Final carry output
19
       assign Cout = carry1 | carry2;
20
21
  endmodule
```

## fullAdder\_tb.v

```
'timescale 1ns/1ns
   'include "fullAdder.v"
2
3
   module fullAdder_tb;
4
       reg A, B, Cin;
5
       wire sum, Cout;
        fullAdder uut(
            .A(A),
9
             .B(B),
10
            .Cin(Cin),
11
            .sum(sum),
12
             .Cout(Cout)
13
       );
14
15
        initial begin
16
            $dumpfile("fullAdder_tb.vcd");
17
            $dumpvars(0, fullAdder_tb);
18
19
            // Test all input combinations
20
            A = 0; B = 0; Cin = 0; #20;
21
            A = 0; B = 0; Cin = 1; #20;
22
            A = 0; B = 1; Cin = 0; #20;
23
            A = 0; B = 1; Cin = 1; #20;
24
            A = 1; B = 0; Cin = 0; #20;
25
            A = 1; B = 0; Cin = 1; #20;
26
            A = 1; B = 1; Cin = 0; #20;
27
            A = 1; B = 1; Cin = 1; #20;
28
29
            $display("Test_Complete!");
            $finish;
31
       end
32
33
        initial begin
34
            monitor("Time=\%0d_{\square}A=\%b_{\square}B=\%b_{\square}Cin=\%b_{\square}sum=\%b_{\square}Cout=\%b",
35
                       $time, A, B, Cin, sum, Cout);
       end
37
   endmodule
```

## fullSubtractor.v

```
module fullSubtractor(
       input A,
2
       input B,
3
       input Bin,
4
       output diff,
       output Bout
  );
       wire diff1, borrow1, borrow2;
9
10
       // First half subtractor
11
       assign diff1 = A ^ B;
12
       assign borrow1 = !A & B;
13
14
       // Second half subtractor
15
       assign diff = diff1 ^ Bin;
16
       assign borrow2 = !diff1 & Bin;
17
       // Final borrow output
19
       assign Bout = borrow1 | borrow2;
20
21
  endmodule
```

#### fullSubtractor\_tb.v

```
'timescale 1ns/1ns
   'include "fullSubtractor.v"
2
3
  module fullSubtractor_tb;
       reg A, B, Bin;
       wire diff, Bout;
       fullSubtractor uut(
            .A(A),
            .B(B),
10
            .Bin(Bin),
11
            .diff(diff),
            .Bout(Bout)
13
       );
14
15
       initial begin
16
            $dumpfile("fullSubtractor_tb.vcd");
17
            $dumpvars(0, fullSubtractor_tb);
18
19
            // Test all input combinations
20
            A = 0; B = 0; Bin = 0; #20;
21
            A = 0; B = 0; Bin = 1; #20;
22
            A = 0; B = 1; Bin = 0; #20;
23
            A = 0; B = 1; Bin = 1; #20;
24
            A = 1; B = 0; Bin = 0; #20;
25
            A = 1; B = 0; Bin = 1; #20;
26
            A = 1; B = 1; Bin = 0; #20;
27
            A = 1; B = 1; Bin = 1; #20;
28
            $display("Test_Complete!");
30
            $finish;
31
       end
32
33
       initial begin
34
            monitor("Time=\%0d_A=\%b_B=\%b_Bin=\%b_diff=\%b_Bout=\%b",
                      $time, A, B, Bin, diff, Bout);
36
       end
37
   endmodule
38
```

## Screenshots

#### Part A - Full Adder Simulation

[Insert screenshot of full adder simulation waveform and results here]

#### Part B - Full Subtractor Simulation

[Insert screenshot of full subtractor simulation waveform and results here]