Lab Report
CSE4010 Computer Architecture

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Lab: Lab 3 - Full Adder and Full Subtractor Implementation

Report

- How can addition and subtraction of large numbers be performed by computers if they are only aware of numbers 0 and 1?
  - Computers perform arithmetic operations on large numbers by breaking them down into binary digits and processing them one bit at a time. For multi-digit numbers:
    - Addition is performed using full adders in cascade, where each full adder processes one bit position and handles the carry from the previous stage
    - Subtraction is similarly performed using full subtractors in cascade, where each subtractor handles one bit position and processes the borrow from the previous stage
    - The carry/borrow propagation between stages allows for handling numbers of any size
  - This binary arithmetic is implemented using combinational circuits that:
    - Process bits from least significant to most significant position
    - Use carry/borrow propagation for managing digit transitions
    - Can be extended to any number of bits by cascading multiple stages

Source Code

fullAdder.v

```
1 /*
2  * File: fullAdder.v
3  * Description: Implements a 1-bit full adder using half adders
4  * A full adder adds three bits (A, B, and carry-in) and produces
       sum and carry-out
5  * A full adder is built from two half adders and an OR gate;
6  * The first half adder adds A and B and produces a sum and a
     carry
```

```
 * The second half adder adds the carry from the first half adder to the carry-in
 * The OR gate adds the carries from the two half adders to produce the final carry-out
 */

// Half Adder Module - Adds two bits and produces sum and carry
module halfAdder(op1, op2, sum, carry);

    // Inputs - two 1-bit operands
    input op1, op2;
    // Outputs - sum and carry bits
    output sum, carry;

    // XOR operation - sum is 1 if either op1 or op2 is 1, but not both
    assign sum = op1 ^ op2; // ^ is the xor operator
    // AND operation - carry is 1 only if both op1 and op2 are 1
    assign carry = op1 & op2; // & is the and operator

endmodule

// Full Adder Module - Adds three bits (A, B, carry-in) and produces sum and carry-out
module fullAdder(A, B, Cin, sum, Cout);

    // Input ports
    input A, B, Cin;  // A and B are the bits to add, carryIn is the carry from previous addition
    // Output ports
    output sum, Cout; // sum is the result bit, carryOut propagates to next addition

    // Internal connections - wires to connect the half adders
    wire c;  // Sum output from first half adder
    wire d;  // Carry output from first half adder
    wire e;  // Sum output from second half adder
    wire f;  // Carry output from second half adder

    // First half adder - adds A and B
    halfAdder u1(A, B, c, d);
    // Second half adder - adds carryIn and the sum from first half adder
    halfAdder u2(Cin, c, e, f);

    // Final carry out is OR of both half adder carries
    assign Cout = f | d;  // | is the OR operator
    // Final sum is the sum output from second half adder
    assign sum = e;

endmodule
```

fullAdder_tb.v

```
/*
 * File: fullAdder_tb.v
 * Description: Testbench for the 1-bit full adder
 * Tests all possible input combinations (0-7) for A, B, carryIn
 * The testbench uses a loop to iterate through all possible input combinations
 * It displays the results of each test case
 */

// Define timescale for simulation: 1 nanosecond time unit, 1 nanosecond precision
`timescale 1 ns / 1 ns
// Include the module to be tested
`include "fullAdder.v"

// Testbench module - no external ports
module fullAdder_tb;

// Test inputs - declared as registers since they will be driven
reg A, B, Cin;
// Test outputs - declared as wires since they will be monitored
wire sum, Cout;

// Instantiate the Unit Under Test (UUT) - connect to test signals
fullAdder uut(A, B, Cin, sum, Cout);

// Test sequence
initial begin
    // Generate VCD file for waveform viewing
    $dumpfile("fullAdder_tb.vcd");
    // Dump variables from the testbench (0 means all variables)
    $dumpvars(0, fullAdder_tb);

    // Test case 0: A=0, B=0, Cin=0
    {A, B, Cin} = 3'd0; #20;
    // Test case 1: A=0, B=0, Cin=1
    {A, B, Cin} = 3'd1; #20;
    // Test case 2: A=0, B=1, Cin=0
    {A, B, Cin} = 3'd2; #20;
    // Test case 3: A=0, B=1, Cin=1
    {A, B, Cin} = 3'd3; #20;
    // Test case 4: A=1, B=0, Cin=0
    {A, B, Cin} = 3'd4; #20;
    // Test case 5: A=1, B=0, Cin=1
    {A, B, Cin} = 3'd5; #20;
    // Test case 6: A=1, B=1, Cin=0
    {A, B, Cin} = 3'd6; #20;
    // Test case 7: A=1, B=1, Cin=1
```

```
47      {A, B, Cin} = 3'd7; #20;
48      // Display a message to indicate completion of test cases
49      $display("Finished additions!");
50
51  end
52
53  endmodule
```

fullSubtractor.v

```
1   /*
2    * File: fullSubtractor.v
3    * Description: Implements a 1-bit full subtractor using half
       subtractors
4    * A full subtractor subtracts three bits (A, B, and borrow-in)
       and produces difference and borrow-out
5    * A full subtractor is built from two half subtractors and an OR
        gate;
6    * The first half subtractor subtracts B from A and produces a
       difference and a borrow
7    * The second half subtractor subtracts the borrow-in from the
       difference of the first half subtractor
8    * The OR gate combines the borrows from the two half subtractors
        to produce the final borrow-out
9    */
10
11  // Half Subtractor Module - Subtracts one bit from another and
      produces difference and borrow
12  module halfSubtractor(op1, op2, diff, borrow);
13
14      // Inputs - two 1-bit operands
15      input op1, op2;
16      // Outputs - difference and borrow bits
17      output diff, borrow;
18
19      // XOR operation - difference is 1 if op1 and op2 are
          different
20      assign diff = op1 ^ op2;
21
22      // AND operation with NOT on op2 - borrow is 1 if op1=1 and
          op2=0
23      assign borrow = op1 & !op2;
24
25  endmodule
26
27  // Full Subtractor Module - Subtracts three bits (A, B, borrow-in
      ) and produces difference and borrow-out
28  module fullSubtractor(A, B, Bin, diff, Bout);
29
30      // Input ports
```

```
    input A, B, Bin;  // A is minuend, B is subtrahend, Bin is borrow-in from previous subtraction
    // Output ports
    output diff, Bout; // diff is the difference bit, Bout propagates borrow to next subtraction

    // Internal connections - wires to connect the half subtractors
    wire c;  // Difference output from first half subtractor
    wire d;  // Borrow output from first half subtractor
    wire e;  // Difference output from second half subtractor (unused)
    wire f;  // Borrow output from second half subtractor

    // First half subtractor - subtracts B from A
    halfSubtractor u1(A, B, c, d);

    // Second half subtractor - subtracts Bin from the result of first half subtractor
    halfSubtractor u2(c, Bin, diff, f);

    // Final borrow out is OR of both half subtractor borrows
    assign Bout = f | d;  // | is the OR operator

endmodule
```

fullSubtractor_tb.v

```
/*
 * File: fullSubtractor_tb.v
 * Description: Testbench for the 1-bit full subtractor
 * Tests all possible input combinations (0-7) for A, B, Bin
 * The testbench uses a loop to iterate through all possible input combinations
 * It displays the results of each test case
 */

// Define timescale for simulation: 1 nanosecond time unit, 1 nanosecond precision
`timescale 1 ns / 1 ns
// Include the module to be tested
`include "fullSubtractor.v"

// Testbench module - no external ports
module fullSubtractor_tb;

// Test inputs - declared as registers since they will be driven
reg A, B, Bin;
// Test outputs - declared as wires since they will be monitored
wire diff, Bout;
```

```
21
22  // Instantiate the Unit Under Test (UUT) - connect to test
        signals
23  fullSubtractor uut(A, B, Bin, diff, Bout);
24
25  // Test sequence
26  initial begin
27      // Generate VCD file for waveform viewing
28      $dumpfile("fullSubtractor_tb.vcd");
29      // Dump variables from the testbench (0 means all variables)
30      $dumpvars(0, fullSubtractor_tb);
31
32      // Test case 0: A=0, B=0, Bin=0
33      {A, B, Bin} = 3'd0; #20;
34      // Test case 1: A=0, B=0, Bin=1
35      {A, B, Bin} = 3'd1; #20;
36      // Test case 2: A=0, B=1, Bin=0
37      {A, B, Bin} = 3'd2; #20;
38      // Test case 3: A=0, B=1, Bin=1
39      {A, B, Bin} = 3'd3; #20;
40      // Test case 4: A=1, B=0, Bin=0
41      {A, B, Bin} = 3'd4; #20;
42      // Test case 5: A=1, B=0, Bin=1
43      {A, B, Bin} = 3'd5; #20;
44      // Test case 6: A=1, B=1, Bin=0
45      {A, B, Bin} = 3'd6; #20;
46      // Test case 7: A=1, B=1, Bin=1
47      {A, B, Bin} = 3'd7; #20;
48      // Display a message to indicate completion of test cases
49      $display("Finished␣subtractions!");
50
51  end
52
53  endmodule
```

Screenshots

Part A - Full Adder Simulation

Part B - Full Subtractor Simulation

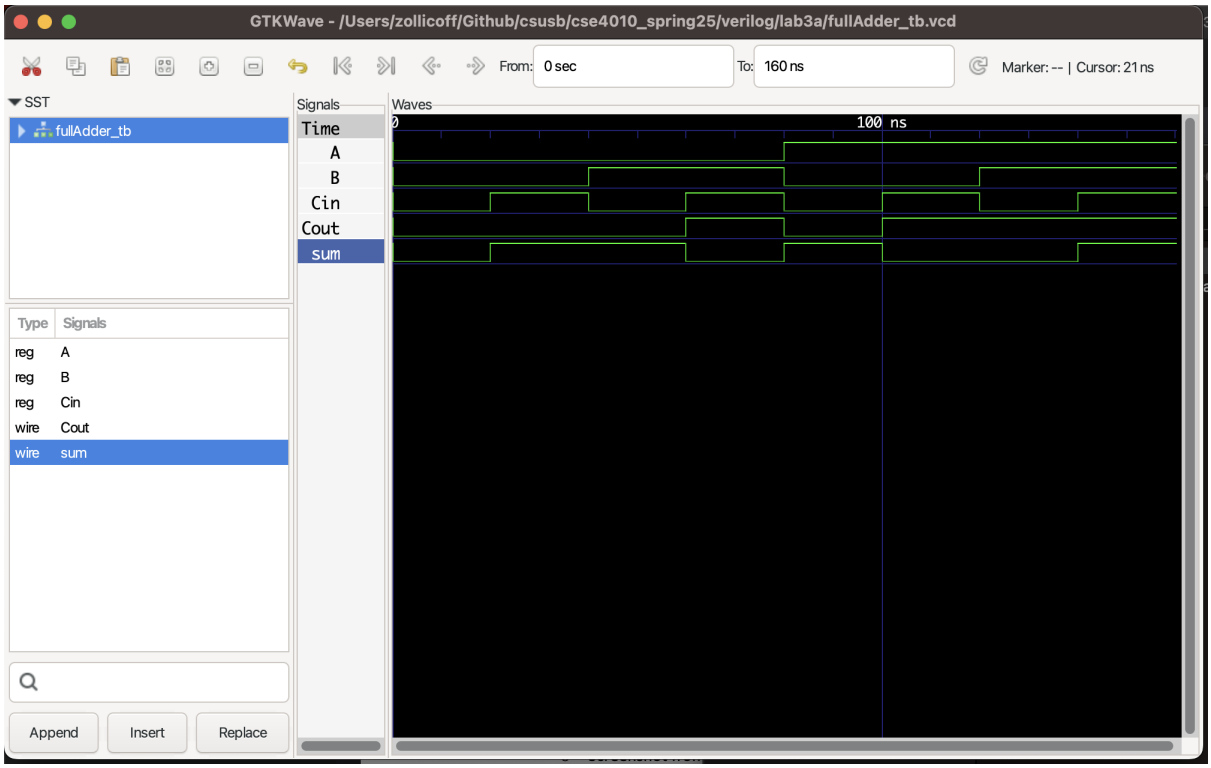

Figure 1: Full Adder Simulation Waveform showing all test cases with inputs A, B, Cin and outputs sum, Cout

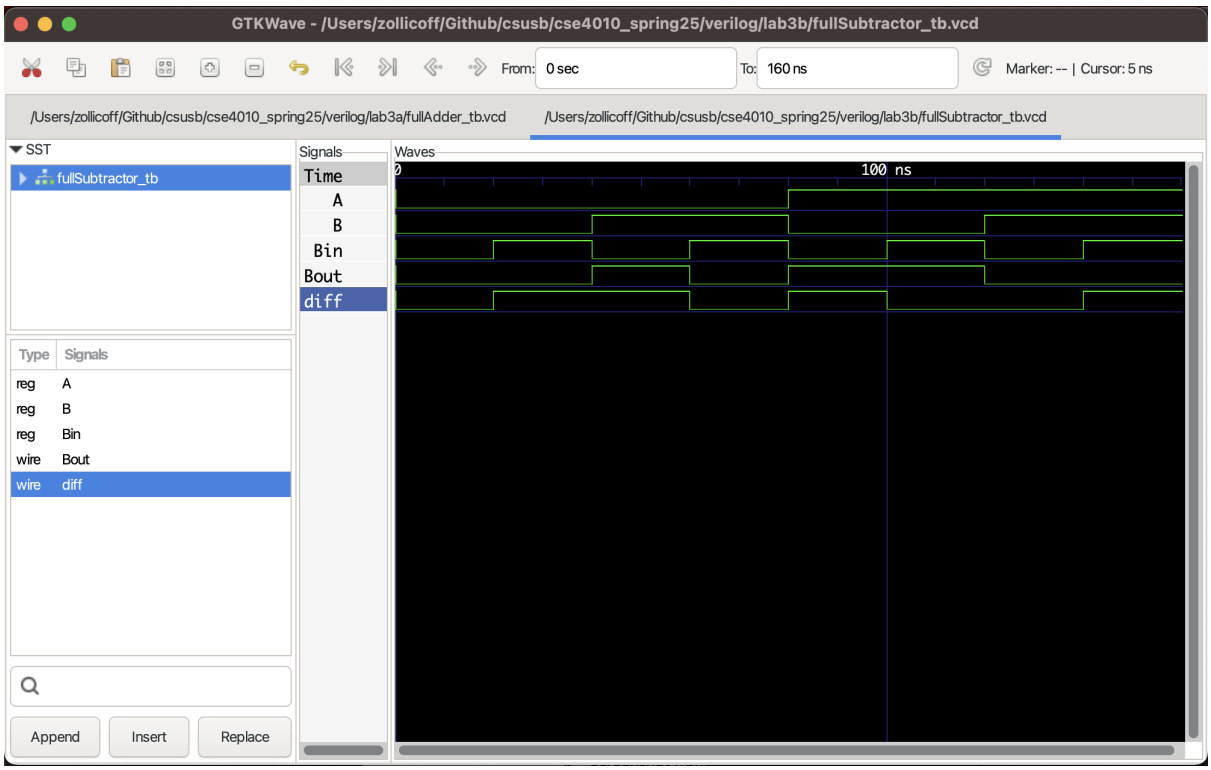

Figure 2: Full Subtractor Simulation Waveform showing all test cases with inputs A, B, Bin and outputs diff, Bout