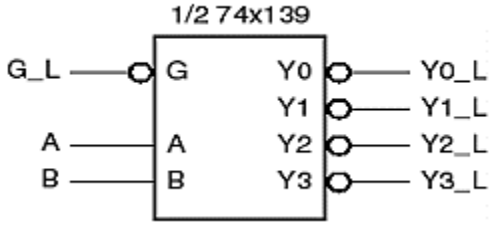
Decoders and Encoders

Problem 1. (20 pts) Sketch a design that can implement a 4-to-16 decoder using multiple 2-to-4 decoders. As shown below, each 2-to-4 decoder has active-low output and an active-low enable input.
Note: when BA = 01, Y1_L=0



Problem 2. (20 pts) Show how to build each of the following single- or multi-output logic functions using one or more 74x138 or 74x139 binary decoders and NAND gates. (*Hint:* Each realization should be equivalent to a sum of minterms.)

a)

$$F = \prod_{A,B,C}(3,4,5,6,7)$$

b)

$$F = \sum_{A,B,C}(2,6)$$

$$G = \sum_{C,D,E}(0,2,3)$$

Problem 3. (20 pts) Design a 10-to-4 encoder with inputs in the 1-out-of-10 code and outputs in a code like normal BCD except that input lines 8 and 9 are encoded into "E" and "F", respectively.

Problem 4. (20 pts) Draw the logic diagram for a 16-to-4 encoder using just four 8-input NAND gates. What are the active levels of the inputs and outputs in your design?

Problem 5. (20 pts) Show how to build all four of the following functions using one SSI package (four 2-input gates) and one 74x138.

$$F1 = \overline{X} \cdot \overline{Y} \cdot \overline{Z} + X \cdot Y \cdot Z$$

$$F2 = \overline{X} \cdot \overline{Y} \cdot Z + X \cdot Y \cdot \overline{Z}$$

$$F3 = \overline{X} \cdot Y \cdot \overline{Z} + X \cdot \overline{Y} \cdot Z$$

$$F4 = X \cdot \overline{Y} \cdot \overline{Z} + \overline{X} \cdot Y \cdot Z$$