

Field-effect transistor (FET)

①

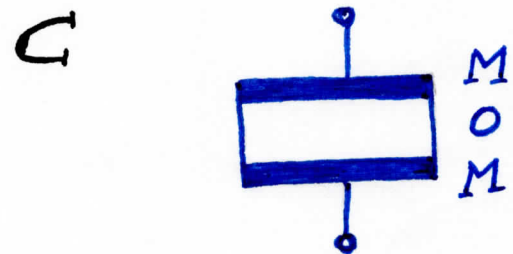
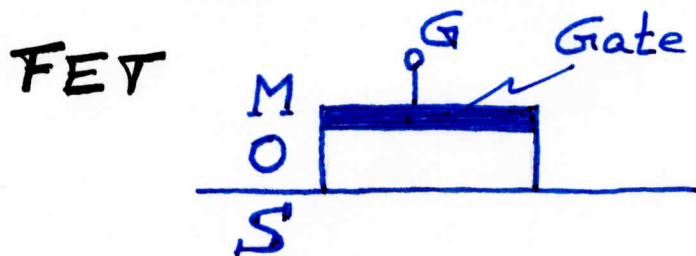
Metal $\Rightarrow M \Rightarrow$ Gate = G

Oxide (e.g. SiO_2) \Rightarrow Insulator

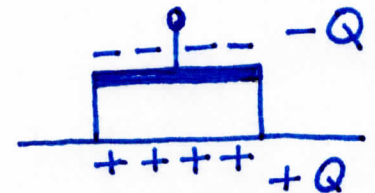
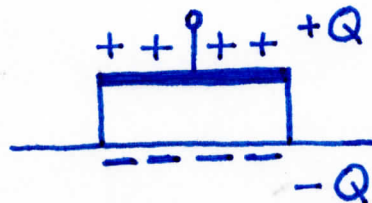
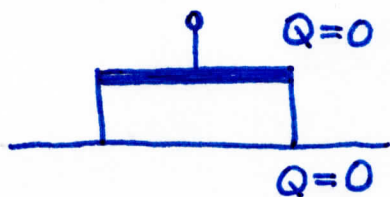
Semiconductor $\Rightarrow S$ (e.g. **Si**)

\Rightarrow MOSFET

MOS \Rightarrow Similar to a capacitor C

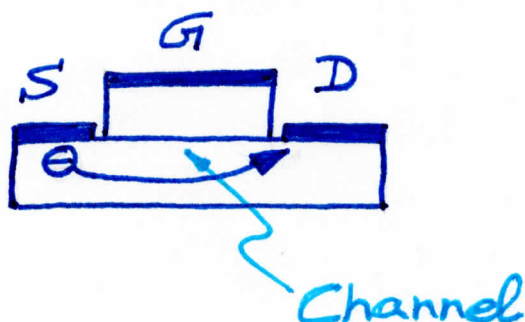


Gate charge induces charge in semiconductor



\Rightarrow Overall charge neutrality

Three electrodes: G (Gate), S (Source) & D (Drain)

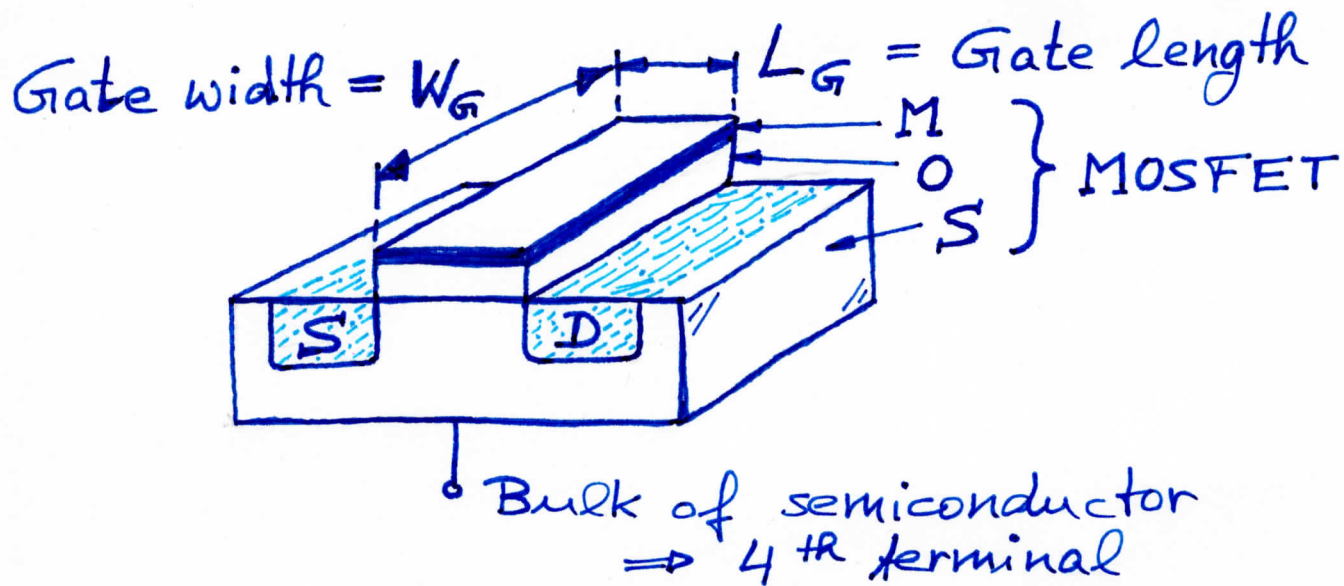


S = Source of charge carriers

D = Drain of charge carriers

G = Gate between S & D

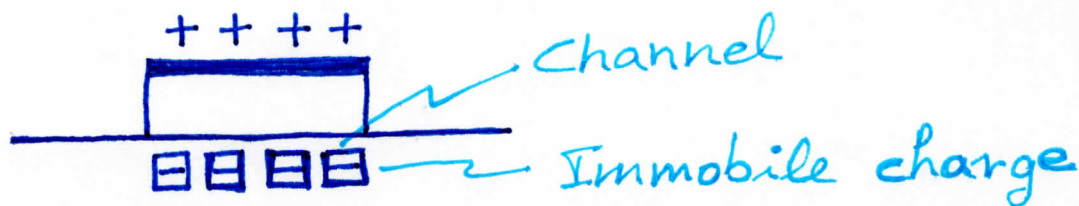
(2)



$V_{GS} > 0 \Rightarrow$ Negative charge induced in channel

$V_{GS} < 0 \Rightarrow$ Positive charge induced in channel

Threshold voltage: Assume there is immobile charge in the channel:



\Rightarrow No electrical conduction in channel

\Rightarrow Voltage needs to exceed "threshold voltage" to induce mobile charges in channel (electrons & holes).

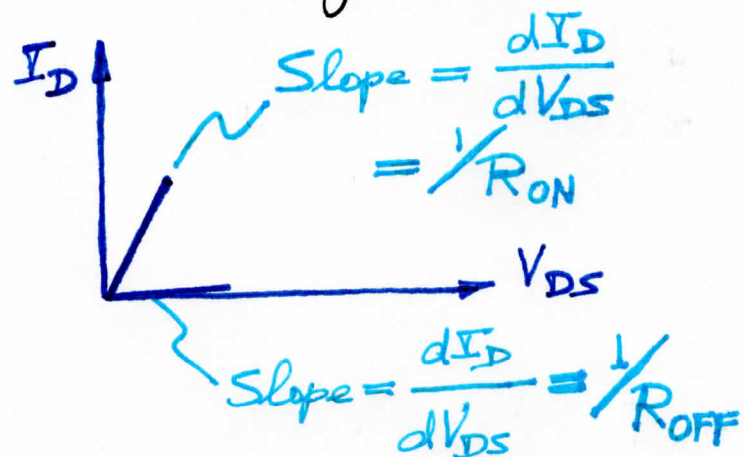
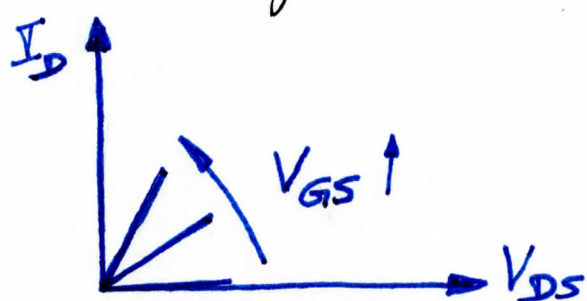
\Rightarrow FETs have a threshold voltage.

It can be negative, zero, or positive.

Our intuition: If we apply $V_{GS} > V_{th}$ ③
(V_{th} = Threshold voltage) \Rightarrow Mobile charge is induced \Rightarrow Current flows in channel.

Output characteristic: I_D versus V_{DS}

① Ohmic regime (= linear regime)



Quantitative formula (not derived here)

$$I_D = k' \frac{W_G}{L_G} (V_{GS} - V_{th}) V_{DS}$$

$\left\{ \begin{array}{l} \rightarrow \text{Geometry of FET} \\ \rightarrow \text{Physics of semiconductor, e.g. carrier mobility} \end{array} \right.$

② Intermediate regime

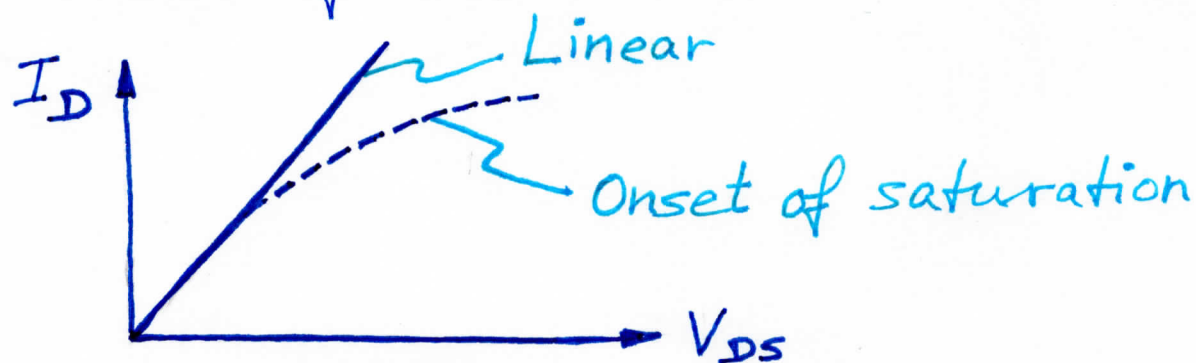
$$I_D = \underbrace{k'}_{k} \frac{W_G}{L_G} \left[(V_{GS} - V_{th}) V_{DS} - \underbrace{\frac{1}{2} V_{DS}^2} \right]$$

→ We initially neglected this factor.

Q: When can we neglect this factor?

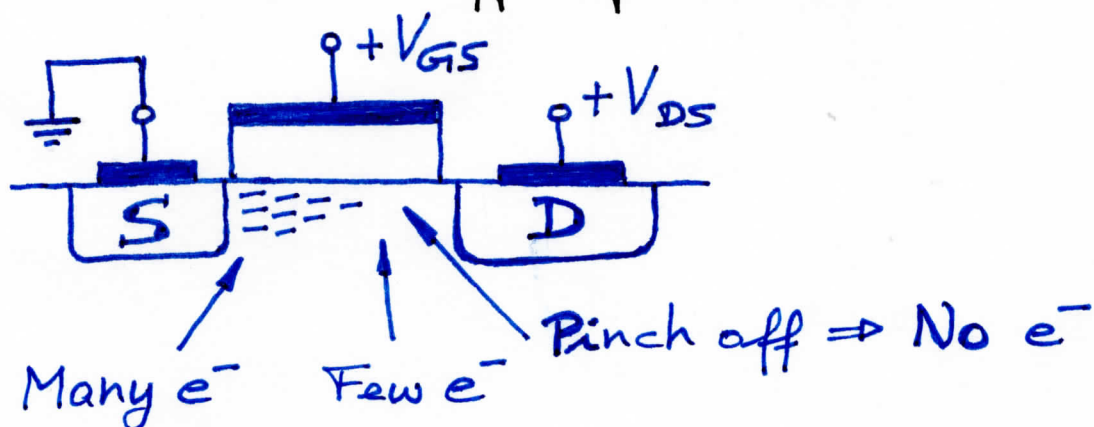
Q: What does this factor do?

⇒ Onset of saturation



Q: What causes onset of saturation?

⇒ Pinch-off of channel.



(5)

⇒ Channel is pinched off when $V_{DS} \uparrow$

⇒ Current does not increase ⇒ Saturation

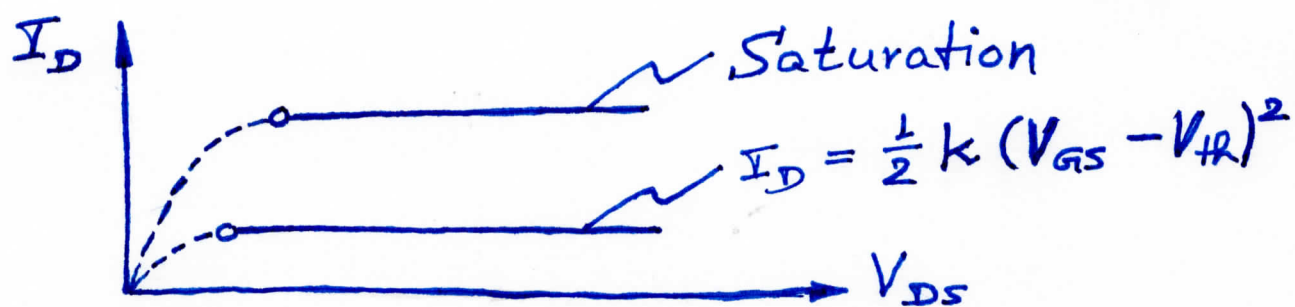
⇒ I_D -versus- V_{DS} slope = 0 at $V_{DS} = V_{GS} - V_{th}$

③ Saturation ⇒ $V_{DS} \geq V_{GS} - V_{th}$

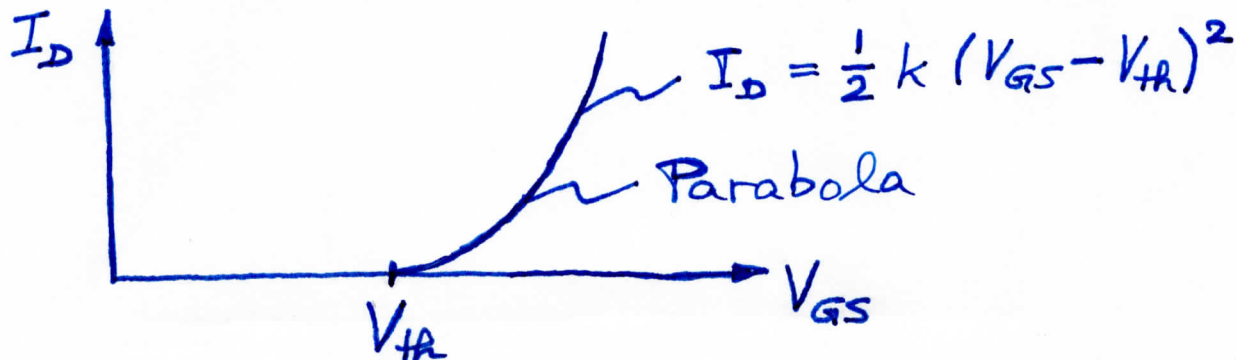
$$I_D = \underbrace{k' \frac{W_G}{L_G}}_{k} \left[(V_{GS} - V_{th}) \underbrace{V_{DS}}_{V_{GS} - V_{th}} - \frac{1}{2} V_{DS}^2 \right]$$

$$= k \left[(V_{GS} - V_{th})^2 - \frac{1}{2} (V_{GS} - V_{th})^2 \right]$$

⇒ $I_D = \frac{1}{2} k (V_{GS} - V_{th})^2$

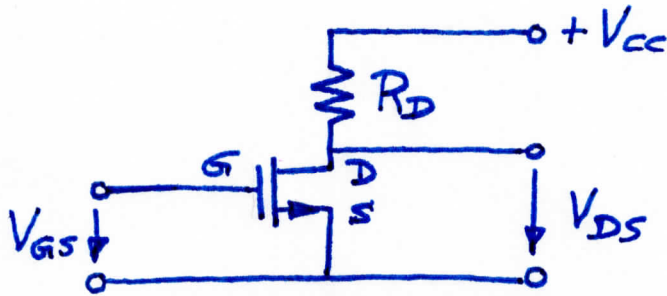


Output current $\hookrightarrow I_D$ versus input voltage $\hookrightarrow V_{GS}$



⑥

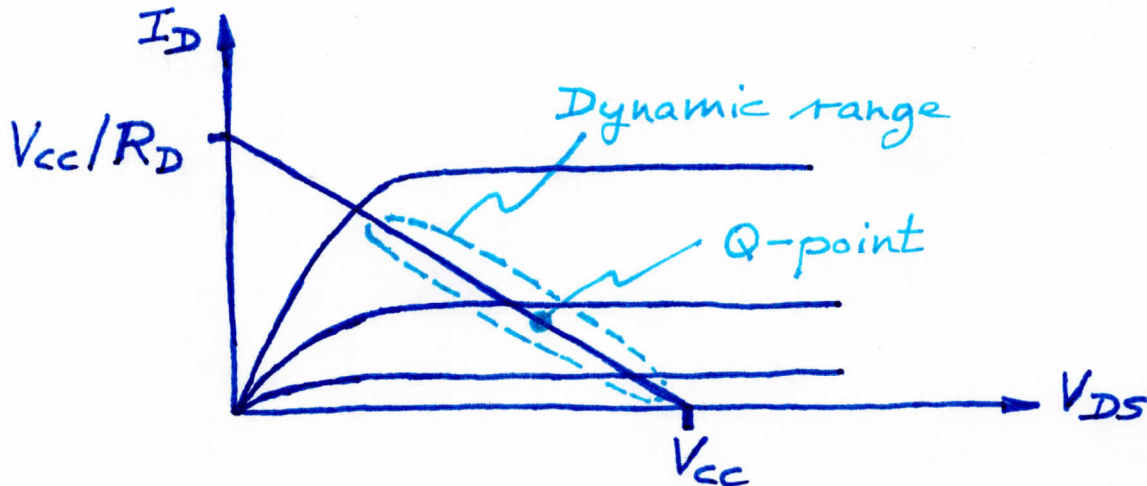
Load line of amplifier circuit



$$V_{RD} = V_{CC} - V_{DS}$$

$$I_D R_D = V_{CC} - V_{DS}$$

$$\Rightarrow I_D = \frac{V_{CC} - V_{DS}}{R_D}$$



Q: We identified 3 regimes: ① Ohmic

② Onset of saturation ③ Saturation.

Can you show these regimes in figure above?

Q: For an amplifier, which regime are we operating the transistor in?