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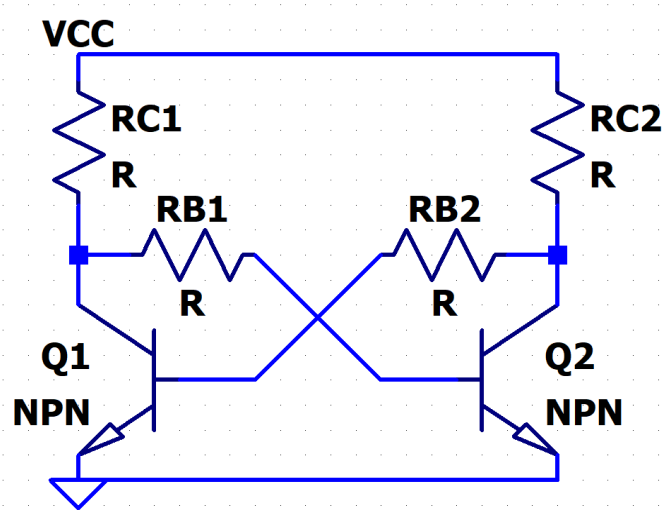
Intro to Electronics HW11

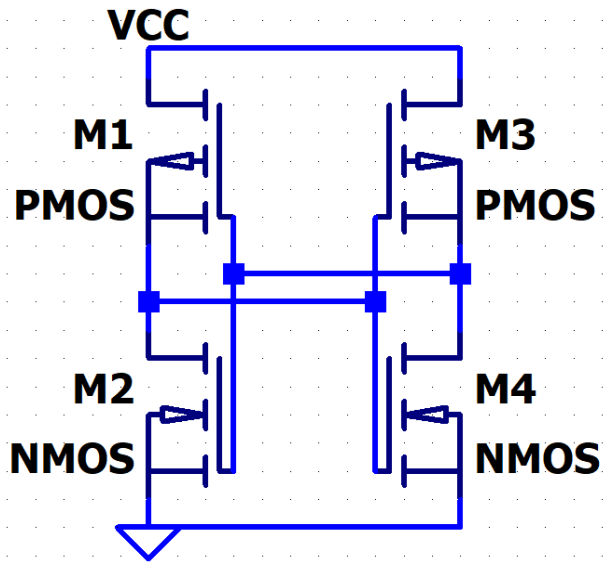
Note: I'm not using the usual digital logic symbols because they're not in LTspice

1. 1. SRAM cell: This problem concerns SRAM cells (SRAM = static random access memory).
    a. (a) Draw the circuit diagram of a BJT SRAM cell consisting of two BJTs and four resistors. Give a formula for the approximate power consumption of the cell.



P~=VCC^2/RC

    b. (b) Draw the circuit diagram of a CMOS FET SRAM cell consisting of four FETs. What is the status power consumption of the cell?

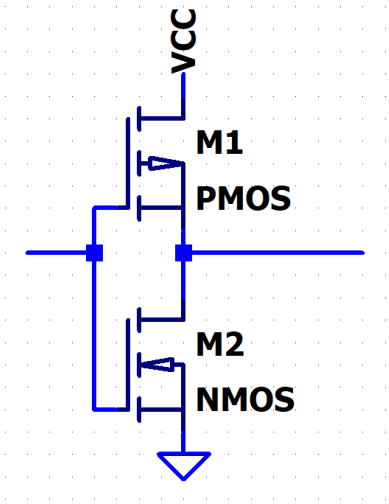


P~=0

    c. (c) What do you conclude from the comparison of BJT-based and FET-based SRAM cells?

BJT SRAM uses far more power than FET SRAM

2. 2. CMOS inverter circuit: The present problem concerns a basic digital CMOS circuit: A CMOS inverter having two transistors and no resistors.
    a. (a) Draw the circuit diagram of the CMOS inverter consisting of two FETs and no resistor. Explain how the inverter works.



When the input is VCC, the non inverting nmos grounds the output. When the input is grounded, the inverting pmos pulls the output to VCC.

    b. (b) Explain why the AC small-signal equivalent circuit is of little or no interest in the present context.

The small signal circuit has no connection between input and output

    c. (c) We generally differentiate between static power consumption (DC power consumption) and dynamic power consumption (power consumption due to the charging of parasitic capacitors, e.g. gate capacitors). What is the static power consumption of a CMOS inverter circuit?

Zero
P=0

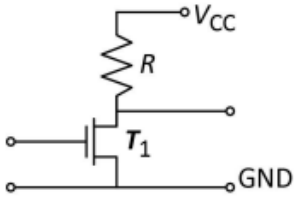
    d. (d) Explain why CMOS FET circuits are very suitable for large-scale integrated circuits.

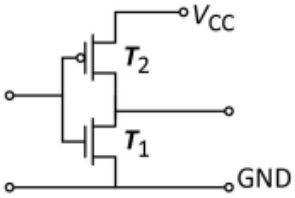
They generate very little heat.

    e. (e) Explain why BJT circuits are very unsuitable for large-scale integrated circuits.

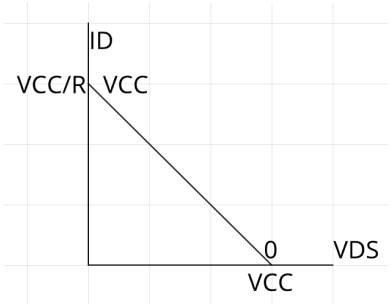
They generate a lot more heat, consuming electricity and creating a need for dissipation.

3. 3. CMOS inverter circuit: Consider the inverter circuits shown below. The LHS (left-hand side) circuit has a transistor T1 and a load resistor. The RHS (right-hand side) circuit has two transistors, T1 and T2 . The inverter circuits have two possible input voltages +VCC and zero (GND); the corresponding output voltages are zero (GND) and +VCC , respectively.



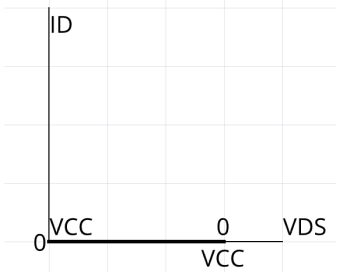


   a. (a) Consider the LHS circuit. Draw the general output characteristic of transistor T1 (ID -versus-VDS). Mark a 1st state (point) in the transistor's output characteristic when the input is zero. Then mark a 2nd state (point) in the transistor's output characteristic when the input is +VCC .



At Vin=0, acts as an open circuit (VDS=VCC, ID=0)
At Vin=VCC, acts an a short circuit (VDS=0, ID=VCC/R)

   b. (b) Next consider the RHS circuit. Draw the general output characteristic of transistor T1 (ID -versus-VDS). Mark a 1st state (point) in the transistor's output characteristic when the input is zero. Then mark a 2nd state (point) in the transistor's output characteristic when the input is +VCC .



At Vin=0, acts as an open circuit (VDS=VCC, ID=0)
At Vin=VCC, acts an a short circuit (VDS=0, ID=0)

   c. (c) Compare the two circuits and describe your observations.

Because either the nmos or pmos is always off, theres always an "open circuit" between VCC and GND, meaning no current can flow, but the output voltage is always "shorted" to either VCC or GND

4. 4. True / false questions: Are the following statements true or false? Explain your answer with one or two sentences.
    a. (a) Although BJT integrated circuits are faster than FET integrated circuits, the vast majority of integrated circuits are made from FETs.

False, FET's are also faster than BJT's (assuming switching in and out of saturation) in addition to their lower power consumption,

    b. (b) Satellite receivers frequently have front-end amplifiers made with FETs, because signals received on Earth from outer-space satellites are inherently weak.

True, the tiny power draw will keep the signal intact.