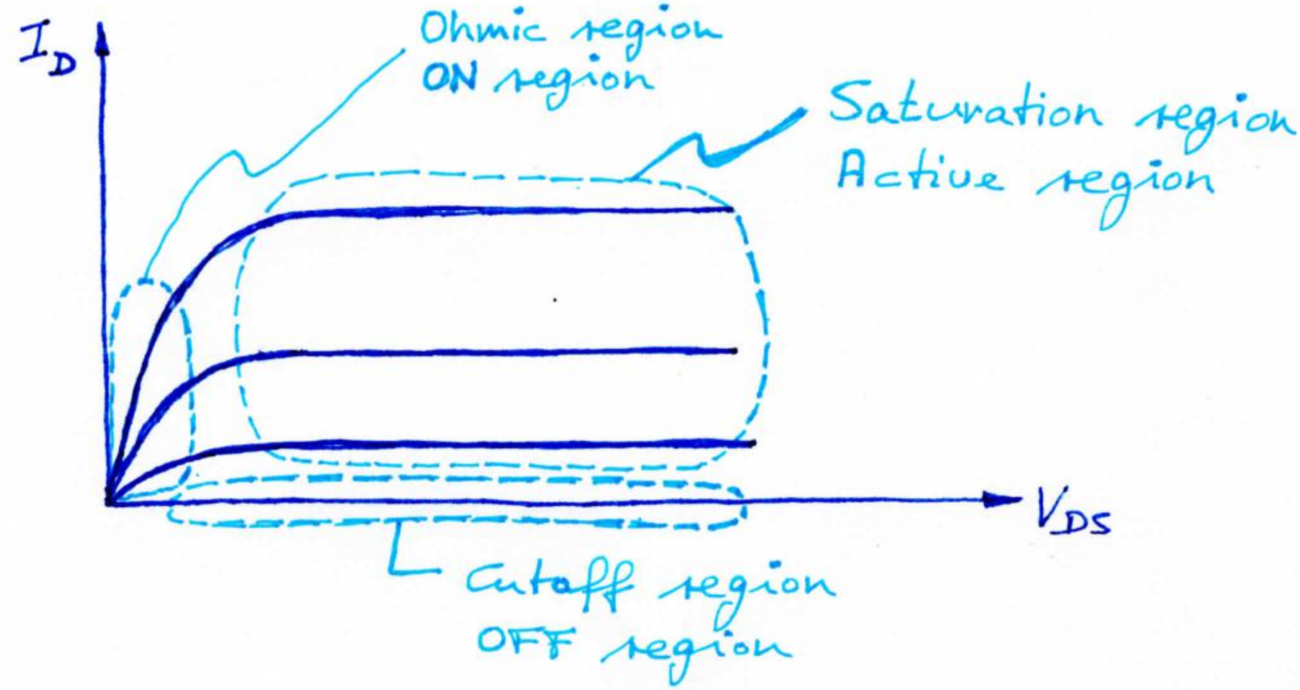
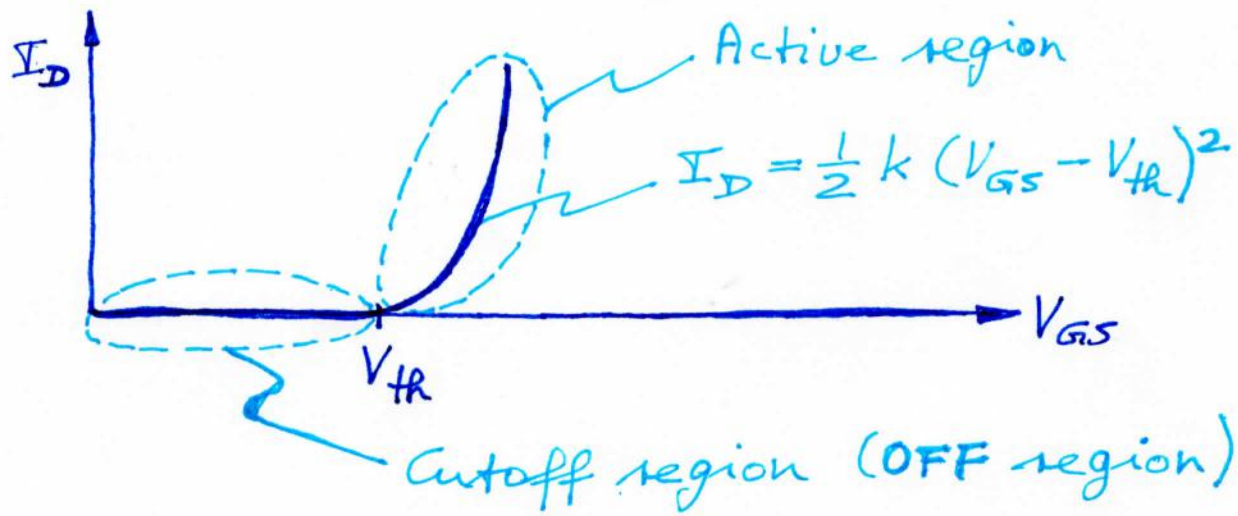
ITE – Homework 9 – Solution

Problem 1

(a) Output characteristic I_D versus V_{DS}



(b)



(c) The two currents are exactly the same.

$$I_D = I_S$$

(d) At the threshold voltage, the FET's channel becomes conductive (enhancement mode FET) or non-conductive (depletion mode FET). Therefore the threshold is the boundary between a conductive and a non-conductive channel.

Problem 2

(a) Gate current is zero due to the insulating oxide under the gate.

(b) Input power consumed by the FET is zero. The BJT consumes a higher input power.

(c) A low-input power amplifier will not overload the signal source.

(d) Similarities

* BJT and FET are three-terminal devices
* Both are amplifier devices
* Emitter ⇒ Source (similar)
* Base ⇒ Gate (similar)
* Collector ⇒ Drain (similar)

(e) Differences

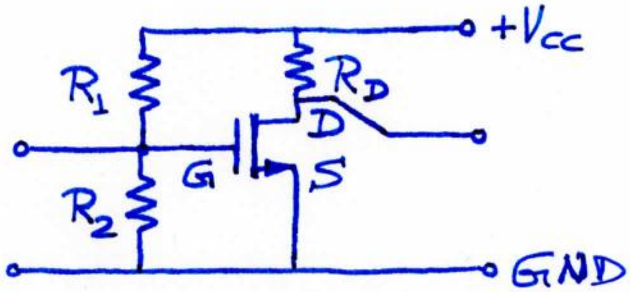
* BJT has a fixed threshold of the BE junction ⇒ 0.7V

  But FET can have any threshold voltage, e.g. −5V, −1V, 0V, 3V, 6V...

* BJT has pn junctions. FET has no pn junctions. ⇒ 0.7V has no relevancy for FETs.

Problem 3 FET bias circuits

(a)



⇒ Common-source amplifier circuit

$I_D = 4\,mA \qquad k = 5\,\frac{mA}{V^2} \qquad V_{th} = 2V$

$$I_D = \frac{1}{2} k \, (\underbrace{V_{GS}}_{\text{unknown}} - V_{th})^2$$

⇒ Solve for V_{GS}

$$\Rightarrow \quad V_{GS} = \sqrt{\frac{2\,I_D}{k}} + V_{th} = \sqrt{\frac{2 \times 4mA}{5mA/V^2}} + 2V$$

$$= 1.26V + 2V = \underline{3.26V}$$

$\Rightarrow V_{Gate} = 3.26V \Rightarrow V_{R1} = 10V - 3.26V = 6.74V$

Assume $I_{R1} = 10\,\mu A$ ⇒

$$\Rightarrow R_1 = \frac{V_{R1}}{I_{R1}} = \frac{6.74V}{10\mu A} = \underline{674\,k\Omega}$$

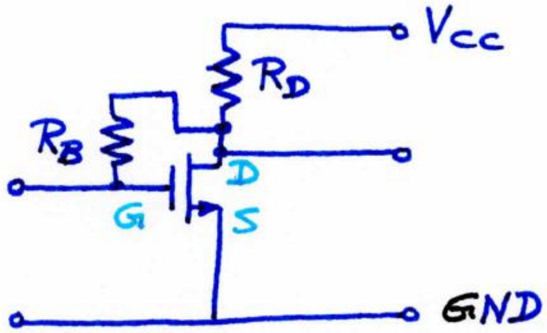
$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{3.26V}{10\mu A} = \underline{326\,k\Omega}$$

(b) Q-point is in the middle of the load line

$\Rightarrow V_{DS} = 5V \Rightarrow V_{RD} = 5V \qquad I_{RD} = I_D = 4\,mA$

$$\Rightarrow R_D = \frac{V_{RD}}{I_{RD}} = \frac{5V}{4mA} = \underline{1.25\,k\Omega}$$

(c)



This is a common-source amplifier

$I_D = 4\,mA$ $\qquad k = 5\,\frac{mA}{V^2}$ $\qquad V_{th} = 2V$

$$I_D = \frac{1}{2} k\,(\underbrace{V_{GS}}_{\text{unknown}} - V_{th})^2$$

$\Rightarrow$ Solve eqn. for V_{GS}

$$\Rightarrow V_{GS} = \sqrt{\frac{2 I_D}{k}} + V_{th} = \sqrt{\frac{2 \times 4mA}{5mA/V^2}} + V_{th}$$

$$= 1.26V + 2V = \underline{\underline{3.26V}}$$

There is no gate current $\Rightarrow I_G = 0 \Rightarrow$

$\Rightarrow$ No voltage drop across R_G

$\Rightarrow V_D = V_G = 3.26V$

$$\Rightarrow R_D = \frac{V_{RD}}{I_{RD}} = \frac{V_{CC} - V_D}{I_{RD}} = \frac{10V - 3.26V}{4\,mA} =$$

$$= \frac{6.74V}{4\,mA} = \underline{\underline{1.68\,k\Omega}}$$

The choice of R_G is not critical.

Can be any value. Let us choose $R_G = \underline{\underline{1\,M\Omega}}$

(d) Advantages of LHS circuit

* Gate bias side separated from load side (we prefer such separation)
* Voltage divider circuit is a standard circuit (which we like)
* Disadvantage: We need two resistors (R_1 and R_2)

(e) Advantage of RHS circuit

* We need only one resistor for gate biasing

Problem 4

True/false questions

(a) True $\qquad I_G = 0 \Rightarrow P_{In} = V_{GS} \times I_G = 0$

(b) True $\qquad$ The bias network will consume some of the incoming power

(c) False $\qquad I_S = I_D$

The two currents are exactly the same