Hayden Fuller 662028619 fulleh
1)VHDL code

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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/02/2022 12:17:14 PM
-- Design Name:
-- Module Name: Fuller_Hayden_Studio2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Fuller_Hayden_Studio2 is
    Port ( input : in STD_LOGIC_VECTOR (3 downto 0);
           leds : out STD_LOGIC_VECTOR (3 downto 0);
           anodes : out STD_LOGIC_VECTOR (3 downto 0);
           disp : out STD_LOGIC_VECTOR (6 downto 0)
           );
end Fuller_Hayden_Studio2;

architecture Behavioral of Fuller_Hayden_Studio2 is
```

```
begin

anodes(0) <= '1';
anodes(1) <= '1';
anodes(2) <= '1';
anodes(3) <= '0';

leds(0) <= input(0);
leds(1) <= input(1);
leds(2) <= input(2);
leds(3) <= input(3);

with input select disp <=
--bcdefg
"1000000" when "0000",
"1111001" when "0001",
"0100100" when "0010",
"0110000" when "0011",
"0011001" when "0100",
"0010010" when "0101",
"0000010" when "0110",
"1111000" when "0111",
"0000000" when "1000",
"0010000" when "1001",
"0001000" when "1010",
"0000011" when "1011",
"1000110" when "1100",
"0100001" when "1101",
"0000110" when "1110",
"0001110" when "1111",
"1111111" when others;


end Behavioral;
```

2)XDC file

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

# Switches
set_property PACKAGE_PIN V17 [get_ports {input[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {input[0]}]
set_property PACKAGE_PIN V16 [get_ports {input[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {input[1]}]
set_property PACKAGE_PIN W16 [get_ports {input[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {input[2]}]
set_property PACKAGE_PIN W17 [get_ports {input[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {input[3]}]


# LEDs
set_property PACKAGE_PIN U16 [get_ports {leds[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {leds[0]}]
set_property PACKAGE_PIN E19 [get_ports {leds[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {leds[1]}]
set_property PACKAGE_PIN U19 [get_ports {leds[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {leds[2]}]
set_property PACKAGE_PIN V19 [get_ports {leds[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {leds[3]}]

#7 segment display
set_property PACKAGE_PIN W7 [get_ports {disp[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {disp[0]}]
set_property PACKAGE_PIN W6 [get_ports {disp[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {disp[1]}]
set_property PACKAGE_PIN U8 [get_ports {disp[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {disp[2]}]
set_property PACKAGE_PIN V8 [get_ports {disp[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {disp[3]}]
set_property PACKAGE_PIN U5 [get_ports {disp[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {disp[4]}]
set_property PACKAGE_PIN V5 [get_ports {disp[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {disp[5]}]
set_property PACKAGE_PIN U7 [get_ports {disp[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {disp[6]}]
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```
set_property PACKAGE_PIN U2 [get_ports {anodes[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {anodes[0]}]
set_property PACKAGE_PIN U4 [get_ports {anodes[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {anodes[1]}]
set_property PACKAGE_PIN V4 [get_ports {anodes[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {anodes[2]}]
set_property PACKAGE_PIN W4 [get_ports {anodes[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {anodes[3]}]
```

3)tests
I went through and tested all switch combinations to get all possible outputs and they were all correct.

4)summary
I went off of the seven segment display labeling according to the PDF, but when I tested my outputs, almost everything was wrong. I then tested each bit individually to see what correlated to what and discovered they were in a different order. I went through and corrected all my outputs and it now works correectly.