Laboratory 7 (3rd/last day):
FET characteristics, Current mirrors, Small signal amplifiers

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Due 2024-04-18

Material covered:

- This laboratory has ***three sessions*** allocated for completion.
    - 1st session: Pre-Lab Exercise 1 and Exercise 1. Exercise 2 is optional.
    - 2nd session: Pre-Lab Exercise 2 and Exercise 3. Exercise 4 is optional.
    - 3rd session: Pre-Lab Exercise 3 and Exercise 5. Exercise 6 is optional.
- MOSFET DC biasing, Ohmic region and Saturation region
- Small signal models for MOSFETS
- Common source, common gate, common drain configurations
- Small signal bandwidth

PSpice:

Add the pwrmos library files to the PSpice directory. Note, I believe Orcad version 17.2 already has this library. Refer to Laboratory 2 for instruction on adding .lib and .olb files to PSpice and editing the nom (nomld) files to add the library link.

Data Acquisition:

As with previous labs, you will need to plot *I-V* characteristics for the devices under consideration.

DC measurements:

Due to the impedance characteristics of the Discovery Board, it is recommended to use the benchtop Multimeters to make the DC measurements in Exercise 2 and 3. When using the Multimeters, make sure your connections are correct or you can damage the device. If you are unsure, ask the TA or the Instructor.

DC Bias/Isolation capacitors:

The capacitors used in Exercises 3 to 6 are used for isolating the DC signals relative to the AC input. The electrolytic capacitors available in the laboratory have polarity. The "–" (negative) side is usually marked with a band and has the negative sign printed on it. This side should be connected to the low voltage side of the DC circuit (the AC polarity does not matter).

AC Sweep:

Bode plots can be obtained on the Discovery Board using the network analyzer tool. You can set the start frequency, stop frequency, input amplitude and points per step (more points gives you a smoother curve, but a longer data acquisition time).

FET internal capacitances (spec sheet values):

The spec sheet provides values based on input, output and reverse transfer capacitances, C_{iss}, C_{oss} and C_{rss}, respectively. They are values we could use in a model and with application of the Miller Theorem, we can find Ciss and Coss via the equivalent amplifier circuit model. In the small signal model we can relate these values to C_{DG}, C_{GS} and C_{DS} with the following equations:

$C_{iss} \approx C_{GS} + C_{DG}$ (given in Data Sheet)

$C_{oss} \approx C_{DG} + C_{DS}$ (given in Data Sheet)

$C_{rss} \approx C_{DG}$ (given in Data Sheet)

Given these equations, we can write:

$$C_{GS} = (C_{GS} + C_{DG}) - C_{DG} = C_{iss} - C_{rss}$$

$$C_{DG} \approx C_{rss}$$

$$C_{DS} = (C_{DG} + C_{DS}) - C_{DG} = C_{oss} - C_{rss}$$

Pre-Lab Exercise 3

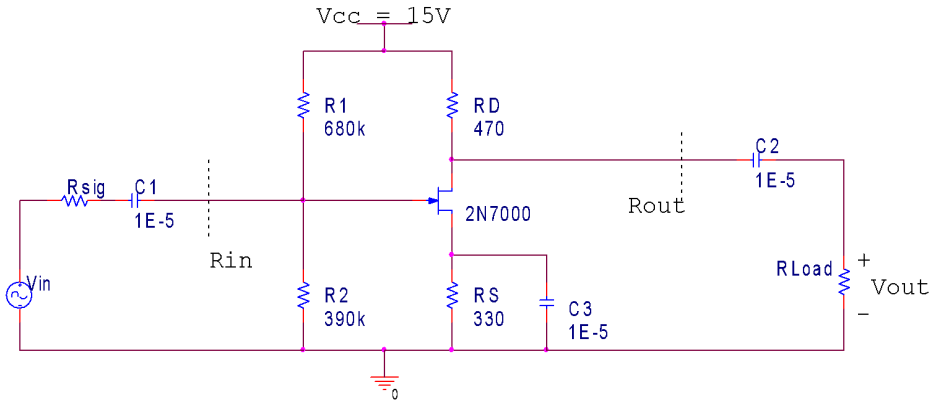


Figure 4: MOSFET circuit

Implement the Exercise 3/5 circuit in PSpice, setting R_{sig} to 100 kΩ and R_{Load} to 470 Ω, and run an AC sweep. Identify the low frequency and high frequency cutoff values (3 dB points).

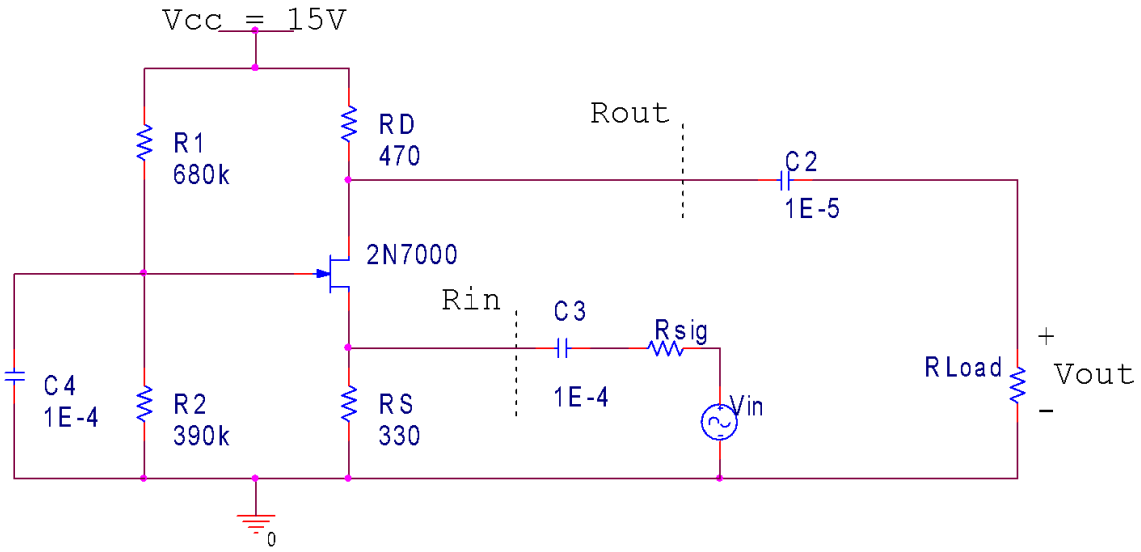


Figure 5: MOSFET circuit

Implement the Exercise 4/6 circuit in PSpice, setting R_{sig} to 22 Ω and R_{Load} to 1 kΩ, and run an AC sweep. Identify the low frequency and high frequency cutoff values (3 dB points).

Exercise 5: Common Source Bandwidth characteristics.

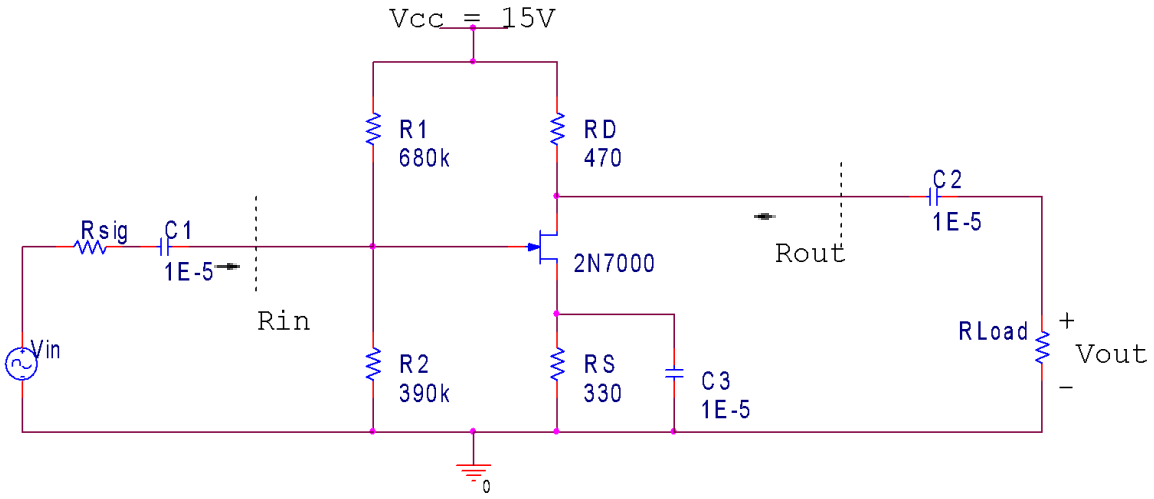


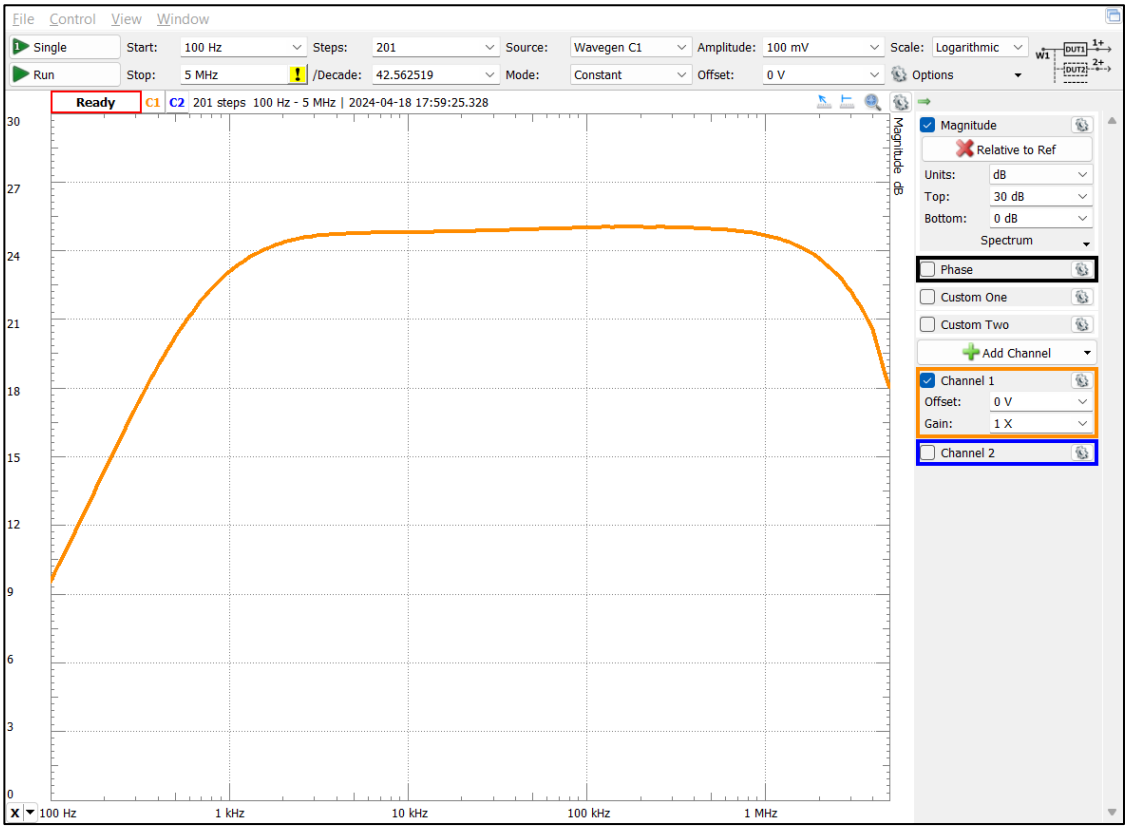
Figure 11: Common source amplifier (same circuit as Figure 9)

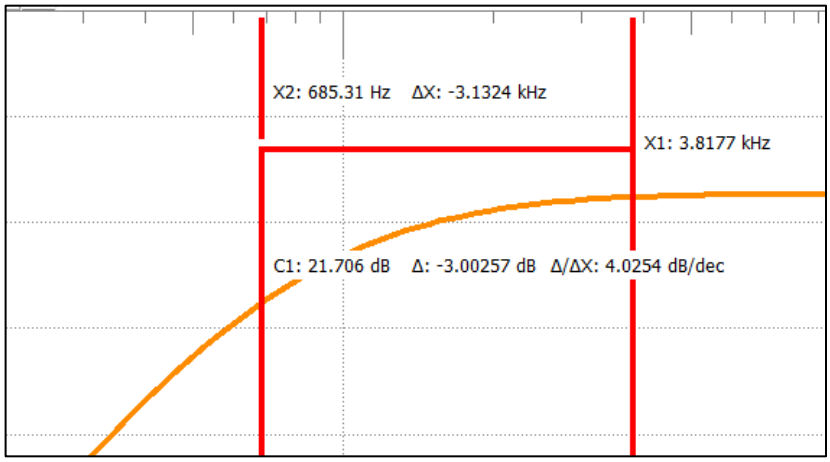
Implement the circuit in Figure 11 (the same circuit as Exercise 3). Set the AC source signal, V_{in}, to a 0.2Vpp sinusoidal signal.

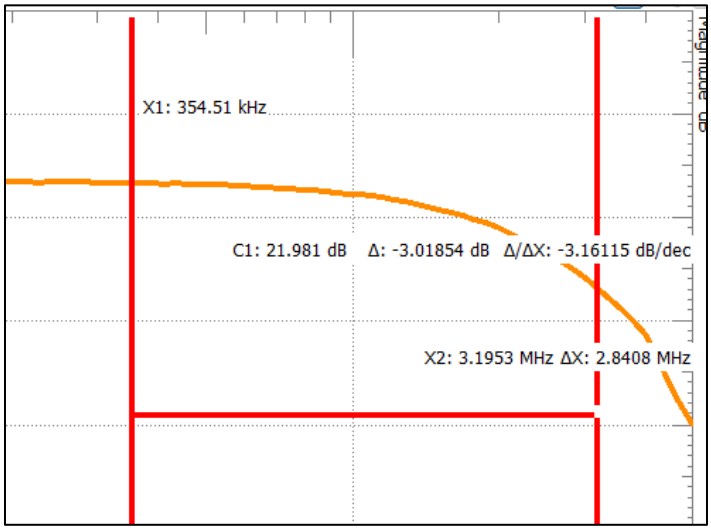
1. Using the 2N7000 spec sheet, identify the typical capacitances C_{GS}, C_{DG} and C_{DS} associated with the N-channel MOSFET (by using the equations given on page 2).

2. Set R_{sig} to 100 Ω and R_{Load} to 100 kΩ. Sweep the frequency and determine the bandwidth characteristics of the amplifier. Identify the passband by finding the 3 dB low and high cutoff frequencies.

   Compare your results to calculated estimates. Include the circuits you used to calculate your estimates. Indicate which capacitors are associated with the dominant poles for the low and high cutoff frequencies.







In the default config with Rsig=100 and Rload=100k, the measured bandwidth characteristics were:
Low cutoff (-3dB) freq is: ~685 Hz, or 700 Hz
High cutoff (-3dB) freq is: 3.2 MHz

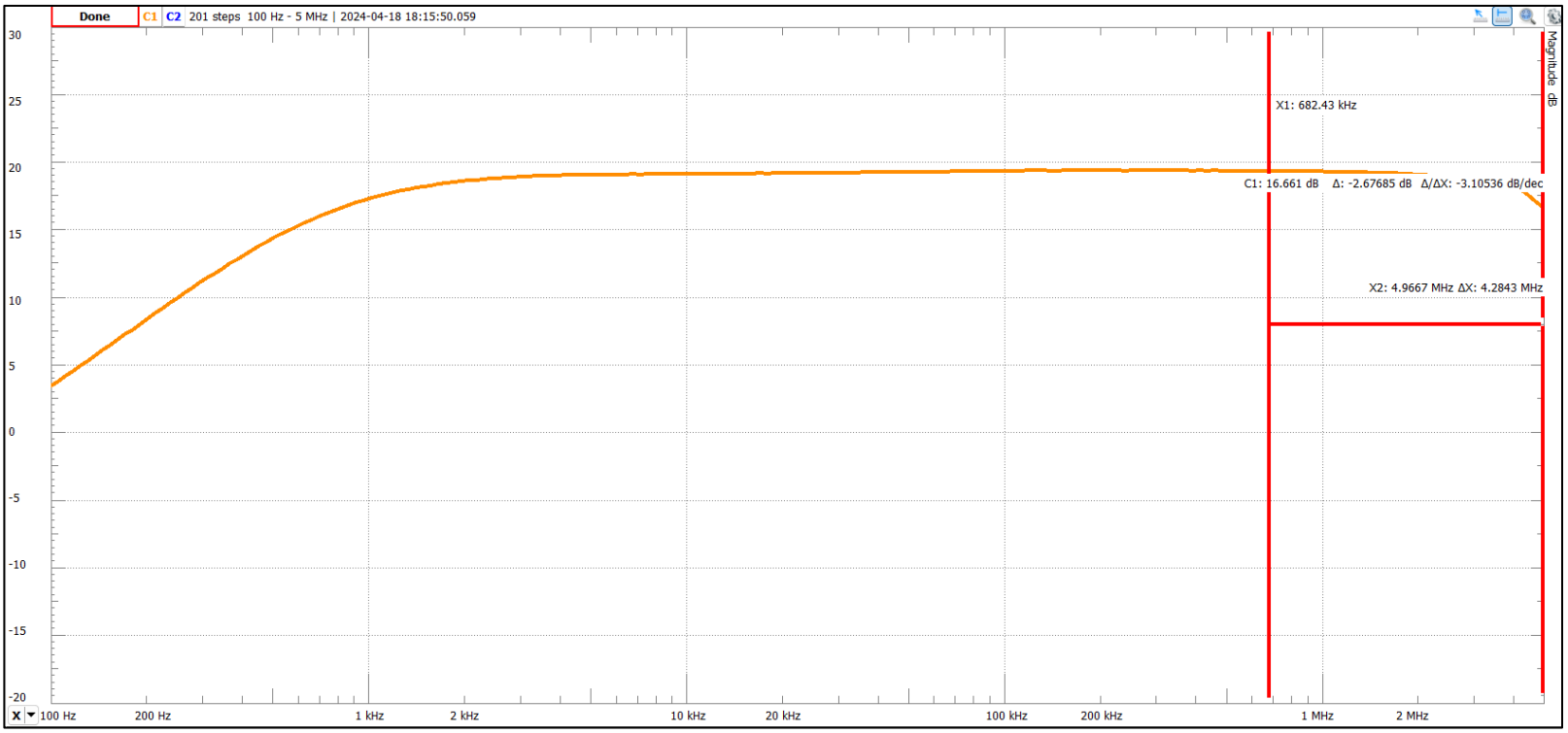
So the circuit's passband ranges from 700 Hz to 3.2 MHz.

Would your results change significantly if you increased R_{sig} to 10 kΩ?

Yes, increasing Rsig to 10k resulted in a high cutoff frequency of ~62 kHz, which is significantly lower than the initially measured 3.2 MHz for Rsig=100. The low cutoff frequency of 700Hz remained largely unchanged.

So, increasing Rsig effectively lowered the high cutoff frequency, making the circuit's operating band much tighter. The new passband ranges from 700 Hz to 62 kHz.

Would your results change significantly if you decreased R_{Load} to 470 Ω?



Yes. Decreasing Rload from 100k to 470 resulted in a high cutoff frequency of around 5 MHz, which is much higher than the initially measured 3.2 MHz for Rsig=100 and Rload=100k. The low cutoff frequency of 700 Hz also remained the same in this case.

So, decreasing Rload effectively increased the high cutoff frequency, and thus widened the circuit's operating band. The new passband ranges from 700 Hz to 5 MHz.