Intro to Elctronics S 2024 Crib Sheet Exam 1+2 Hayden Fuller

Basic:

Voltage divider: $V_2 = \frac{R_2}{R_1+R_2}$

Current divider: $I_2 = I\frac{G_2}{G_1+G_2}$

Capacitor: $Z_C = \frac{1}{jwC}$, $I = C\frac{dV}{dt}$, $E = \frac{1}{2}CV^2$

Inductor: $Z_L = jwC$, $V = C\frac{dI}{dt}$, $E = \frac{1}{2}LI^2$

LCR: resonance: $w = \frac{1}{\sqrt{LC}}$

Superposition: Short voltage, open current, analyze the thing, add.

Voltage to current: $I_{IS} = V_{VS}$, $R_{CS} = \frac{1}{RVS}$

OP AMP: Inverting Amp: $A = \frac{V_{out}}{V_{in}} = -\frac{R_F}{R_in}$

Summing Inverting Amp: $V_{out} = -R_F(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3})$

Subtraction: Inverting amp with voltage divider on plus: $V_{out} = V_{plus}\frac{R_G}{R_{in,plus}+R_G} \cdot \frac{R_{in,minus}+R_F}{R_{in,minus}} - V_{minux}\frac{R_F}{R_{in,minus}}$

H response: $H(w) = \frac{V_{out}}{V_{in}}$

Integrator: R_F is a capacitor, $V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}dt$

Detailed amplification: op amp

diff: $V_{out} = A_{diff}(V_+ - V_-)$

CM: $V_{out} = A_{CM}(V_+ + V_-)$

total amplification: $V_{out} = A_{diff}(V_+ - V_-) + A_{CM}(V_+ + V_-)$

CMRR: common mode rejection ratio: $\frac{A_{diff}}{A_{CM}}$, $20\log(CMRR)dB$

Gain Bandwidth Product: Gain$\cdot$Bandwidth, $A \cdot f$

Constant gain at low frequency, decreases linearly because slew rate at high frequency

knee frequency: $w = \frac{1}{RC} = \frac{1}{T} = \frac{1}{2\pi RC}$, $=>$ $H(w) = \frac{1}{\sqrt{2}}$, $-3dB$

above knee frequncy: $H(w) = \frac{1}{wRC}$, $-20dB$ per decade

high pass: $H(w) = wRC$, $20dB$ per decade, slope multiplied by N stages.

Slew rate: $= dV_{out}/dt$

ex: $SR = 1V/us$, pulse $0-2V$, $T = 2us$, 1V triangle wave

good sine wave: $SR >= 2\pi f V_0$

DIODES: forward bias, apply +V to holes, push holes(p) and electrons(n) together, get conduction

IV: $I = I_0(e^{\frac{V}{V_t}} - 1)$

Thermal voltage: $V_t = \frac{kT}{e} = 26mV$

Threashold voltage: $V_{th} = 0.7V$

Reverse saturation current: I_0 around 10^{-10}

For $V >> V_t$, $I = I_0 e^{\frac{V}{V_t}}$

Differential resistance: $r_D = \frac{V_t}{I}$ (I from above equation)

Basic DR circuit: $V_B = IR + V_D$, $I = I_D = I_0 e^{\frac{V}{V_t}}$

Graphically solve: $V_B = I_0 e^{\frac{V}{V_t}} R + V_D$, $V_B - V_D = I_0 e^{\frac{V}{V_t}}$

Approximate analytic solution: $V_D = V_{th} = 0.7V$, $I = \frac{V_B - 0.7}{R}$

Linearization: $r_D = \frac{V_t}{I_D}$, can treat as this resistor for an AC signal, just account for DC offset with superposition.

find I with DC (probably $\frac{V-0.7}{R}$), and $r_D = \frac{.026}{I}$, then add AC signal with r_D

Rectification: $P = V_{th}I$ AM: through diode and R and past C to filter out frequency, left with audio.Also LED and solar cell.

ZENER DIODE: width of depletion region changed with doping

Breakdown: at $V = V_{breakdown} = V_Z$

IV: turn on at $V_{th} = 0.7$, reverse turn on at $-V_Z$, typically used backwards, so flip V, expect $+ \ | < \ -$

$V < V_Z \ => \ r_Z = \frac{dV}{dI} = \infty$ OR $V >= V_Z$, $r_Z = \frac{dV}{dI} = 0$

$I = I_0 e^{\frac{V-V_Z}{V_t}}$

Basic ZDR circuit:

Graphical: $V_{Bat} - IR = V_Z(I)$

Approx analytical assume V_Z =constant, $I = \frac{V_B - V_Z}{R}$

Voltage stabalization: $V_{out} = V_Z =$ constant, wastes power, must have significant R_Load

Voltage clipper: two parallel to load, facing away, V clipped at $V_Z + V_{th}$

Voltage shifter: one series, cuts V_Z off of input

pnp, E+ arrow in top, holes flow in E, most make it to C, need current E to B, $V_{BE} < 0$
npn, E+ arrow out bot, holes flow out E, most come from C, need current B to E, $V_{BE} > 0$
common base:, in in E, out out C, grounded out B
common emitter: in out B, out out C, grounded in E
common collector: in out B, out in E, grounded out C
$I_C = \alpha I_E$
$I_C = \beta I_B$
$I_E = (\beta + 1) I_B$
$\beta = \alpha/(1 - \alpha)$
base << diffusion length
Equivalent:
Current from B, $\alpha' I'_C$ to E, $\alpha I'_E$ to C
Diode to B, I'_E from E, I'_C from C ($\alpha' < \alpha$)
simplifies to:
diode E to B, current out B, current B to C $\alpha I_E = \beta I_B$
npn is just flipped, $I_C = \alpha I_E$, diode B to E
graph output characteristic I_C vs V_{CE} ,
steep start goes (nearlly) flat, $I_C = \beta I_B$, flat section goes up with I_B
linear(small signal): output, current, effect $\propto$ input, voltage, cause: RCL, non: Diode, BJT, FET
small signal can count VCC as GND
C-B-E, equiv current αI_E - Diode I_E , near opp, $r_E + DC$, small signal r_E , $r_E = V_t/I_E = 26mV/I_E$
Common E: E grounded, B input, C output and RC to VCC,
$I_C = -V_{CE}/R_C + V_{CC}/R_C = V_{CC}/R_C - 1/R_C$ ($I_C = 0$ at $V_C C$)
solve $I_C = \beta I_B = -V_{CE}/R_C + V_{CC}/R_C$
saturation fully on at top left, $V_{CE} \approx 0.1 - 0.2V$
forward activev linear in middle, $I_C = \beta I_B$, $V_{BE} \approx 0.7V$
cutoff off at bottom, $V_{BE} < 0.7V$, $I_B = I_C = 0$, CE impedance $= \infty$
Quiescent point around middle of forward active region/dynamic range,
frequently middle of $I_C = V_{CC}/R_C - 1/R_C$, determined by DC bias network
find B current, find C current, find CE voltage (output voltage)
Primative common E
Voltage amplification $A_{VOC} = V_{in}/V_{out} = -\beta i_B R_C / i_E r_E = -\beta i_B R_C / (\beta + 1) i_B + r_E \approx -R_C/r_E$
Current amplification $A_{ISC} = i_{out}/i_{in}$
Input impedance $Z_{in} = V_{in}/I_{in} = r_E i_E / i_B = r_E (\beta + 1) i_B = \beta r_E$
Output impedance $Z_{out} = V_{out}/I_{out} = R_C I_C / I_C = R_C$
Emitter follower, RB to VCC, RE to GND, $V_{out} = V_{in} - V_{BE}$,
$Z_{in} \approx \beta R_E$ (high), $Z_{out} \approx R_E$ (low), $A_{VOC} \approx 1$ (low), $A_{ISC} <= \beta$ (high)
Non-idealities of BJTs
Finite output impedance (current source), $r_{CE} \neq \infty$
output characteristic graph isnt flat, but sloped with $r_{CE}{}^{-1}$,
meets at Early Voltage $\approx$-10V to -100V
$\beta = \Delta I_C / \Delta I_B$ increases with V_{CE} due to base width modulation
$I_C = \alpha I_0 e^{V_{BE}/V_t} (1 + (V_{CE}/V_{Early}))$
slope= $r_{CE}{}^{-1} = I_C / (V_{Early} + V_{CE})$
Breakdown of CB at high VCE, reverse breakdown of neglected BC diode comes into play, out char slopes increase
100V for Si, increasing order Ge, Si, GaAs, SiC, GaN, C

DIFFERENTIAL AMPLIFIER, used in op amp and Emitter Coupled Logic
C is outputs and R_C to $+V_{CC}$, B is inputs, E connects and shares R_E to GND
if input 1 is the input, output 1 is inverting
single input, single output, oposite sides, $A = R_C/(2r_E)$, differential output gives $A = R_C/r_E$
differential input and output $A = 2R_C/r_E$; Q-point $V_{CE} \approx V_{CC} - \beta I_{B1}(R_C + 2R_E)$
$\Delta I_{C1} = -\Delta I_{C2}$, so total current is constant, I_{RE} is constant, V is constant, Virtual Ground
Input Output Gain $r_E = V_t/I_E = 26mV/I_E$
single single $R_C/(2r_E)$
single differential $R_C/(r_E)$
differential differential $2R_C/(r_E)$
FLIP FLOP, SRAM(fast, power hungry, small)
C connects to V_{CC} through R_C and to other B through R_B. $P \approx V_{CC}{}^2/R_C$
R_C limits current flow while on, R_B stops other transistor from getting turned on.
ASTABLE FLIP FLOP, Multivibrator $R_B >> R_C$
same as above, but replace R_B with capacitor C, and have resistor R_B from the other side (B) of C to V_{CC}
Assume T1 on T2 off, $\tau = RC = R_{B1}C_1$, $T = 2\tau = 2R_BC$, change f with R_B (could do C)
C2 charged to VCC-0.7V, C1 charge slow RB1, T2 VBE hit 0.7 turn on, T2 VC=0, C2 charge brings VB1 negative
CURRENT MIRROR
T1 and T2 share E GND and B, T1 has CB shorted and R_C above that, load on T2 C
shared V_{BE} so turned on the same, $I_{RC} = (\beta + 2)I_B$, $I_{Load} = \beta I_B$, $I_{Load} \approx I_{RC}$
CLASS A AMPLIFIERS, basic, quality, high power draw
E GND, B in, B R_B to V_{CC}, C out, C R_C to V_{CC}
Q point power $P = I_C * V_{CE}$, constant power draw, good pre amp
CLASS B AMPLIFIER, push pull, crossover distortion, low power,
signal split bwtween two, top is NPN (normal), bottom is PNP (inverting), stacked between VCC+ and VCC-
less than 0.7V is lost, crossover distortion
CLASS AB AMPLIFIER, better push pull, low distortion, med-low power,
add caps to isolate each input and resistors + diodes to bias (1.4V between them), both have $V_{BE} = 0.7V$
CLASS C AMPLIFIER, pulse amplifier
CLASS D AMPLIFIER, digital audio quality, low power
triangle wave at 100kHz, gets compared to audio. Audio higher, high FET drives high, triangle higher, low fet drives low, gets smothed to 20kHz range by inductor
DARLINGTON TRANSITOR
C is shared, E connects to next B. $V_{BE} = 1.4V$, $\beta = \beta^2$, $V_{CE} = V_{BE2} + V_{CE1} >= 0.9V$
T2 doesn't saturate, can be good for high speed, used for RF