Chapter 16-3. MOS C-V characteristics

The measured MOS capacitance (called gate capacitance) varies with the applied gate voltage

- – A very powerful diagnostic tool for identifying any deviations from the ideal in both oxide and semiconductor

- – Routinely monitored during MMOS device fabrication

Measurement of C-V characteristics

- – Apply any dc bias, and superimpose a small (15 mV) ac signal

- – Generally measured at 1 MHz (high frequency) or at variable frequencies between 1KHz to 1 MHz

- – The dc bias V_G is slowly varied to get **quasi-continuous** C-V characteristics

C-V characteristics of MOS-capacitor on p- and n-type Si

C_G

C_G

V_G

V_G
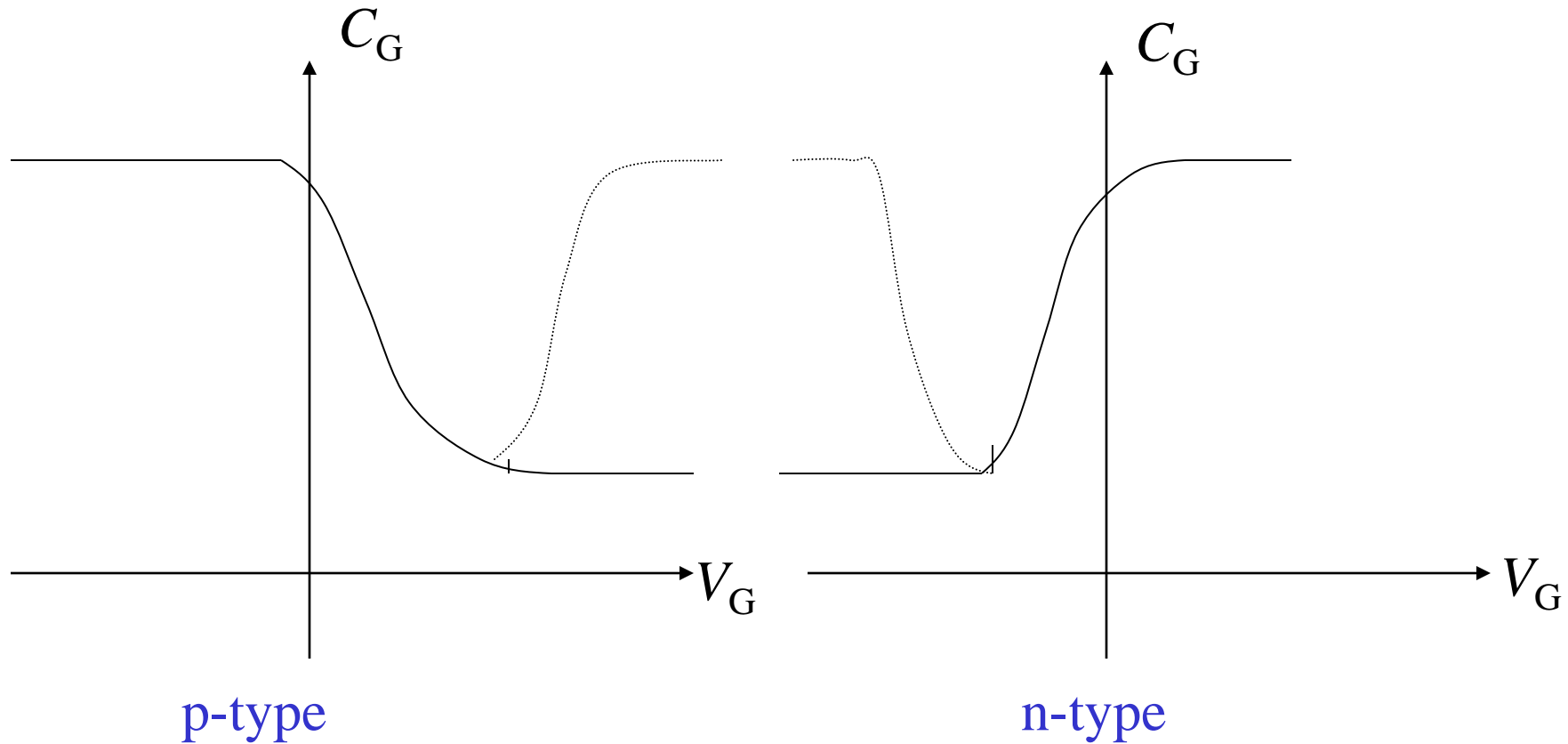
p-type

n-type

The *C-V* data depends on the measurement frequency as well.
The dotted line represents the low-frequency *C-V* data.

Measured C-V characteristics on an n-type Si
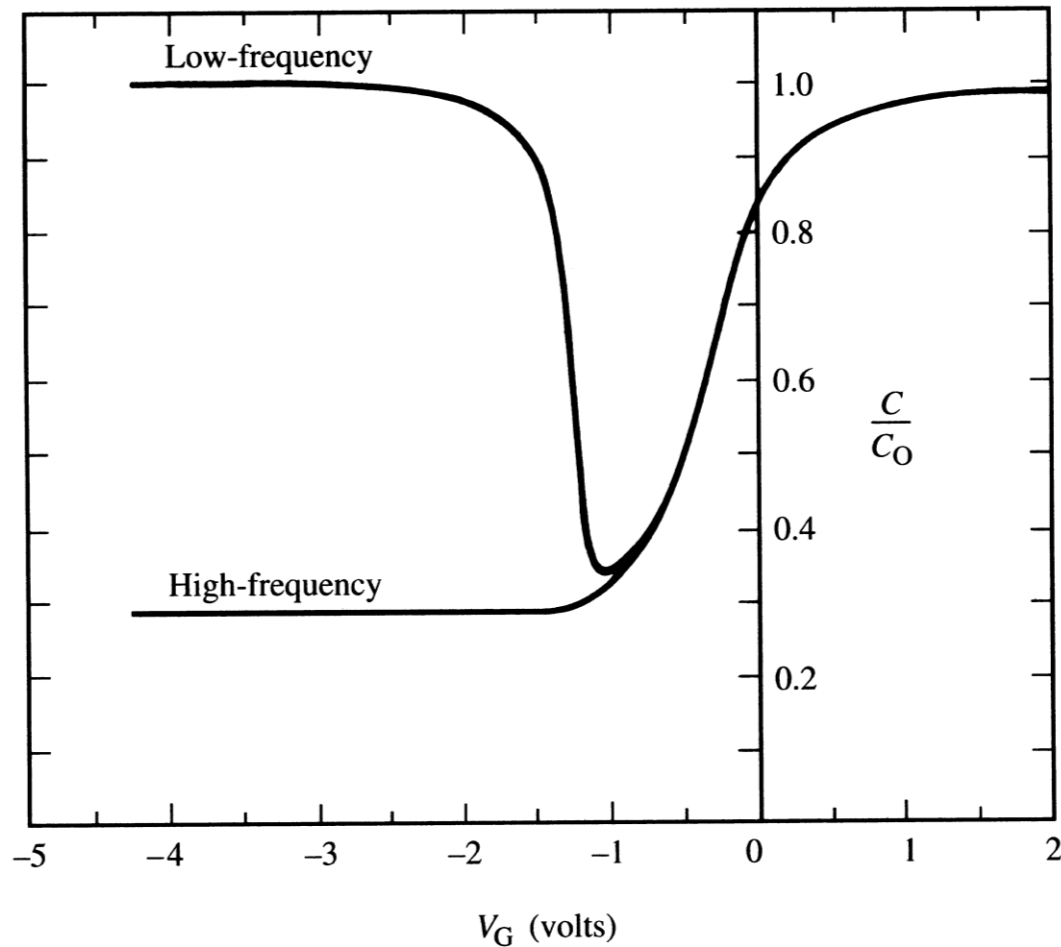
$N_D = 9.0 \times 10^{14} \text{ cm}^{-3}$
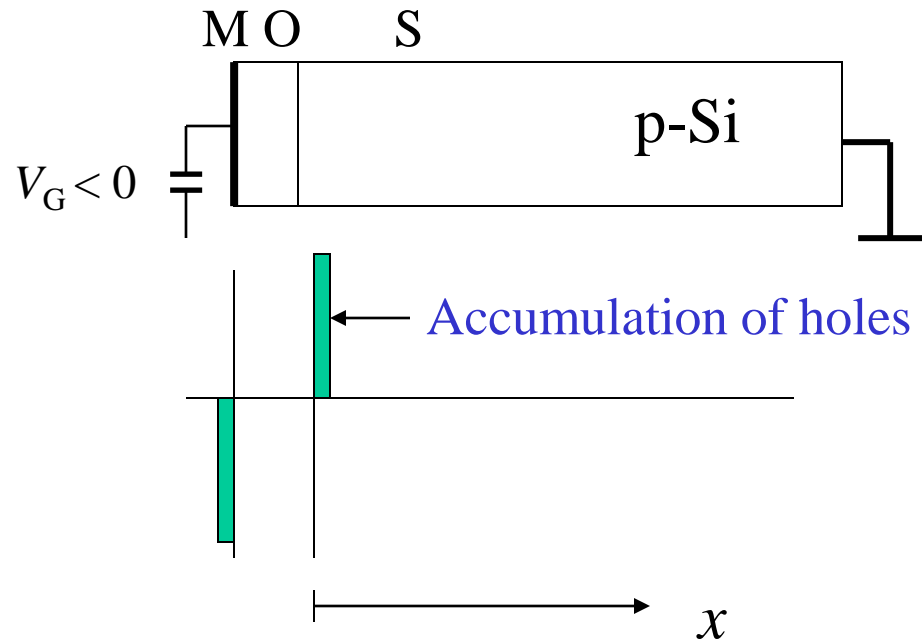
$x_{ox} = 0.119 \ \mu\text{m}$

Figure 16.11

MOS-capacitor under accumulation

Consider p-type Si under accumulation.

$V_G < 0$.
Looks similar to parallel plate capacitor.

$C_G = C_{ox}$

where $C_{ox} = (\varepsilon_{ox} A) / x_{ox}$

M O   S

$V_G < 0$

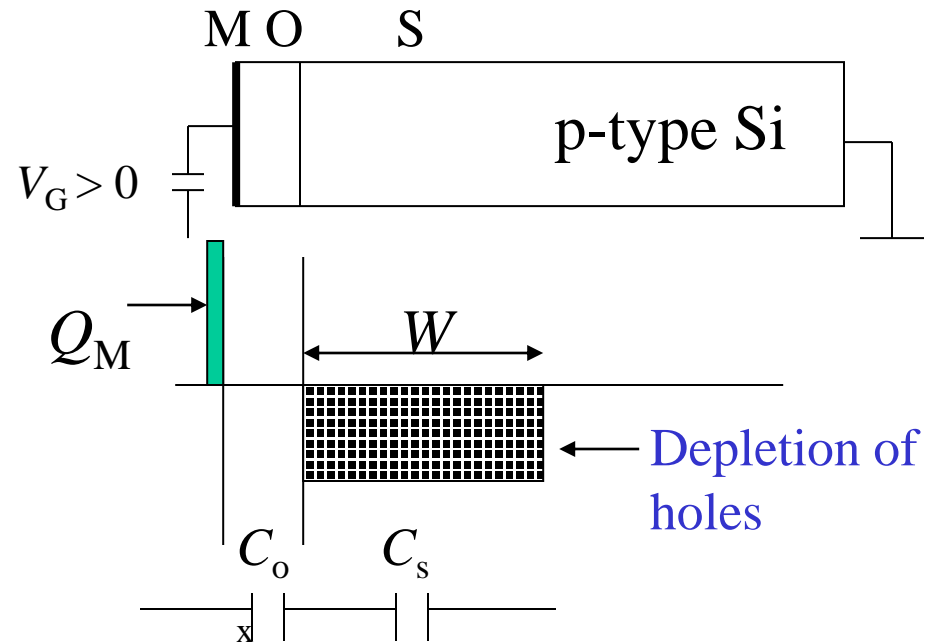p-Si

← Accumulation of holes

x

Thus, for all accumulation conditions, the gate capacitance is equal the oxide capacitance.

MOS-capacitor under depletion

Depletion condition:
$V_G > 0$

C_G is C_{ox} in series with C_s where C_s can be defined as "semiconductor capacitance"

$C_{ox} = \varepsilon_{ox} \, A / x_{ox}$
$C_s = \varepsilon_{Si} \, A / W$

$C_G = C_{ox} \, C_s / (C_{ox} + C_S)$

M O   S

p-type Si

$V_G > 0$

Q_M

W

C_o C_s

Depletion of holes

$$W = \sqrt{\dfrac{2\varepsilon_{Si}}{qN_A} \phi_s}$$

where ϕ_s is surface potential

In this case, the gate capacitance decreases as the gate voltage is increased. Why?

MOS-capacitor under inversion

$V_G = V_T$ and $V_G > V_T$

Inversion condition $\phi_s = 2\,\phi_F$

$$W = W_T = \sqrt{\frac{2\,\varepsilon_{Si}}{q\,N_A}\,2\phi_F}$$
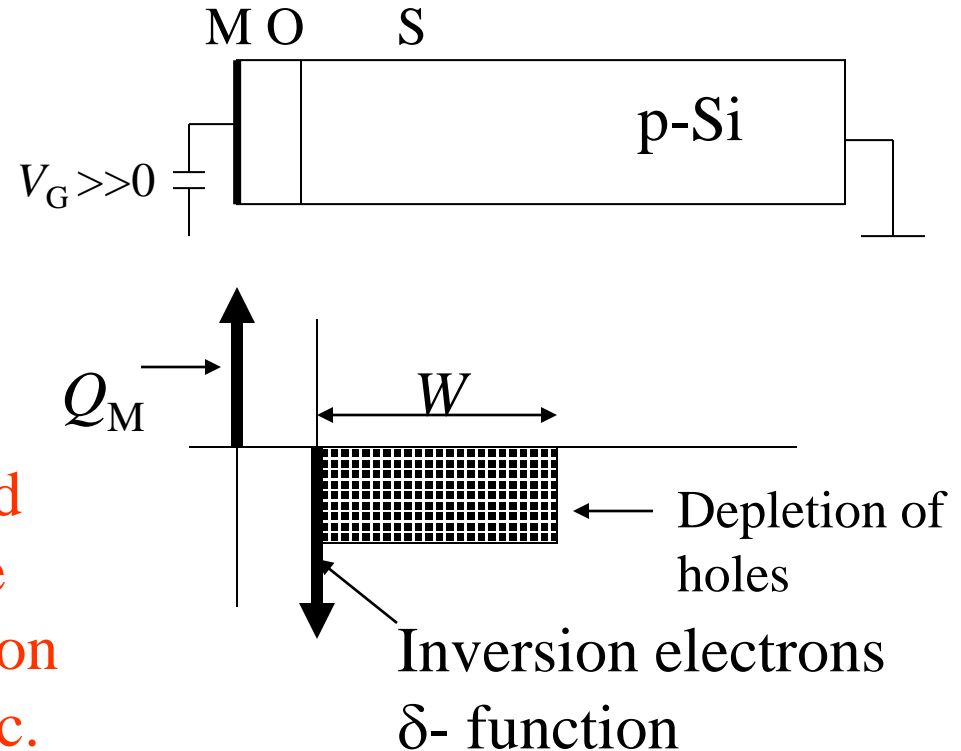
At high frequency, inversion electrons are not able to respond to ac voltage. So, to balance the charge on the metal, the depletion layer width will vary with the ac.

$C_{ox} = \varepsilon_{ox}\,A\,/\,x_{ox}$

$C_s = \varepsilon_{Si}\,A\,/\,W_T$

$C_G\,(\omega \rightarrow \infty) = C_{ox}\,C_s\,/\,(C_{ox} + C_S)$

So, C_G will be constant for $V_G \geq V_T$

M O   S

$V_G >> 0$

p-Si

Q_M

W

Depletion of holes

Inversion electrons
δ- function

C_o C_s

x

MOS-capacitor under inversion

At low frequency, the inversion electrons will be able to respond to the ac voltage (Why?). So, the gate capacitance will be equal to the "oxide capacitance" (similar to a parallel plate capacitance).

$$C_G (\omega \to 0) = C_{ox}$$
$$= \varepsilon_{ox} A / x_{ox}$$

For $V_G > V_T$, the high frequency capacitance remains constant. Why?

C_G

C_{ox}

Low frequency

$C_{ox} C_s / (C_{ox} + C_s)$

High frequency

V_T

V_G
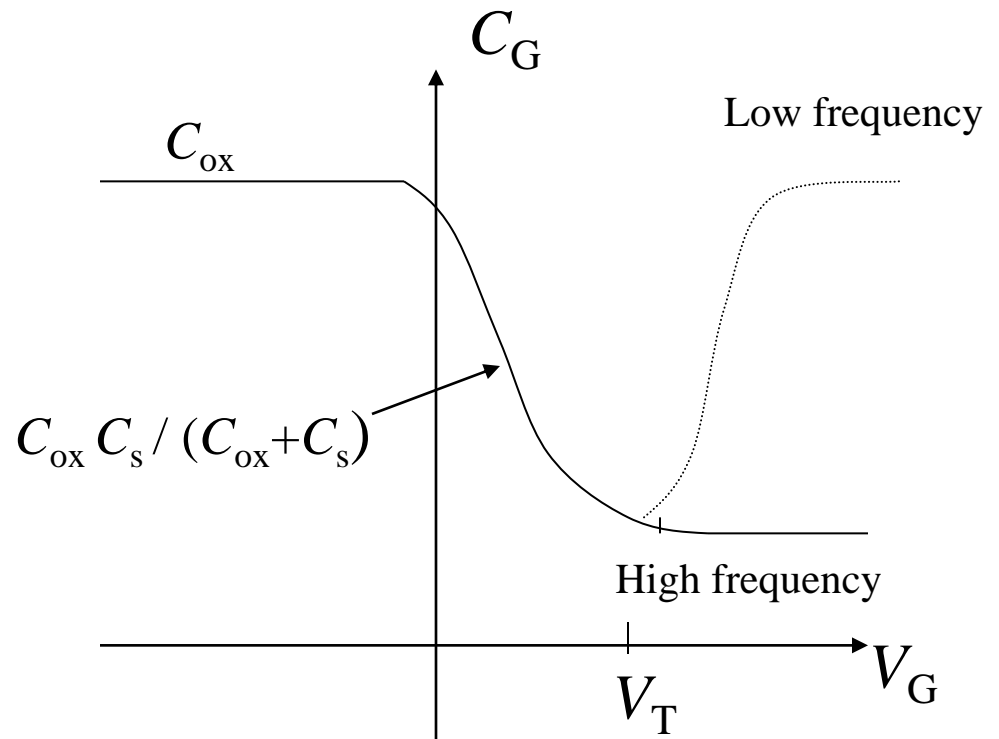
p-type Si

Example 1

Consider p-type silicon doped with $N_A = 10^{16}$ cm^{-3}. The oxide thickness is 100 nm. Plot the C_G vs. V_G characteristics when V_G is varied **slowly** from -5 V to $+5$ V. Assume MOS has area of 1 cm^2.

Find C_{ox}.

$$C_{ox} = \frac{3.9 \times 8.9 \times 10^{-14}\,(\text{As/Vcm})}{1000 \times 10^{-8}\,\text{cm}} \times 1\text{cm}^2 = 3.47 \times 10^{-8}\,\text{F}$$

Find C_s (min) when $W = W_T$ (Note that C_s decreases as the depletion layer width increases. It is minimum when the depletion layer width is maximum, i.e. when $W = W_T$).

$$W_T = \sqrt{\frac{2 \times 11.9 \times 8.85 \times 10^{-12}\,\text{As/(Vm)}}{1.6 \times 10^{-19}\,\text{C} \times 10^{16}\,\text{cm}^{-3}} \times 2 \times 0.357\,\text{V}} = 0.298\,\mu\text{m}$$

$$C_s(\text{min}) = \frac{10^{-12}\,\text{As/(Vcm)}}{0.298 \times 10^{-4}\,\text{cm}} \times 1\text{cm}^2 = 3.35 \times 10^{-8}\,\text{F}$$

$$C_G(\text{min}) = (3.47 \times 10^{-8} \times 3.35) / (3.47 + 3.35)\,\text{F} = 1.7 \times 10^{-8}\,\text{F}$$

Example 1 (continued)

$$V_G = V_T = \phi_s + x_{ox} \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \sqrt{\frac{2 q N_A}{\varepsilon_{Si}} \phi_s} \quad \text{when} \quad \phi_s = 2\phi_F$$
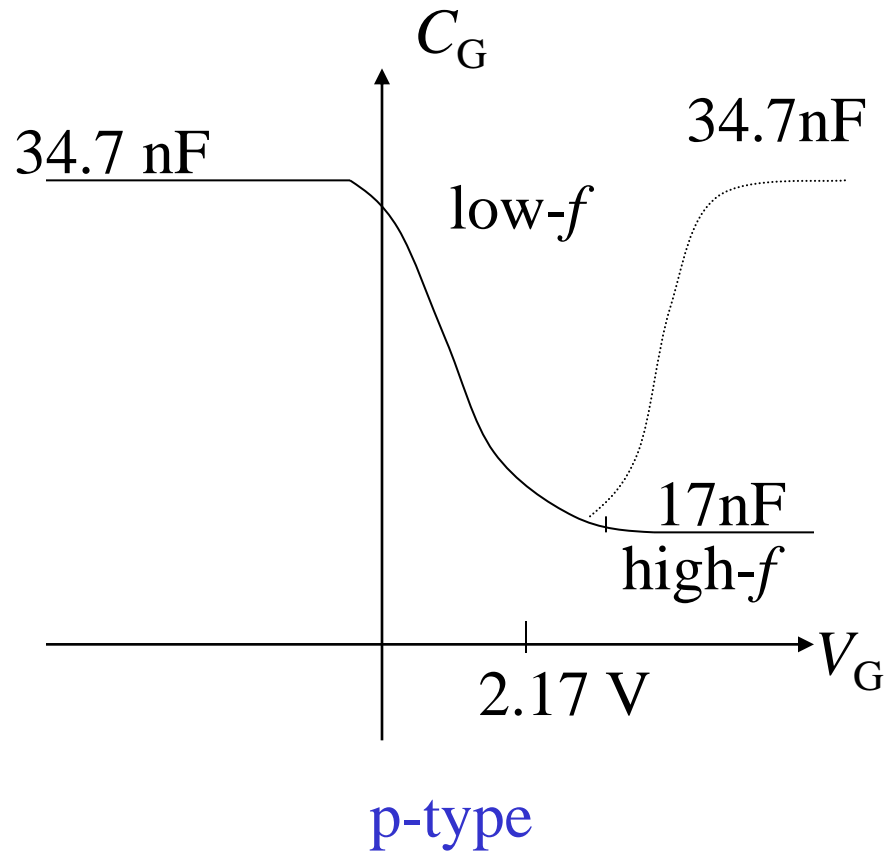
$$= 2.15 \text{ V}$$

Plot the C-V characteristics

Explain why C_G does not vary for $V_G > V_T$

Question: How will you calculate C_G when $V_G = 1V$?
Answer: Calculate ϕ_s when $V_G = 1V$ using the eqn. above. From ϕ_s find W, then calculate C_s. Then, calculate $C_G = (C_{ox} C_s) / (C_{ox} + C_s)$

C_G

34.7 nF

34.7nF

low-*f*

17nF
high-*f*

2.17 V

V_G

p-type

9

MOS-capacitor characteristics: Deep depletion

The previous discussions pertain to the condition when the gate voltage is ramped **slowly**, from accumulation condition to depletion and then to inversion condition. When the ramp rate is high, the inversion layer does not form and does not have time to equilibrate. This is called "deep depletion" condition. In this case, W will continue to increase beyond W_T and C_G will continue to decrease as shown when the dc bias is varied from accumulation bias to deep depletion bias.

To calculate W under deep depletion condition, invert the V_G versus ϕ_s relationship. Solve for $\phi_s^{1/2}$ and hence ϕ_s. Then, calculate W using W versus ϕ_s relationship.

Some observations

- V_T = gate voltage required for start of inversion
  = (+) for p-type Si
  = (−) for n-type Si

$$V_T = 2\phi_F + \left(\pm x_{ox} \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \sqrt{\frac{2qN_A}{\varepsilon_{Si}} |2\phi_F|} \right)$$

(+)	(+)	-	for p-type Si
(−)	(−)	-	for n-type Si

- Higher the doping, higher the $|V_T|$ value
- $C_{max} = C_{ox}$ and $C_{min} = C_{ox} C_s / (C_{ox} + C_s)$
- Lower the doping, lower C_s and hence lower C_{min}

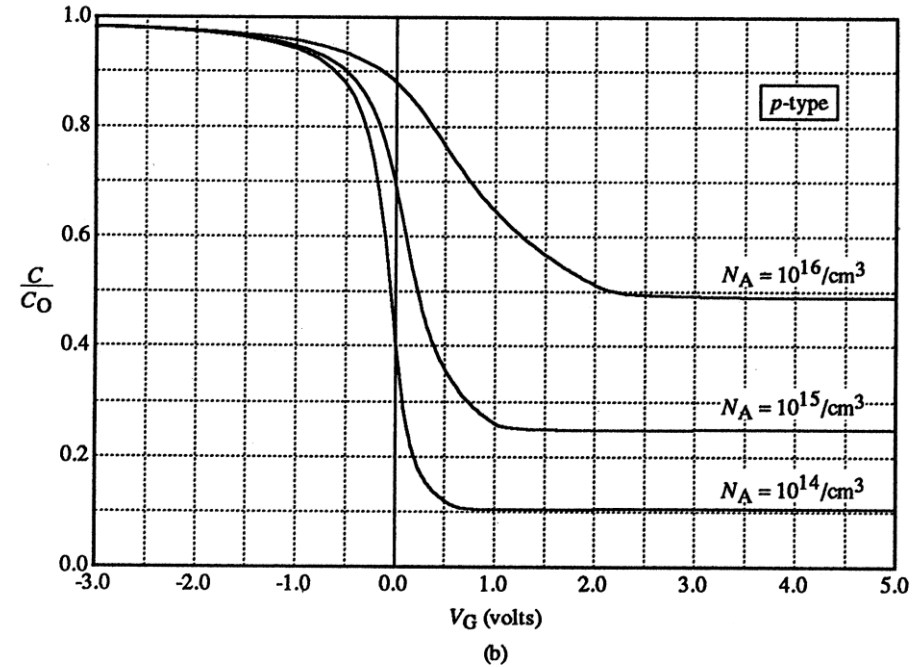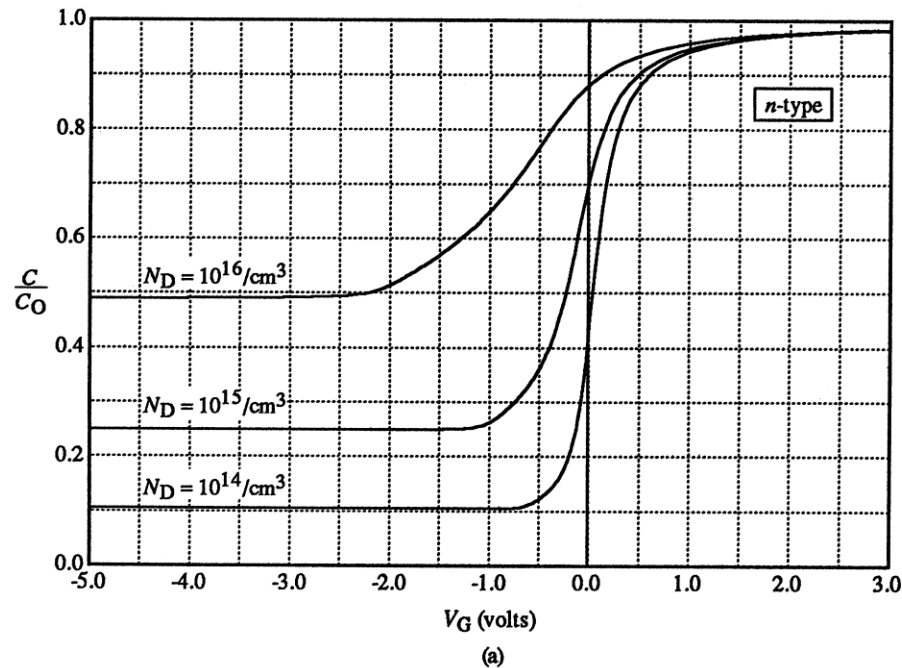# Doping dependence of MOS-capacitor high frequency C-V characteristics, with $x_{ox} = 0.1$ µm
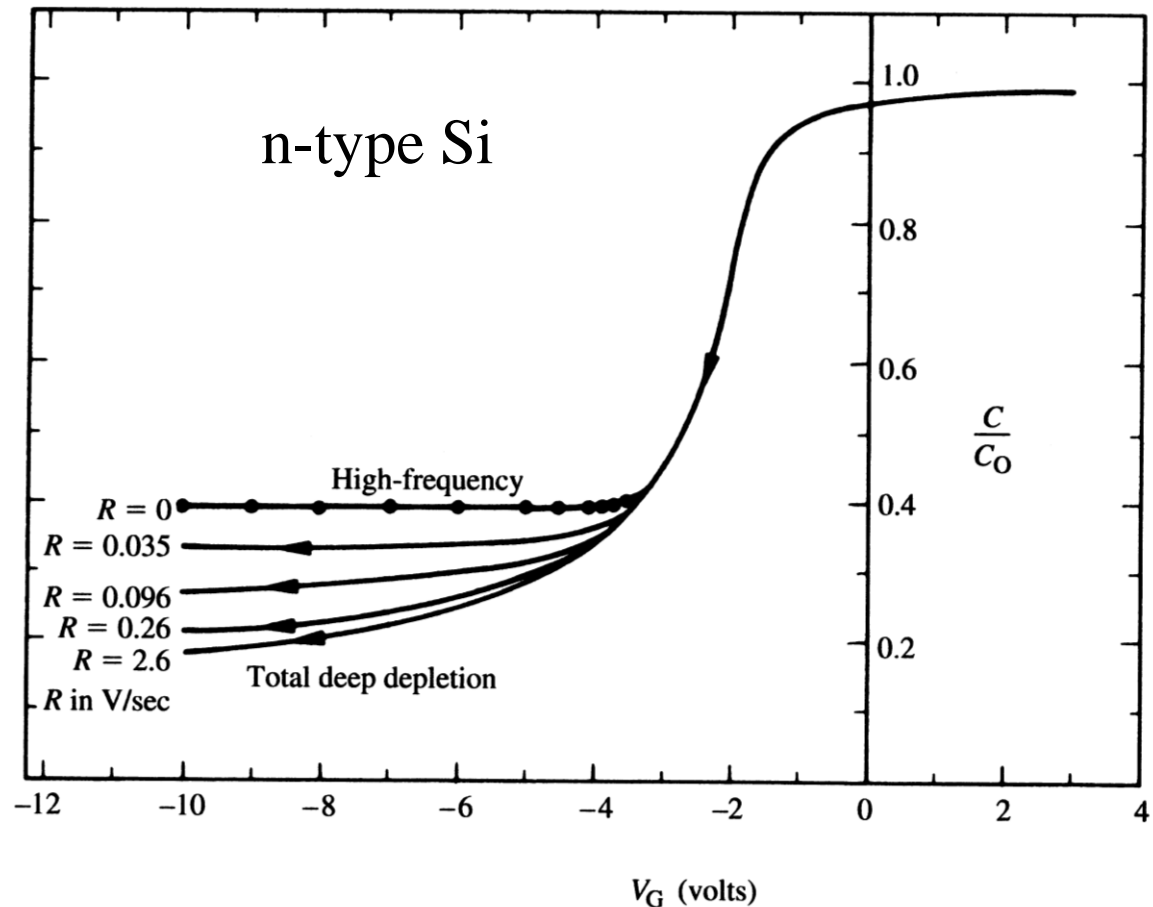

Figure 16.14

MOS-capacitor under deep depletion

$$V_G = \phi_s + x_{ox}\,\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\sqrt{\frac{2\,q\,N_A}{\varepsilon_{Si}}\,\phi_s}$$

$$W = \sqrt{\frac{2\,\varepsilon_{Si}}{q\,N_A}\,\phi_s}$$

$$C_s = \varepsilon_{Si}\,A\,/\,W$$

$$C_{ox} = \varepsilon_{ox}\,A\,/\,x_{ox}$$

$$C_G = C_{ox}\,C_s\,/\,(C_{ox} + C_s)$$

n-type Si

High-frequency

$R = 0$
$R = 0.035$
$R = 0.096$
$R = 0.26$
$R = 2.6$
R in V/sec

Total deep depletion

1.0

0.8

0.6

$\frac{C}{C_O}$

0.4

0.2

−12   −10   −8   −6   −4   −2   0   2   4

V_G (volts)

Example 2

Consider example 1. Plot C-V characteristics if V_G is varied from -5 V to $+5$ V **rapidly**.

$C_G (-5 \text{ V}) = C_{ox} = 34.7$ nF, as before.
$C_G (V_G = V_T) = 17$ nF, as before.

$C_G (V_G > V_T)$ will continue to reduce (unlike the quasi-steady state condition of example 1). When $V_G = 5$ V,

$$5 = \phi_s + 1000 \times 10^{-8} \times 3 \sqrt{\frac{2 \times 1.6 \times 10^{-19} 10^{16}}{10^{-12}}} \phi_s$$

$$= y^2 + 1.69 y \quad \text{where} \quad y^2 = \phi_s$$

Solving for ϕ_s , we get $\phi_s = 2.38$ V

$W = 0.545$ μm; $C_s = 18.3$ nF; $C_G = 12$ nF

Not under steady state

34.7 nF C_G

12 nF

2.15 V   5V V_G