Laboratory 5 (1 day):
Differential Amplifier

Material covered:

- This laboratory has ***one session*** allocated for completion.
  - Pre-Lab Exercise 1 is mandatory, please complete before the actual lab session.
  - Pre-Lab Exercise 2 is optional.
  - Exercise 1 is mandatory. Please proceed as far as you can get given the time available.
- Linear region of operation
- Differential gain, Common Mode gain, Common Mode Rejection Ratio (CMRR)
- Half-circuit model

Overview notes:

When setting up the pair of transistors for differential circuits, there is a tendency to rotate one of the transistors 180^{o} since that is how the circuits are typically drawn. Don't do that.

Discovery Board:

When using both Wave Generation channels of the Discovery Board to generate two sinusoids with a phase difference, it is necessary to trigger both channels at the same time. On the Wave Generation window, a Run All option appears as a tab in the upper left of the screen. Pressing that will start both channels and set the appropriate phase difference.

Pre-Lab Exercise 1

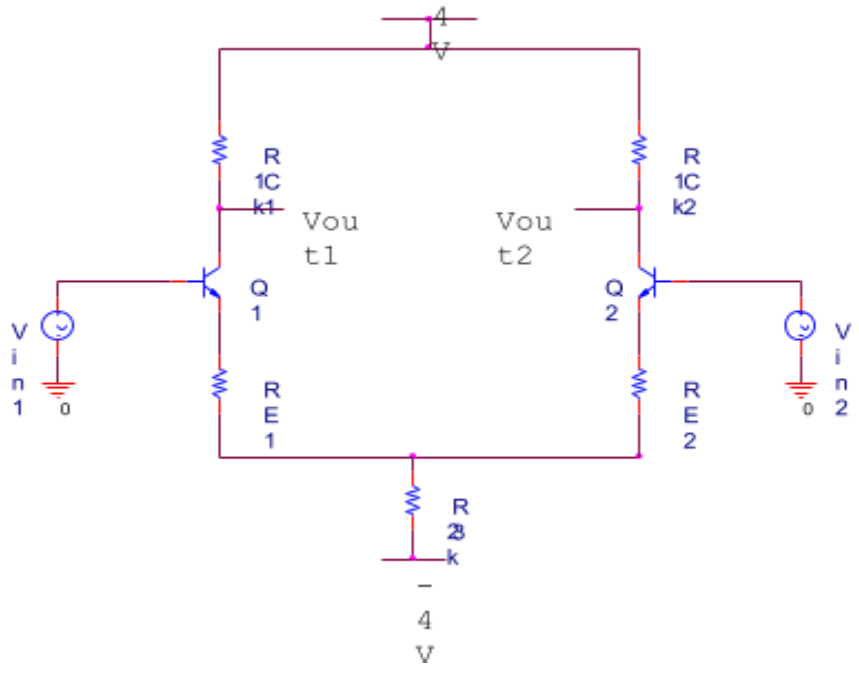

Figure 1: BJT differential amplifier

(R_{C1} = R_{C2} = 1 kΩ; Shared emitter resistor R_3 = 2 kΩ)

1. Build the circuit in PSpice with R_{E1} = R_{E2} = 0 Ω (grounded) Ground V_{in2} and run a DC sweep for V_{in1} (–2 to 2 V), plotting I_{C1} and I_{C2} versus V_{in1}.
   In your plot, estimate the range of V_{DM} (V_{DM} = V_{in1} – V_{in2} = V_{in}) such that both currents have approximately linear changes due to changes in V_{DM}.
2. Repeat step 1 with R_{E1} = R_{E2} = 25 Ω
3. Repeat step 1 with R_{E1} = R_{E2} = 100 Ω
4. Repeat step 1 with R_{E1} = R_{E2} = 500 Ω
5. Repeat step 1 with R_{E1} = R_{E2} = 5 kΩ
   Hint: Figure 8.18 of the Sedra & Smith textbook shows the curves to expect:

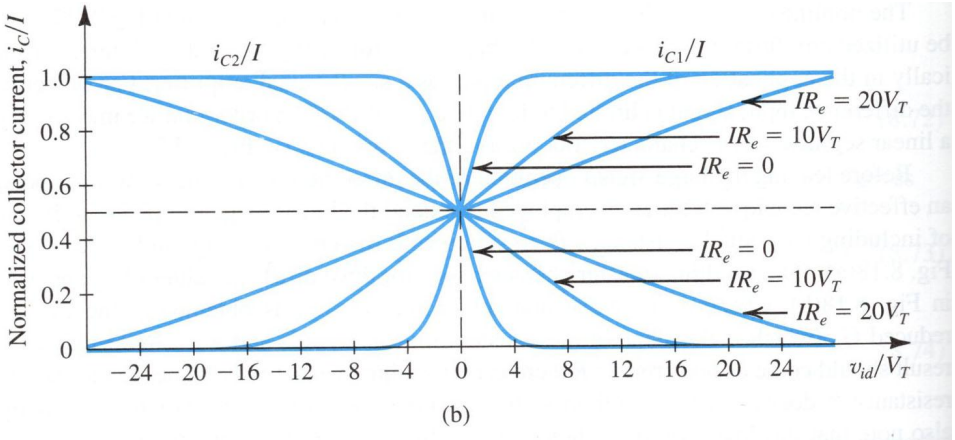

Figure 8.18 The transfer characteristics of the BJT differential pair **(a)** can be linearized **(b)** (i.e., the linear range of operation can be extended) by including resistances in the emitters.

Pre-Lab Exercise 2

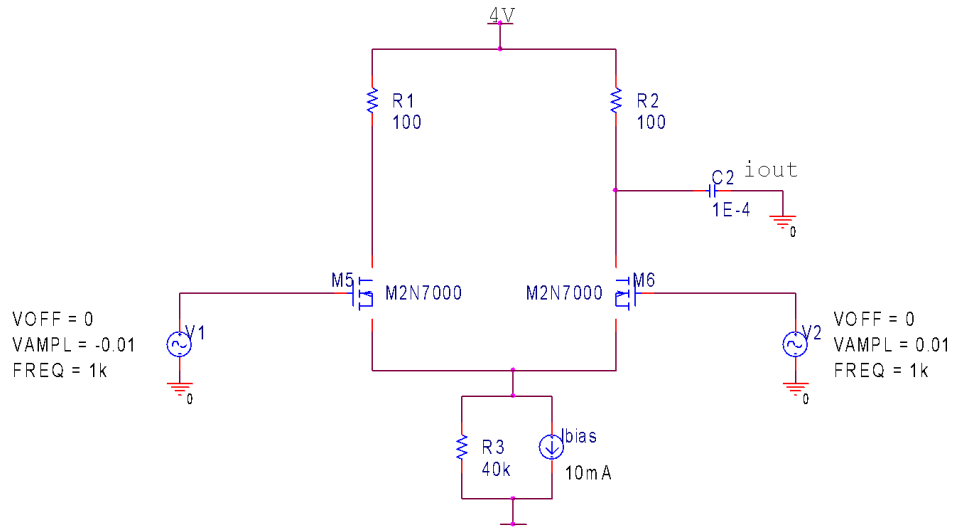

Figure 2: BJT differential amplifier with passive loads (R_1, R_2)

1. Build the above circuit in PSpice and measure the output current, i_{out}. The inputs are differential, as indicated by the signs of the amplitude for the two inputs.

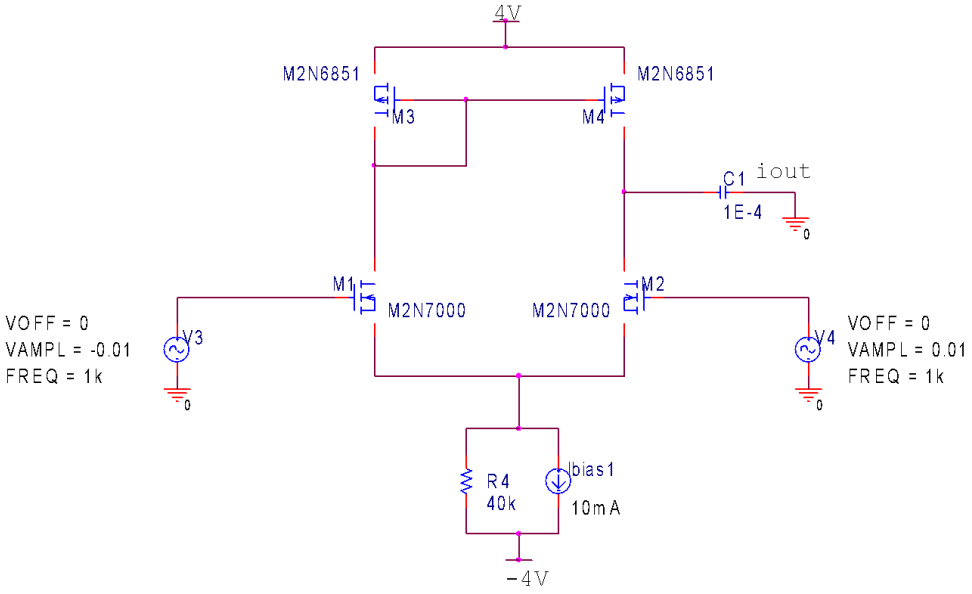

Figure 3: BJT differential amplifier with active loads (M3, M4)

1. Build the above circuit in PSpice and measure the output current, i_{out}. Again, the inputs are differential. M3 and M4, are PMOS components in the pwrmos library, M2N6851. Be careful when placing the components, the default orientation is vertically inverted relative to what is shown in the above circuit.

   Did the small signal output current double, as expected with the active load?

Exercise 1: Differential inputs

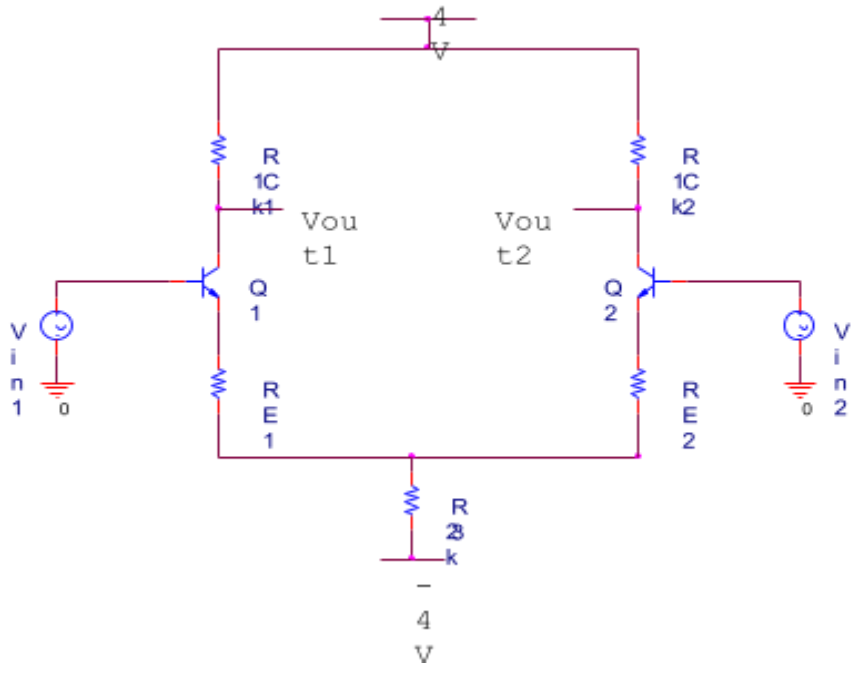

Figure 4: BJT differential amplifier

($R_{C1} = R_{C2} = 1$ kΩ; Shared emitter resistor $R_3 = 2$ kΩ)

1. Build the differential amplifier shown in Figure 4, using $R_{E1} = R_{E2} = 0$ Ω.

2. With both V_{in1} and V_{in2} grounded (equal to each other), compare V_{out1} and V_{out2}.

   Are they equal as expected? If they are not equal, is resistor tolerance sufficient to explain the error, i.e. less than 5 % error?

3. Measure I_C and V_{CE} to determine the DC bias conditions of each transistor.

4. Connect both inputs together to the same voltage source with a 200 mV peak-to-peak 1 kHz sine wave with zero offset. For the common mode (CM) input, measure the differential output voltage, i.e. the voltage $V_{out2} – V_{out1}$. Determine the common mode gain, $A_{CM} = (V_{out2} – V_{out1}) / V_{CM}$

   Is the differential output close to zero? If not (which is likely), in context of your part 2 answer, is the difference explained by resistor tolerances? transistor characteristics?

5. For the same common mode input, measure the output at just V_{out1}. Determine the half circuit gain, $A_{CM\text{-}HC} = V_{out1} / V_{CM}$.

   Is the gain consistent with the common mode half-circuit amplifier model?

6. Set $R_{E1} = R_{E2} = 470$ Ω and repeat steps 2-5.

7. Keeping the emitter resistors, set V_{in1} to 50 mV and V_{in2} to –50 mV (180° phase shift). Measure the differential mode (DM) gain, $A_{DM} = (V_{out2} – V_{out1}) / (V_{in2} – V_{in1})$.

Is the gain consistent with the estimate using the half circuit model?

8. The Common Mode Rejection Ratio (CMRR) is defined as CMRR = A_{DM} / A_{CM} = 10 $\log_{10} (A_{DM} / A_{CM})^2$ dB. Based on your above results, what is the CMRR?

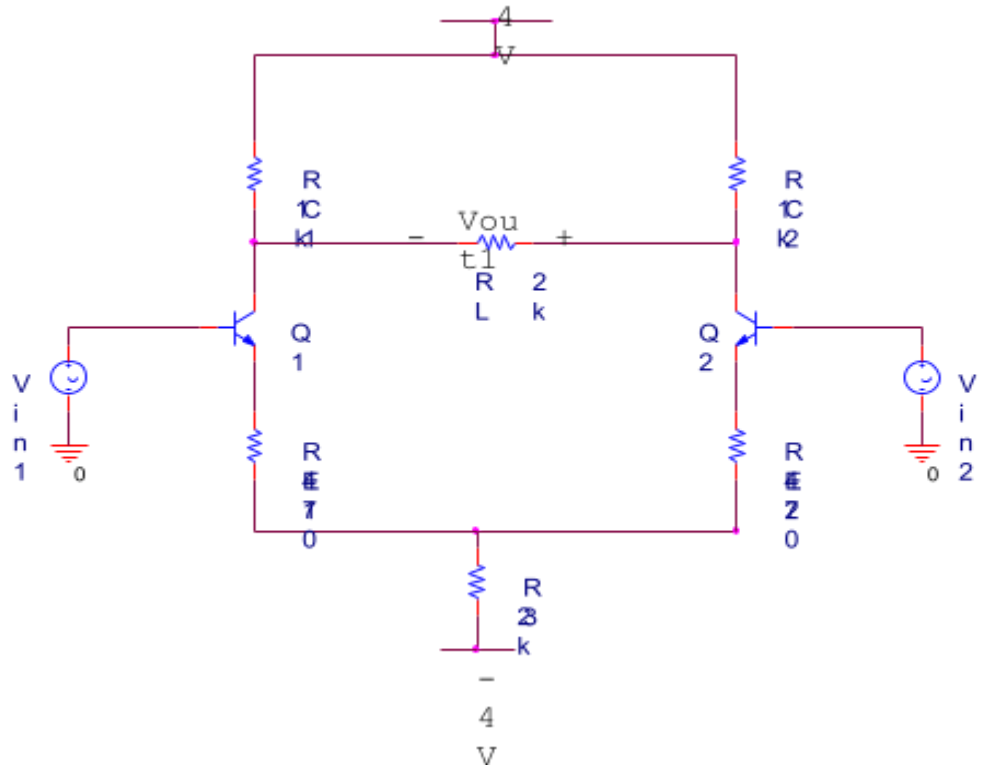

Figure 5: BJT differential amplifier

(R_{C1} = R_{C2} = 1 kΩ; Shared emitter resistor R_3 = 2 kΩ)

9. Add a 2 kΩ load resistor. Apply the same common mode and differential mode inputs as above.

   Is the common mode output approximately the same with and without the load resistor?

   Is the differential output approximately one-half the open circuit gain?

10. Based on your above results, what is the CMRR?