Chapter 7. Small-signal admittance

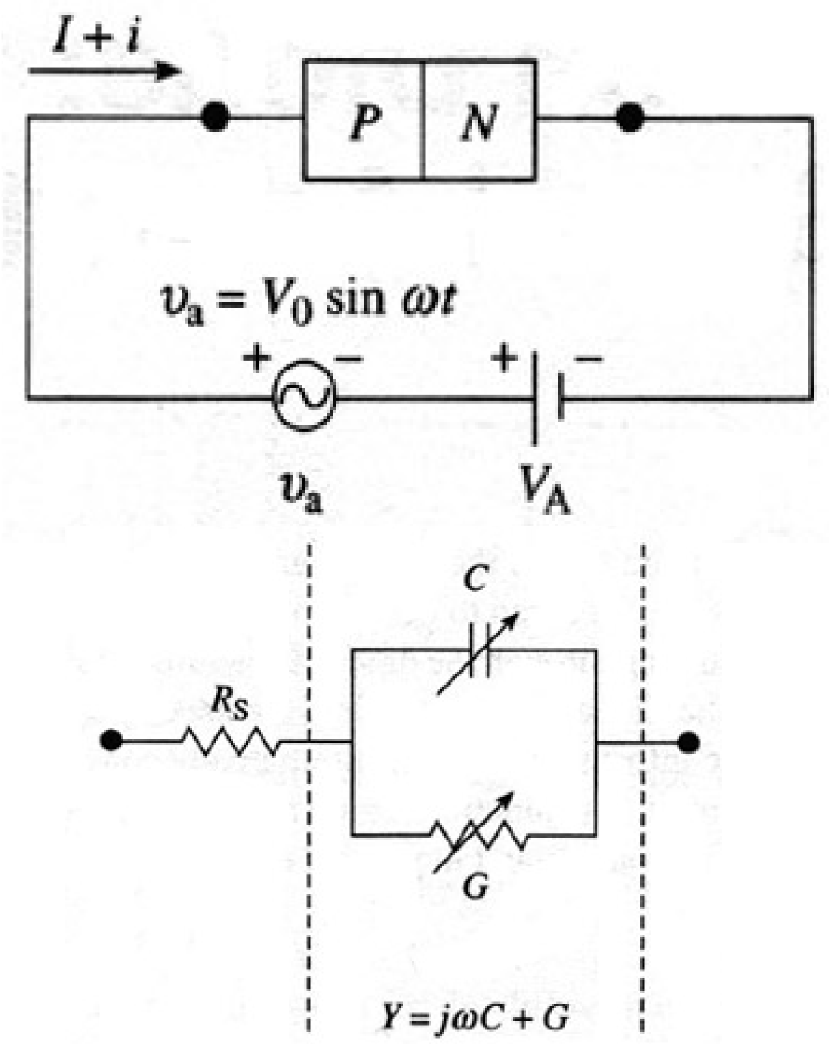
We will study the small signal response of the pn junction diode. A small ac signal (v_a) is superimposed on the DC bias. This results in ac current (i). Then, admittance Y is given by:

$$Y = \mathrm{i} / v_a = G + \mathrm{j}\omega C$$

Specifically, the following parameters will be studied:

- Reverse bias junction or depletion layer capacitance
- Forward bias diffusion or charge storage capacitance
- Forward and reverse bias conductance.

Capacitance measurements



I = DC

i = ac

Y = admittance

$$= \frac{i}{v_{ac}} = G + j\omega C$$

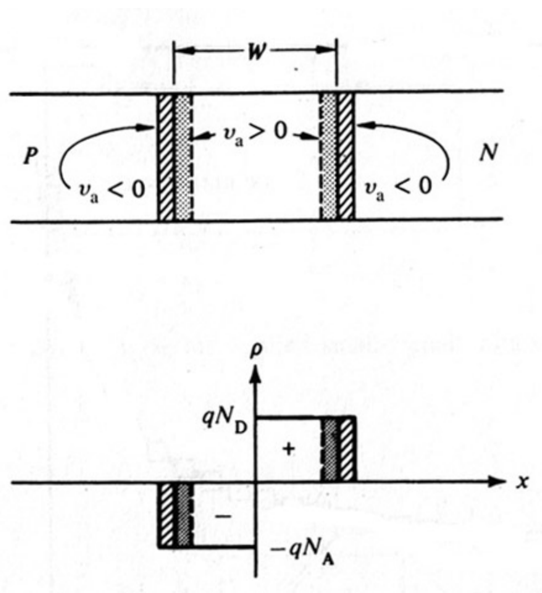
i and v_a depend on the applied DC bias

Model for a diode under ac

Reverse bias junction capacitance

A pn junction under reverse bias behaves like a capacitor.

Such capacitors are used in ICs as voltage-controlled capacitors.



Depletion layer width under small ac superimposed on DC bias voltage.

Looks similar to a parallel plate capacitor.

$$\boxed{C_j = \frac{\varepsilon_{Si} A}{W}}$$

where W is the depletion-layer width under DC bias.

Reverse bias junction capacitance

$$W = \left[\frac{2\varepsilon_{Si}}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} - V_A)\right]^{1/2}$$

For pn junction

$$= \left[\frac{2\varepsilon_{Si}}{qN_B}(V_{bi} - V_A)\right]^{1/2}$$

For p^+n or pn^+ junction where N_B is the doping on the lightly doped side

$$C_J = \frac{\varepsilon_{Si} A}{W} = A\left(\frac{\varepsilon_{Si}\, q\, N_B}{2(V_{bi} - V_A)}\right)^{1/2}$$

For asymmetrically doped junction

C_J increases with $N_B^{1/2}$

C_J decreases with applied reverse bias

Parameter extraction/profiling

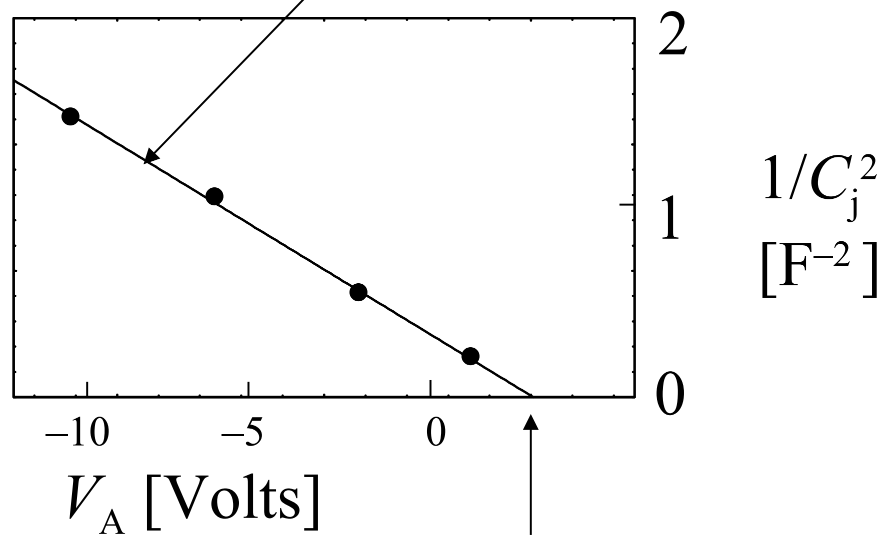
C-V data from a pn junction is routinely used to determine the doping profile on the lightly doped side of the junction.

$$C_J = \frac{\varepsilon_{Si} A}{W} = A\left(\frac{\varepsilon_{Si}\, q\, N_B}{2(V_{bi} - V_A)}\right)^{1/2}$$

$$\frac{1}{C_J^2} = \frac{2}{A^2 q N_B \varepsilon_{Si}}(V_{bi} - V_A)$$

If the doping on the lightly doped side is uniform, a plot of $1/C_J^2$ versus V_A should be a straight line with a slope inversely proportional to N_B and an extrapolated $1/C_J^2 = 0$ intercept equal to V_{bi}.

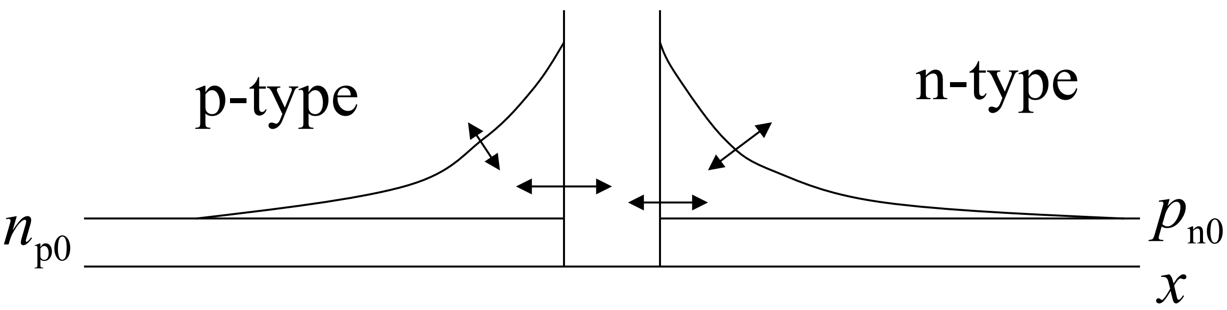
$$\text{Slope} = \frac{2}{qN_B\varepsilon_{Si}A^2}$$



Intercept = V_{bi}

Forward bias diffusion capacitance, C_D

C_D is also called the charge storage capacitance. The variation of the injected minority-carrier charge, which is a function of the applied bias, results in the diffusion capacitance. Both C_J and C_D are always present, but for the forward-bias case, C_D becomes dominant.



Origin of diffusion capacitance

For a p$^+$n junction, $I = Q_p/\tau_p$ where Q_p is total excess charge in n-side

$$Q_p = I\tau_p = qA\frac{D_p\tau_p}{L_p}p_{n0}\left[\exp\left(\frac{qV_A}{kT}\right)-1\right] \approx qAL_p\, p_{n0}\, e^{\frac{qV_A}{kT}}$$

$$C_D = \frac{dQ_p}{dV} = \frac{q}{kT}qAL_p p_{n0}\exp\left(\frac{qV_A}{kT}\right) = \frac{q}{kT}I\,\tau_p$$

Forward bias conductance

$$G_D = \frac{dI}{dV} = \frac{qAD_p p_{n0}}{L_p} \frac{d}{dV}\left(e^{\frac{qV_A}{kT}}\right) = \frac{q}{kT} I$$

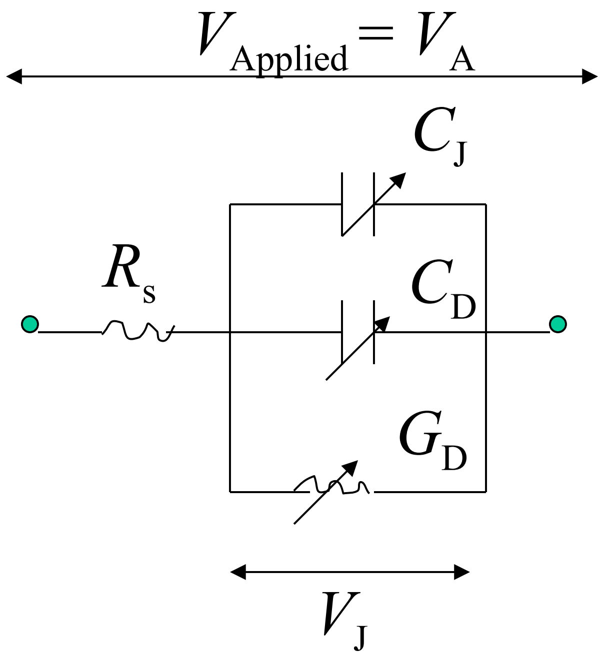
Assumes

$\omega\tau_p << 1$

Complicated at higher frequencies.

$$\boxed{G_D = \frac{q}{kT} I}$$

$$\boxed{C_D = \frac{q}{kT} I \tau_p}$$



Equivalent circuit for a diode

Example

Problem: Consider a p^+n junction forward biased such that the forward current is 1 mA. Assume the lifetime of holes is 10^{-7} s. Calculate the diffusion capacitance and the diffusion resistance.

Solution: $C_D = 3.86$ nF $\quad\quad r_d = 1/G_D = 25.9\ \Omega$

The current through the depletion layer will mostly be carried by (holes, electrons: choose one)?

Plot the current carried by the holes and electrons through the n-type region, assuming that the diffusion length of holes is 1 μm.