Laboratory 8 (1 day):
Digital circuits

Material covered:

- This laboratory has ***one session*** allocated for completion:
  - Mandatory: Pre-Lab Exercise 1 and Exercise 1. Optional: Exercise 2
- Transistor-resistor logic
- Transistor-transistor logic
- Digital circuits

Propagation delay:

The ***propagation delay*** is the time it takes for the digital output to change after the digital input changes. It is defined as the time difference between when the input is halfway between $V_{\text{In,Low}}$ and $V_{\text{In,High}}$ to when the output is halfway between $V_{\text{Out,Low}}$ and $V_{\text{Out,High}}$. The two times are defined as $t_{\text{P,LH}}$ (output transitions from LO to HI) and $t_{\text{P,HL}}$ (output transitions from HI to LO). An example for an inverter circuit is shown below. The **red line is the input** and the **green line is the output**.

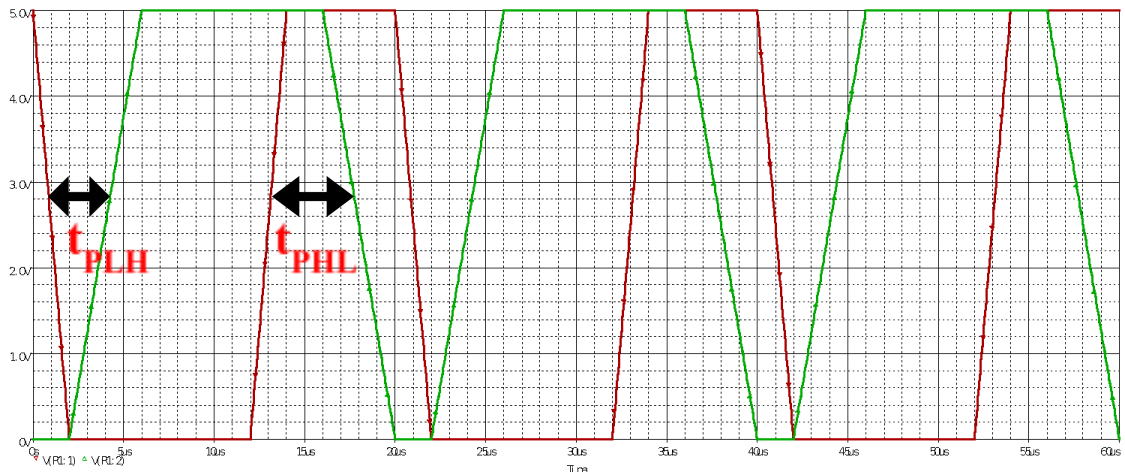

Figure 1: Inverter timing diagram (input and output)

Pre-Lab Exercise 1

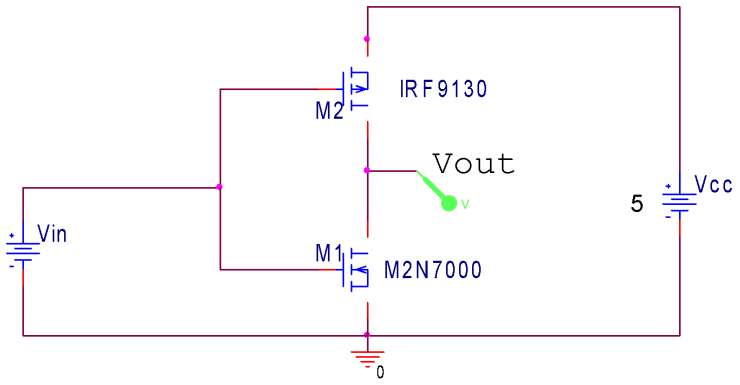

Figure 2: CMOS inverter (M1 = N-channel FET; M2 = P-channel FET)

1. Simulate the circuit shown above. Note, the PMOS transistor needs to be 'mirrored vertically' so that the source is on the 'top'. You can change the orientation of a component by right clicking on it. Set the simulation to a DC voltage sweep for $0 < V_{in} < 5$ V.
   Estimate the output high voltage, the output low voltage, the low noise margin and the high noise margin.

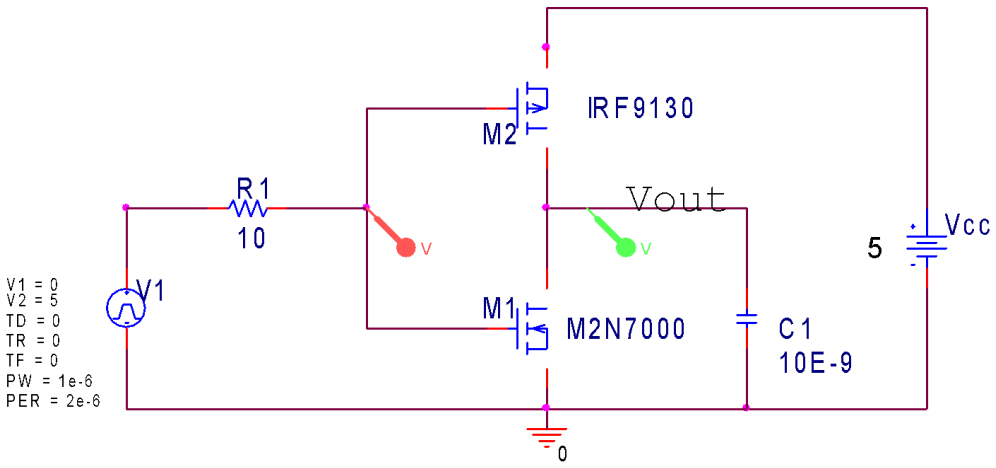

Figure 3: CMOS inverter (M1 = N-channel FET; M2 = P-channel FET)

2. Add an input side resistance and an output side capacitance. Set V_{in} to a pulse stream with a 50% duty cycle and a 2 µs period.
   Estimate the propagation delay as the output switches from LO to HI and from HI to LO.

Exercise 1: CMOS inverter

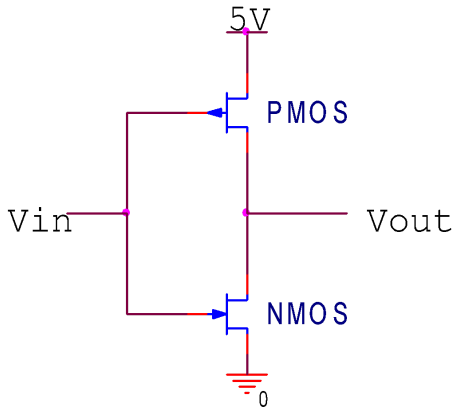

Figure 4: CMOS inverter

1. Build the circuit above using the IRF9120 PMOS and 2N7000 NMOS transistors. Set the input signal to a 10 Hz sawtooth triangle wave, oscillating between 0 V and 5 V.

2. Use the *x-y* channel to plot the voltage transfer function, V_{out} versus V_{in}.

   Determine the LO and HI output voltages, $V_{Out,Low}$ and $V_{Out,High}$.
   Estimate the high and low noise margins.

3. Add a 10 nF capacitor at the load (V_{out}) and change the input signal to a square wave. You will need to 'zoom in' to see the t_{PLH} and t_{PHL}. In order to do that, you need to set the horizontal axis to ~100 ns/div. The triggering must also be set correctly. Set the triggering source to the oscilloscope channel connected to the input and the triggering level to ~2 V. You can change the condition ("Cond.") to Rising and Falling, giving you the two different propagation delays.

   Estimate the propagation delays.

$\boldsymbol{V_{OL}}$ (Output voltage – Low)	
$\boldsymbol{V_{OH}}$ (Output voltage – High)	
$\mathbf{NM_{Low}}$ (Noise margin – Low)	
$\mathbf{NM_{High}}$ (Noise margin – High)	
$\boldsymbol{t_{PLH}}$ (Propagation delay – L-to-H)	
$\boldsymbol{t_{PHL}}$ (Propagation delay – H-to-L)	

Exercise 2: Logic circuits

Design an OR or an AND gate (you choose). You may use any type of circuit design. Build the circuit and verify the truth table.

Estimate the propagation delays for the gate. You only need to change one input such that the output toggles.