## Integrated circuits (I

ICS use two types of FETS

N-channel

P-channel

G of S

G - 13

-IL

-4L

VHR > 0

 $V_{HR} < 0$ 

Both FETs are enhancement-type FETS.

 $\Rightarrow V_{GS} = 0 \Rightarrow I_D = 0$ 

In real devices, there is no difference between S and D. => No difference in circuit symbols between S and D.

In ICs, resistors are to be avoided.

Q: Why? => Because resistors generate

In ICs, transistors are either ON  $(R_{ON}=0)$  or OFF  $(R_{OFF}=00)$ 

Q: Do transistors generate heat? If RON = 0 and ROFF = 00, no heat is generated.

Nevertheless, heat generation is a major problem in Si IC technology.

Q: Is a fan a good solution? => Not really, because we do not like fans (noise).

## Example:

## GMOS inverter



$$V_{\text{In}} = OV \implies T_1 = ON \qquad T_2 = OFF$$

$$\implies V_{\text{out}} = V_{\text{cc}} = 5V$$

$$V_{\text{In}} = 5V \implies T_1 = OFF \qquad T_2 = ON$$

$$\implies V_{\text{out}} = GND = OV$$

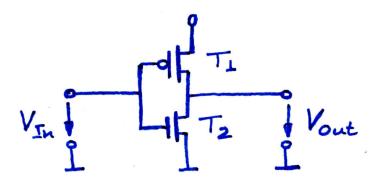
- We have an inverter.

=> This is called a GMOS inverter

=> GMOS technology
L= C = Complementary

CMOS => Always N& P-channel FETS

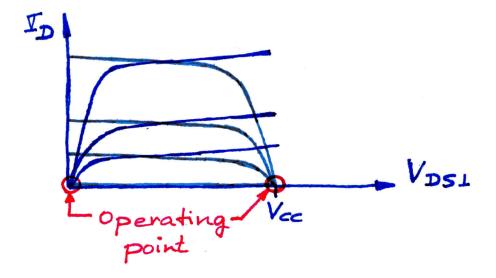
## Load line of GMOS inverter



$$V_{CC} = V_{DSL} + V_{DS2}$$

$$\mathcal{I}_{\mathcal{D}} = \mathcal{I}_{\mathcal{D}} = \mathcal{I}_{\mathcal{D}2}$$

$$V_{DS2} = V_{Cc} - V_{DS1}$$



Convince yourself that these are the two operating points of the GMOS inverter.

- GMOS highy advantageous technology > >95% of ICs are CMOS ICs.
- Q: What is the great advantage of a GMOS circuit?

Static power consumption is zero.

- Q: Is CMOS power consumption zero in practice?
  - No, because parasitic capacitances

    need to be charged and discharged,

    causing some resistive power losses.

    Ron is close to zero but not zero.