Chapter 17-1. MOSFET

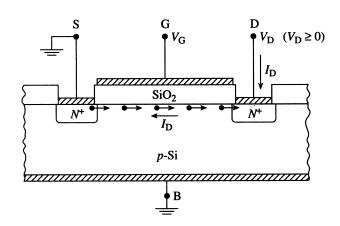
MOSFET based ICs have become dominant technology in the semiconductor industry.

We will study the following in this chapter:

Qualitative theory of operation

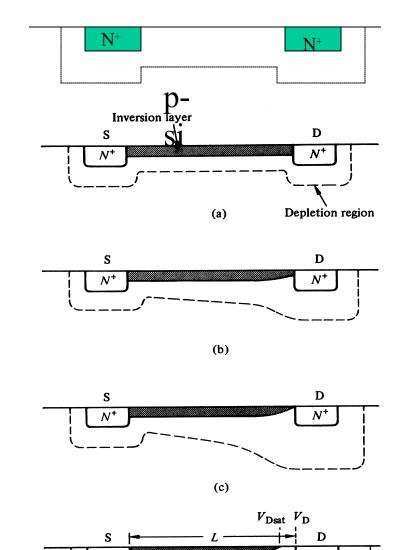
Quantitative I_D -versus- V_{DS} characteristics

Small-signal equivalent circuits.



N-channel MOSFET Substrate: p-type Si

Qualitative discussion: NMOS



(d)

 $0 < V_{\rm G} < V_{\rm T}$; $V_{\rm DS}$ small or large no channel, no current

$$V_{\rm G} > V_{\rm T}$$
; $V_{\rm DS} \approx 0$
 $I_{\rm D}$ increases with $V_{\rm DS}$

 $V_{\rm G} > V_{\rm T}; \ V_{\rm DS} \ {\rm small}, > 0$ $I_{\rm D}$ increases with $V_{\rm DS}$, but rate of increase decreases.

 $V_{\rm G} > V_{\rm T}; \ V_{\rm DS} \approx {\rm pinch-off}$ $I_{\rm D}$ reaches a saturation value, $I_{\rm D,sat}$ The $V_{\rm DS}$ value is called $V_{\rm DS,sat}$

$$V_{\rm G} > V_T$$
; $V_{\rm DS} > V_{\rm DS,sat}$
 $I_{\rm D}$ does not increase further, saturation region.

$I_{\underline{D}}$ - $V_{\underline{DS}}$ characteristics for NMOS derived from qualitative discussions

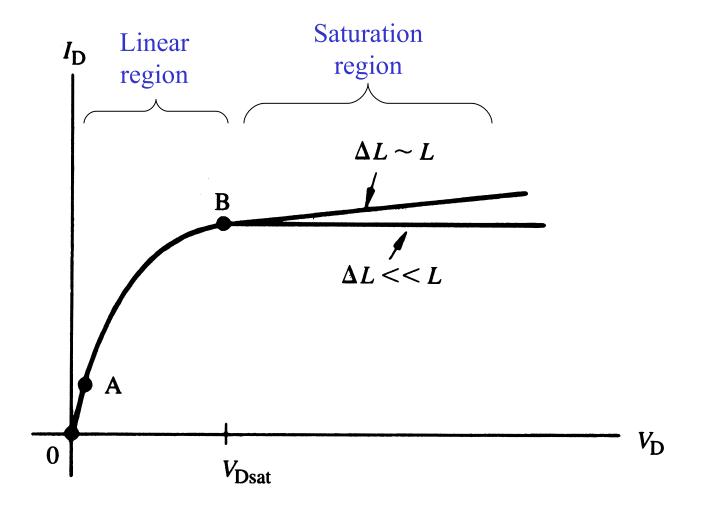


Figure 17.3

$I_{\underline{D}}$ - $V_{\underline{DS}}$ characteristics expected from a long channel ($\Delta L << L$) MOSFET (n-channel), for various values of $V_{\underline{G}}$

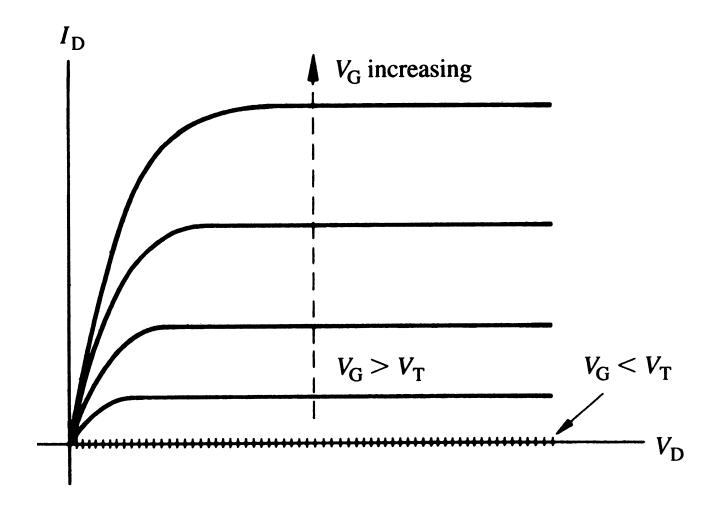


Figure 17.4

Threshold voltage for NMOS and PMOS

When $V_G = V_T$, $\phi_s = 2 \phi_F$; using equation 16.28, we get expression for $V_{\rm T}$.

$$V_{\rm T} = 2 \phi_{\rm F} + x_{\rm ox} \frac{\epsilon_{\rm Si}}{\epsilon_{\rm ox}} \sqrt{\frac{2q N_{\rm A}}{\epsilon_{\rm Si}}} 2 \phi_{\rm F}$$

Ideal n-channel (p-silicon) device both terms positive

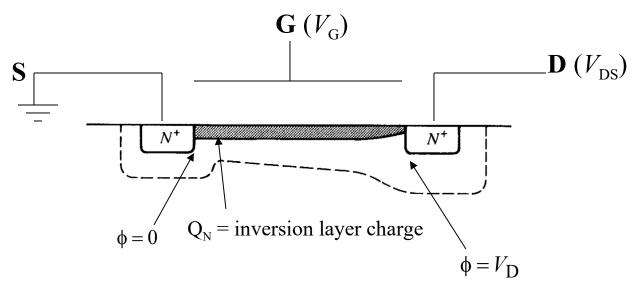
$$V_{\rm T} = 2\phi_{\rm F} + \left(-x_{\rm ox} \frac{\varepsilon_{\rm Si}}{\varepsilon_{\rm ox}} \sqrt{\frac{2qN_{\rm D}}{\varepsilon_{\rm Si}}} | 2\phi_{\rm F} | \right)$$
 Ideal p-channel (n-silicon) device

both terms negative

$$\varepsilon_{\text{Si}}/\varepsilon_{\text{ox}} = (\varepsilon_{\text{r,Si}} \varepsilon_0)/(\varepsilon_{\text{r,ox}} \varepsilon_0) = 11.9/3.9 \approx 3$$

 $\varepsilon_{\rm r,Si} = 11.9 = {\rm relative\ dielectric\ constant\ of\ Si}$ ε_0 = absolute dielectric constant = $8.85 \times 10^{-12} \,\mathrm{A\,s/(V\,m)}$

Quantitative I_D - V_{DS} relationships



Let ϕ be the potential along the channel

For $V_G \le V_T$, Inversion layer charge is zero.

For
$$V_G > V_T$$
, $Q_n(y) = -Q_G = -C_{ox}(V_G - \phi - V_T)$

In general, $J_n = q \mu_n n \mathcal{E}$ when the diffusion current is neglected. Here, current I_D is the same everywhere, but J_n (current density) can vary from position to position.

Device structure, dimension, and coordinate orientations assumed in the quantitative analysis

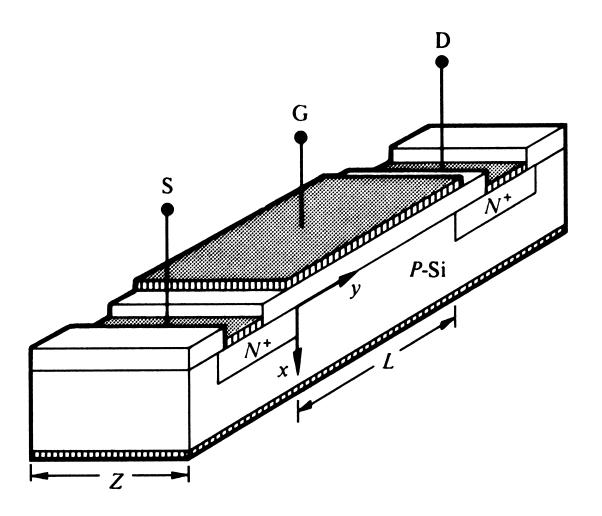


Figure 17.6

Quantitative I_D - V_{DS} relationships (Shockley model)

$$J_{\rm n} = J_{\rm ny} = q\mu_{\rm n}n\mathcal{E} = -q\mu_{\rm n}n\frac{\mathrm{d}\phi}{\mathrm{d}y}$$
 since $\mathcal{E}(y) = -\frac{\mathrm{d}\phi}{\mathrm{d}y}$

To find current, we have to multiply the above with area, but J_{ny} , n, etc. are functions of x and z. Hence,

$$I_{\rm D} = \iiint J_{\rm ny} \, \mathrm{d}x \, \mathrm{d}z = Z \iint J_{\rm ny} \, \mathrm{d}x = -Z \mu_{\rm n} \frac{\mathrm{d}\phi}{\mathrm{d}y} \iint q n \, \mathrm{d}x$$
$$= -Z \mu_{\rm n} \frac{\mathrm{d}\phi}{\mathrm{d}y} Q_{\rm n}(y) \qquad Q_{\rm n}(y) = \text{charge/unit area}$$

Integrating the above equation, and noting that I_D is constant, we get

$$I_{\rm D} = -\frac{Z}{L} \mu_{\rm n} \int_{0}^{V_{\rm DS}} Q_{\rm n}(y) \, \mathrm{d}\phi$$
Since we know expression for $Q_{\rm n}(y)$ in terms of ϕ , we can integrate this to get $I_{\rm D}$

Quantitative I_D - V_{DS} Relationships (cont.)

$$I_{\rm D} = \frac{Z\mu_{\rm n}}{L} C_{\rm ox} \left[(V_{\rm G} - V_{\rm T}) V_{\rm DS} - \frac{V_{\rm DS}^2}{2} \right] \qquad 0 < V_{\rm DS} < V_{\rm DS,sat} \; ; \quad V_{\rm G} > V_{\rm T}$$

 $I_{\rm D}$ will increase as $V_{\rm DS}$ is increased, but when $V_{\rm G} - V_{\rm DS} = V_{\rm T}$, pinchoff of channel occurs, and current saturates when $V_{\rm DS}$ is increased further. This value of $V_{\rm DS}$ is called $V_{\rm DS,sat}$. i.e., $V_{\rm DS,sat} = V_{\rm G} - V_{\rm T}$ and the current when $V_{\rm DS} = V_{\rm DS,sat}$ is called $I_{\rm DS,sat}$.

$$I_{\text{D,sat}} = \frac{Z \mu C_{\text{ox}}}{2L} (V_{\text{G}} - V_{\text{T}})^2$$
 $V_{\text{D}} > V_{\text{DS,sat}}$; $V_{\text{G}} > V_{\text{T}}$

Here, C_{ox} is the oxide capacitance per unit area, $C_{\text{ox}} = \varepsilon_{\text{ox}} / x_{\text{ox}}$

Example 1

Plot the I_D vs. V_{DS} characteristics for an NMOS with the following parameters:

Substrate doping: 10^{16} cm⁻³. Oxide thickness = 100 nm Gate width = 15 µm; Gate length = 1 µm. Assume $\mu_n = 500$ cm²/(Vs)

Find
$$C_{\text{ox}}$$
: $C_{\text{ox}} = \varepsilon_{\text{ox}} / x_{\text{ox}} = 33.3 \text{ nF/cm}^2$

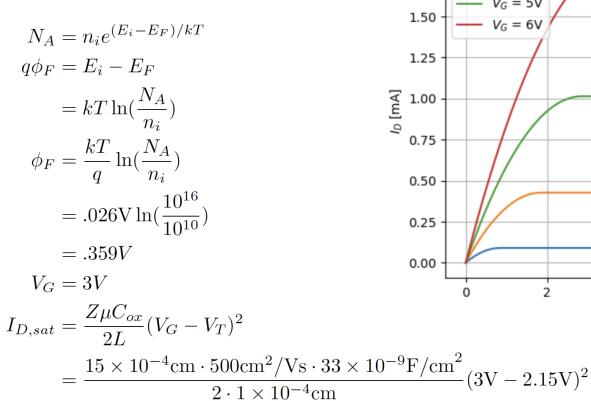
$$V_{\rm T} = 2\phi_{\rm F} + x_{\rm ox} \frac{\varepsilon_{\rm Si}}{\varepsilon_{\rm ox}} \sqrt{\frac{2q N_{\rm A}}{\varepsilon_{\rm Si}}} 2\phi_{\rm F} = 2.15 \text{ V}$$

$$I_{\text{D,sat}} = \frac{Z \mu C_{\text{ox}}}{2I} (V_{\text{G}} - V_{\text{T}})^2$$
 $V_{\text{DS}} > V_{\text{DS,sat}}$; $V_{\text{G}} > V_{\text{T}}$

$$V_{\mathrm{DS,sat}} = V_{\mathrm{G}} - V_{\mathrm{T}}$$

Find $I_{D,sat}$ for different values of V_G and plot the graph

Solution



 $= 89.4 \mu A$

