Hayden Fuller
662028619

1)Logic expressions
ABgtCD <= (A AND (NOT C)) OR ((NOT D) AND ((B AND (NOT C)) OR (B AND A)));
ABeqCD <= (NOT ((B OR D) AND (NOT (B AND D)))) AND (NOT ((A OR C) AND (NOT (A AND C))));
ABltCD <= (C AND (NOT A)) OR (((D AND C) AND (NOT B)) OR (((NOT A) AND (NOT B)) AND D));

2)VHDL

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity fuller_hayden_studio1 is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C : in STD_LOGIC;
           D : in STD_LOGIC;
           ABgtCD : out STD_LOGIC;
           ABeqCD : out STD_LOGIC;
           ABltCD : out STD_LOGIC);
end fuller_hayden_studio1;

architecture Behavioral of fuller_hayden_studio1 is

begin
ABgtCD <= (A AND (NOT C)) OR ((NOT D) AND ((B AND (NOT C)) OR (B AND A)));
ABeqCD <= (NOT ((B OR D) AND (NOT (B AND D)))) AND (NOT ((A OR C) AND (NOT (A AND
C))));
ABltCD <= (C AND (NOT A)) OR (((D AND C) AND (NOT B)) OR (((NOT A) AND (NOT B)) AND
D));

end Behavioral;
```

3)XDC

```
set_property PACKAGE_PIN W5 [get_ports CLK100MHZ]

        set_property IOSTANDARD LVCMOS33 [get_ports CLK100MHZ]
        create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports
CLK100MHZ]

# Switches
set_property PACKAGE_PIN V17 [get_ports {A}]
        set_property IOSTANDARD LVCMOS33 [get_ports {A}]
set_property PACKAGE_PIN V16 [get_ports {B}]
        set_property IOSTANDARD LVCMOS33 [get_ports {B}]
set_property PACKAGE_PIN W16 [get_ports {C}]
        set_property IOSTANDARD LVCMOS33 [get_ports {C}]
set_property PACKAGE_PIN W17 [get_ports {D}]
        set_property IOSTANDARD LVCMOS33 [get_ports {D}]

# LEDs
set_property PACKAGE_PIN U16 [get_ports {ABgtCD}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ABgtCD}]
set_property PACKAGE_PIN E19 [get_ports {ABeqCD}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ABeqCD}]
set_property PACKAGE_PIN U19 [get_ports {ABltCD}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ABltCD}]
```

4)testing
I flipped the switches in “binary order” and checked if each output was correct, which they all were.

5)summary
It would have been much easier to do this if we had already been introduced to SOP expressions first, though I don’t know why I didn’t think of doing it that way in the lab and instead went through the logic behind each with other logic gates and then converting everything to AND OR NOT