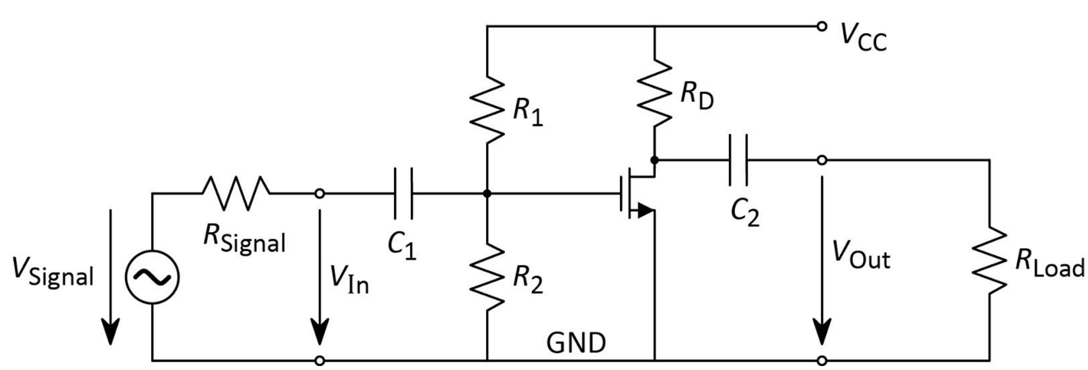
Homework 10

1. ***FET amplifier circuits***: The present problem concerns common-source, common-drain, and common-gate amplifier circuits. Assume that the amplifiers do not have a gate-biasing-resistor network.
   (a) Draw the FET circuit symbol of an n-channel FET and the corresponding AC small-signal equivalent circuit.
   (b) Draw a basic common-source (common-S) amplifier circuit and include a drain resistance R_D (but no other resistance). Draw the AC small-signal equivalent circuit of the amplifier (mark the G, S, and D terminals). Derive a symbolic expression for z_{in} (input impedance), z_{out} (output impedance), A_{VOC} (open-circuit voltage amplification), and A_{ISC} (short-circuit current amplification).
   (c) Draw a basic common-drain (common-D) amplifier circuit and include a source resistance R_S (but no other resistance). Follow the same instructions as for the previous question.
   (d) Draw a basic common-gate (common-G) amplifier circuit and do not include any resistor. Follow the same instructions as for the previous question.
   (e) Make a table having three columns listing the three basic transistor configurations (common-source, common-drain, and common-gate configuration) and four rows listing the amplifier parameters (z_{in}, z_{out}, A_{VOC}, and A_{ISC}).
   (f) Which of the three circuits has the lowest output impedance? Is this desirable?
   (g) Which of the three circuits has the lowest input impedance? Is this desirable?
   (h) Which of the three circuits has a voltage amplification (A_{VOC}) of about 1.0?
   (i) Which of the three circuits are the most useful ones?

2. ***FET amplifier circuit and Miller capacitance***: The present problem concerns an FET amplifier circuit and its frequency response. The circuit diagram is shown in the figure below. The FET has a k-value of k = 20 mA/V^2 and a threshold voltage of V_{th} = 1 V. The FET gate-bias network consists of two resistors with R_1 = 80 kΩ and R_2 = 20 kΩ. The AC signal source has an AC voltage amplitude of V_{Signal} and an internal resistance of R_{Signal} = 5 kΩ. The load resistance is R_{Load} = 1 kΩ. The DC power supply voltage is V_{CC} = 10 V. Assume that the capacitors C_1 and C_2 are sufficiently large to let pass all AC signals (yet block DC signals).



(a) Which one of the three basic amplifier configurations does the present amplifier have? Determine the Q-point of the amplifier circuit by calculating the drain current I_D.

(b) Choose R_D so that the Q-point is in the middle of the load line, that is, at V_{DS} = 5 V.

(c) Determine the transconductance of the amplifier circuit (g_m) at the Q-point.

(d) Draw the AC small-signal equivalent circuit of the amplifier; include the signal source and load.

(e) Calculate the open-circuit voltage amplification A_{VOC} (symbolic expression and numerical value). Also calculate the voltage amplification A_V (symbolic expression and numerical value).

(f) Explain the following quantities: (**i**) Drain-gate capacitance C_{DG} and (**ii**) the Miller capacitance C_{Miller}.

(g) The experimental analysis of A_V as a function of frequency reveals that the amplifier has a high-frequency cutoff at frequency f_{Cutoff} = 20 MHz. It is determined that the high-frequency cutoff is due to the Miller capacitance. Redraw the AC small signal equivalent circuit and now include the Miller capacitance. Determine the *RC* time constant (τ = *RC*) of the input side of the circuit (symbolic expression and numerical value).

(h) Calculate the Miller capacitance (numerical value). Calculate the drain-gate capacitance C_{DG} (numerical value).

(i) Is there a basic amplifier configuration that suffers less (or not at all) from the limitations of the Miller capacitance?