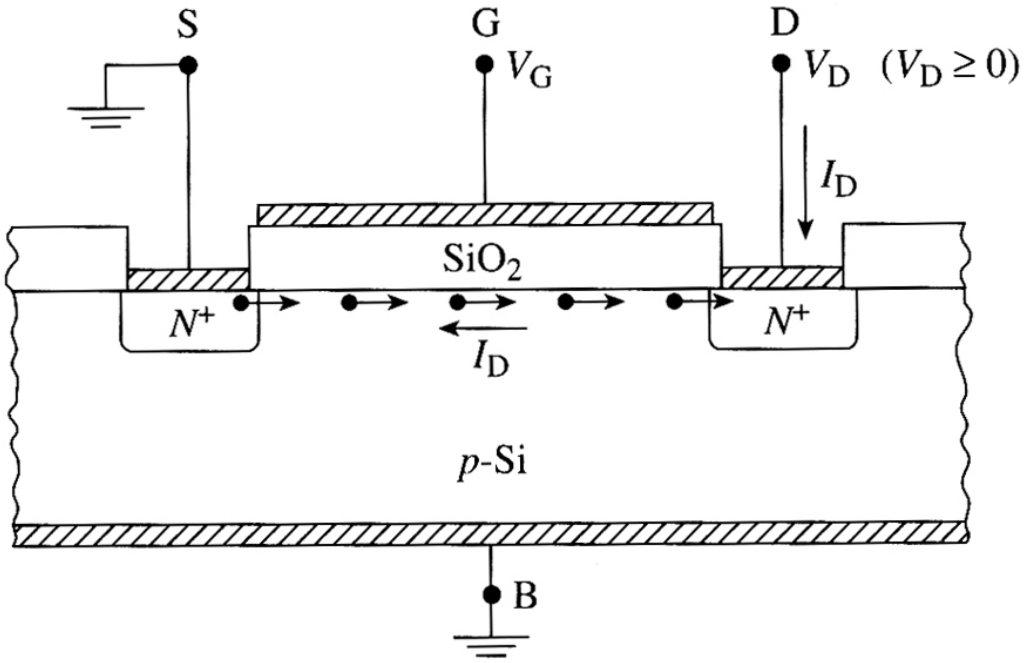
Chapter 16-1. MOS fundamentals

Metal-oxide-semiconductor FET is the most important device in modern microelectronics.

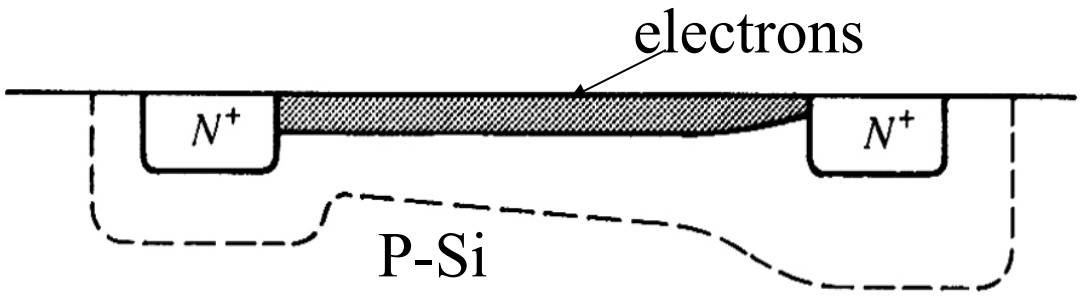
In this chapter, we will study:

- Ideal MOS structure electrostatics
- MOS band diagram under applied bias
- Gate voltage relationship
- capacitance-voltage relationship under low frequency and under high frequency.

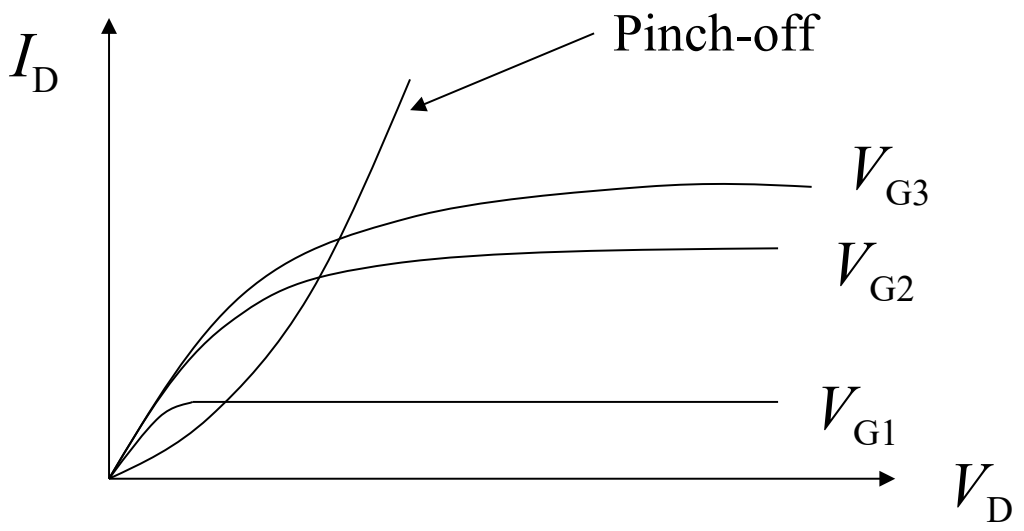
MOSFET



N-channel MOSFET (NMOS) uses p-type substrate



MOSFET operation



$$V_{G3} > V_{G2} > V_{G1}$$

When a positive voltage V_G is applied to the gate relative to the substrate, mobile negative charges (electrons) gets attracted to Si-oxide interface. These induced electrons form the channel.

For a given value of V_G, the current I_D increases with V_D, and finally saturates.

Ideal MOS capacitor

Let us consider a simple MOS capacitor and call it “ideal”

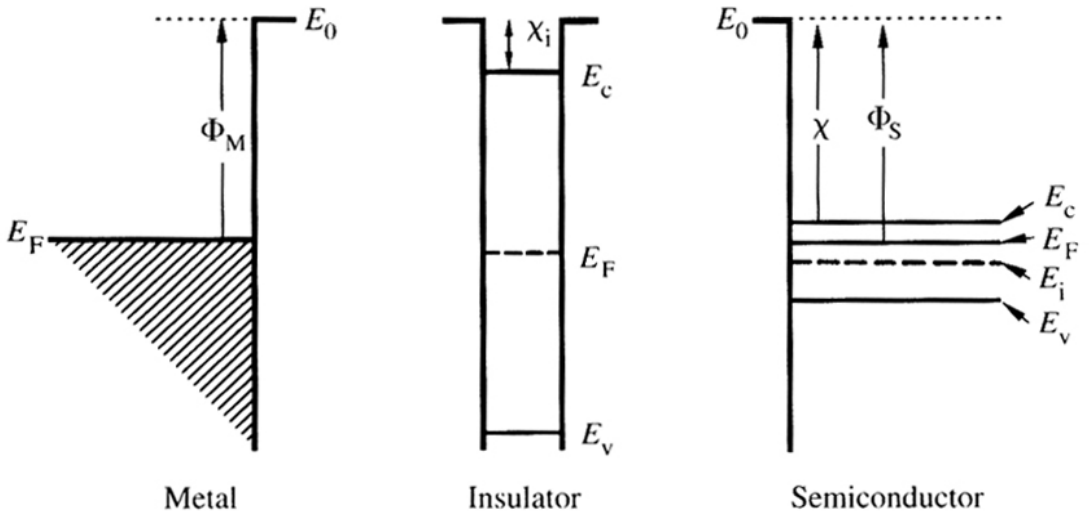
Oxide has zero charge, and no current can pass through it.

No charge centers are present in the oxide or at the oxide-semiconductor interface.

Semiconductor is uniformly doped

$$\Phi_M = \Phi_S$$

$$= \chi + (E_C - E_F)_{FB}$$



Equilibrium energy band diagram for an ideal MOS structure

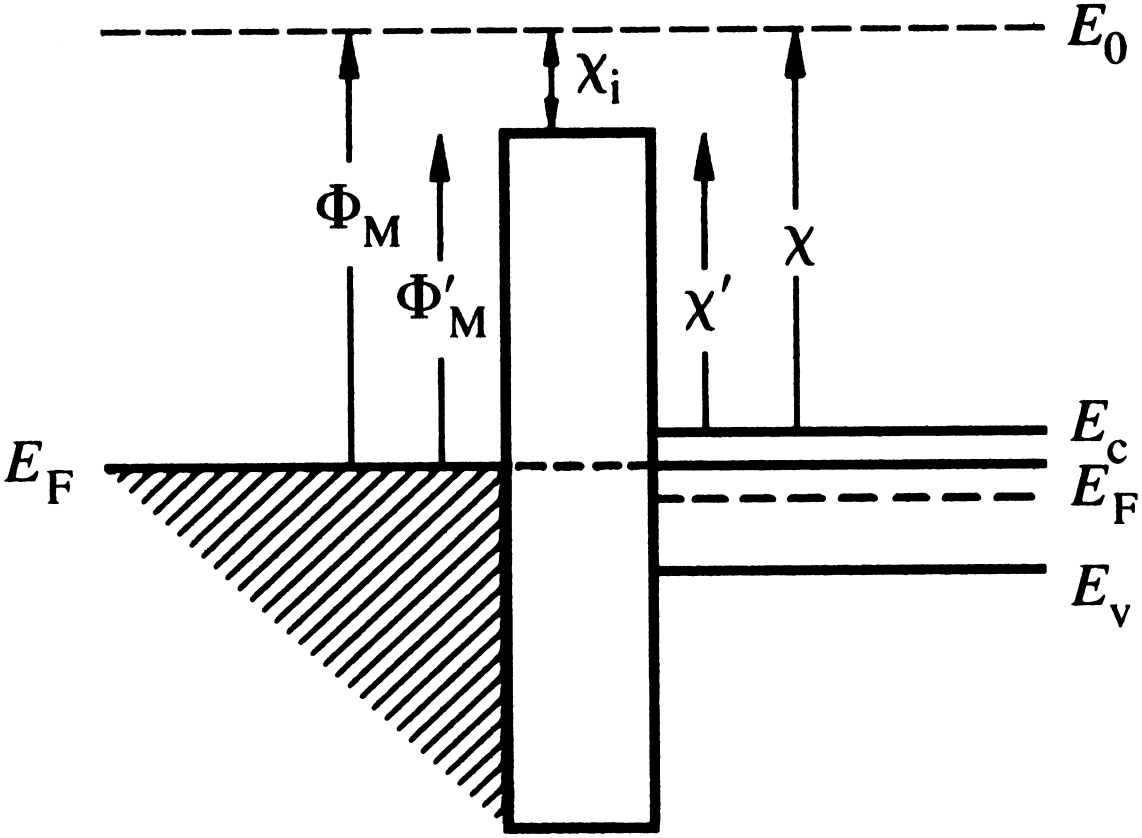


Figure 16.4

Effect of an applied bias

Let us ground the semiconductor and start applying different voltages, $V_{G,}$ to the gate

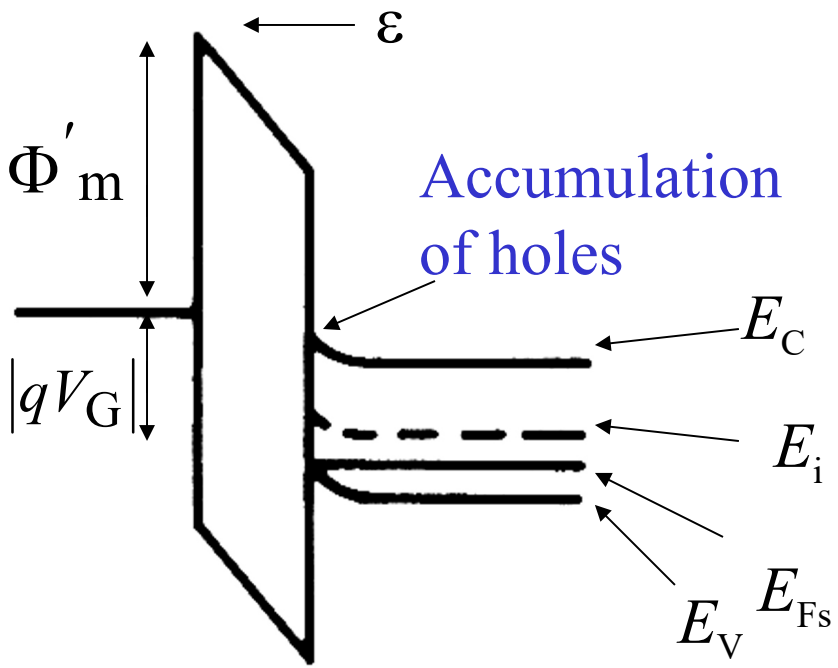
V_G can be positive, negative or zero with respect to the semiconductor

$$E_{F,\,metal} - E_{F,\,semiconductor} = -\,q\,V_G$$

(Since electron energy = $-\,q\,V$, when $V < 0$, electron energy increases)

Since oxide has no charge, $d\,\mathcal{E}_{oxide} / dx = \rho/\varepsilon = 0$; i.e. the $\mathcal{E}$-field inside the oxide is constant.

Consider p-type Si, apply $V_G < 0$

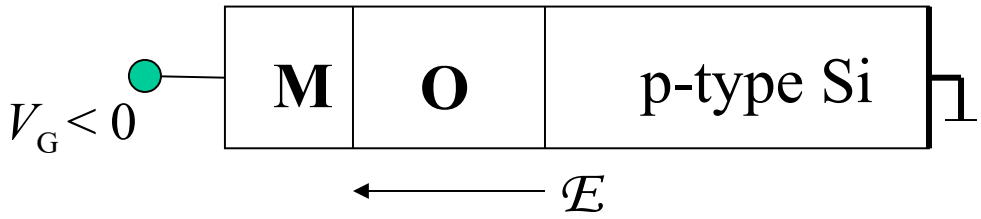


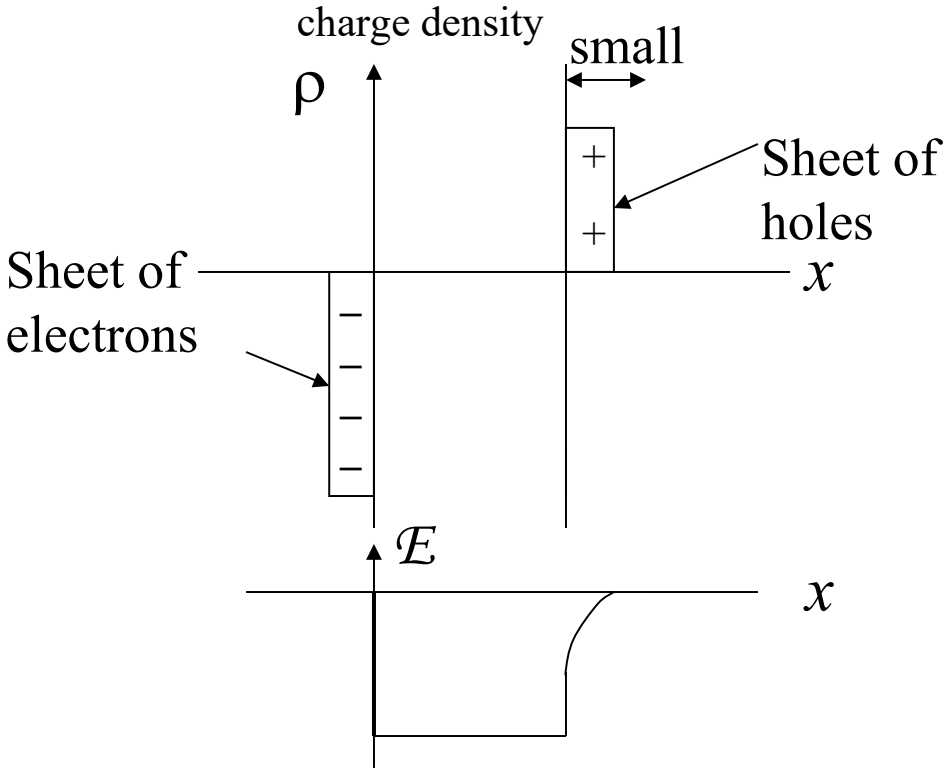
Negative voltage attracts holes to the Si-oxide interface. This is called accumulation condition. $E_i - E_F$ should increases near the surface of Si.

$$\frac{\partial \mathcal{E}_{oxide}}{\partial x} = 0 \quad \Rightarrow \quad \mathcal{E}_{oxide} = \text{const.} = \frac{1}{q}\frac{\partial \mathcal{E}_i}{\partial x}$$

The oxide energy band has constant slope as shown. No current flows in Si ➔ E_F in Si is constant.

Accumulation condition, $V_G < 0$, p-type Si

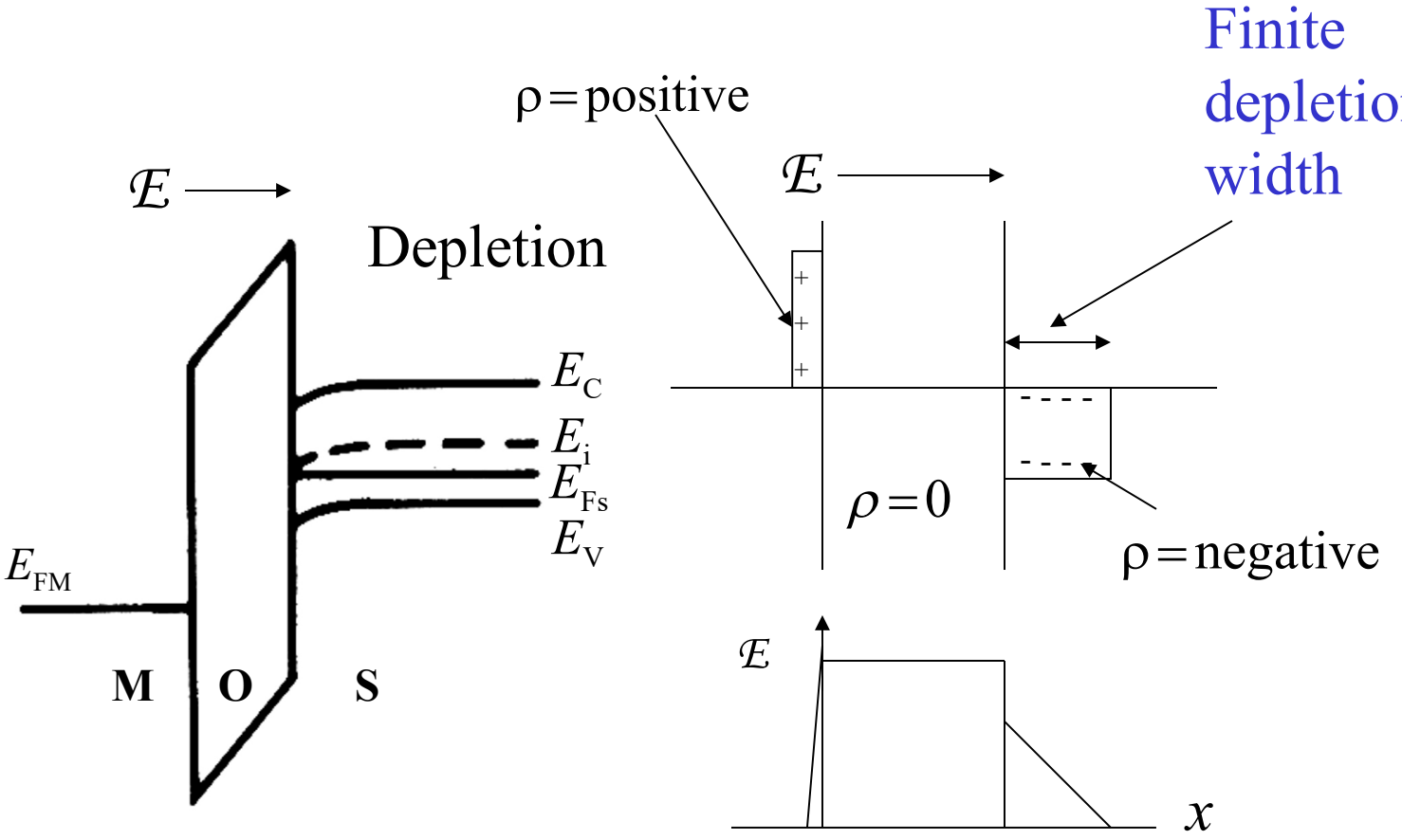




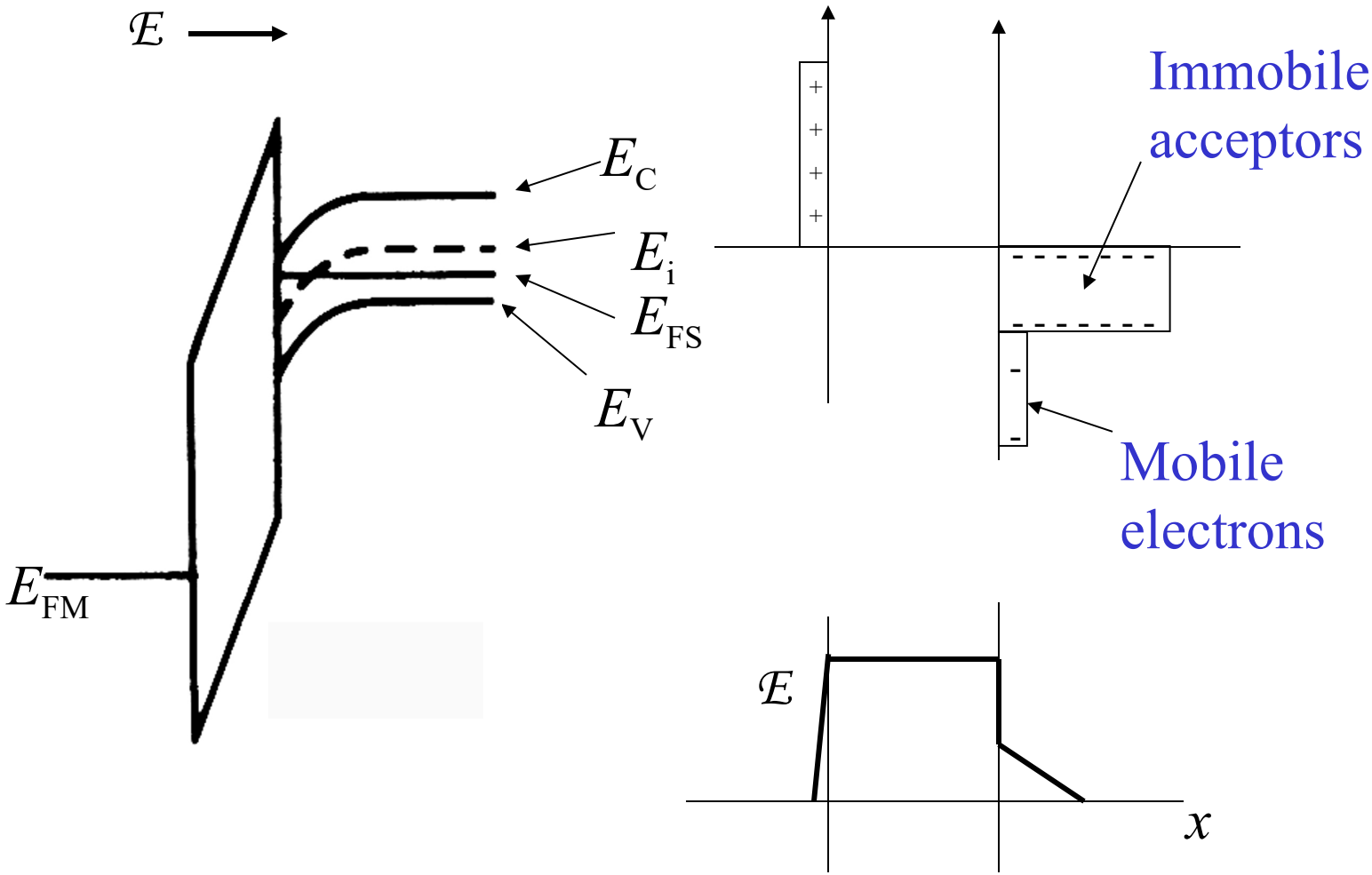
Accumulation of holes near silicon surface, and electrons near the metal surface.

Similar to a parallel plate capacitor structure.

Consider p-type Si, apply $V_G > 0$ (Depletion condition)



Consider p-Si, apply $V_G >> 0$ (Inversion condition)



Inversion condition

If we continue to increase the positive gate voltage, the bands at the semiconductor bends more strongly. At sufficiently high voltage, E_i can be below E_F indicating large concentration of electrons in the conduction band.

We say the material near the surface is "inverted". The "inverted" layer is not gotten by doping, but by applying $\mathcal{E}$-field. Where did we get the electrons from?

When E_i(surface) – E_i(bulk) = 2 [E_F – E_i(bulk)], the condition is start of "inversion", and the voltage V_G applied to gate is called V_T (threshold voltage). For $V_G > V_T$, the Si surface is inverted.

Energy band diagrams and charge density diagrams describing MOS capacitor in n-type Si

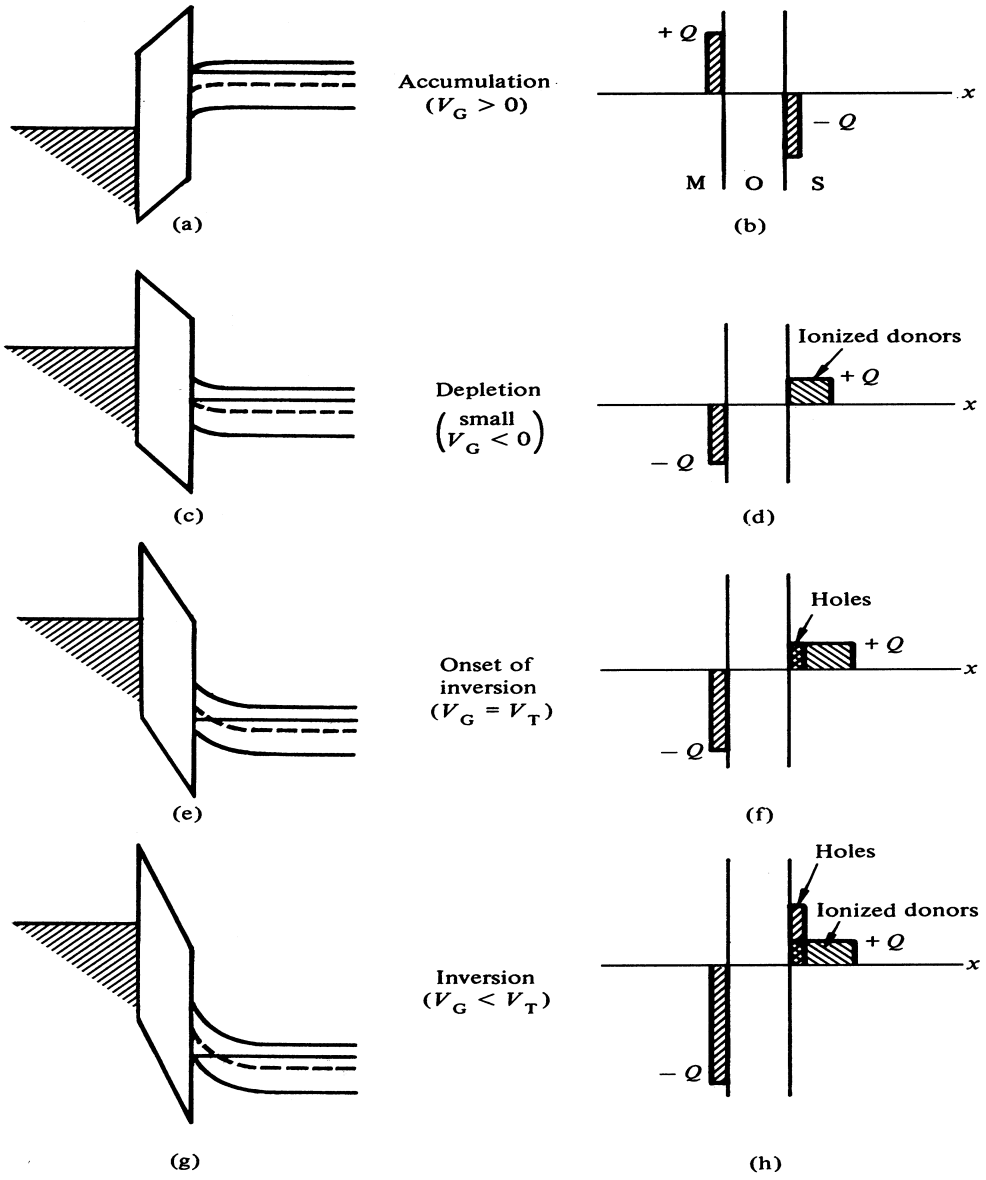


Figure 16.5

Energy band diagrams and charge density diagrams describing MOS capacitor in p-type Si

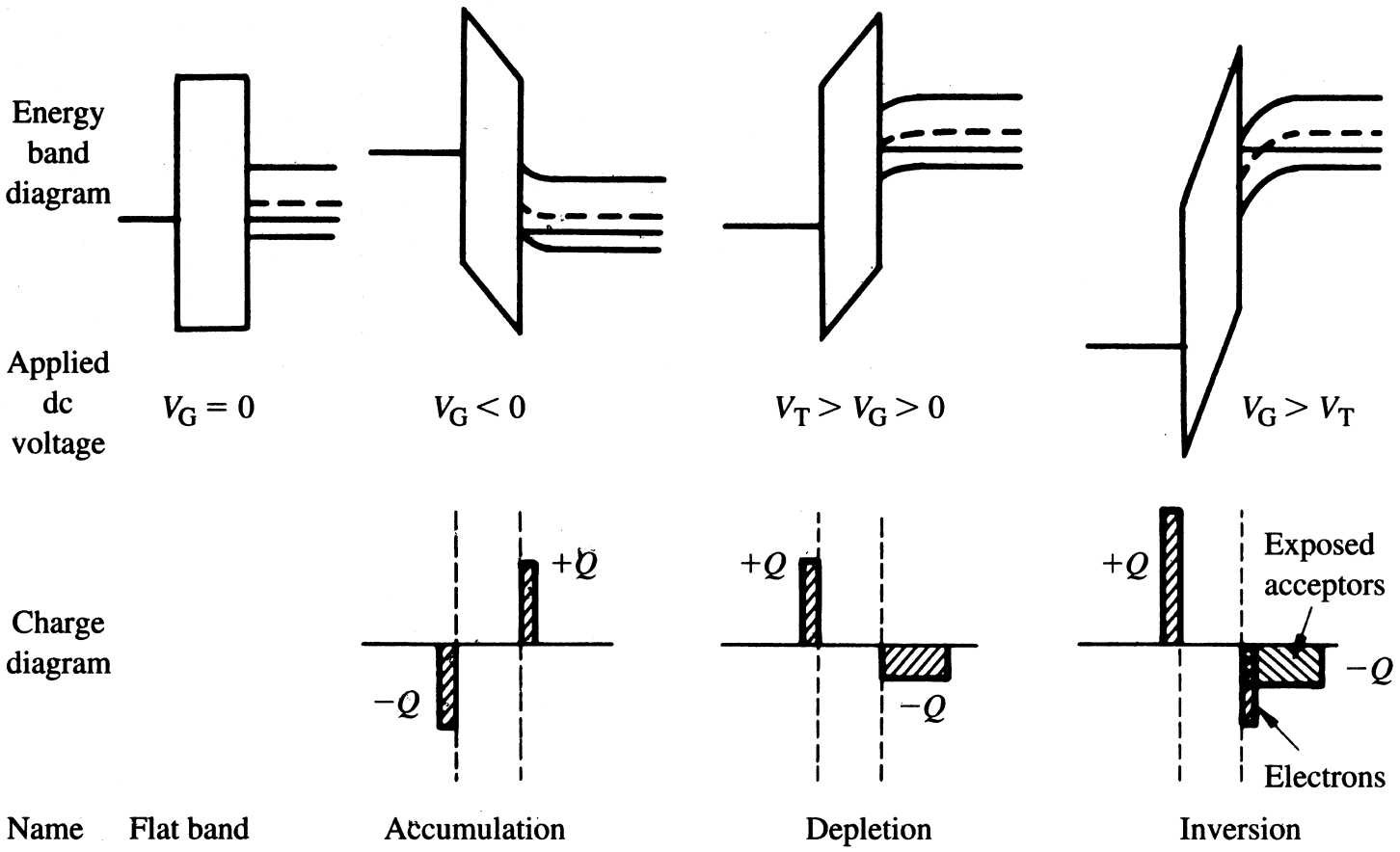


Figure 16.6

Example 1

Construct line plots that visually identify the voltage ranges corresponding to accumulation, depletion and inversion in ideal n-type Si (i.e. p-channel) and p-type Si (i.e. n-channel) MOS devices.

Answer:

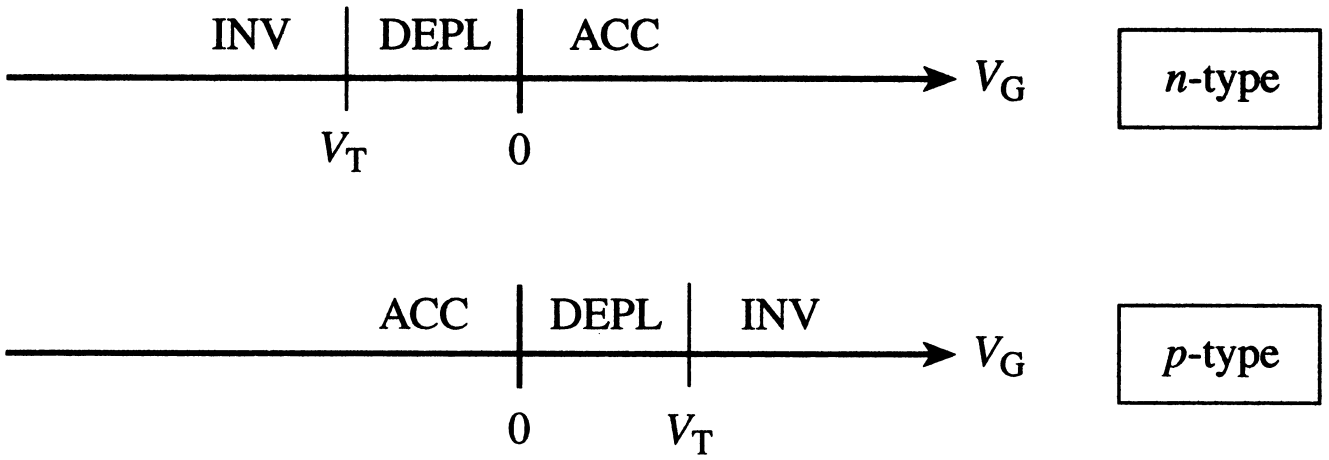


Figure E16.1