Laboratory 7 (Day 2):
FET characteristics, Current mirrors, Small signal amplifiers

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Material covered:

- This laboratory has ***three sessions*** allocated for completion.
    - 1st session: Pre-Lab Exercise 1 and Exercise 1. Exercise 2 is optional.
    - 2nd session: Pre-Lab Exercise 2 and Exercise 3. Exercise 4 is optional.
    - 3rd session: Pre-Lab Exercise 3 and Exercise 5. Exercise 6 is optional.
- MOSFET DC biasing, Ohmic region and Saturation region
- Small signal models for MOSFETS
- Common source, common gate, common drain configurations
- Small signal bandwidth

PSpice:

Add the pwrmos library files to the PSpice directory. Note, I believe Orcad version 17.2 already has this library. Refer to Laboratory 2 for instruction on adding .lib and .olb files to PSpice and editing the nom (nomld) files to add the library link.

Data Acquisition:

As with previous labs, you will need to plot *I-V* characteristics for the devices under consideration.

DC measurements:

Due to the impedance characteristics of the Discovery Board, it is recommended to use the benchtop Multimeters to make the DC measurements in Exercise 2 and 3. When using the Multimeters, make sure your connections are correct or you can damage the device. If you are unsure, ask the TA or the Instructor.

DC Bias/Isolation capacitors:

The capacitors used in Exercises 3 to 6 are used for isolating the DC signals relative to the AC input. The electrolytic capacitors available in the laboratory have polarity. The "–" (negative) side is usually marked with a band and has the negative sign printed on it. This side should be connected to the low voltage side of the DC circuit (the AC polarity does not matter).

AC Sweep:

Bode plots can be obtained on the Discovery Board using the network analyzer tool. You can set the start frequency, stop frequency, input amplitude and points per step (more points gives you a smoother curve, but a longer data acquisition time).

FET internal capacitances (spec sheet values):

The spec sheet provides values based on input, output and reverse transfer capacitances, C_{iss}, C_{oss} and C_{rss}, respectively. They are values we could use in a model and with application of the Miller Theorem, we can find Ciss and Coss via the equivalent amplifier circuit model. In the small signal model we can relate these values to C_{DG}, C_{GS} and C_{DS} with the following equations:

$C_{iss} \approx C_{GS} + C_{DG}$ (given in Data Sheet)

$C_{oss} \approx C_{DG} + C_{DS}$ (given in Data Sheet)

$C_{rss} \approx C_{DG}$ (given in Data Sheet)

Given these equations, we can write:

$$C_{GS} = (C_{GS} + C_{DG}) - C_{DG} = C_{iss} - C_{rss}$$

$$C_{DG} \approx C_{rss}$$

$$C_{DS} = (C_{DG} + C_{DS}) - C_{DG} = C_{oss} - C_{rss}$$

Pre-Lab Exercise 2

Exercise 3: Common source amplifiers

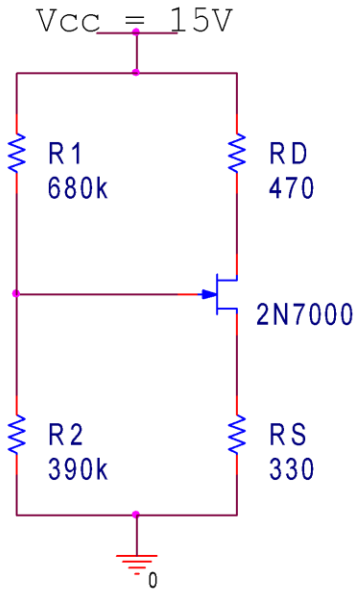

Figure 8: Four resistor biasing

Implement the circuit in Figure 8.

1. Build and measure the DC bias values, V_{DS}, V_{GS}, and I_D for the circuit shown in Figure 8. It is recommended to use the benchtop multimeter to check V_{DS} and V_{GS} (determine I_D from Ohm's Law across R_D or R_S). The benchtop multimeter has a larger input impedance than the Discovery Board.

   Vds = 7.8 V

   Vgs = 2.49 V

   Id = V(RD)/470 = (4.218 V)/470 = 8.97 mA

2. Verify that your FET is operating in the saturation region by checking that

   $$V_{DS} > V_{GS} - V_{TN}$$

   If the circuit is not in saturation, try replacing R_2 with a smaller resistance until the saturation condition is met.

   Compare your measured voltages with calculated values using your measurements from Exercise 1.

   In exercise 1, we found that V_{TN} was ~2.25V, so we ARE in the saturation region, because:

   7.8V > (2.49 – 2.25) holds true

Keep the above circuit on your protoboard. You will use this DC biasing circuit for all remaining exercises.

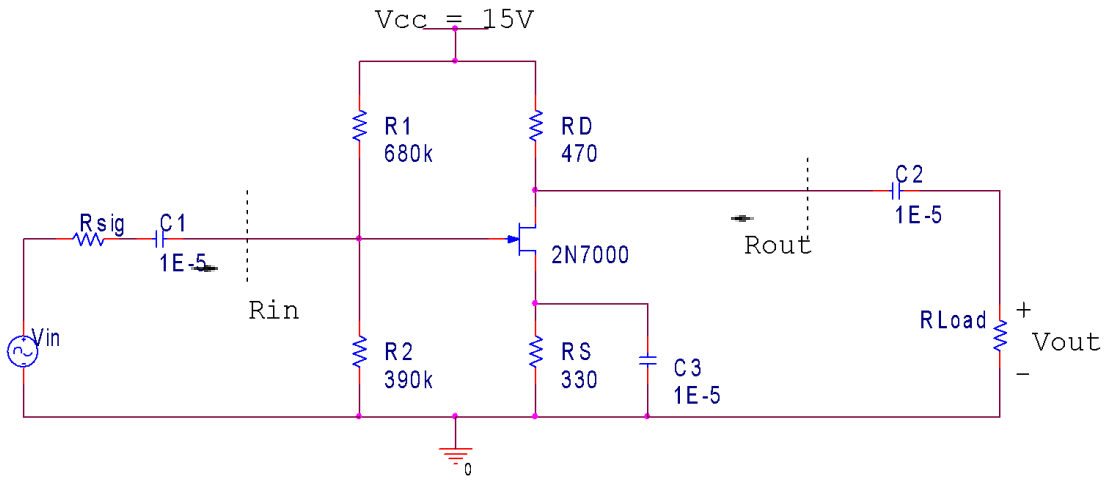

Figure 9: Common source amplifier

Implement the circuit in Figure 9. The DC bias portion of the circuit is the same as the circuit in the previous part of this exercise. Set the AC source signal, V_{in}, to a 0.2 Vpp sinusoidal signal at 1 kHz. As indicated on the front, the isolation capacitors have a DC polarity orientation. For example, in the above circuit, the negative (low) side of C_1 is connected to R_{sig} and the positive (high) side of C_1 is connected to the gate of the NMOS (and R_1, R_2).

After constructing the circuit and turning power on, it may take a long time (> 10 seconds) for the gate voltage to reach the expected value. What causes this effect?

1. Set R_{sig} to 100 Ω and R_{Load} to 100 kΩ Measure the amplitude of the output voltage, V_{out}. Estimate the open-circuit gain of the amplifier, $A_{VOC} = v_{out,o}/v_{in,o}$. (Note, for this R_{sig} and R_{Load}, the above circuit is approximately equal to the open-circuit with $R_{sig} = 0$ and $R_{Load} \longrightarrow \infty$.)

   Our measured value of Vout(open circuit) = 2.9069V-pp, or an amplitude of 1.4359V.
   AVOC = Vout/Vin = 2.9069/0.2 = 14.53

   Include a sketch of the small signal model in your report.
   Compare your results to calculated values.
   Why are the resistances for R_{sig} and R_{Load} appropriate for measuring the open-circuit gain, A_{VOC}, of the amplifier?

   The Rsig resistance of 100 ohms makes sense, because it is low and would ideally not impede the signal source. The Rload of 100k ohms is also reasonable, since we give the load a HIGH impedance in order to properly measure voltage there. If Rload was a low

impedance, then excessive current draw could lead to voltage sag and thus a bad measurement.

2. Set R_{sig} to 100 kΩ and R_{Load} to 470 Ω. Measure the amplitude of the output voltage, V_{out}. Estimate the overall gain of the amplifier, $A_V = v_{out} / v_{in}$.

	Name	Value
C1	Amplitude	0.54154 V
C1	Peak2Peak	1.0922 V

We measured:
Vout = 1.0922V-pp or amplitude of 0.54154V.
So the overall gain is:
Av = 1.0922/0.2 = 5.461

3. Measure the current through R_{sig} and estimate the input resistance, R_{in}, seen looking into the amplifier (the input resistance does not include R_{sig}).

$$i_{in} = \frac{v_{in}}{R_{sig} + R_{in}}$$

Isig = 0.022V / 100k = 0.22uA

$$0.22uA = \frac{0.2V}{100k + Rin}$$
$$0.22uA(100k + Rin) = 0.2V$$
$$Rin = \frac{0.2V - (0.22 * 100 * 10^{-3})}{0.22 * 10^{-6}}$$
$$Rin = 809k\ Ohms$$

This passes our sanity check, since the input impedance at the Gate should be INFINITE ideally, in order to draw very low current from the signal source.

4. Use voltage divider concepts with $V_{out,open}$ (open-circuit load voltage) and V_{out} (load voltage with finite load resistor) to determine the output resistance.

$$V_{out} = \frac{R_{Load}}{R_{out} + R_{Load}} V_{out_{open}}$$

We measured:

Vout(open circuit) = 2.9069V-pp

Vout(finite load resistor) = 1.0922V-pp

$$1.0922V = \frac{470}{R_{out} + 470} * 2.9069V$$

$$0.375726V = \frac{470}{R_{out} + 470}$$

$$R_{out} + 470 = \frac{470}{0.375726}$$

$$R_{out} = \frac{470}{0.375726} - 470$$

$$R_{out} = \frac{470}{0.375726} - 470$$

$$R_{out} = 780\ \Omega$$

Compare your measured R_{in} and R_{out} to calculated values obtained using your 1.1 V_{TN} and k_n estimates.

Our VTN = 2.25V, so 1.1*2.25= 2.475V

Our kn = 0.0296, or 0.0296/Vds

5. Remove capacitor C_3 and repeat parts 1 to 4.
   Why do the amplifier characteristics change?
   (Try to keep this circuit on your protoboard, only pulling out the transistor for Exercise 4. Alternatively, skip to Exercise 5 and record the frequency characteristics of the circuit.)

For Rsig=100 and Rload=100k, we get:

	Name	Value
C1	Amplitude	131.29 mV
C1	Peak2Peak	267.31 mV

Vout(open)= 267 mV
So AVOC=(267*10^-3)/(0.2)=1.33655 (much lower AVOC)

	Name	Value
C1	Amplitude	47.142 mV
C1	Peak2Peak	96.311 mV

For Rsig=100k and Rload=470, we get:
Vout(real load)=96.311 mV
So AV= (96.311*10^-3)/(0.2)=0.4815
So the overall circuit gain went from ~5 to 0.5, which now means that there is a LOSS.

The other measurements for input and output resistance are also skewed, since the C3 capacitor had previously been acting as an alternative path to GND for AC signals (like the input signal).