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IE lab 4 part2

Exercise 3:

1. Build the circuit shown in Figure 6 (below) using VCC = 4 V, RL = 100 kΩ, and RSig = 100 Ω.
   Analytically, using your measured β from Exercise 1 estimate the input resistance, RIn , output resistance, ROut , and the open-circuit voltage gain, AVOC.

B=203.351
B=a/(1-a)
a=0.9951

rE=1k
Rc=1k
Rin = B*rE = 208.3k Ohms
Rout = Rc = 1k Ohms
AVOC = -Rc/rE = 1

2. Set RSig to 100 Ω and RL to 100 kΩ. Apply an input voltage with DC offset = 0 V, Vpk-pk = 0.2 V, frequency = 1 KHz.
3. Experimentally estimate the open-circuit voltage gain AVOC. Remember to set the V/Div such that the input profile of the measurement does not interfere with the circuit.

Vin_pp=193.30mV
Vout_pp=183.41mV
AVOC=Vout/Vin=0.9488

4. Change RSig to 1 kΩ and RL to 1 kΩ.
5. Experimentally, determine the input resistance, RIn . This can be done by measuring the current through RSig and the voltage on the RHS of RSig (= vin). Recall: RIn = vin / iin

V_Rsig=89.14mV
I_in=V_Rsig/R_sig=89.14mV/1000 Ohms=89.14uA
R_in=V_in/I_in=113.96mV/89.14uA=1278.43 Ohms

6. Experimentally, determine the output resistance, ROut . This can be done by removing RL , applying a small AC voltage to the amplifier output, and measuring the current into the amplifier. Recall: ROut = vout / iout

R_L=1k
V_Rtest=124.54mV
I_out=V_Rtest/R_test=124.53uA
R_out=V_out/I_out=630.828 Ohms

7. For the same RSig and RL , determine the overall voltage gain, AV .
   For all the above values, how do the experimental results compare to the analytic estimates?

A_V=V_outpp/V_inpp=0.9487

Exercise 4:

1. Build the circuit shown in Figure 7 (below) using RL = 100 kΩ with Vin set to zero. Set VCC to 4 V. Note: when you apply power, the current will increase slowly (why?). Wait until it reaches its final value before making measurements.
2. Verify that the DC bias characteristics are consistent with the previous exercise. Analytically, using your measured β from Exercise 3.1 estimate the input resistance, RIn , output resistance, ROut , and the open-circuit gain, AVOC .

B=203

rE=1k
Rc=1k
Rin = B*rE = 208.3k Ohms
Rout = Rc = 1k Ohms
AVOC = -Rc/rE = 1

3. Set RSig to 100 Ω and RL to 100 kΩ. Apply an input voltage with DC offset = 0 V, Vpk-pk = 0.02 V, frequency = 1 kHz.
4. Experimentally estimate the open-circuit voltage gain AVOC. Remember to set the V/Div such that the input profile of the measurement does not interfere with the circuit.

V_inpp=152.41mV
V_outpp=1.0320V
AVOC=V_outpp/V_inpp=6.7712

5. Measure the current through RSig. Use this measurement to experimentally estimate the input resistance, RIn.

V_Rsig=50.03mV
I_in=V_Rsig/R_sig=500.3uA
R_in=V_in/I_in=305.276 Ohms

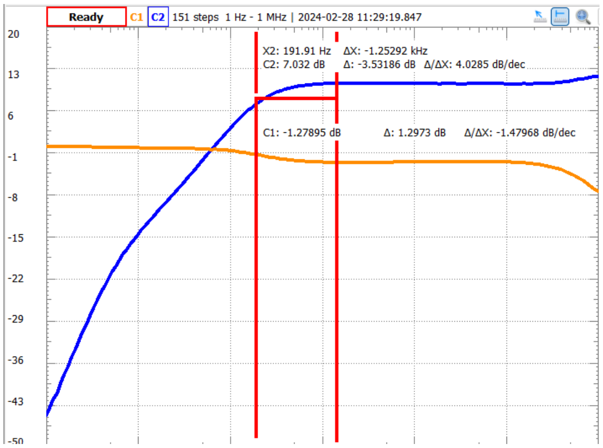
6. Replace RL with a 1 kΩ resistor and the output voltage. Use this measurement to estimate the output resistance, ROut.

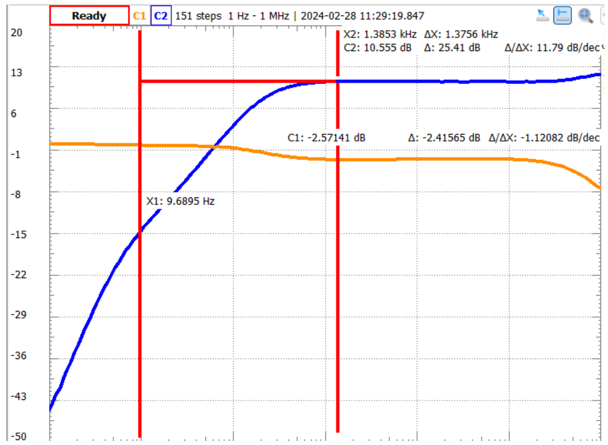
V_Rtest=100.61mV
I_out=V_Rtest/R_test=100.61uA
R_out=V_out/I_out=1022.06 Ohms

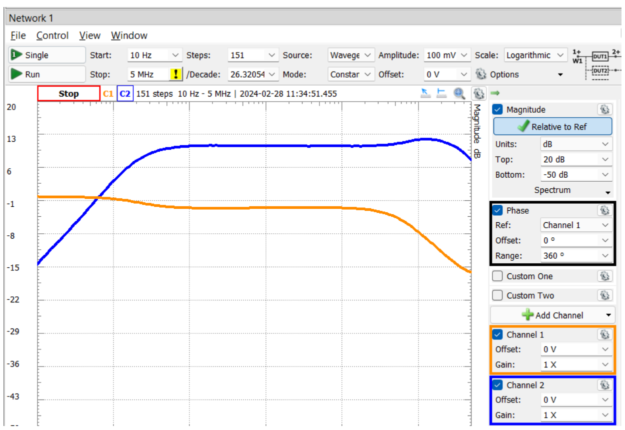
7. For the same RSig and RL, determine the overall voltage gain, AV.
   For all the above values, how do the experimental results compare to the analytic estimates?

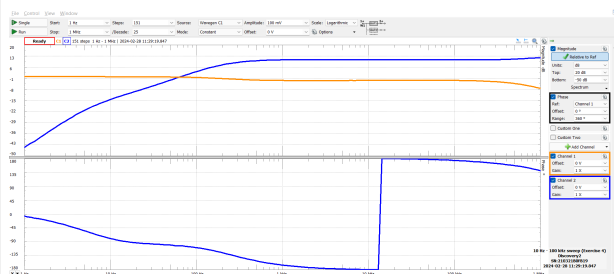
A_V=V_outpp/V_inpp=3.361

8. With VCC = 4 V, RSig = 100 Ω, and RL = 1 kΩ, do a frequency sweep with VIn,pk-pk = 0.02 V and determine the 3 dB low and high frequency cutoffs.









9. Analytically, estimate the (low-frequency) cutoff frequency associated with each capacitor.
   How do your experimental values compare with an analytic estimate?

C3 has a cutoff around 0.160Hz, and C1 has a cutoff around 3.19Hz. These are significantly lower than the experimental values.