COURSE SYLLABUS

ECSE-49XX: INDEPENDENT STUDIES IN ECSE

Topics in Integrated Circuit Design and Testing

Course Catalog Description: Supervised readings, research and project. *1 credit hours*

Pre-Requisite Courses: ECSE-2610 Computer Components and Operations and ECSE-2050 Intro. to Electronics

Co-Requisite Courses: None, but need junior or senior standing and a strong commitment to the project (Recommended: ECSE-4220 VLSI Design or ECSE-4040 Digital Electronics)

Pre-Requisites by Topic: 1. Fundamentals of logic design 2. Digital & analog circuit theory 3. Some knowledge of the process to create ICs 4. Ability to use EDA tools

Textbook: None

References:

https://files.ef.link/pdf/efabless.overview.202206.pdf
https://efabless.com
https://github.com/efabless/caravel

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Overall Educational Objective: To provide ECSE students with a hands-on project experience to create a foundry fabricated and working IC design using Efabless design tools and fully document the process for other follow-on projects.

Course Learning Outcomes: Students will be able to: 1. Conduct user overview of EDA tools and determine appropriate level of project complexity. 2. Layout two project designs for the semester; a more basic one with a high success probability and a more complex design that involves features. The design criteria details for these projects will be determined after further research into the particulars of the Efabless design environment. 3. Continue the background research to complete schematics for both designs, to include user interface and the function components themselves, including functional block diagrams to be presented in the form of a report. 4. Finalize the designs and present to the part of the team that will check and verify the completed details. 5. Prepare final designs for fabrication at Efabless. 6. Prepare documentation for final project presentations and test procedure to follow when the fabricated hardware is received. Also, review and revise documentation for the process used to create these projects.

How Course Objectives are Assessed: Grades will be determined based on the completeness and quality of the interim & final project presentations and provided reports. Each report is worth a portion of the grade for the course and is the primary form of acquiring grades. It may be helpful if a laboratory notebook is kept documenting the process each step of the way.

The weights of the deliverables are:

Initial project presentation and Schematic Design	20%
Second project presentation and Schematic design	20%
Evaluation & Midterm report	10%
Verification of projects	30%
Final Documentation of process	20%
TOTAL	100%

Topics Covered: This course will introduce the student to the entire process of product design, from user interviews, to preparing background research, to ordering the components and fabricating the system.

Computer Usage: All design task will use the provided EDA tools from Efabless.

--Laboratory Experiences (follow up course planned for spring 2023): Upon fabrication of the system, it shall be calibrated, tested, and verified to acquire full credit for the course. This process will generate preliminary laboratory data.

Design Experiences: The full integrated circuit and user interface system for 2 separate projects are designed by the student.

Independent Learning Experiences: Although students work as a team while splitting up the design tasks and verification tasks of the projects, : 1. Research of design solutions, 2. Determining hardware requirements, 3. Preparing for foundry fabrication, 4. Reading documentation for the design process, 5. Verification/Troubleshooting/Determining how to achieve correctly functioning subsystems.

Class/Lab Schedule: ~4 hr/wk of independent research and design

Contribution to the Professional Component:

(a) College-level mathematics and basic sciences:	0 credit hours
(b) Engineering Topics (Science and/or Design):	1 credit hours
(c) General Education:	0 credit hours

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Academic Integrity: Academic dishonesty is a very serious matter, and we suggest that you read the remainder of this statement carefully:

Student-teacher relationships are built upon trust. For example, students must trust that teachers have made appropriate decisions about the structure and content of the courses they teach, and teachers must trust that the assignments, which students turn in, are their own. Acts that violate this trust undermine the educational process.

The Rensselaer Handbook defines various forms of Academic Dishonesty and procedures for responding to them. All forms are violations of the trust between students and teachers. Students should familiarize themselves with this portion of the Rensselaer Handbook and should note that the penalties for plagiarism and other forms of cheating can be quite harsh.

Any portion of work handed in that is not your own, should cite the author. Just as you would not write a history paper by copying text from the encyclopedia, you should not take credit for another person's engineering work. Reference should also be made to any personal communications you have had with anyone outside your group that contributed substantially to the successful completion of an assignment. (Please read the IEEE Code of Ethics, especially item number 7. http://www.ieee.org/web/membership/ethics/code_ethics.html The ASME has a similar code. http://files.asme.org/ASMEORG/Governance/3675.pdf)

At all times, we reserve the right to take formal action against anyone engaging in academic dishonesty. This action may range from failing an assignment to failing the course, or to being reported to the Dean of Students. If you have any questions about these rules or how they apply to any specific assignment or exam, discuss it with one of the instructors or course administrators.