Laboratory 7 (3 days):
FET characteristics, Current mirrors, Small signal amplifiers

Material covered:

- This laboratory has ***three sessions*** allocated for completion.
  - 1st session: Pre-Lab Exercise 1 and Exercise 1. Exercise 2 is optional.
  - 2nd session: Pre-Lab Exercise 2 and Exercise 3. Exercise 4 is optional.
  - 3rd session: Pre-Lab Exercise 3 and Exercise 5. Exercise 6 is optional.
- MOSFET DC biasing, Ohmic region and Saturation region
- Small signal models for MOSFETS
- Common source, common gate, common drain configurations
- Small signal bandwidth

PSpice:

Add the pwrmos library files to the PSpice directory. Note, I believe Orcad version 17.2 already has this library. Refer to Laboratory 2 for instruction on adding .lib and .olb files to PSpice and editing the nom (nomld) files to add the library link.

Data Acquisition:

As with previous labs, you will need to plot *I-V* characteristics for the devices under consideration.

DC measurements:

Due to the impedance characteristics of the Discovery Board, it is recommended to use the benchtop Multimeters to make the DC measurements in Exercise 2 and 3. When using the Multimeters, make sure your connections are correct or you can damage the device. If you are unsure, ask the TA or the Instructor.

DC Bias/Isolation capacitors:

The capacitors used in Exercises 3 to 6 are used for isolating the DC signals relative to the AC input. The electrolytic capacitors available in the laboratory have polarity. The "–" (negative) side is usually marked with a band and has the negative sign printed on it. This side should be connected to the low voltage side of the DC circuit (the AC polarity does not matter).

AC Sweep:

Bode plots can be obtained on the Discovery Board using the network analyzer tool. You can set the start frequency, stop frequency, input amplitude and points per step (more points gives you a smoother curve, but a longer data acquisition time).

FET internal capacitances (spec sheet values):

The spec sheet provides values based on input, output and reverse transfer capacitances, C_{iss}, C_{oss} and C_{rss}, respectively. They are values we could use in a model and with application of the Miller Theorem, we can find Ciss and Coss via the equivalent amplifier circuit model. In the small signal model we can relate these values to C_{DG}, C_{GS} and C_{DS} with the following equations:

$C_{iss} \approx C_{GS} + C_{DG}$ (given in Data Sheet)

$C_{oss} \approx C_{DG} + C_{DS}$ (given in Data Sheet)

$C_{rss} \approx C_{DG}$ (given in Data Sheet)

Given these equations, we can write:

$C_{GS} = (C_{GS} + C_{DG}) - C_{DG} = C_{iss} - C_{rss}$

$C_{DG} \approx C_{rss}$

$C_{DS} = (C_{DG} + C_{DS}) - C_{DG} = C_{oss} - C_{rss}$

Pre-Lab Exercise 1

If necessary, add the pwrmos library as indicated on the first page of the laboratory.

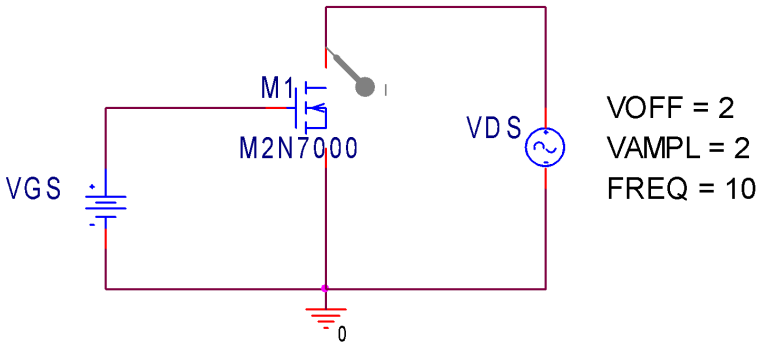

Figure 1: MOSFET circuit

In PSpice, implement the MOSFET circuit shown above. The FET part is 2N7000 in the pwrmos library.

1. Plot the MOSFET current I_D-versus-V_{DS} curve for V_{GS} = 1 V. Vary V_{DS} by running a DC sweep from 0 V to 10 V with an increment of 0.2 V. You can obtain *I-V* curves by placing a current probe as shown above. Edit the Axis Settings under the Plot tab.
   How would you describe the I_D-versus-V_{DS} curve (for V_{GS} = 1 V)?

2. Repeat for V_{GS} = 2 V, 2.5 V and 3 V. For each case, determine the approximate saturation current (where the current levels off).
   What is the dependence of the drain saturation current ($I_{D,sat}$) on the gate-source voltage (V_{GS})?

Pre-Lab Exercise 2

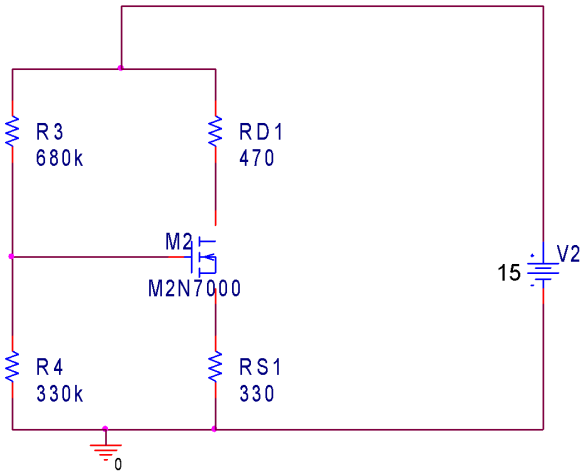

Figure 2: MOSFET circuit

1. Implement the circuit in PSpice and run a Bias Point analysis. Recall, the FET is the 2N7000 in the pwrmos library. Verify that your circuit is in saturation. Note, the PSpice model for the 2N7000 has different characteristics, V_{TN} = 1.73 V and $k_n \approx 0.06$ A/V^2.
   For the PSpice values, compare the simulated results to calculated results using the characteristics of the FET model for the 2N7000.

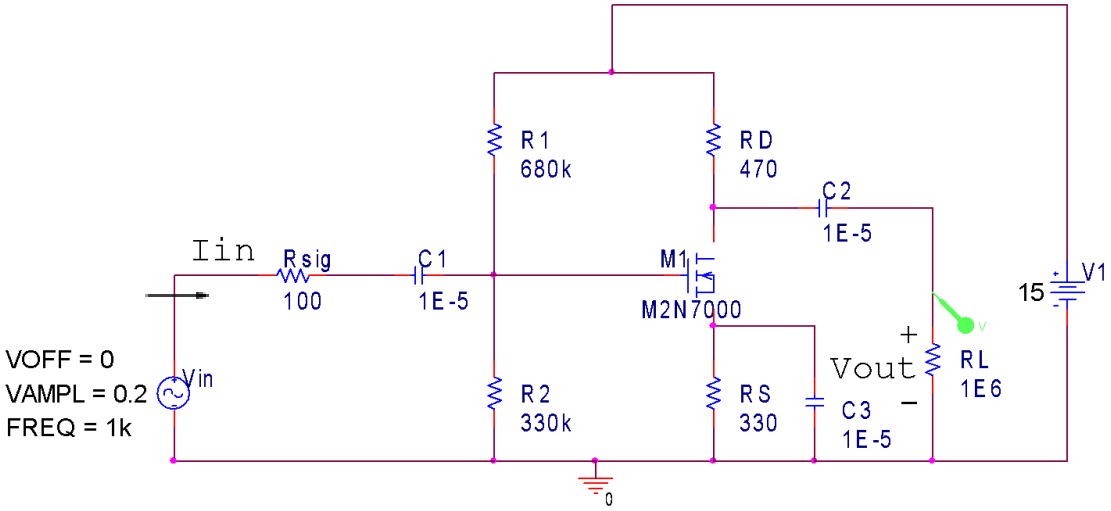

Figure 3: MOSFET circuit

2. Implement the above circuit in PSpice and determine the open circuit gain, $A_{VOC} = |v_{out}| \,/\, |v_{in}|$ and the input resistance, $R_{in} = |v_{in}| \,/\, |i_{in}|$.

Pre-Lab Exercise 3

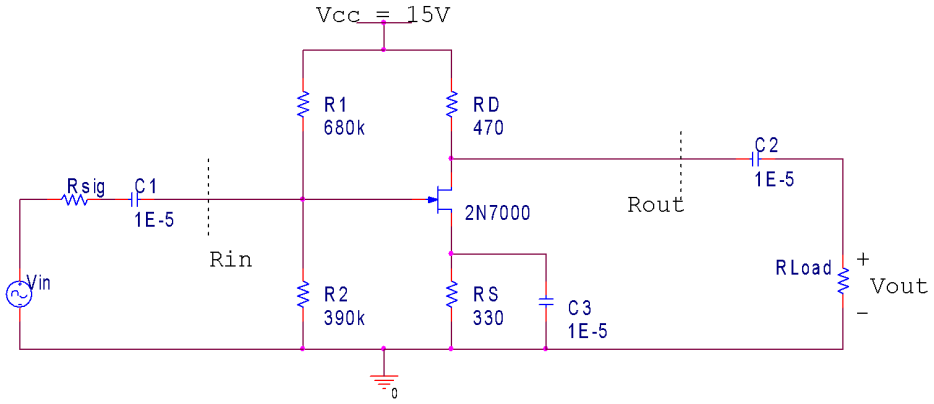

Figure 4: MOSFET circuit

Implement the Exercise 3/5 circuit in PSpice, setting R_{sig} to 100 kΩ and R_{Load} to 470 Ω, and run an AC sweep. Identify the low frequency and high frequency cutoff values (3 dB points).

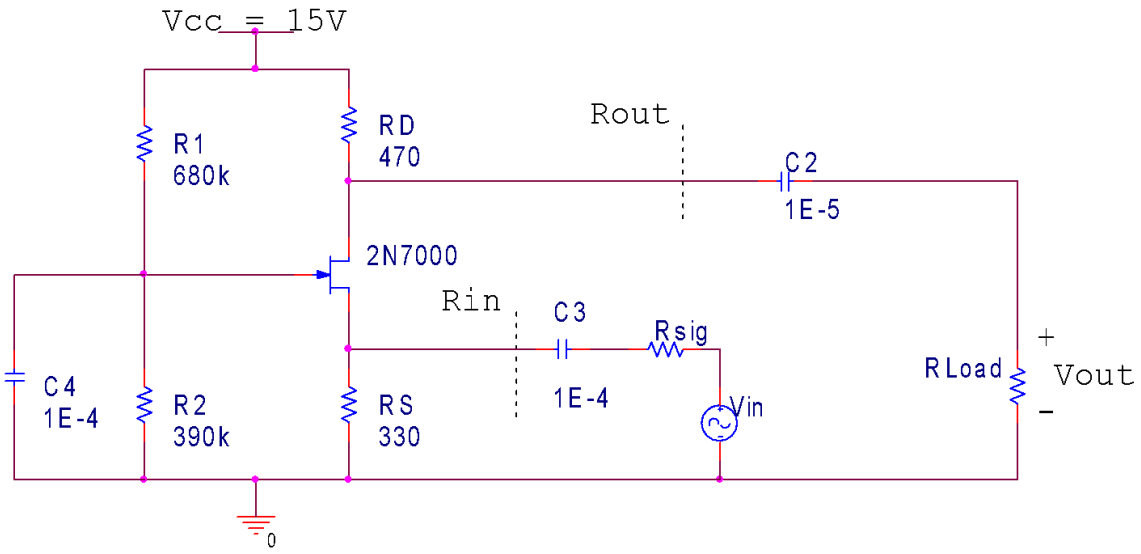

Figure 5: MOSFET circuit

Implement the Exercise 4/6 circuit in PSpice, setting R_{sig} to 22 Ω and R_{Load} to 1 kΩ, and run an AC sweep. Identify the low frequency and high frequency cutoff values (3 dB points).

Exercise 1: Investigate MOSFET operation in ohmic mode

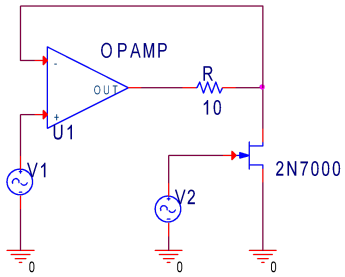

Figure 6: MOSFET analysis circuit

Implement the circuit in Figure 6. Use 15 / –15V voltage supply levels for the LF351/LF353 amplifier.

1. Set the positive amplifier input, V_1 (V_{DS}), to a 0.1 V DC using one of the Mobile Studio / Discovery Board channels. Set the gate input, V_2 (V_{GS}), to the MOSFET to a 1 kHz, 3 Vpp triangle wave with a 1.5 V DC offset using the other channel (the high voltage should be 3 V and the low voltage should be 0 V).

2. Measure the current through resistor, $I_R = I_D$, (Ohm's Law). Recall, you will need to use differential measurements to measure the voltage across the resistor.

3. Export the data or use the Math functions to plot the *I-V* characteristics of the MOSFET, I_D-versus-V_{GS}

4. Estimate the threshold voltage for the MOSFET, $V_{GS} \approx V_{TN}$, by determining the voltage at which point the current starts flowing through the MOSFET.

5. Estimate the k_n parameter by determining the slope of the linear portion of the I_D-versus-V_{GS} curve.
   Recall, in the ohmic region

$$I_D = k_n [(V_{GS} - V_{TN}) V_{DS} - ½ V_{DS}^2]$$

   with a linear approximation for the condition $V_{DS} << V_{GS} - V_{TN}$

$$I_D = k_n' (W_G / L_G) [(V_{GS} - V_{TN}) V_{DS}] \qquad \text{where} \qquad k_n = k_n' (W_G / L_G)$$

   Record the values you measured in part 4 and 5. Use those values in the other Exercises. Save the transistor for the other Exercises. Keep the circuit. If you wind up losing your transistor, use the circuit to again determine the threshold voltage and transconductance parameter of your new transistor.

6. Set the positive amplifier input, V_1 (V_{DS}), to a 1 kHz, 5 Vpp triangle wave with a 2.5 V DC offset using the other channel (the high voltage should be 5 V and the low voltage should be 0 V). Set V_2 (V_{GS}) to DC and adjust the gate input such that you start to see current flowing through the resistor (the resistor voltage becomes nonzero for part of the cycle). Make a note of that threshold voltage and compare it to your earlier estimate. Increase the gate voltage by 0.04 V (DC) such that you see a larger current through the resistor.

7. Measure the current through the resistor and the drain source voltage, V_{DS}. Again, export the data or use the Math function to plot I_D versus V_{DS}. In the plot, identify the ohmic region and the saturation region. In this case, exporting the data is useful so that you can plot multiple curves on the same graph.

8. Repeat part 7, generating several curves increasing V_{GS} by 0.04 V each time. If the result starts to look 'strange', you are close to the limit of the component characteristics. In your report, try to put the I_D-versus-V_{DS} plots on a single graph for comparison.

Exercise 2: Build and test a current mirror.

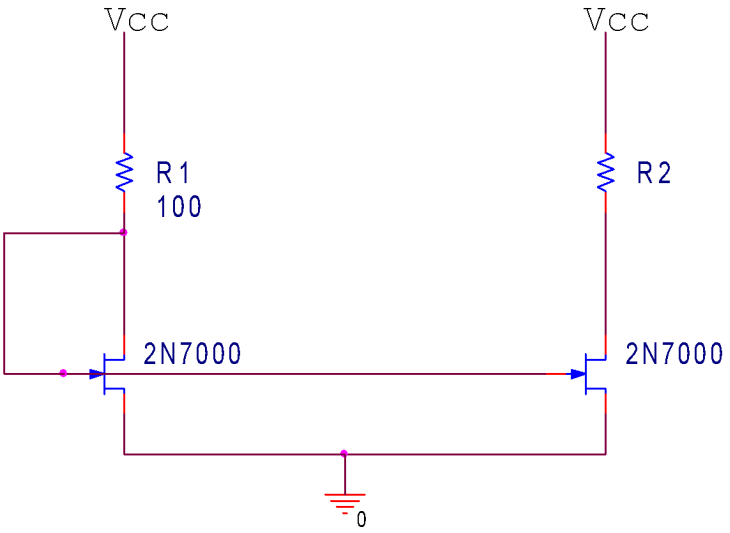

Figure 7: Current mirror

Implement the circuit in Figure 7. Set V_{cc} to 6 V.

1. Short circuit R_2 and measure the current through R_1 and R_2. It is recommended to use the benchtop Multimeter to measure the currents.
2. Change R_2 to 22 Ω, 47 Ω, 100 Ω, 220 Ω and 470 Ω and again measure the current through R_2.
3. Estimate the resistance value for R_2 when the current mirror stops working.
   Are the results somewhat consistent with expectations?

Exercise 3: Common source amplifiers

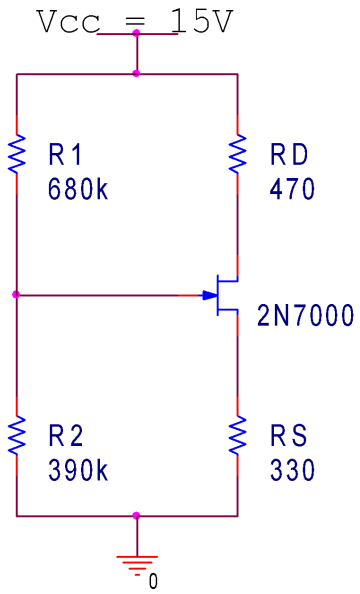

Figure 8: Four resistor biasing

Implement the circuit in Figure 8.

1. Build and measure the DC bias values, V_{DS}, V_{GS}, and I_D for the circuit shown in Figure 8. It is recommended to use the benchtop multimeter to check V_{DS} and V_{GS} (determine I_D from Ohm's Law across R_D or R_S). The benchtop multimeter has a larger input impedance than the Discovery Board.

2. Verify that your FET is operating in the saturation region by checking that

   $$V_{DS} > V_{GS} - V_{TN}$$

   If the circuit is not in saturation, try replacing R_2 with a smaller resistance until the saturation condition is met.
   Compare your measured voltages with calculated values using your measurements from Exercise 1.

Keep the above circuit on your protoboard. You will use this DC biasing circuit for all remaining exercises.

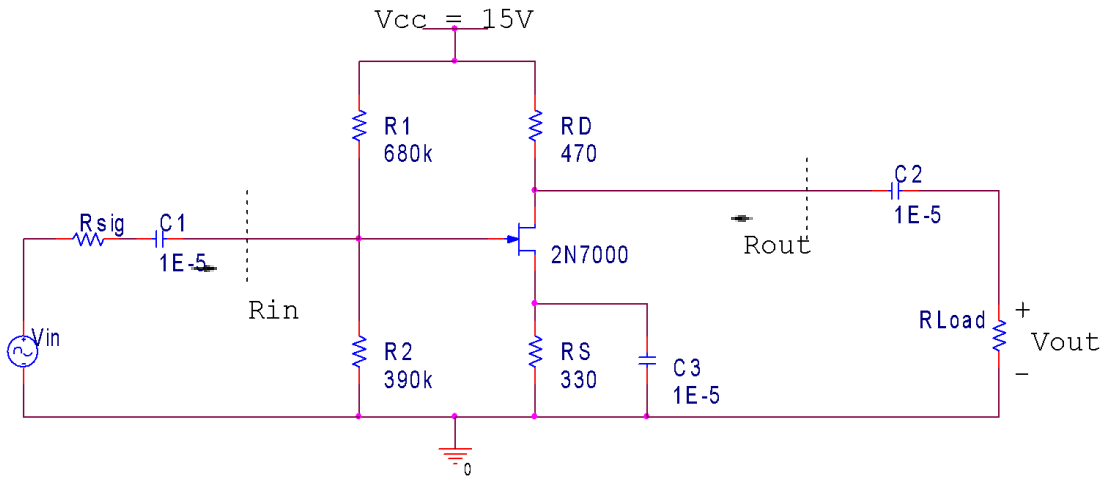

Figure 9: Common source amplifier

Implement the circuit in Figure 9. The DC bias portion of the circuit is the same as the circuit in the previous part of this exercise. Set the AC source signal, V_{in}, to a 0.2 Vpp sinusoidal signal at 1 kHz. As indicated on the front, the isolation capacitors have a DC polarity orientation. For example, in the above circuit, the negative (low) side of C_1 is connected to R_{sig} and the positive (high) side of C_1 is connected to the gate of the NMOS (and R_1, R_2).

After constructing the circuit and turning power on, it may take a long time (> 10 seconds) for the gate voltage to reach the expected value. What causes this effect?

1. Set R_{sig} to 100 Ω and R_{Load} to 100 kΩ Measure the amplitude of the output voltage, V_{out}. Estimate the open-circuit gain of the amplifier, $A_{VOC} = v_{out,o}/v_{in,o}$. (Note, for this R_{sig} and R_{Load}, the above circuit is approximately equal to the open-circuit with $R_{sig} = 0$ and $R_{Load} \rightarrow \infty$.)
   Include a sketch of the small signal model in your report.
   Compare your results to calculated values.
   Why are the resistances for R_{sig} and R_{Load} appropriate for measuring the open-circuit gain, A_{VOC}, of the amplifier?

2. Set R_{sig} to 100 kΩ and R_{Load} to 470 Ω. Measure the amplitude of the output voltage, V_{out}. Estimate the overall gain of the amplifier, $A_V = v_{out} / v_{in}$.

3. Measure the current through R_{sig} and estimate the input resistance, R_{in}, seen looking into the amplifier (the input resistance does not include R_{sig}).

$$i_{in} = \frac{v_{in}}{R_{sig} + R_{in}}$$

4. Use voltage divider concepts with $V_{out,open}$ (open-circuit load voltage) and V_{out} (load voltage with finite load resistor) to determine the output resistance.

$$V_{out} = \frac{R_{Load}}{R_{out} + R_{Load}} V_{out_{open}}$$

Compare your measured R_{in} and R_{out} to calculated values obtained using your 1.1 V_{TN} and k_n estimates.

5. Remove capacitor C_3 and repeat parts 1 to 4.
   Why do the amplifier characteristics change?
   (Try to keep this circuit on your protoboard, only pulling out the transistor for Exercise 4. Alternatively, skip to Exercise 5 and record the frequency characteristics of the circuit.)

Exercise 4: Common gate amplifiers

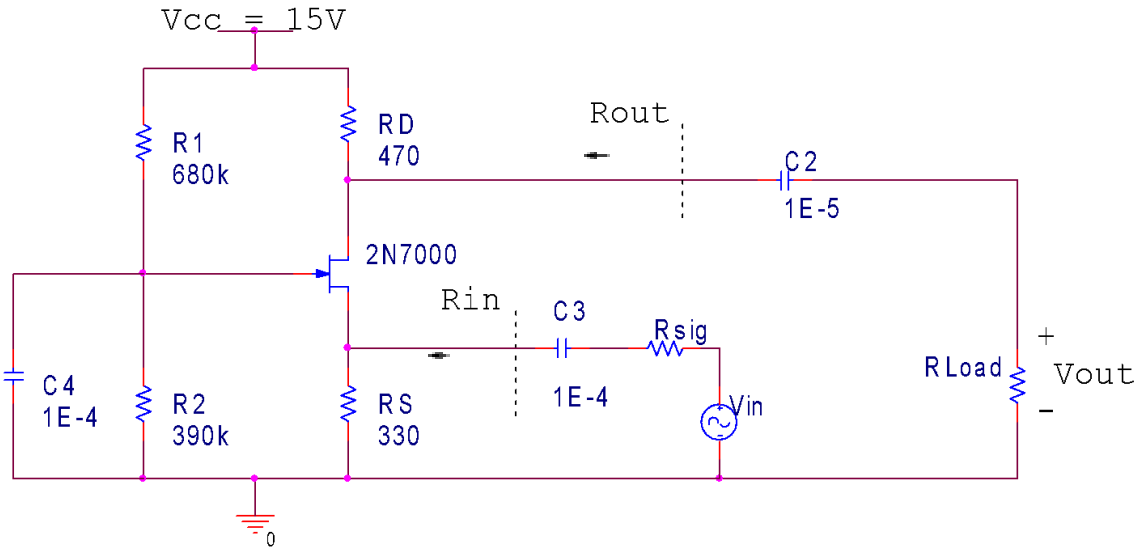

Figure 10: Common gate amplifier circuit

Implement the circuit in Figure 10 with R_{sig} = 10 Ω and R_{Load} = 100 kΩ. Set the source to a 0.1 Vpp, 10 kHz sinusoidal signal.

1. Experimentally determine the amplifier open circuit gain, amplifier input resistance, amplifier output resistance and the overall gain of the circuit. In this case, you can determine R_{in} by measuring the current through R_{sig} and recognizing that $I_{Rsig} = V_{in} / (R_{sig} + R_{in})$. Similarly to the last exercise, a 100 kΩ load resistor is effectively an open circuit load. After measuring the open circuit load, replace R_{Load} with 470 Ω and use voltage divider concepts to find the output resistance. Note: When determining A_{VOC}, the R_{sig} value is not negligible. You can try to short it out
   Compare your results to calculated results.
   (Try to keep this circuit on your protoboard, only pulling out the transistor for Exercise 5. Alternatively, skip to Exercise 6 and record the frequency characteristics of the circuit.)

Exercise 5: Common Source Bandwidth characteristics.

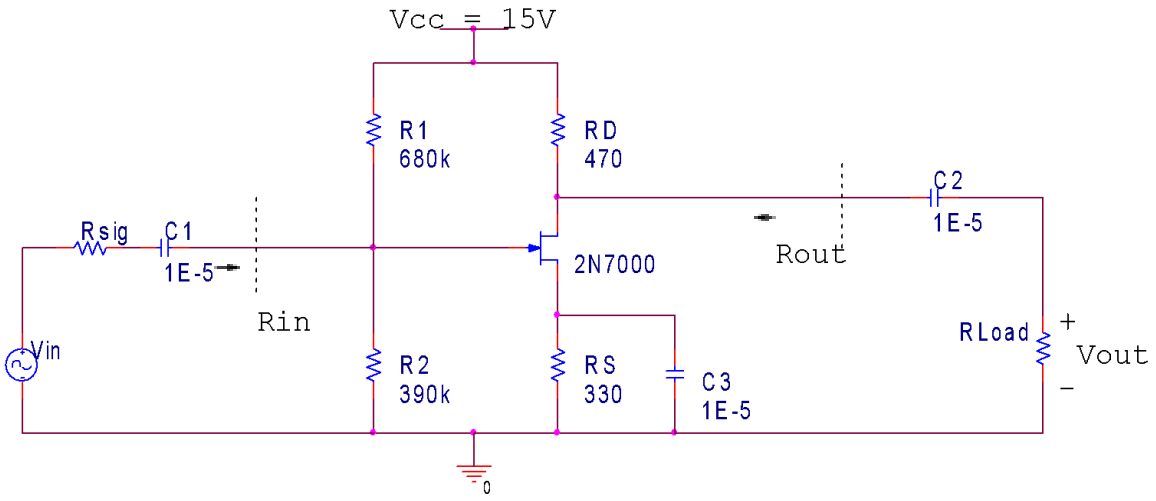

Figure 11: Common source amplifier (same circuit as Figure 9)

Implement the circuit in Figure 11 (the same circuit as Exercise 3). Set the AC source signal, V_{in}, to a 0.2Vpp sinusoidal signal.

1. Using the 2N7000 spec sheet, identify the typical capacitances C_{GS}, C_{DG} and C_{DS} associated with the N-channel MOSFET (by using the equations given on page 2).

2. Set R_{sig} to 100 Ω and R_{Load} to 100 kΩ. Sweep the frequency and determine the bandwidth characteristics of the amplifier. Identify the passband by finding the 3 dB low and high cutoff frequencies.
   Compare your results to calculated estimates. Include the circuits you used to calculate your estimates. Indicate which capacitors are associated with the dominant poles for the low and high cutoff frequencies.
   Would your results change significantly if you increased R_{sig} to 10 kΩ?
   Would your results change significantly if you decreased R_{Load} to 470 Ω?

Exercise 6: Common gate bandwidth characteristics

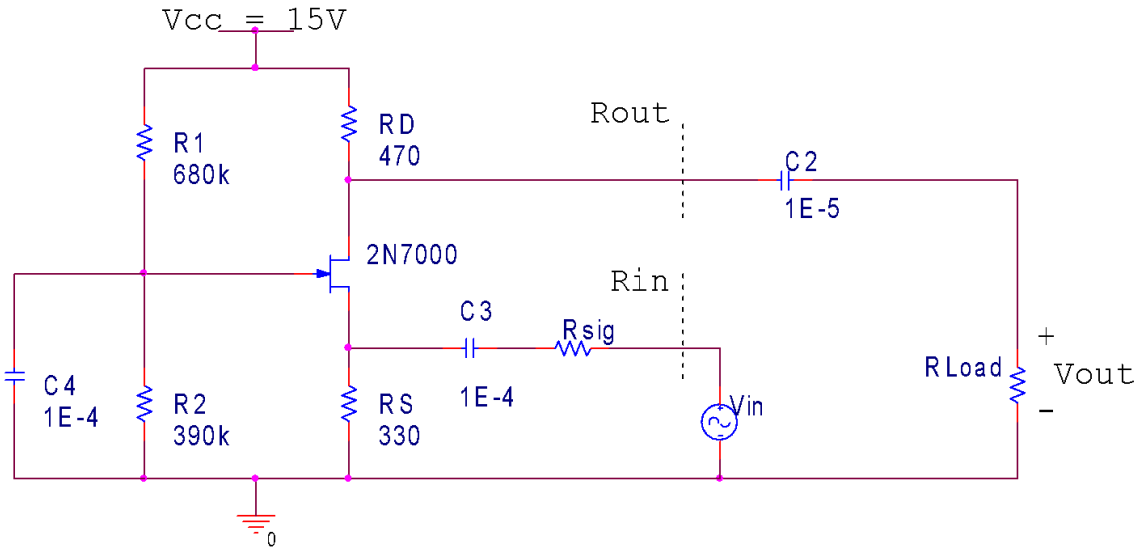

Figure 12: Common gate amplifier (same circuit as Figure 10)

Implement the circuit in Figure 12 (the same circuit as Exercise 4). Set the AC source signal, Vin, to a 0.1 Vpp sinusoidal signal.

1. Set R_{sig} to 100 Ω and R_{Load} to 470 Ω. Sweep the frequency and determine the bandwidth characteristics of the amplifier. Identify the passband by finding the 3 dB low and high cutoff frequencies.
   Compare your results to calculated estimates. Include the circuits you used to calculate your estimates. Indicate which capacitors are associated with the dominant poles for the low and high cutoff frequencies.