Laboratory 7 (3 days):
FET characteristics, Current mirrors, Small signal amplifiers

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Material covered:

- This laboratory has ***three sessions*** allocated for completion.
    - 1st session: Pre-Lab Exercise 1 and Exercise 1. Exercise 2 is optional.
    - 2nd session: Pre-Lab Exercise 2 and Exercise 3. Exercise 4 is optional.
    - 3rd session: Pre-Lab Exercise 3 and Exercise 5. Exercise 6 is optional.
- MOSFET DC biasing, Ohmic region and Saturation region
- Small signal models for MOSFETS
- Common source, common gate, common drain configurations
- Small signal bandwidth

PSpice:

Add the pwrmos library files to the PSpice directory. Note, I believe Orcad version 17.2 already has this library. Refer to Laboratory 2 for instruction on adding .lib and .olb files to PSpice and editing the nom (nomld) files to add the library link.

Data Acquisition:

As with previous labs, you will need to plot *I-V* characteristics for the devices under consideration.

DC measurements:

Due to the impedance characteristics of the Discovery Board, it is recommended to use the benchtop Multimeters to make the DC measurements in Exercise 2 and 3. When using the Multimeters, make sure your connections are correct or you can damage the device. If you are unsure, ask the TA or the Instructor.

DC Bias/Isolation capacitors:

The capacitors used in Exercises 3 to 6 are used for isolating the DC signals relative to the AC input. The electrolytic capacitors available in the laboratory have polarity. The "–" (negative) side is usually marked with a band and has the negative sign printed on it. This side should be connected to the low voltage side of the DC circuit (the AC polarity does not matter).

AC Sweep:

Bode plots can be obtained on the Discovery Board using the network analyzer tool. You can set the start frequency, stop frequency, input amplitude and points per step (more points gives you a smoother curve, but a longer data acquisition time).

Pre-Lab Exercise 1

If necessary, add the pwrmos library as indicated on the first page of the laboratory.

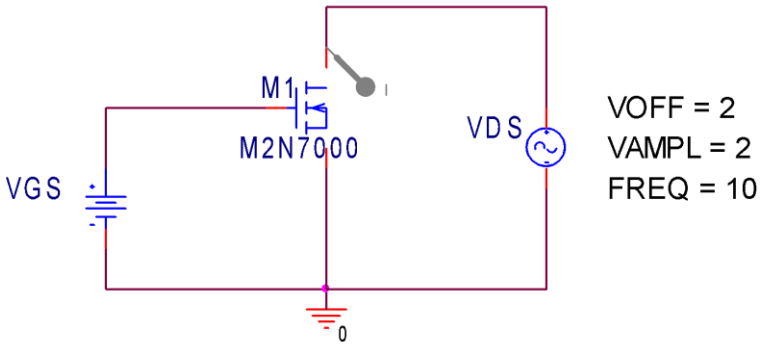
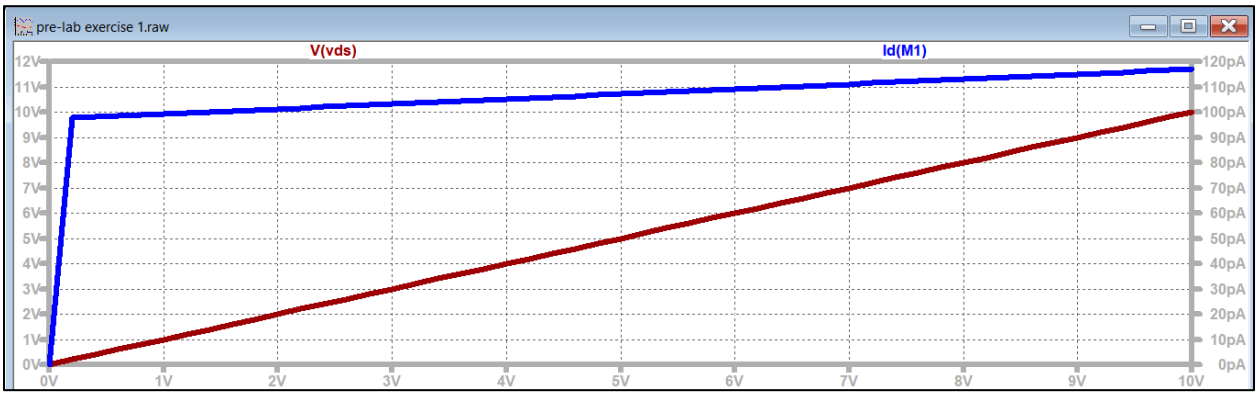


Figure 1: MOSFET circuit

In PSpice, implement the MOSFET circuit shown above. The FET part is 2N7000 in the pwrmos library.

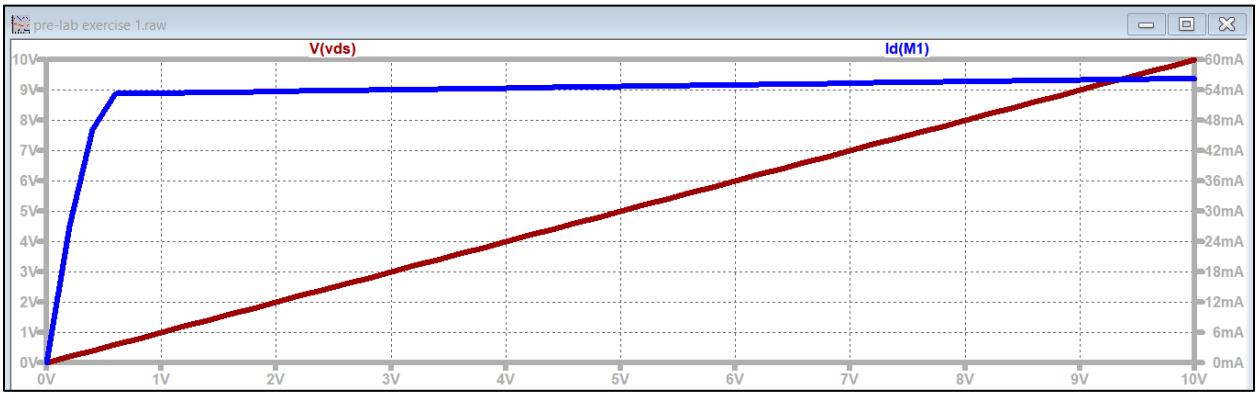
1. Plot the MOSFET current I_D-versus-V_{DS} curve for V_{GS} = 1 V. Vary V_{DS} by running a DC sweep from 0 V to 10 V with an increment of 0.2 V. You can obtain *I-V* curves by placing a current probe as shown above. Edit the Axis Settings under the Plot tab. *How would you describe the I_D-versus-V_{DS} curve (for V_{GS} = 1 V)?*



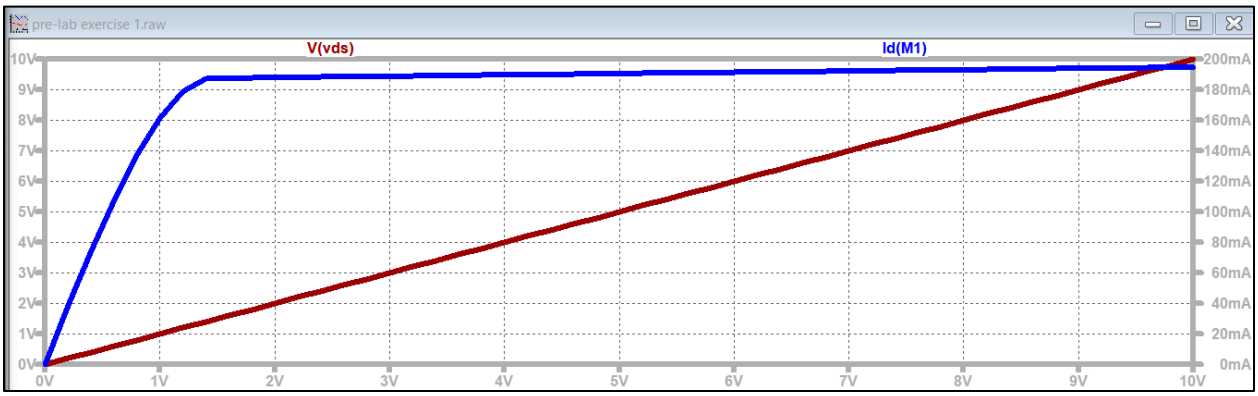
For V_{GS}=1V, the I_D-versus-V_{DS} curve has a linear region from 0V to 0.22V. Past that, it saturates and has a fairly flat slope. The current level at saturation is around 100 pA, which is extremely low (practically negligible).

2. Repeat for V_{GS} = 2 V, 2.5 V and 3 V. For each case, determine the approximate saturation current (where the current levels off).
   What is the dependence of the drain saturation current ($I_{D,sat}$) on the gate-source voltage (V_{GS})?

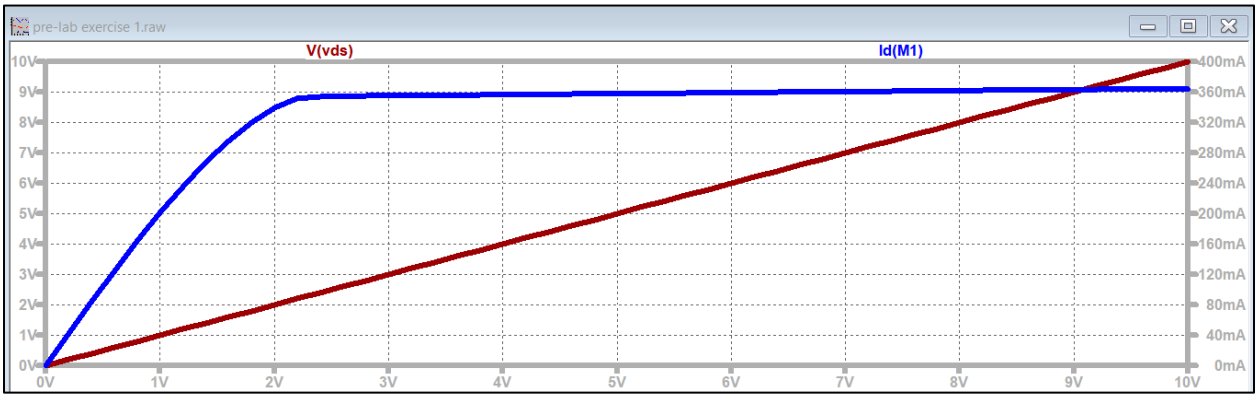
For V_{GS}=2V: saturation current of ~54 mA



For V_{GS}=2.5V: saturation current of ~190 mA



For V_{GS}=3V: saturation current of ~mA



The drain saturation current I_{DSat} is directly proportional to V_{GS}. So, as V_{GS} goes up, the maximum I_{DSat} goes up as well. In order to have a reasonable I_D, the value of V_{GS} must be high enough!

Exercise 1: Investigate MOSFET operation in ohmic mode

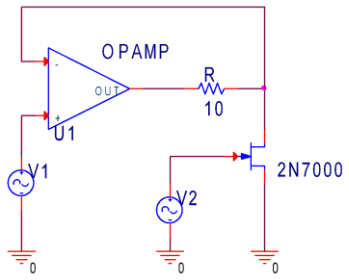


Figure 6: MOSFET analysis circuit

Implement the circuit in Figure 6. Use 15 / –15V voltage supply levels for the LF351/LF353 amplifier.

1. Set the positive amplifier input, V_1 (V_{DS}), to a 0.1 V DC using one of the Mobile Studio / Discovery Board channels. Set the gate input, V_2 (V_{GS}), to the MOSFET to a 1 kHz, 3 Vpp triangle wave with a 1.5 V DC offset using the other channel (the high voltage should be 3 V and the low voltage should be 0 V).

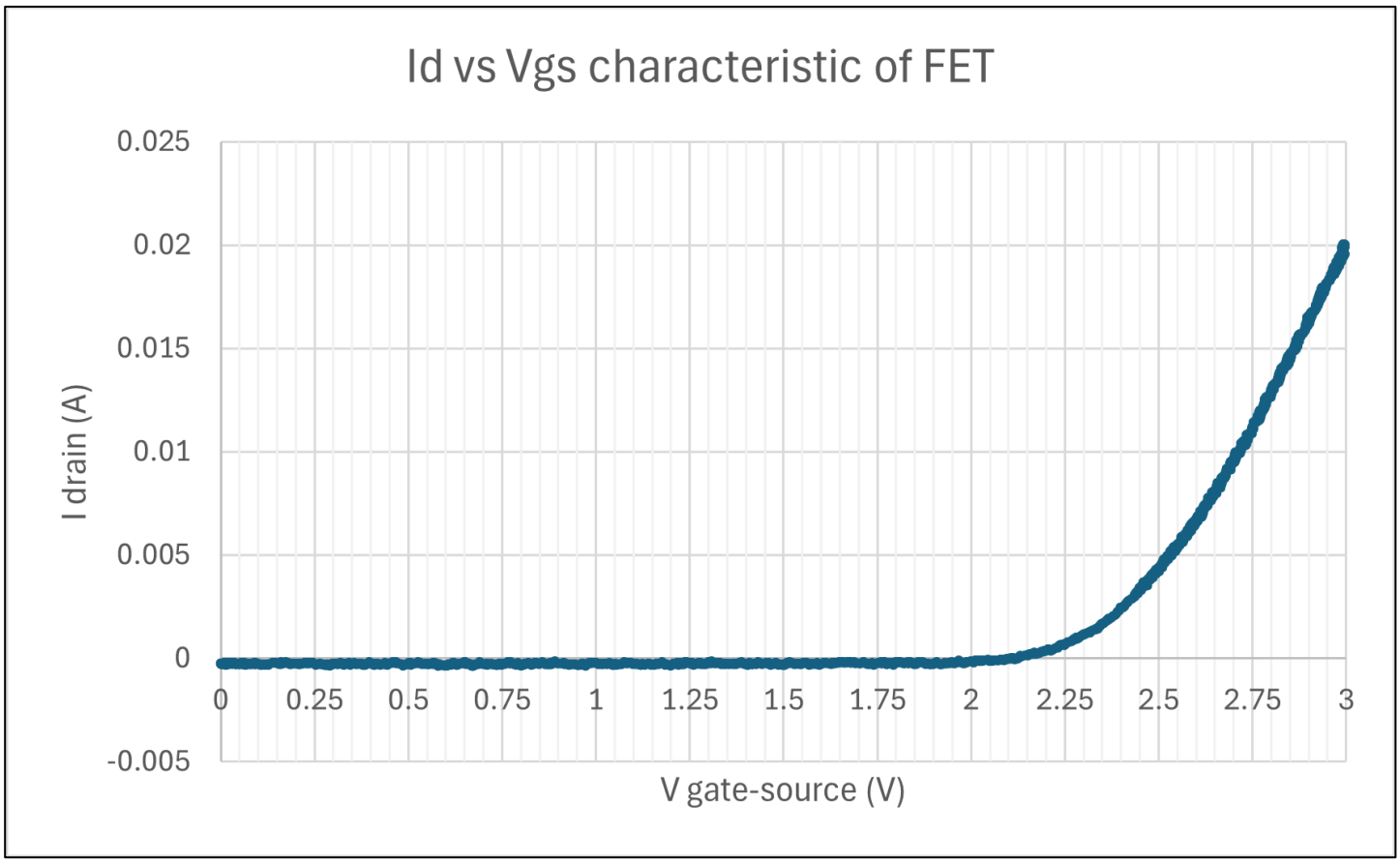
2. Measure the current through resistor, $I_R = I_D$, (Ohm's Law). Recall, you will need to use differential measurements to measure the voltage across the resistor.

	Channel 1	Channel 2
DC	130 mV	100 mV
True RMS	144 mṼ	100 mṼ
AC RMS	62 mṼ	2 mṼ

$$V_{resistor} = 130mV - 100mV = 30mV$$

$$I_R = \frac{V_R}{10\Omega} = \frac{0.030V}{10\Omega} = 3\ mA$$

3. Export the data or use the Math functions to plot the *I-V* characteristics of the MOSFET, I_D-versus-V_{GS}



We see exponential-esque behavior once a certain threshold voltage of Vgs is reached, which matches our theoretical expectation!

4. Estimate the threshold voltage for the MOSFET, $V_{GS} \approx V_{TN}$, by determining the voltage at which point the current starts flowing through the MOSFET.

The current starts flowing around a value of $V_{GS} = 2.25V$, so it is safe to estimate that:

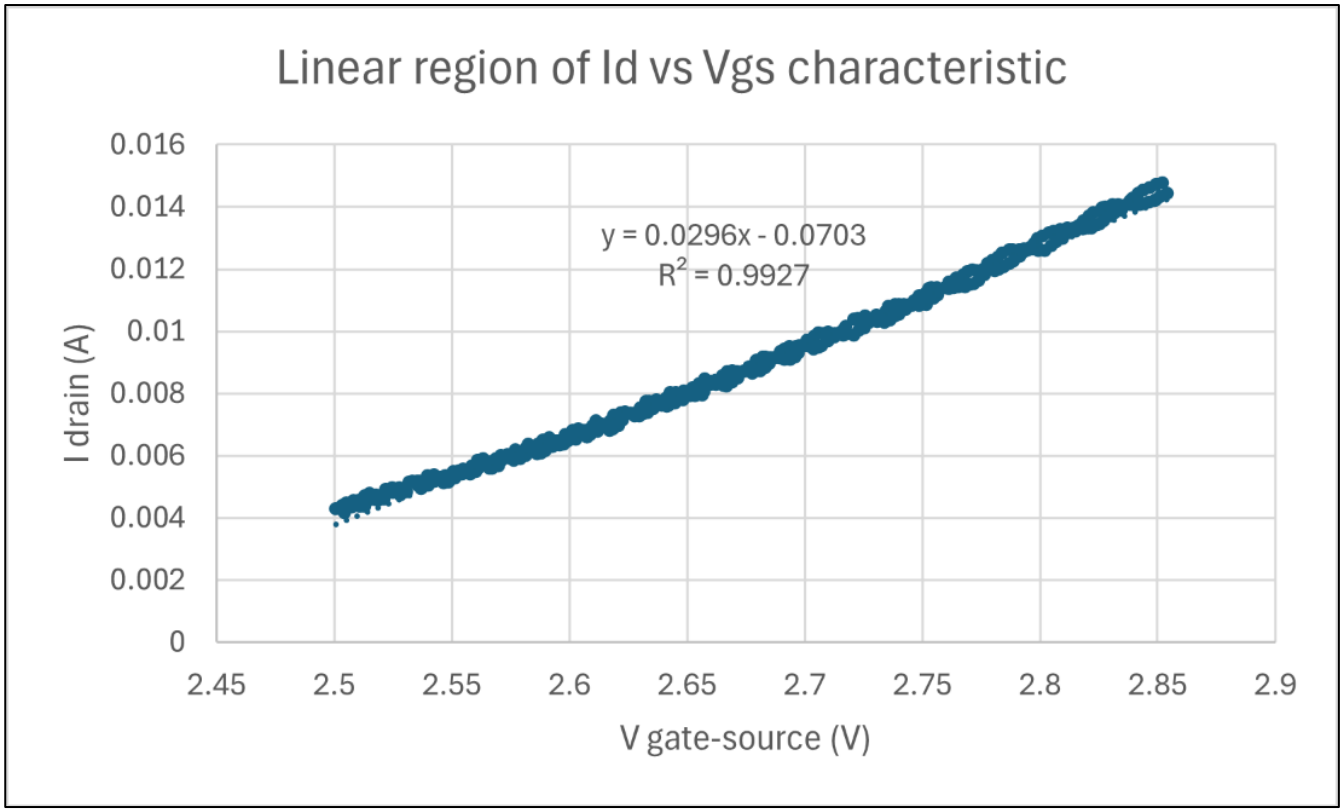
$$\boldsymbol{V_{TH} \approx 2.25V}$$

5. Estimate the kn parameter by determining the slope of the linear portion of the ID-versus-VGS curve. Recall, in the ohmic region

$$ID = kn\,[\,(VGS - VTN)\,VDS - \tfrac{1}{2}\,VDS2\,]$$

with a linear approximation for the condition VDS << VGS – VTN

$$ID = kn'\,(WG/LG)\,[\,(VGS - VTN)\,VDS\,] \qquad \text{where } kn = kn'\,(WG/LG)$$



So our value of kn=0.0296

Or it might be the case that based on the equation kn=0.0296 / Vds, but we were unable to measure Vds simultaneously with Vgs (would have needed a 3rd channel on the AD2).

Record the values you measured in part 4 and 5. Use those values in the other Exercises. Save the transistor for the other Exercises. Keep the circuit. If you wind up losing your transistor, use the circuit to again determine the threshold voltage and transconductance parameter of your new transistor.

6. Set the positive amplifier input, V_1 (V_{DS}), to a 1 kHz, 5 Vpp triangle wave with a 2.5 V DC offset using the other channel (the high voltage should be 5 V and the low voltage should be 0 V). Set V_2 (V_{GS}) to DC and adjust the gate input such that you start to see current flowing through the resistor (the resistor voltage becomes nonzero for part of the cycle). Make a note of that threshold voltage and compare it to your earlier estimate. Increase the gate voltage by 0.04 V (DC) such that you see a larger current through the resistor.

At Vgs=2.1V: Max durrent Id = 38 uA (basically nothing)

At Vgs = 2.2V: Max current Id = 0.5 mA (still low)

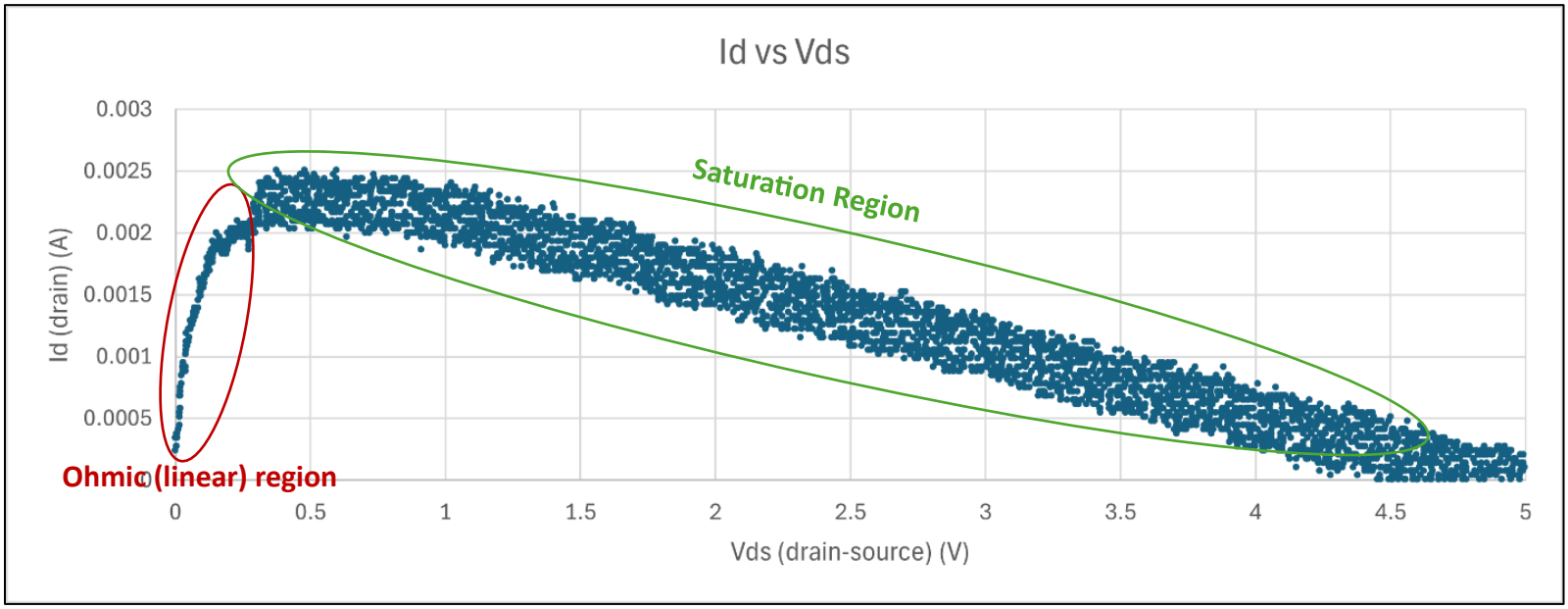
At Vgs = 2.25V: Max current Id = 0.85 mA

At Vgs = 2.3V: Max current Id = 1.52 mA

So since we got noticeable current in the ~1 mA range around a Vgs of 2.25V, it is reasonable to say that our earlier estimate of $V_{TH} = 2.25V$ was accurate

7. Measure the current through the resistor and the drain source voltage, V_{DS}. Again, export the data or use the Math function to plot I_D versus V_{DS}. In the plot, identify the ohmic region and the saturation region. In this case, exporting the data is useful so that you can plot multiple curves on the same graph.

After increasing Vgs to 2.3 + 0.04 = 2.34V, we measure:



8. Repeat part 7, generating several curves increasing V_{GS} by 0.04 V each time. If the result starts to look 'strange', you are close to the limit of the component characteristics.
   In your report, try to put the I_D-versus-V_{DS} plots on a single graph for comparison.

   For Vds above, where Vgs=2.34V, the saturation region has a noticeable "sag" or downward slope.

   As the value of Vgs is increased, the downward slope in the saturation region becomes less extreme.