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IE lab 7p2

Pre-Lab Exercise 2:

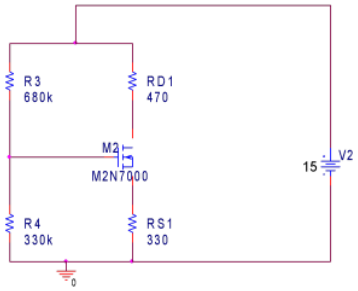

Figure 2: MOSFET circuit

1. Implement the circuit in PSpice and run a Bias Point analysis. Recall, the FET is the 2N7000 in the pwrmos library. Verify that your circuit is in saturation. Note, the PSpice model for the 2N7000 has different characteristics, VTN = 1.73 V and kn ≈ 0.06 A/V2 . For the PSpice values, compare the simulated results to calculated results using the characteristics of the FET model for the 2N7000.

Saturation: VDS>=VGS-VTN
VD=10.766V
VG=4.9V
VS=2.973V
VDS=7.793V
VGS=1.927V
VTN=1.73V
7.793V>=1.927V-1.73V
The MOSFET is well in saturation

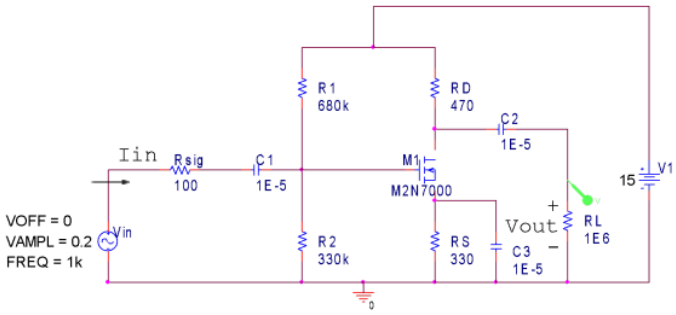

Figure 3: MOSFET circuit

2. Implement the above circuit in PSpice and determine the open circuit gain, AVOC = |vout| / |vin| and the input resistance, Rin = |vin| / |iin|.

AVOC=Vout/Vin
Vout=3.06V
Vin=0.2V
AVOC=15.3
Rin=Vin/Iin
Vin=0.2V
Iin=734.4nA
Rin=0.2V/734.4nA=272kOhms

Exercise 3: Common source amplifiers

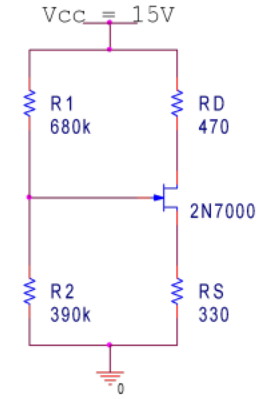

Figure 8: Four resistor biasing

Implement the circuit in Figure 8.

1. Build and measure the DC bias values, VDS , VGS , and ID for the circuit shown in Figure 8. It is recommended to use the benchtop multimeter to check VDS and VGS (determine ID from Ohm's Law across RD or RS). The benchtop multimeter has a larger input impedance than the Discovery Board.

VDS=7.8V
VGS=2.49V
ID=V(RD)/RD=4.218V/470Ohm=8.97mA

2. Verify that your FET is operating in the saturation region by checking that
   VDS > VGS – VTN
   If the circuit is not in saturation, try replacing R2 with a smaller resistance until the saturation condition is met. Compare your measured voltages with calculated values using your measurements from Exercise 1.

VTN~=2.25V
7.8V>2.49V-2.25
The MOSFET is well in saturation

Keep the above circuit on your protoboard. You will use this DC biasing circuit for all remaining exercises

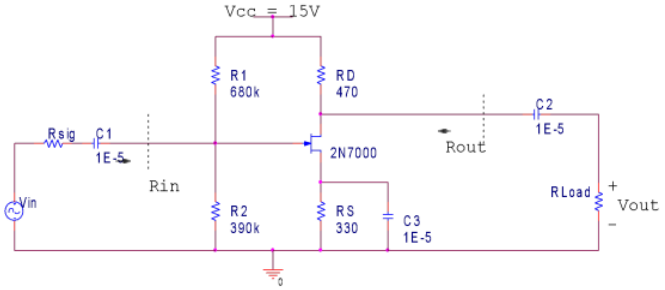

Figure 9: Common source amplifier

Implement the circuit in Figure 9. The DC bias portion of the circuit is the same as the circuit in the previous part of this exercise. Set the AC source signal, Vin , to a 0.2 Vpp sinusoidal signal at 1 kHz. As indicated on the front, the isolation capacitors have a DC polarity orientation. For example, in the above circuit, the negative (low) side of C1 is connected to Rsig and the positive (high) side of C1 is connected to the gate of the NMOS (and R1 , R2).
After constructing the circuit and turning power on, it may take a long time (> 10 seconds) for the gate voltage to reach the expected value. What causes this effect?

1. Set Rsig to 100 Ω and RLoad to 100 kΩ Measure the amplitude of the output voltage, Vout . Estimate the open-circuit gain of the amplifier, AVOC = vout,o /vin,o . (Note, for this Rsig and RLoad , the above circuit is approximately equal to the open-circuit with Rsig = 0 and RLoad → ∞.)
   Include a sketch of the small signal model in your report.
   Compare your results to calculated values.
   Why are the resistances for Rsig and RLoad appropriate for measuring the open-circuit gain, AVOC , of the amplifier?

Voutoc=2.9069Vpp
Vin=0.2Vpp
AVOC=14.53

Rsig and Rload are appropriate, offering low series input impedance and high parallel output impedance, avoiding current limitations on the input and voltage sag on the output

2. Set Rsig to 100 kΩ and RLoad to 470 Ω. Measure the amplitude of the output voltage, Vout . Estimate the overall gain of the amplifier, AV = vout/ vin .

	Name	Value
C1	Amplitude	0.54154 V
C1	Peak2Peak	1.0922 V

Vout=1.0922Vpp
AV=1.0922V/0.2V=5.461

3. Measure the current through Rsig and estimate the input resistance, Rin , seen looking into the amplifier (the input resistance does not include Rsig).

$$i_{in} = \frac{v_{in}}{R_{sig} + R_{in}}$$

Isig=0.22V/100kOhm=220pA
220pA=0.2V/(100k+Rin)
Rin=809kOhm
This is an appropriate “near infinite” value

4. Use voltage divider concepts with Vout,open (open-circuit load voltage) and Vout (load voltage with finite load resistor) to determine the output resistance.

$$V_{out} = \frac{R_{Load}}{R_{out} + R_{Load}} V_{out_{open}}$$

Compare your measured Rin and Rout to calculated values obtained using your 1.1 VTN and kn estimates

Voutoc=2.9069Vpp
Voutload=1.0922Vpp
Voutload=Voutoc Rload/(Rout+Rload)
1.0922V=2.9069V 470Ohm(Rout+470)
Rout=780Ohm

VTN=2.25V, 1.1*2.25V=2.475V
kn=0.0296

5. Remove capacitor C3 and repeat parts 1 to 4. Why do the amplifier characteristics change?

Rsig=100, Rload=100k

	Name	Value
C1	Amplitude	131.29 mV
C1	Peak2Peak	267.31 mV

Voutoc=267mV
AVOC=1.33655 (much lower)

Rsig=100k, Rload=470

	Name	Value
C1	Amplitude	47.142 mV
C1	Peak2Peak	96.311 mV

Voutload=96.311mV
AV=0.4815, (much lower, now below 1)

Input and output resistance should also change slightly as they pass AC to GND

(Try to keep this circuit on your protoboard, only pulling out the transistor for Exercise 4. Alternatively, skip to Exercise 5 and record the frequency characteristics of the circuit.)