NCTU-EE IC LAB – Fall 2019

Lab12 Exercise

Design: Artificial Neural Network APRII

Data Preparation

1. Extract test data from TA's directory:

   % tar xvf ~iclabta01/Lab12.tar

2. The extracted LAB directory contains:

   a. 00_TESTBED
   b. 01_RTL
   c. 02_SYN
   d. 03_GATE
   e. 04_MEM
   f. 05_APR
   g. 06_POST

Description

In this lab you are gonna finish the **backend flow (APR)** for this design and use the **IR drop and Power Analysis** tool for your layout.

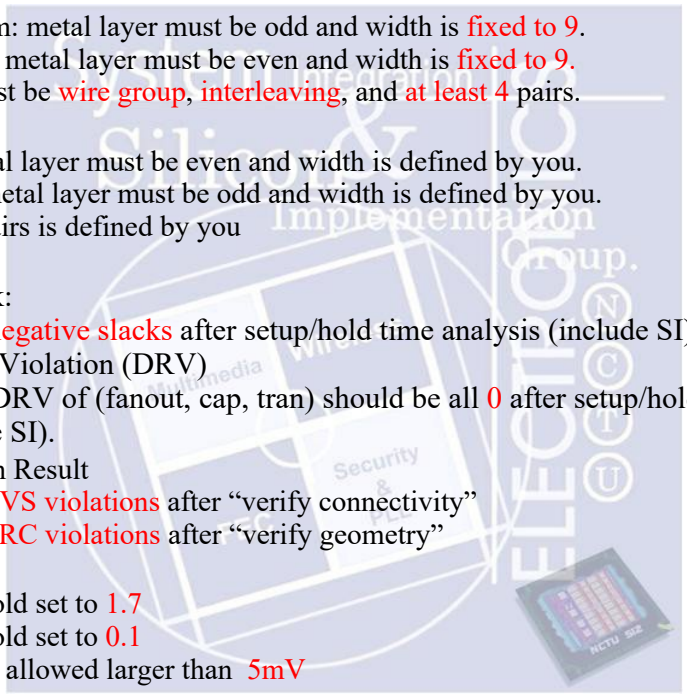
Inputs and Outputs

Input Signals	Bit Width	Definition
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid_d	1	High when data_point is valid.
in_valid_t	1	High when target is valid.
in_valid_w1	1	High when weight1 is valid
in_valid_w2	1	High when weight2 is valid
data_point	8	The input data point, 4 data points represent a data. The arithmetic representation follows the IEEE-754 floating number format.
target	8	The target for current data. The arithmetic representation follows the IEEE-754 floating number format.
weight1	8	The weight for first layer. The arithmetic representation follows the IEEE-754 floating number format.
weight2	8	The weight for second layer. The arithmetic representation follows the IEEE-754 floating number format.

Output signal	Bit width	Definition
out_valid	1	Enable output check
out	8	Output number

Layout Specifications

1. CHIP.sdc (provided by TA) period is fixed to 20ns input/output delay is fixed to 10ns
2. Core power pad and io power pad
   a. At least one pair at each side.
3. Floorplanning
   a. Core size:
      ✓ Defined by you
   b. Core to IO boundary:
      ✓ Each side must larger than 100
4. Power Planning
   a. Core Ring
      ✓ Top & Bottom: metal layer must be odd and width is fixed to 9.
      ✓ Left & Right: metal layer must be even and width is fixed to 9.
      ✓ Each side must be wire group, interleaving, and at least 4 pairs.
   b. Stripes
      ✓ Vertical: metal layer must be even and width is defined by you.
      ✓ Horizontal: metal layer must be odd and width is defined by you.
      ✓ Number of pairs is defined by you
   c. Timing Analysis
      ✓ Timing Slack:
        NO negative slacks after setup/hold time analysis (include SI)
      ✓ Design Rule Violation (DRV)
        The DRV of (fanout, cap, tran) should be all 0 after setup/hold time analysis (include SI).
   d. Design Verification Result
      ✓ LVS : No LVS violations after "verify connectivity"
      ✓ DRC : No DRC violations after "verify geometry"
   e. Rail Analysis:
      ✓ VDD Threshold set to 1.7
      ✓ GND Threshold set to 0.1
      ✓ No IR drop is allowed larger than 5mV



Note

1. Complete CHIP.io and CHIP_SHELL.v
2. Do all the flow as in APRI (Lab11) with Layout Specification above
3. Run Power Analysis (Setup & Run)
4. Run Rail Analysis
   - Set PG Library Mode
   - Generate PG Library
   - Setup Rail Analysis
   - Run Rail Analysis
5. Report Power Grid Library
6. Observe the IR Drop to analyze whether IR drop is within 5mV.
7. Please upload the following file on e3 platform before (2019/12/30 Mon 12:00)
   - CHIP_APR2_iclab??.tar:
     Please follow the following steps to put all required files in one folder named CHIP_APR_iclab??/ and compress the folder as CHIP_APR2_iclab??.tar:
     1) In Exercise/05_APR folder, create a folder named CHIP_APR2_iclab??
        ```
        linux01[Exercise/05_APR]% mkdir CHIP_APR2_iclab??
        ```
     2) Copy the following files/directories into the folder:
        i. CHIP.inn
        ii. CHIP.inn.dat (this one is a directory so remember to use -r)

iii. CHIP_SHELL.v
iv. CHIP.io

3) Compress the CHIP_APR2_iclab?? folder into the tar file CHIP_APR2_iclab??.tar

```
linux01[Exercise/05_APR]% tar cvf CHIP_APR2_iclab??.tar CHIP_APR2_iclab??/
```

Grading Policy

- **Post simulation correctness & Within Tolerable IR Drop: 100%**

Appendix

- Provided library files
  - Timing libraries

Directory	Contain
/05_APR/Library/lib/	slow.lib
	fast.lib
	umc18io3v5v_slow.lib
	umc18io3v5v_fast.lib

  - Physical libraries

Directory	Contain
/05_APR/Library/lef/	umc18_6lm.lef
	umc18_6lm_antenna.lef
	umc18io3v5v_6lm.lef

  - RC extraction table/files

Directory	Contain
/05_APR/Library/rc/	umc18_1p6m.captbl
	RCGen.tch

  - CeltIC libraries

Directory	Contain
/05_APR/Library/cdb/	slow.cdb
	fast.cdb

  - Layermap

Directory	Contain
/05_APR/Library/layermap/	lefdef.layermap
	qrc_lefdef.layermap