NCTU-EE IC LAB – Fall 2019

Lab11 Exercise

Design: Local Binary Pattern

Data Preparation

1. Extract test data from TA's directory:

   % tar xvf ~iclabta01/Lab11.tar

2. The extracted LAB director contains:

   a. Exercise

Design Description

This lab will use a basic digital image process operation, local binary pattern, to enhance image, and you don't have to write the design just run the APR flow for LBP.

Input and outputs

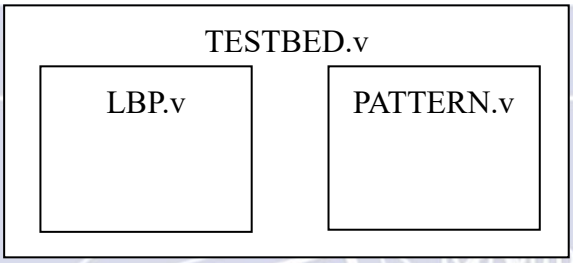
Input signal	Bit width	Definition
clk	1	Clock
rst_n	1	Asynchronous active-low reset
invalid	1	in_image is valid when invalid is high
in_image[7:0]	8	input image

Output signal	Bit width	Definition
out_valid	1	Should be set to low after reset and not be raise when in_valid is high. Should set to high when image[7:0] is ready.
out_image[7:0]	8	Asynchronous active-low reset

Specifications

1. Top module name : LBP
2. Asynchronous , active low reset
3. The clock period is 3ns for RTL to gate-sim, defined by yourself at APR and post-sim
4. Input delay is half of clock period except clock signal
5. Output delay is 1ns at APR anf post-sim
6. The SRAM has been given , memory files are in 04_MEM

Block Diagram



Constraints of the design in APR flow

1. Floorplaning
   - **a.** Core size
     - ➢ Define by user, by it matters your performance
   - **b.** Core to IO boundary
     - ➢ Each side must be more than **100**.
2. Power planning
   - **a.** Core Ring
     - ➢ Top & Bottom: metal layer must be odd (1,3,…) and width is 9.
     - ➢ Left & Right: metal layer must be even (2,4,…) and width is 9.
     - ➢ Each side must be **wire group**, **interleaving**, and at least **3 pairs**.
   - **b.** Stripes
     - ➢ Vertical: metal layer must be even (2,4,…) and width is 4.
     - ➢ Horizontal: metal layer is must be odd (1,3,…) and width is 4.
     - ➢ The maximum distance between two stripes or the stripe and edge should be less than **200**.
3. Timing analysis results
   - **a.** Timing Slack
     - ➢ **NO negative slacks** after setup/hold time analysis (include SI).

b. Design Rule Violation (DRV)

- The **DRV of (fanout, cap, tran)** should be **all 0** after post-Route setup/hold time analysis (including SI)

4. Design verification results
   a. Layout vs. Schematic (LVS)
   - **NO LVS violations** after ***"verify connectivity"***.

   b. Design Rule Check (DRC)
   - **NO DRC violations** after ***"verify geometry"***.

Grading Policy

APR and Post Simulation Correctness (70%)

a. Complete the APR flow and meet all the constraints above.

b. Pass the post-layout gate-level simulation

Performance(30%)

a. Core area*Clock_Period(@posim)
   *** (Latency is not counted) ***

b. You will only get performance score with correct APR and Post Simulation Result

Note

1. Please upload the required files on new e3 platform
   a. Naming rule: iclabXX.tar
   b. The archive file must include the following files:
   (1)cycle_iclabXX.txt : record the clock period of your post-layout simulation
   (2)CHIP_iclabXX.v (Rename from the file "CHIP_LAYOUT.v ")
   (3)CHIP_iclabXX.sdf (Rename from file "CHIP.sdf ")
   (4)iclabXX.inn.dat.tar
   (Rename the file "CHIP.inn.dat" to "iclabXX.inn.dat" and compress the file)
   (5)iclabXX.inn (Rename from the file "CHIP.inn ")
   (6)CHIP_iclabXX.sdc (Rename from the file "CHIP.sdc ")
   (7)CHIP_iclabXX.io (Rename from the file "CHIP.io ")
2. Template folders and reference commands:
   00_TESTBED/ (PATTERN files)
   04_MEM/(no need to modify)
   05_APR/ (Place & Route Folder)
   06_POST/ (Post Layout Simulation) **./01_run**
   You can key in **./09_clean_up** to clear all log files and dump files in each folder