NCTU-EE IC LAB – Fall 2019

Lab05 Exercise

Design: Matrix Computation

Data Preparation

1. Extract files from TA's directory:
   % tar xvf ~iclabta01/Lab05.tar
2. The extracted LAB directory contains:
   a. Practice/
   b. Exercise/

Design Description

In this exercise, you will build a design to complete matrix computations. For the matrix requires large space to store, you are suggested to use memory for finishing this lab.

There is a current matrix C in memory, and you will receive an input matrix M. Then the 7 possible operations are given to do with them:

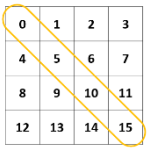
- **Set-up**:
  Set current matrix C as input matrix M. (C ← M)
  Matrix size will be 4x4, 8x8, 16x16 and 32x32
  This operation will be given as the first operation to set matrix at the beginning, and it is also used to reset matrix.

- **Addition**:
  Add current matrix C with input matrix M. Their sizes are same. (C ← M + C)

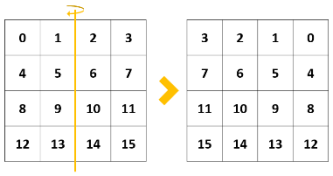
- **Multiplication:**
  Multiply current matrix C with input matrix M. Their sizes are same. (C ← MC)

- **Transpose:**
  Transpose current matrix C. (C ← C^T)
  This operation will not input matrix.

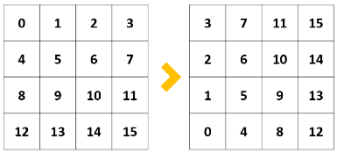
- **Trace:**
  Compute trace of current matrix C.
  This operation will not input matrix.



- **Mirror:**
  Mirror current matrix.
  This operation will not input matrix.



- **Rotate counterclockwise:**
  Rotate current matrix.
  This operation will not input matrix.



Inputs

Input	Bit Width	Definition and Description
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid	1	High when input signals are valid.
in_data	32	Element of input matrix, **unsigned**. It will be sent in **raster scan order** continuously.
size	2	The signal will be given at the first cycle of **in_valid** and **only given with set-up operation**. It defines which size to be use to set up or reset matrix. **2'b00:** 4x4 **. 2'b01:** 8x8**. 2'b10:** 16x16**. 2'b11:** 32x32**.**
action	3	The signal will be given at the first cycle of **in_valid**. The definition is as following: **3'b000**: Trace. **3'b001**: Mirror. **3'b010**: Transpose. **3'b011**:. Rotate counterclockwise **3'b100**: Set-up. **3'b101**: Addition. **3'b110**: Multiplication.

Outputs

Output	Bit Width	Definition and Description
out_valid	1	High when out is valid. It cannot be overlapped with **in_valid** signal. If operation is trace, **out_valid** last for 1 cycle
out_data	32	Output result matrix in raster scan order.

1. The input of **in_data** is delivered in **raster scan order** for **current size of**

matrix(16x16, 32x32…) cycles continuously. When **in_valid** is low, input is tied to unknown state.

2. All input signals are synchronized at negative edge of the clock.

3. The bit width of elements of input matrix and current matrix is 32. It is ensured the current matrix will not be overflow.

4. The output signal **out_data** must be delivered for **current size of matrix cycles continuously**, and **out_valid** should be high simultaneously. If operation is trace, **out_valid** last for 1 cycle and **out_data** must be trace value.

Specifications

1. Top module name: MC (design file name: MC.v)
2. **It is asynchronous reset and active-low architecture. If you use synchronous reset in your design, you may fail to reset signals should be reset after the reset signal is asserted.**
3. **The reset signal (rst_n) would be given only once at the beginning of simulation. All output signals should be reset after the reset signal is asserted.**
4. The data type in the synthesis result **CAN NOT** include any **LATCH**.
5. After synthesis, the area report is valid only when the slack in the end of timing report is **non-negative** and the result should be **MET**.
6. The next input will come in **3~5** cycles after your **out_valid** is pulled down.
7. The **out_valid** cannot overlap with **in_valid**.
8. The execution latency is limited in **50000 cycles.** The latency is the clock cycles between the falling edge of the **in_valid** and the rising edge of the **out_valid**. The definition of latency can be view from the sample waveform, and the minimum latency is 0.
9. **In this lab, you must use the memory and generate it yourself. The multiplexer width is fixed to 4, where the number of words and the bits per each word is defined by yourself. We will check it at MC.area in**

02_SYN/Report/ folder. **The area of Macro/Black Box must not be 0. The example is shown in following figure.**

```
Number of ports:                          72
Number of nets:                         5203
Number of cells:                        4530
Number of combinational cells:          4440
Number of sequential cells:               87
Number of macros/black boxes:              3
Number of buf/inv:                       665
Number of references:                    129

Combinational area:             119650.608400
Buf/Inv area:                     7607.477007
Noncombinational area:            5624.942463
Macro/Black Box area:           441686.250000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                566961.800863
Total area:                 undefined
1
```

Fig 1. The area of your memory

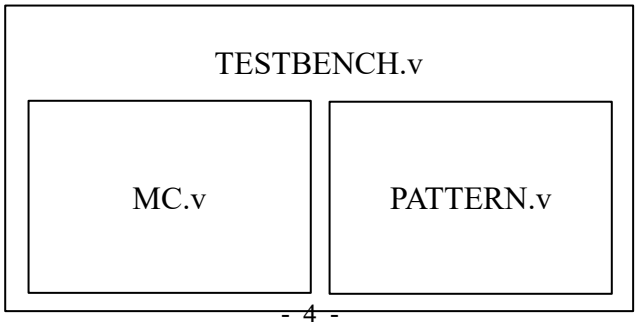
10. **If any port of memory is connected with mismatch width, the memory will not be synthesized and you will get an error message as shown in Fig 2. Even though the design may still pass gate level simulation, you will lose 16 points. In this case, memory area will be 0 in MC.area. We will check it at syn.log and MC.area.**

```
Error: Width mismatch on port 'D' of reference to 'RA1SH' in 'MC'. (LINK-3)
Warning: Unable to resolve reference 'RA1SH' in 'MC'. (LINK-5)
```

Fig 2. Memory port width mismatch error

11. The **out_data** should be correct when **out_valid** is high.
12. The input delay is set to **0.5*(clock period)**.
13. The output delay is set to **0.5*(clock period)**, and the output loading is set to **0.05**.
14. The gate level simulation cannot include any timing violations without the *notimingcheck* command.

Block Diagram



Grading Policy

The performance is determined by the area and delay of your design. The less cost your design has, the higher grade you get.

Function Validity: 70%

Performance: 30% ($Area^3$*(1 + Total Latency*0.001))

Note

1. Please upload the following file on e3 platform before **12:00** on **Oct. 21**:

   MC_iclab??.v (?? is your account no.)

   Ex: MC_iclab99.v

   RA1SH_iclab??.v (?? is your account no.)

   RA1SH_iclab??.db (?? is your account no.)

   Ex: RA1SH_iclab99.v RA1SH_iclab99.db

   a. You can only use one kind of memory.

   b. If these two file are not handed in, **you would fail in the demo**.

   clk_iclab??.txt (?? is your account no.)

   Ex: 7.0_iclab99.txt

2. Template folders and reference commands:

   In RTL simulation, the name of template folder and reference commands is:

   01_RTL:

   "**./01_run**"

   02_SYN/ (Synthesis):

   ./01_run_dc

   (Check **latch** by searching the keyword "**Latch**" in 02_SYN/**syn.log**)

   (Check the design's timing in /Report/MC.timing)

   03_GATE_SIM/:

   ./01_run

   04_MEM/ (Memory location)

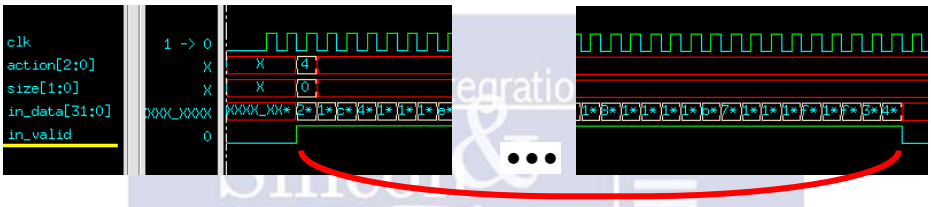
   (You should generate your own memory and put the required files here)

   You can key in **./09_clean_up** to clear all log files and dump files in each folder

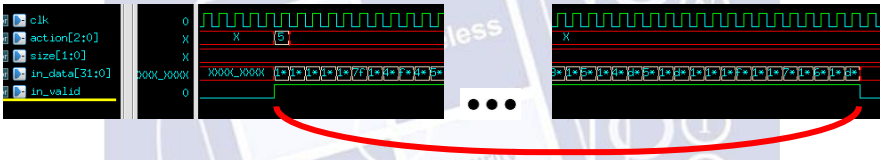
Example Waveform

Input and output signal:

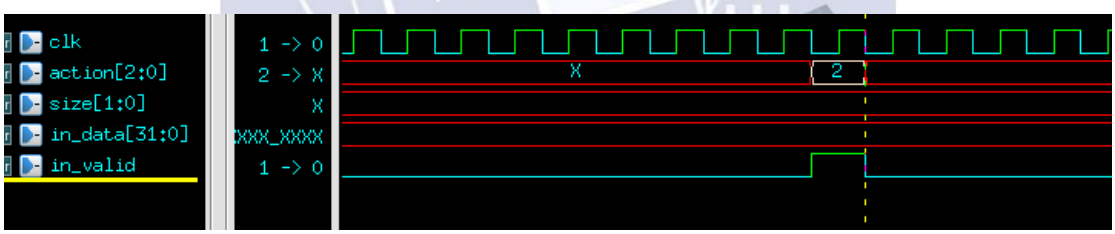
Set-up



Addition



Transpose



Multiplication