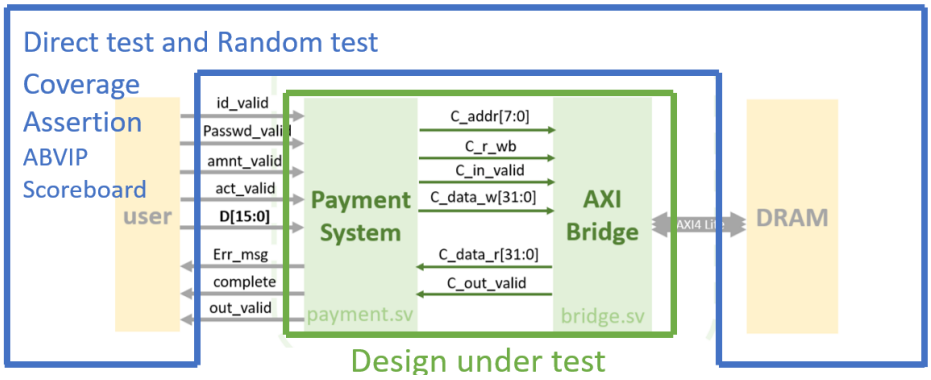
Experience in Verification Using System Verilog

These are labs in IC design Lab course.

1. Purpose:

   To verify a Coin Transaction System. The specification of design is to implement 6 operations: 1. Log in, 2. Transfer money (transfer fee = amount*1/16), 3. Make a deposit, 4. Change ID password, 5. Check balance 6. Exit



2. Method:

   A. Verification with System Verilog Coverage

      (1). Use auto_bin_max to create coverpoint :

         i. ID : 256 bins, each bin hit at least 1 times.

         ii. Complete : 2 bins, each bin hit at least 100 times.

      (2). User-defined state bin:

         i. Passwd : divided into 4 bins, each bin hit 10 times.

      (3). Transition bin :

         i. Action : 24 transition bins, each bins hit at least 10 times.

      (4). Cross bin :

         i. Combination of complete & balance bins : each combination occur at least 20 times.

   B. Verification with System Verilog Assertion

      (1). SVA

         i. If action is completed, inf.err_msg must be 4'b0.

      (2). SVA + Glue Logic

         i. When aciotn is trnsf, id_valid should come earlier than amnt_valid. The gap length between id_valid and amnt_valid is at least 1 cycle.

      (3). SVA + Nondeterministic Constants

         i. Assume AXI in_valid will not occur during bridge transmit data.

      (4). ABVIP + Glue Logic

         i. Use glue logic to define test mode which is used to control ABVIP outgoing port.