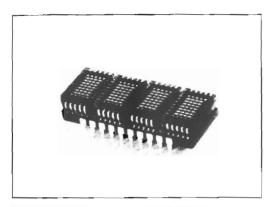
0.270" 4-Character, 5 × 7 Dot Matrix Alphanumeric Programmable Display™ With Built-In CMOS Control Functions



NOT FOR NEW DESIGNS

(Refer to the Improved Extended Performance of PD 3535/7 for Similar Applications)

FEATURES

- Four 0.27" Character Subassemblies, Surface-Mounted on Ceramic Substrate in Bright Green or High-Efficiency Red
- Readable from 12 Feet (4 meters)
- . Built-In Memory, Decoders, Multiplexer and Drivers
- Wide Viewing Angle, X Axis +55°, Y Axis +70°
- 96-Character ASCII Format (Both Upper and Lower Case Characters)
- . 8-Bit Bidirectional Data BUS
- READ/WRITE Capability
- Resistant to Most Common Solvents
- . Categorized for Luminous Intensity
- 100% Burned In and Tested
- Dual In-Line Package Configuration, 0.600" Wide, 0.100" Pin Centers
- End-Stackable Package
- Internal or External Clock
- Built-In Character Generator ROM
- TTL Compatible
- Easily Cascaded for Multidisplay Operation
- · Less CPU Time Required
- Software Controlled Features:

Programmable Highlight Attribute (Blinking, Non-Blinking)

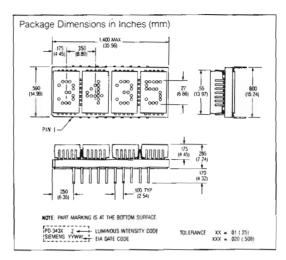
Asynchronous Memory Clear Function

Lamp Test

Display Blank Function

Single or Multiple Character Blinking Function Programmable Intensity, Three Brightness Levels

Specifications are subject to change without notice



DESCRIPTION

The PD 3435 and PD 3437 are four digit display system modules. The display portion consists of four surface-mounted 7×5 dot matrix arrays. The arrays consist of the latest technology in solid state light emitting diodes fully encapsulated in double molded packages. The $0.27'' \times 0.19''$ characters, readable from 12 feet, come in either High Efficiency Red or Bright Green.

Completing the display system are two CMOS IC's mounted and encapsulated within a ceramic substrate. The CMOS intelligence provides timing and control logic to efficiently strobe and drive the display matrixes for maximum viewability, with minimum power consumption. The intelligent CMOS also provides memory to hold four ASCIIcharacters and one control word. The on-board IC has an ASCII character ROM and generator that translates 96 alphanumeric ASCII symbols into the appropriate drive signals for the four displays. The control word commands display attributes to allow the user to software program any of the following features: clear memory, test all LED's, blink the entire display, blink individual characters, display cursors, alternately flash cursors and characters, or set the intensity to one of four pre-programmed levels. Finally, all interface buffering is also controlled by the integrated silicon circuits. Data and control words are exchanged (either read or write) asynchronously over an 8 bit bidirectional, TTL compatible data bus. Clock selection and generator/slave options allow for complete synchronization of any number of displays, each individually addressable via the 3 bit address code and the chip enable inputs. A separate reset pin allows for immediate reset of all cascaded displays.

The complete module $1.4'' \times 0.6'' \times 0.3''$ package has

standard 20 pin DIP construction with 0.6" rows on 0.1"

centers. It is wave solderable and fully qualified to operate

Brightness (D0, D1): The state of the lower two bits of the Control Word are used to set the brightness of the entire display, from 0% to 100%. The table below shows the correspondence of these bits to the brightness.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|----|----|----|----|----|----|----|----|-----------------|
| 0 | 0 | Х | Х | X | X | 0 | 0 | Blank |
| 0 | 0 | X | Χ | X | X | 0 | 1 | 25% brightness |
| 0 | 0 | X | X | Χ | X | 1 | 0 | 50% brightness |
| 0 | 0 | X | X | X | X | 1 | 1 | Full brightness |

X = don't care

Attributes (D2-D4): Bits D2, D3, and D4 control the visual attributes (i.e., blinking) of those display digits which have been written with bit D7 set high. In order to use any of the four attributes, the Cursor Enable bit (D4 in the Control Word) must be set. When the Cursor Enable bit is set, and bit D7 in a character location is set, the character will take on one of the following display attributes.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|----|----|----|----|----|-----|----|----|--|
| 0 | 0 | 0 | 0 | X | X | В | В | Disable highlight attribute |
| 0 | 0 | 0 | 1 | 0 | 0 | В | В | Display cursor* instead of character |
| 0 | 0 | 0 | 1 | 0 | 1 | В | В | Blink single character |
| 0 | 0 | 0 | 1 | 1 | 0 | В | В | Display blinking cursor instead of character |
| 0 | 0 | 0 | 1 | 1 | 1 - | В | В | Alternate character with cursor* |

[&]quot;Cursor" refers to a condition when all dots in a single character space are lit to half brightness, character RAM contents are highlighted.

X = don't care

B = depends on the selected brightness

Attributes are non-destructive. If a character with bit D7 set is replaced by a cursor (Control Word bit D4 is set, and D3=D2=0) the character will remain in memory and can be revealed again by clearing D4 in the Control Word.

Blink (D5): The entire display can be caused to blink at a rate of approximately 2Hz by setting bit D5 in the Control Word. This blinking is independent of the state of D7 in all character locations.

In order to synchronize the blink rate in a bank of these devices, it is necessary to tie all devices' clocks and resets together as described in a later section of this data sheet.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | DO | Operation |
|----|----|----|----|----|----|----|----|------------------|
| 0 | 0 | 1 | Х | Χ | Χ | В | В | Blinking display |

Lamp Test (D6): When the Lamp Test bit is set, all dots in the entire display are lit at half brightness. When this bit is cleared, the display returns to the characters that were showing before the lamp test. A lamp test will override the clear data (D7) instruction.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|----|----|----|----|----|----|----|----|-----------|
| 0 | 1 | 0 | Χ | X | X | X | Χ | Lamp test |

Clear Data (D7): When D7 is set in the Control Word, all character and Control Word memory bits are reset to zero.

This causes total erasure of the display, and returns all digits to a non-blink, full brightness, non-cursor status. Clear data does not override an active lamp test.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation |
|----|----|----|----|----|----|----|----|-----------|
| 1 | 0 | Х | Х | Х | Х | Х | Χ | Clear |

DATA PROTOCOL

The display module continuously executes all control words programmed in the registers. Randomly, before new control words are completely defined, valid unintentional transient control words may be executed. This may present a problem if the memory clear instruction is one of the transients. To avoid the inadvertant clearing of display memory, it is suggested that display data be loaded after changes in control word programming. Alternatively, D7 must be stable in the low state throughout the complete write cycle.

CASCADING

Cascading the PD 3435 (PD 3437) is a simple operation. The requirements for cascading are: 1) decoding the correct address to determine the chip select for each additional device, 2) assuring that all devices are reset simultaneously, and 3) selecting one display as the clock source and setting all others to accept clock input (the reason for cascading the clock is to synchronize the flashing of multiple displays). One display as a source is capable of driving six other PD 3435s (PD 3437s). If more displays are required, a buffer will be necessary. The source display must have pin 3 tied low.

VOLTAGE TRANSIENT SUPPRESSION

It has become common practice to provide 0.01 μ f bypass capacitors liberally in digital systems. Like other CMOS circuitry, the Intelligent Display controller chip has very low power consumption and the usual 0.01 μ f would be adequate were it not for the LEDs. The module itself can, in some conditions, use up to 100 mA. In order to prevent power supply transients, capacitors with low inductance and high capacitance at high frequencies are required. This suggests a solid tantalum or ceramic disc for high frequency bypass. For multiple display module systems, distribute the bypass capacitors evenly, keeping capacitors as close to the power pins as possible. Use a 0.01 μ f capacitor for each display module and a 22 μ f for every third display module.

HOW TO LOAD INFORMATION INTO THE PD 3435 (PD 3437)

Information loaded into the PD 3435 can be either ASCII data or Control Word data. The following procedure (see also typical loading sequence) will demonstrate a typical loading sequence and the resulting visual display. The word STOP is used in all of the following examples.

SET BRIGHTNESS

Step 1 Set the brightness level of the entire display to your preference (example: 100%)

LOAD FOUR CHARACTERS

- Step 2 Load an "S" in the left-hand digit.
- Step 3 Load a "T" in the next digit.
- Step 4 Load an "O" in the next digit.
- Step 5 Load a "P" in the right-hand digit.

 If you loaded the information correctly, the PD 3435 should now show the word "STOP"

BLINK A SINGLE CHARACTER

- Step 6 Into the digit, second from the right, load the hex code "CF," which is the code for an "O" with the D7 bit added as a control bit.

 NOTE: the "O" is the only digit which has the control bit (D7) added to normal ASCII data.
- Step 7 Load enable blinking character into the control word register.

 The PD 3435 should now display "STOP" with a flashing "O."

ADD ANOTHER BLINKING CHARACTER Step 8 Into the left hand digit, load the hex code

- Into the left hand digit, load the hex code "D3" which is for an "S" with the D7 bit added as a control bit.
 - The PD 3435 should display "STOP" with a flashing "O" and a flashing "S."

ALTERNATE CHARACTER/ CURSOR ENABLE

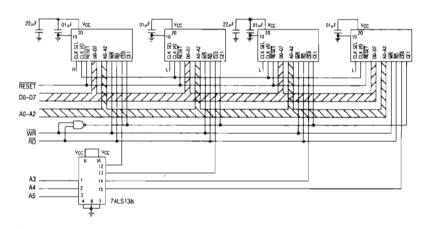
- Step 9 Load enable alternate character/cursor into the control word register.
 - The PD 3435 should now display "STOP" with the "O" and the "S" alternating between the letter and a cursor (which is all dots lit).

INITIATE FOUR-CHARACTER BLINKING

(Regardless of Control Bit setting) **Step 10** Load enable display blinking.

The PD 3435 should now display the entire word "STOP" blinking.

CASCADING THE PD 3435 (PD 3437)



TYPICAL LOADING SEQUENCE

| | E | Ĕ | 80 | Z. | 9 | = | 9 | | 9 | 5 | 4 | 23 | 2 | 2 | 8 | DISPLAY |
|-----|----|---|-----|----|---|---|---|------|---|---|---|----|---|---|---|----------|
| | 10 | _ | /22 | - | _ | _ | _ | _ | _ | | | _ | _ | _ | | |
| 1. | L | Н | Н | L | L | Х | X | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| 2. | L | Н | Н | L | Η | Н | Н | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | S |
| 3. | L | Н | Н | L | Н | Н | L | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | ST |
| 4. | L. | Н | Н | L | Н | L | Н | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | STO |
| 5. | L | Н | Н | L | Н | L | L | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | STOP |
| 6. | L | Н | Н | L | Н | L | Н | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | STOP |
| 7. | L | Н | Н | L | L | Х | Χ | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | STO*P |
| 8. | L | Н | Н | L | H | Н | Н | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | S*TO*P |
| 9. | L | Н | Н | L | L | Х | Χ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | STOTP |
| 10. | Ĺ | Н | Н | L | L | Χ | Χ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | S.1.0.b. |

^{*}Blinking Character

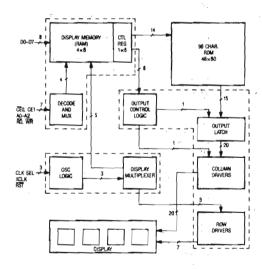
Character alternating with cursor (all dots lit)

| | DATA INPUT COMMANDS | | | | | | | | | | | | | | |
|-----|---------------------|-----|----|----|----|------|-----|----|----|----|-----|----|----|----|---|
| CEŌ | CE1 | RD. | WR | A2 | A1 | Α0 - | D7 | D6 | D5 | Q4 | DЗ | D2 | D1 | ĎΟ | OPERATION |
| 1 | 0 | х | X | x | X | Χ | х | Х | Х | Χ | X | X | X | Х | No Change |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | Χ | X | Х | Read Digit 0 Data To Bus |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 - | 0 | 0 | 1 | 0 | 0 ~ | 1 | 0 | 0 | (\$) Written To Digit 0 |
| 0 | 1 | 1 | 0 | 11 | 0 | 1 | ø | 1 | 0 | 1 | 0 | 1 | 1 | 1 | (W) Written to Digit 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | . 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | (f) Written To Digit 2 |
| 0 | 1 | 1 | 0 | -1 | 1 | 1 | 0 | 0- | 1 | 1 | 0 | 0 | 1 | 1 | (3) Written to Digit 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | Х | X | X | X | × | × | Х | Char, Written To Digit 0 And Cursor Enabled |

| | | M | ODE | SELECTION |
|-----|-----|----|-----|------------|
| CE0 | CE1 | RD | WR | OPERATION |
| 0 | 1 | 0 | 0 | Illegal |
| 1 | X | X | X | No Change, |
| Х | 0 | X | X. | No Change |
| X | Χ | 1 | 1 | No Change |

NOTE: 0 = Low Logic Level, 1 = High Logic Level, X = Don't Care.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The PD 3435 (PD 3437) block diagram includes the major blocks and internal registers.

Display Memory consists of a 5×8 bit RAM block. Each of the four 8-bit words holds the 7-bit ASCII data (bits D0–D6). The fifth 8-bit memory word is used as a control word register. A detailed description of the control register and its functions can be found under the heading Control Word, Each 8-bit word is addressable and can be read from or written to.

The **Control Logic** dictates all of the features of the display device and is discussed in the Control Word section of this data sheet.

The Character Generator converts the 7-bit ASCII data into the proper dot pattern for the 96 characters shown in the character set chart.

The Clock Source can originate either from the internal oscillator clock or from an external source—usually from the output of another PD 3435 (PD 3437) in a multiple module display.

The **Display Multiplexer** controls all display output to the digit drivers so no additional logic is required for a display system.

The Column Drivers are connected directly to the display.

The **Display** has four digits. Each of the four digits is comprised of 35 LEDs in a 5x7 dot array which makes up the alphanumeric characters.

The intensity of the display can be varied by the Control Word in steps of 0% (Blank), 25%, 50%, and full brightness.

MICROPROCESSOR INTERFACE

The interface to the microprocessor is through the address lines (A0–A2), the data bus (D0–D7), two chip select lines (\overline{CEO} , CE1), and read (\overline{RO}) and write (\overline{WR}) lines.

To derive the appropriate enable signal, the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ lines should be "NANDED" into the CE1 input. The CE0 should be held low when executing a read, or write operation.

The read and write lines are both active low. During a valid read the data input lines (D0-D7) become outputs. A valid write will enable the data as input lines.

INPUT BUFFERING

If a cable length of 18 inches or more is used, all inputs to the display should be buffered with a tri-state non-inverting buffer mounted as close to the display as conveniently possible. Recommended buffers are: 74HCT245 for the data lines and 74HCT244 or 74HC541 for the control lines.

PROGRAMMING THE PD 3435

There are five registers within the PD 3435/3437. Four of these registers are used to hold the ASCII code of the four display characters. The fifth register is the Control Word, which is used to blink, blank, clear or dim the entire display, or to change the presentation (attributes) of individual characters.

ADDRESSING

The addresses within the display device are shown below. Digit 0 is the rightmost digit of the display, while digit 3 is on the left. Although there is only one Control Word, it is duplicated at the four address locations 0–3. Data can be read from any of these locations. When one of these locations is written to, all of them will change together.

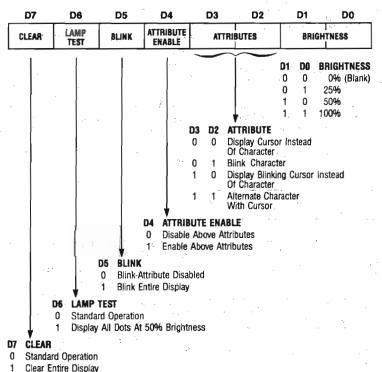
| Address | Contents | |
|---------|--------------------------|---|
| 0 | Control Word | |
| 1 | Control Word (Duplicate) | |
| 2 | Control Word (Duplicate) | |
| 3 | Control Word (Duplicate) | Ì |
| 4 | Digit 0 (rightmost) | |
| 5 | Digit 1 | |
| 6 | Digit 2 | ı |
| 7 | Digit 3 (leftmost) | |

Bit D7 of any of the display digit locations is used to allow an attribute to be assigned to that digit. The attributes are discussed in the next section. If bit D7 is set to a one, that character will be displayed using the attribute If bit D7 is cleared, the character will display normally.

CONTROL WORD

When address bit A2 is taken low, the Control Word is accessed. The same Control Word appears in all four of the lower address spaces of the display. Through the Control Word, the display can be cleared, the lamps can be tested, display brightness can be selected, and attributes can be set for any characters which have been loaded with their most significant bit (D7) set high.

CONTROL WORD FORMAT



DESCRIPTION (Continued)

from $-20\,^{\circ}\text{C}$ to $+70\,^{\circ}\text{C}$. All products are 100% burned in and 100% tested. Outgoing A.Q.L.'s are set at 0.25% for catastrophic electrical parameters and 1.0% for: mechanical and dimensional specifications, optical defects, lead solderability and package integrity, local defects on die, brightness matching LED to LED, digit to digit, and device to device. All devices are intensity binned to allow users to construct uniform displays of any length.(1)

Note: 1. Refer to the end of this data sheet or to Appnotes 18, 19, 22, and 23 for further details on handling and assembling Siemens Programmable Displays.

Maximum Ratings

| DC Supply Voltage 0.5 to | +6.0 Vdc |
|--|----------|
| Input Voltage Levels Relative | |
| to GND (all inputs) 0.5 to V _{CC} | +0.5 Vdc |
| Operating Temperature 20 °C to | o +70°C |
| Storage Temperature 20°C to | o +70°C |
| Maximum Solder Temperature .063" (1.59 mm) | |
| below Seating Plane, t < 5 sec | 260°C |
| Relative Humidity @60°C | 90% |
| | |

Optical Characteristics @ 25°C

| Optical characteristics @ 25 C | |
|--|--|
| Spectral Peak Wavelength (3435) 635 nm typ. | |
| (3437) 565 nm typ. | |
| Viewing Angle, horizontal ±55° | |
| (off normal axis) vertical ±70° | |
| Digit Size | |
| Time Averaged Luminous Intensity(1) | |
| (100% brightness, 5 Vdc=V _{CC}) 250 μcd/LED typ. | |
| HER75 μcd/LED min. | |
| Green | |
| LED to LED Intensity Matching 1.8:1.0 max. | |

Bin to Bin (adjacent bins) 1.9:1.0 max.

Note: 1. Peak luminous intensity values can be calculated by multiplying these values by 7.

Device to Device (one bin) 1.5:1.0 max.

SWITCHING SPECIFICATIONS

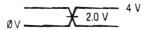
(@25°C and V_{CC} = 4.5 V)(1)

| | READ CYCLE TIMING | |
|-----------|--|----------|
| Parameter | Spec. (ns) Minimum | |
| TAD | Address set up delay after CE | 0 |
| TACC | Access time for data valid after address | 175 |
| TDD | Delay time for data valid after read pulse | 150 max. |
| TRC | Total read cycle time | 200 |
| TDH | Data valid after end of read pulse | 0 |
| TRD | Read pulse | 175 |

| WRITE CYCLE TIMING | | | | | | | | | | |
|--------------------|---|-----------------------|--|--|--|--|--|--|--|--|
| Parameter | Description | Spec. (ns) Minimum | | | | | | | | |
| TWD | Delay time for write pulse after control signals and data | 50 | | | | | | | | |
| TDH | Data hold after write pulse | 50 | | | | | | | | |
| TWC | Total write cycle time | 200 | | | | | | | | |
| TWR | Write pulse width | 100 | | | | | | | | |

Note: 1 Timing characteristics are guaranteed values at the worst case condition of V_{CC} = 4.5 Vdc. Characterization data indicates these values also hold over temperature from −20°C to +70°C except for TAD and TDH. These two read cycle timing minimums may extend to 5ns at +70°C.

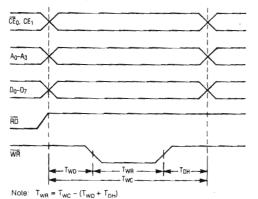
TIMING MEASUREMENT LEVELS



TIMING CHARACTERISTICS AT 25°C

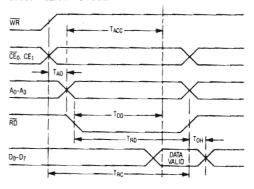
 $V_{CC} = 4.5V$

DATA "WRITE" CYCLE



 $T_{RD} = T_{RC} - T_{AD} - (T_{ACC} - T_{DD})$

DATA "READ" CYCLE



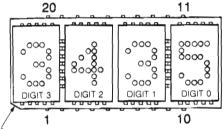
DC CHARACTERISTICS (@25°C)

| | | Limits | | | | | |
|---|------|--------|--------|-------|---|--|--|
| Parameters | Min. | Typ. | Max. | Units | Conditions | | |
| Vcc | 4.5 | 5.0 | 5.5 | Volts | Nominal | | |
| I _{CC} Blank (All Inputs Low) | | 2.5 | 5.0 | mA | V _{CC} = 5 V, V _{IN} = .8 V, WR = 5 V | | |
| I _{CC} Lamp Test (1/2 Brightness) | | 62 | | mA | V _{CC} = 5 V | | |
| I _{CC} 80 LEDs/unit (100% Bright) | 100 | 150(1) | 200(2) | mA | V _{CC} = 5 V | | |
| V _{IL} (All Inputs) | -0.5 | | 0.8 | Volts | V _{CC} = 4.5 V to 5.5 V | | |
| V _{IH} (All Inputs) | 2.0 | | 5.5 | Volts | V _{CC} = 4.5 V to 5.5 V | | |
| Iii (Ali Inputs) | | | 200 | μA | V _{CC} = 5 V, V _{IN} = 0.8 V | | |

Notes: 1. Typical average LED drive current is 1.9 mA. Peak current at 1/7 multiplex rate is 13 mA.

2. Characterization data indicates max I_{CC} will vary from 230 mA at -20°C to 170 mA at 70°C.

TOP VIEW



Pin 1 indicator, painted beveled corner.

PIN ASSIGNMENTS

| PD 3435, PD 3437 PINOUT | | | | | | | | | | | | |
|-------------------------|---------|--------------|-----|----------|----------|--|--|--|--|--|--|--|
| Pin | | Function | Pin | | Function | | | | | | | |
| 3 | RD | READ | 11 | WR | WRITE | | | | | | | |
| 2 | CLK I/O | CLOCK I/O | 12 | D7 | DATA MSB | | | | | | | |
| 3 | CLKSEL | CLOCK SELECT | 13 | D6 | DATA | | | | | | | |
| 4 | AST | RESET | 14 | D5 | DATA | | | | | | | |
| 5 | CE1 | CHIP ENABLE | 15 | D4 | DATA | | | | | | | |
| 6 | CE0 | CHIP ENABLE | 16 | D3 | DATA | | | | | | | |
| 7 | A2 | ADDRESS MSB | 17 | D2 | DATA | | | | | | | |
| 8 | A1 | ADDRESS | 18 | D1 | DATA | | | | | | | |
| 9 | A0 | ADDRESS LSB | 19 | D0 | DATA LSB | | | | | | | |
| 10 | GND | | 20 | V_{CC} | | | | | | | | |

PIN DEFINITIONS

| Pin | | |
|----------------------|-----------------------------------|---|
| 1. RD | | ve low, will enable a processor to read egisters in the PD 3435 (PD 3437). |
| 2. CLF | (I/O If Cl exte SEL mas | LK SEL (pin 3) is low, then expect an irnal clock source into this pin. If CLK is high, then this pin will be the iter or source for all other devices th have CLK SEL low. |
| 3. CLF | pin : | cK SELect, determines the action of 2. CLK I/O, see the section on cading for an example. |
| 4. RS | T Rese volts blink | et. Must be held low until V _{CC} > 4.5 s. Reset is used only to synchronize king and will not clear the display mory. |
| 5. CE1 | | o enable (active high). |
| 6. ČE(| | o enable (active low). |
| 7. A2 8. A1 | | lress input (MSB). Iress input. |
| 9. AO | | Iress input (LSB). |
| 10. Gn | | und. |
| 11. WF | sele the | e. Active Low. If the device is cted, a low on the write input loads data into the PD 3435s (PD 3437s) nory. |
| 12. D7 | | a Bus bit 7 (MSB). |
| 13. D6 14. D5 | | a Bus bit 6. a Bus bit 5 |
| 15. D4 | | a Bus bit 4. |
| 16. D3 | | Bus bit 3. |
| 17. D2 | | a Bus bit 2. |
| 18. D1 | | a Bus bit 1. |
| 19. DO | | a Bus bit 0 (LSB). |
| 20. V _C (| ; Plus | 5 volts power pin. |
| | | |

CHARACTER SET

| | | | DØ | L | н | L | н | L | Н. | L | н | L | Н | L | Н | L | Н | L | Н |
|----|----|----|-----|------|---------------------------|-------|------|------|------|---------------|-----|------|--------|-------|-------------|----|-------|------|---|
| | | | D1 | L | L | Н | Н | L | L | Н | Н | L | L | Н | Н | L. | L | Н | Н |
| | | | D2 | L | L | L | L | Н | Н | Н | Н | L | L | L | L | H | Н | Н | Н |
| | | | D3 | L | L | L | L | L | L | L | L | Н | Н | Н | Н | Н | Н | Н | Н |
| D6 | D5 | D4 | HEX | Ø | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | Α | В | С | D | E | F |
| L | L | L | ø | | | | | | THE | e cc | nee | nien | 1 AV E | I ANE | , | | | | |
| L | L | н | 1 | | THESE CODES DISPLAY BLANK | | | | | | | | | | | | | | |
| L | н | L | 2 | | | ii | # | # | | | | 1 | | # | | # | •••• | 11 | |
| L | н | н | 3 | | 1 | | | :4 | | <u></u> . | 1. | :::: | | :: | :: | : | ***** | ÷ | • |
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Notes: 1. A2 must be held high for ASCII data.

Bit D7 = 1 enables attributes for the assigned digit.

 A cursor is defined as all dots/digit lit. When an ASCII character is in memory, an enabled cursor will "highlight" that character with slightly brighter LEDs.

ELECTRICAL AND MECHANICAL CONSIDERATIONS

The CMOS IC of the PD 3435 and PD 3437 is designed to provide resistance to both Electrostatic Discharge Damage and Latch Up due to voltage or current surges. Several precautions are strongly recommended to avoid overstressing these built-in safeguards.

ESD PROTECTION

Users of the PD 3435 and PD 3437 should be careful to handle the devices consistent with standard ESD protection procedures. Operators should wear appropriate wrist, ankle or feet ground straps and avoid clothing that collects static charges. Work surfaces, tools and transport carriers that come into contract with unshielded devices or assemblies should also be appropriately grounded.

LATCH UP PROTECTION

Latch up is a condition that occurs in CMOS IC's after the input protection diodes have been broken down. These diodes can be reversed through several means:

 $\rm V_{IN} < \rm GND, \, V_{IN} > \rm V_{CC} + 0.5 \, V$, or through excessive currents beign forced on the inputs. When these situations exist, the IC may develop the response of an SCR and begin conducting as much as 1 amp through the $\rm V_{CC}$ pin. This destructive condition will persist (latched) until device failure or the device is turned off.

The Voltage Transient Suppression Techniques and buffer interfaces for longer cable runs help considerably to prevent latch conditions from occuring. Additionally, the following Power Up and Power Down sequence should be observed.

POWER UP SEQUENCE

- Float all active signals by tri-stating the inputs to the displays.
- 2. Apply V_{CC} and Gnd to the display.
- Apply active signals to the displays by enabling all input signals per application.

POWER DOWN SEQUENCE

- Float all active signals by tri-stating the inputs to the display.
- 2. Turn off the power to the display.

SOLDERING CONSIDERATIONS

PD 3435's and PD 3437's can be hand soldered with SN63 solder using a grounded iron set to 260 °C.

Wave soldering is also possible following these conditions: Preheat that does not exceed 93 °C on the solder side of the PC board or a package surface temperative of 70 °C. Water soluble organic acid flux or rosin-based RMA flux are preferred; however, virtually any system that does not contain methalenechloride or cyclopentane (such a TCM) can be used.

Wave temperature of 245 °C ±5 °C with a dwell between 1.5 sec. to 3.0 sec. Wave temperature should not exceed 260 °C, at 0.063" below the seating plane. If temperature is this high, exposure should not exceed 5 seconds. The packages should not be immersed in the wave.

POST SOLDER CLEANING PROCEDURES

The least offensive cleaning solution is hot D.I. water (60°C) for less than 15 minutes. Addition of mild saponifiers is acceptable. Do not use commercial dishwasher detergents.

Solvents, for faster cleaning, may be used. Care should be exercised in choosing these as some may chemically attack the MG-18, or ceramic package. Maximum exposure should not exceed two minutes at elevated temperatures. Acceptable solvents are TF (trichlorotrifluoroethane), TA, 111 Trichloroethane, and unheated acetone, alcohoi, methanol, ethanol, TP35, TMC, TMS+, TE, or TES.

Unacceptable solvents contain methalenechloride or cyclopentane such as TCM. Since many commercial mixtures exist, you should contact your preferred solvent vendor for chemical composition information. Some major solvent manufacturers are: Allied Chemical Corporation, Specialty Chemical Division, Morristown, NJ; Baron-Blakeslee, Chicago, IL; Dow Chemical, Midland, MI; E.I. DuPont de Nemours & Co., Wilmington, DE.

Further information is available in Siemens Appnotes 18 and 19 (see current Optoelectronic Data Book).

An alternative to soldering and cleaning the display modules is to use sockets. Naturally, 20 pin DIP sockets. 600" wide with .100" centers work well for single displays. Multiple display assemblies are best handled by longer SIP sockets or DIP sockets when available for uniform package alignment. Socket manufacturers are Aries Electronics, Inc., Frenchtöwn, NJ; Garry Manufacturing, New Brunswick, NJ; Robinson-Nugent, New Albany, IN; and Samtec Electronic Hardware, New Albany, IN.

Further information is available in Siemens Appnote 22.

OPTICAL CONSIDERATIONS

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The .270"high character of the PD 3435 and PD 3437 allow readability up to 12 feet. Proper filter selection will allow the user to build a display that can be utilized over this distance.

Filters allow the user to enhance the contrast ratio between a fit LED and the character background. This will maximize discrimination of different characters as perceived by the display user. The only limitation is cost. The cost/benefit ratio for filters can be maximized by first considering the ambient lighting environment.

Incandescent (with almost no green) or fluorescent (with almost no red) lights do not have the flat spectral response of sunlight. Plastic band-pass filters are inexpensive and effective in optimizing contrast ratios. The PD 3435 is a high efficiency red display and should be matched with a long wavelength pass filter in the 570 nm to 590 nm range. The PD 3437 should be matched with a yellow-green band-pass filter that peaks at 565 nm. For displays of multiple colors, neutral density grey filters offer the best compromise.

Additional contrast enhancement can be gained through shading the displays. Plastic band-pass filters with built-in louvers offer the "next step up" in contrast improvement. Finally, plastic filters can be further improved with anti-reflective coatings to reduce glare. The trade-off is "fuzzy" characters, but mounting the filters close to the display reduces this effect. Care should be taken not to overheat the plastic filters by allowing for proper air flow.

Finally, optimal filter enhancements for any condition can be gained through the use of circular polarized, anti-reflective, band-pass filters. Circular polarizing further enhances contrast by reducing the light that travels through the filter and reflects back off the display to less than 1%. Proper intensity selection of the displays will allow 10,000 foot candle sunlight viewability.

Several filter manufacturers supply quality filter materials. Some of them are: Panelgraphic Corporation, W. Caldwell, NJ; SGL Homelite, Wilminington, DE; 3M Company, Visual Products Division, St. Paul, MN; Polaroid Corporation, Polarizer Division, Cambridge, MA; Marks Polarized Corporation, Deer Park, NY; Hoya Optics, Inc., Fremont, CA.

One final note on mounting filters. Recessing display and bezel assemblies is an inexpensive way to provide a shading effect in overhead lighting situations. Several Bezel manufacturers are: R.M.F. Products, Batavia, IL; Nobex Components, Griffith Plastic Corp., Burlingame, CA; Photo Chemical Products of California, Santa Monica, CA; I.E.E. Atlas, Van Nuys, CA.

Please refer to Siemens Appnote 23 for further information.