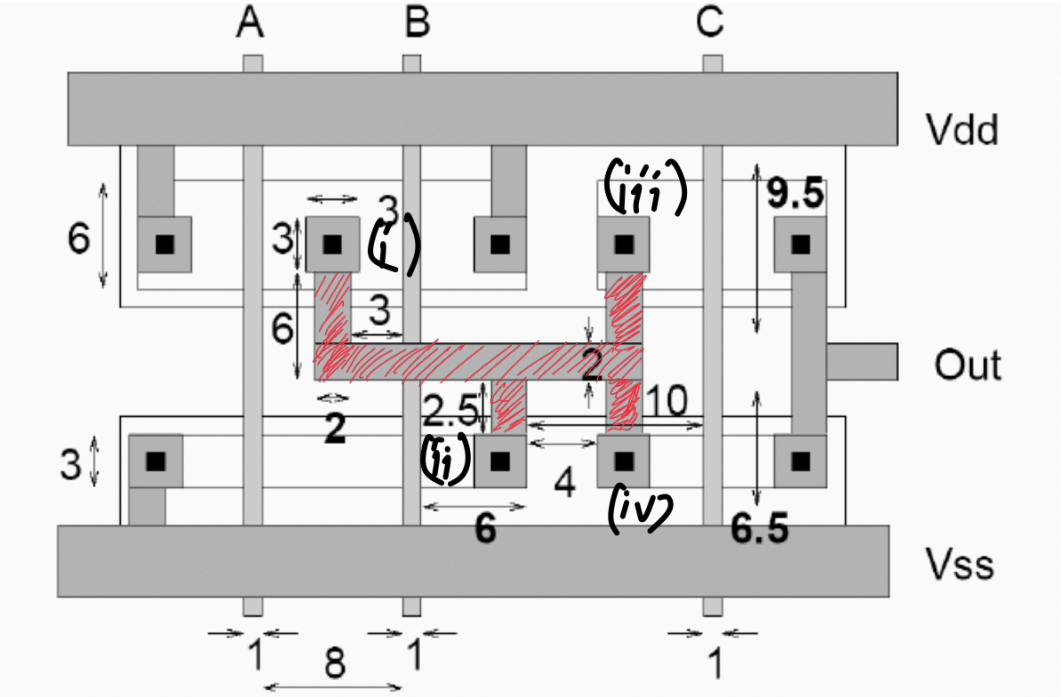
HW Question 1

Estimate the total capacitance at the output of the NAND gate in the following layout. All dimensions are in microns and drawn to scale. Assume that Cja = 0.5 fF/um2 and Cjp = 0.45fF/um for both n and p transistors. Consider only the parallel plate capacitance component of the interconnect capacitance and use the interconnect capacitance values given in the previous slide.



Solution:-

The output of the NAND gate is affected by the junctions at i, ii, iii and iv.

So, total capacitance = Capacitance$_{jn}$(i) + Capacitance$_{jn}$(ii) + Capacitance$_{jn}$(iii) + Capacitance$_{jn}$(iv) + Interconnect capacitance

jn = junction

(i) capacitance in $C(i) = C_{ja}(W_p \times Y_p) + C_{jp}(2Y_p)$

Since A_{PMOS} and B_{PMOS} have same drain.

At junction (i), $W_p = 6$, $Y_p = 8$

$\therefore C(i) = (0.5)(48) + (0.45)(16)$

$C(i) = 31.2\ fF$ → (A)

Similarly for Capacitance in $C(ii)$, $W_n = 3$, $Y_n = 6$

Using $C_{ja}(WY) + C_{jp}(2Y + W)$

$C(ii) = (0.5)(18) + (0.45)(15)$

$C(ii) = 15.75\ fF$ → (B)

For $C(iii)$, $W_p = 6$ & $Y_p = 6$

$C(iii) = (0.5)(36) + (0.45)(18)$

$C(iii) = 26.1\ fF$ → (C)

. My for c(iv), $W_{pn} = 3$ & $Y_n = 6$

$$C(iv) = (0.5)(18) + (0.45)(15)$$

$$\boxed{C(iv) = 15.75\,fF} \longrightarrow (D)$$

we need to calculate interconnect capacitance for the shaded region (red) in the diagram.

Given, metal 1 over field oxide = $0.03\,fF/\mu m^2$

metal 1 over poly = $0.053\,fF/\mu m^2$

$\therefore$ C(interconnect) = (12)(0.030) + (6)(0.030) + (21)(0.030) + (12)(0.030) + (5)(0.030) + (5)(0.030) + (0.053)(2)

$$= 0.36 + 0.18 + 0.63 + 0.36 + 0.15 + 0.15 + 0.106$$

$$\boxed{C(\text{interconnect}) = 1.876\,fF} \longrightarrow (E)$$

Output capacitance = A + B + C + D + E

= 31.2 + 15.75 + 26.1 + 15.75

+ 1.876.

Output capacitance = 90.676 fF