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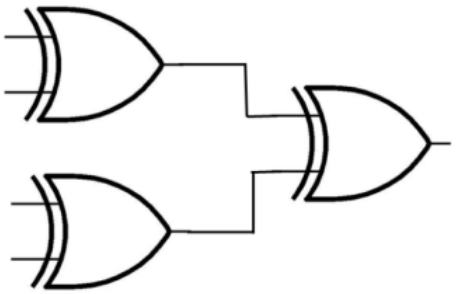
CAD Assignment 2

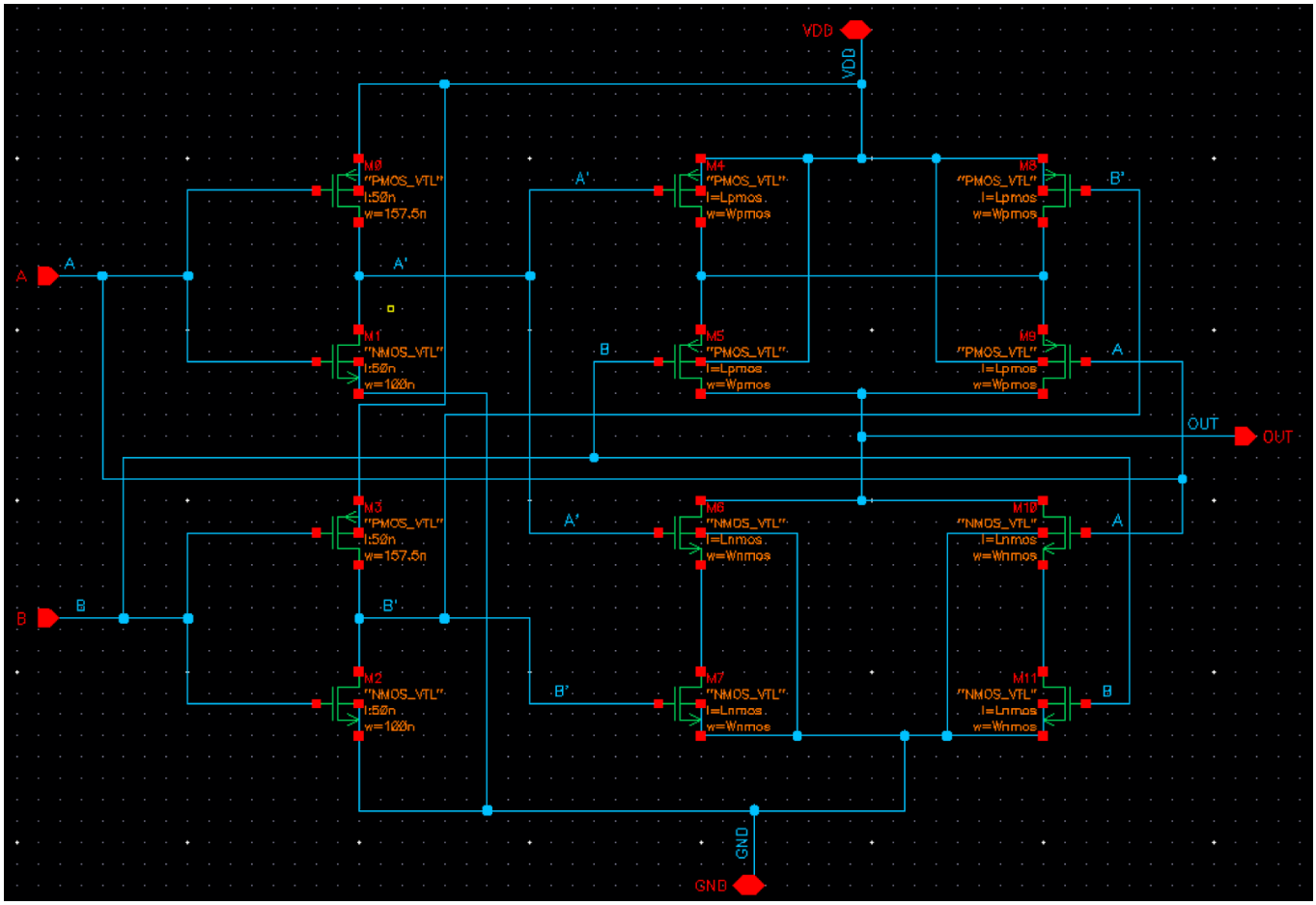
Objective: Design and verify a four-input parity generator consisting of three XOR gates in the 45 nm CMOS technology.



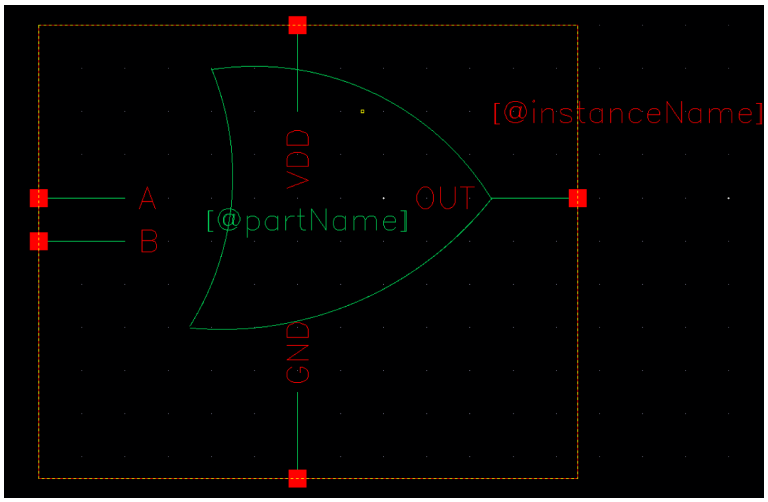
The nominal supply voltage is set to 1.1 Volts. The circuit should drive an external load of 12 fF in addition to the internal parasitic capacitances that exist in the circuit. Assume 50 ps of rise/fall times for your input signals.

Design constraints: The primary design objective is to minimize the power-delay product of the circuit for the input pattern provided below. Delay should correspond to the worst-case delay between input and output. Power should correspond to the average power consumption over 7 ns for the input pattern below. In the worst case, the circuit should have a propagation delay of no more than 200 ps.

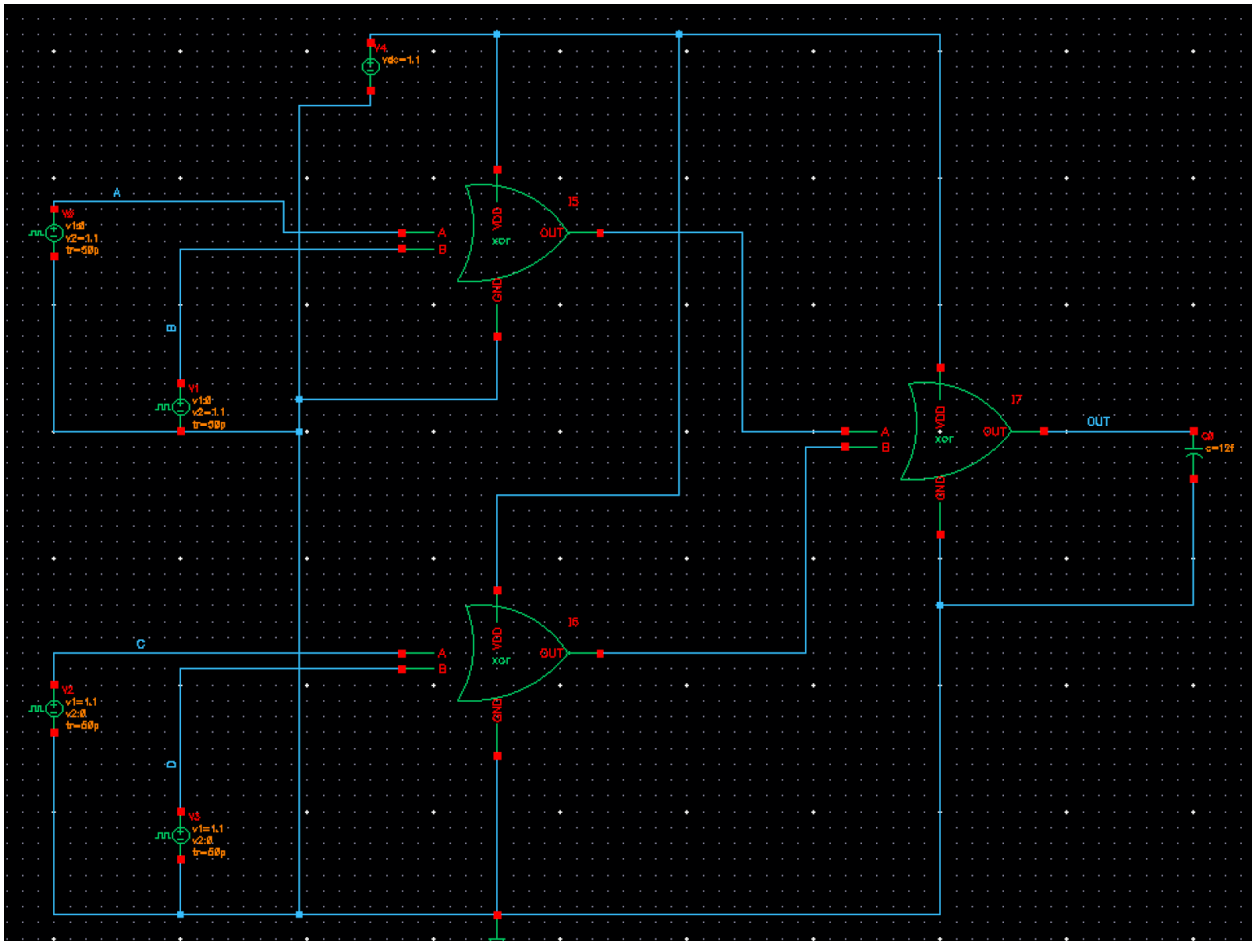
Schematic of XOR gate



Symbol of XOR gate



Schematic view of parity generator



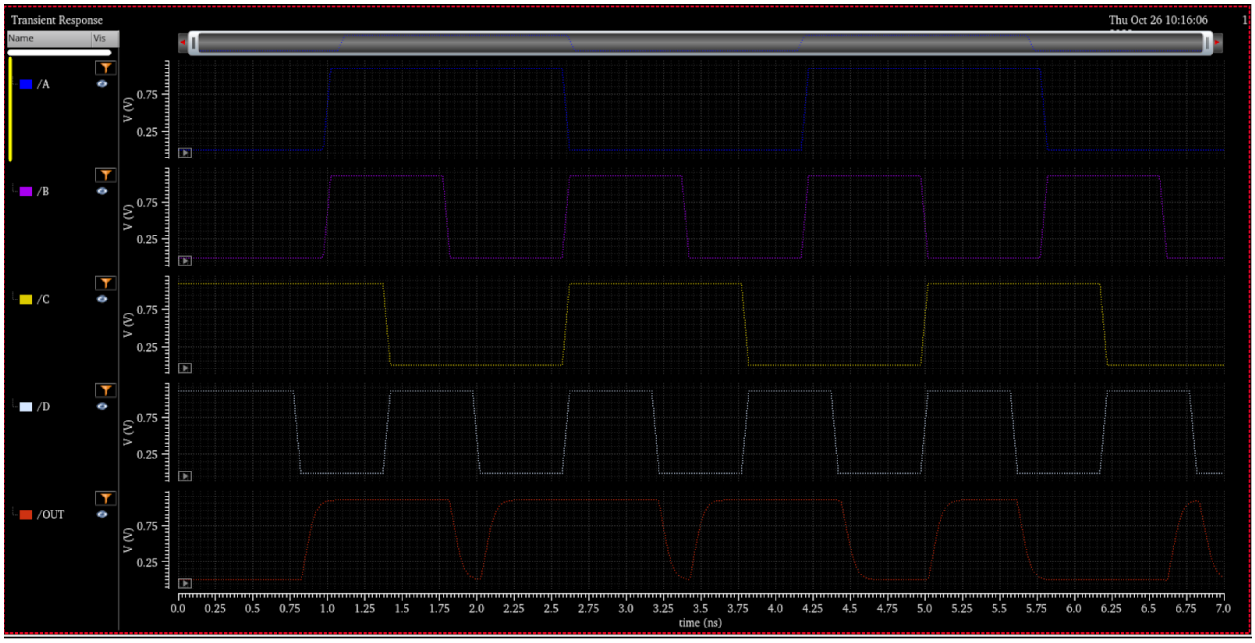
	Wnmos	(delay(?w...e nil))/2	(average(...)) * 1.1)
1	100.0E-9	116.8E-12	-17.37E-6
2	116.7E-9	106.9E-12	-18.22E-6
3	133.3E-9	98.18E-12	-18.93E-6
4	150.0E-9	90.63E-12	-19.55E-6
5	166.7E-9	84.21E-12	-20.12E-6
6	183.3E-9	78.79E-12	-20.67E-6
7	200.0E-9	74.41E-12	-21.26E-6
8	216.7E-9	70.70E-12	-21.87E-6
9	233.3E-9	67.56E-12	-22.48E-6
10	250.0E-9	64.84E-12	-23.08E-6

The goal in designing a 4-bit parity generator is to minimize the power-delay product. This involves a tradeoff between reducing power consumption by decreasing parasitic capacitance and minimizing average propagation delay by increasing the W/L ratio of ON transistors. Transistor resizing is done by sweeping the NMOS width(Wnmos) from 100 nm to 250 nm while keeping the PMOS width (Wpmos) at 1.6 times of Wnmos and both transistor lengths are fixed at 50nm.

We're getting the minimum power-delay when Wnmos = 200 nm, therefore, Wpmos = 1.6 * 200 = 320 nm

Wnmos = 200 nm
Wpmos = 320 nm

Transient analysis waveform:

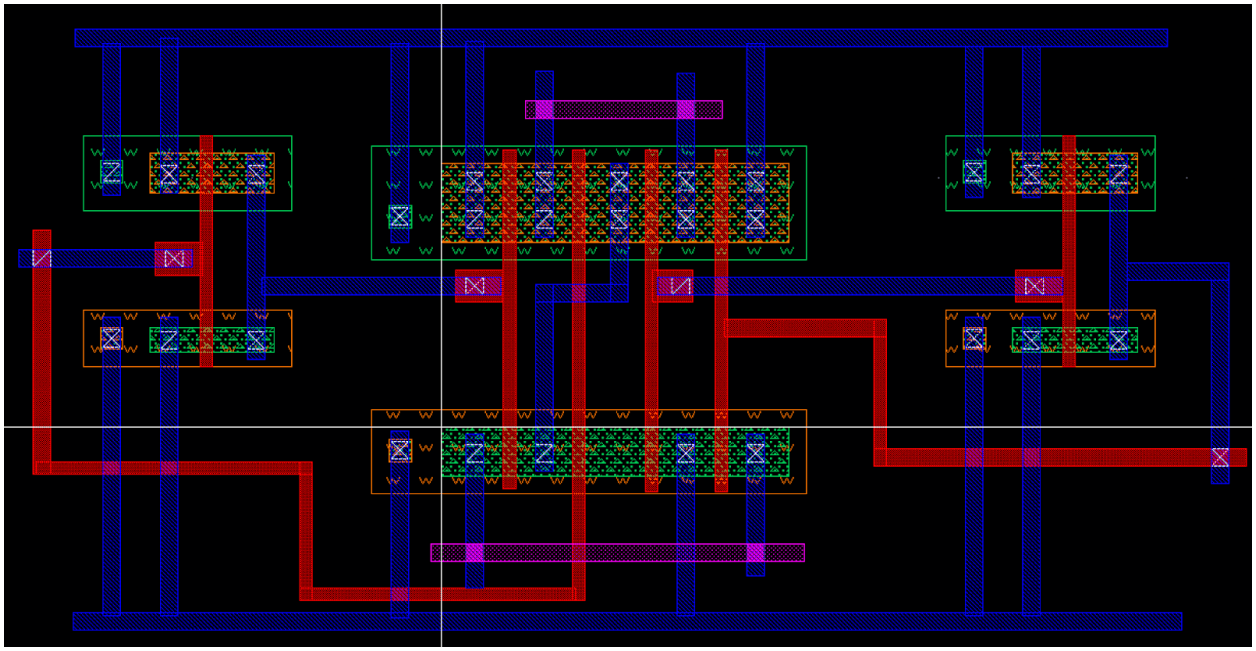


Outputs

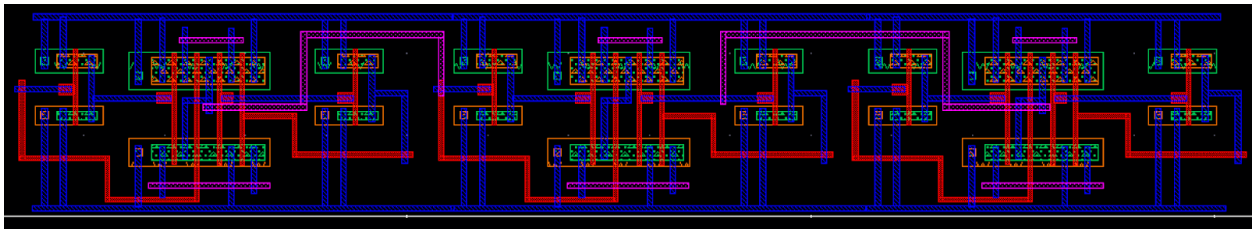
	Name/Signal/Expr	Value	Plot	Save	Save Options
1	A		☑	☐	allv
2	B		☑	☐	allv
3	C		☑	☐	allv
4	D		☑	☐	allv
5	OUT		☑	☐	allv
6	V4/PLUS		☑	☑	yes
7	Low to High	79.4p	☑	☐	
8	High to Low	69.42p	☑	☐	
9	Average Propagation Delay	74.41p	☑	☐	
10	Dynamic Power	-21.26u	☑	☐	

Average Propagation delay: **74.41 ps**

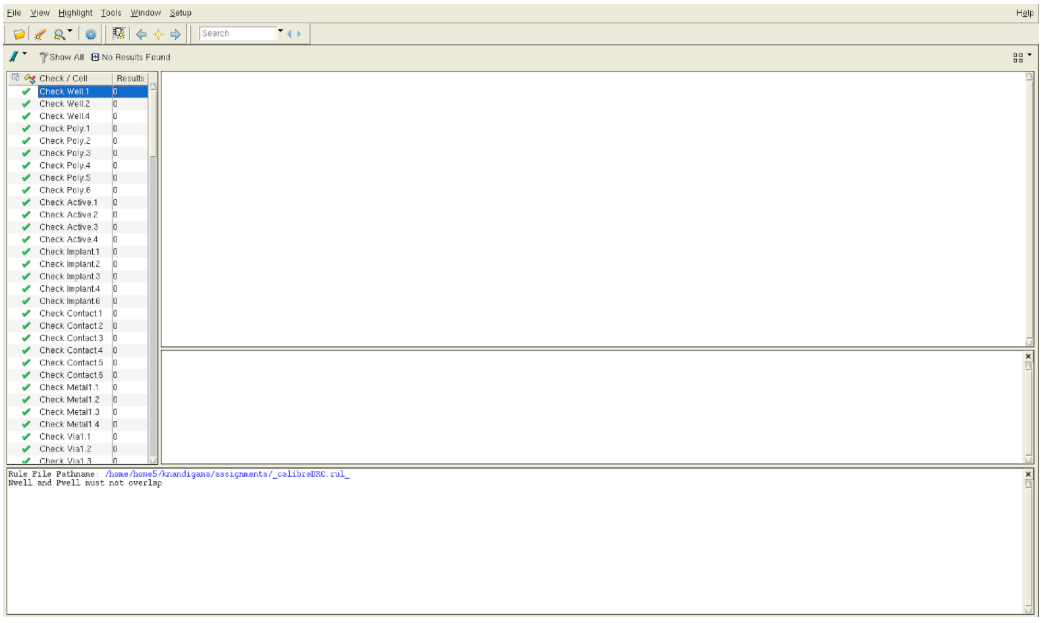
XOR Layout



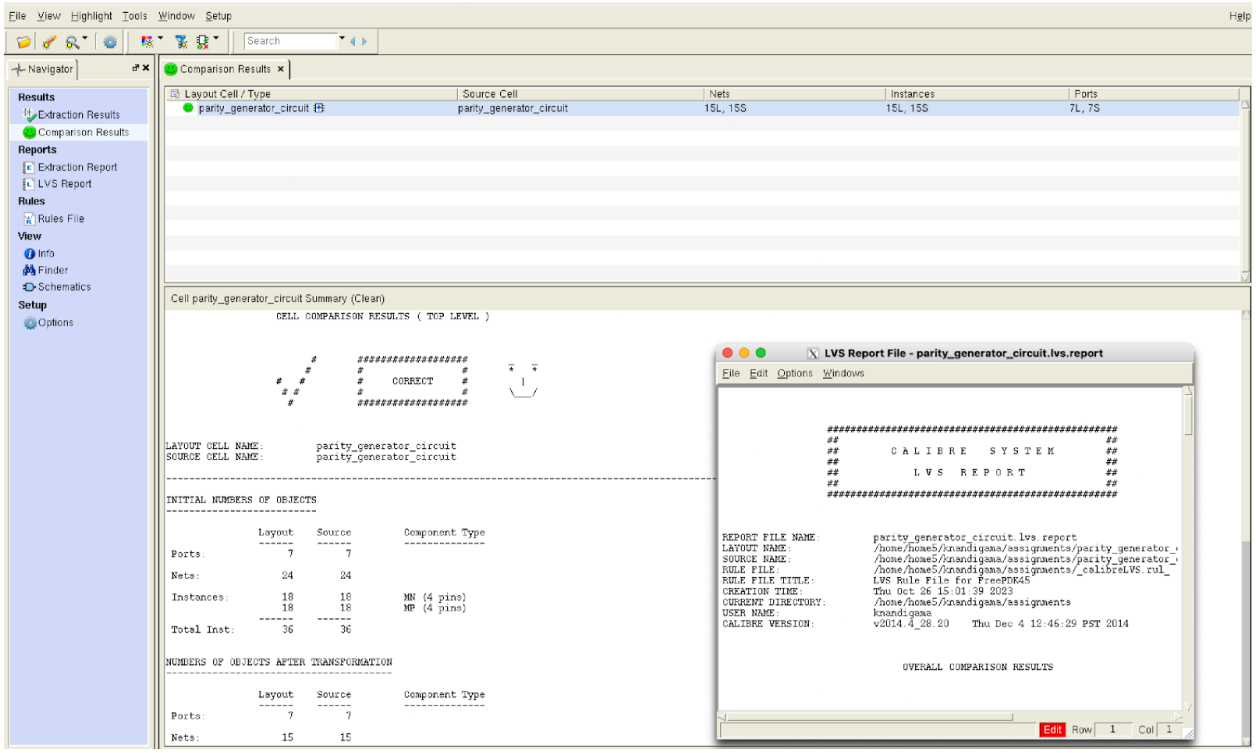
Parity Generator Layout



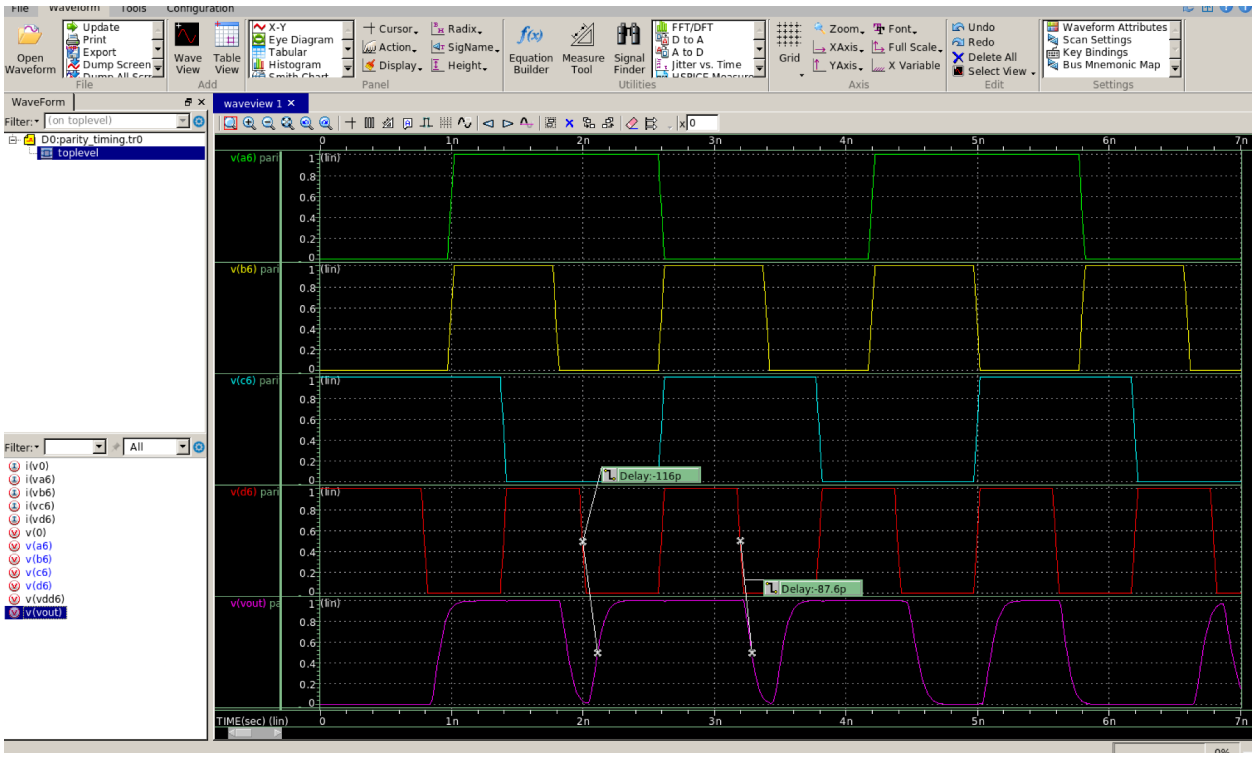
Parity Generator DRC



Parity Generator LVS

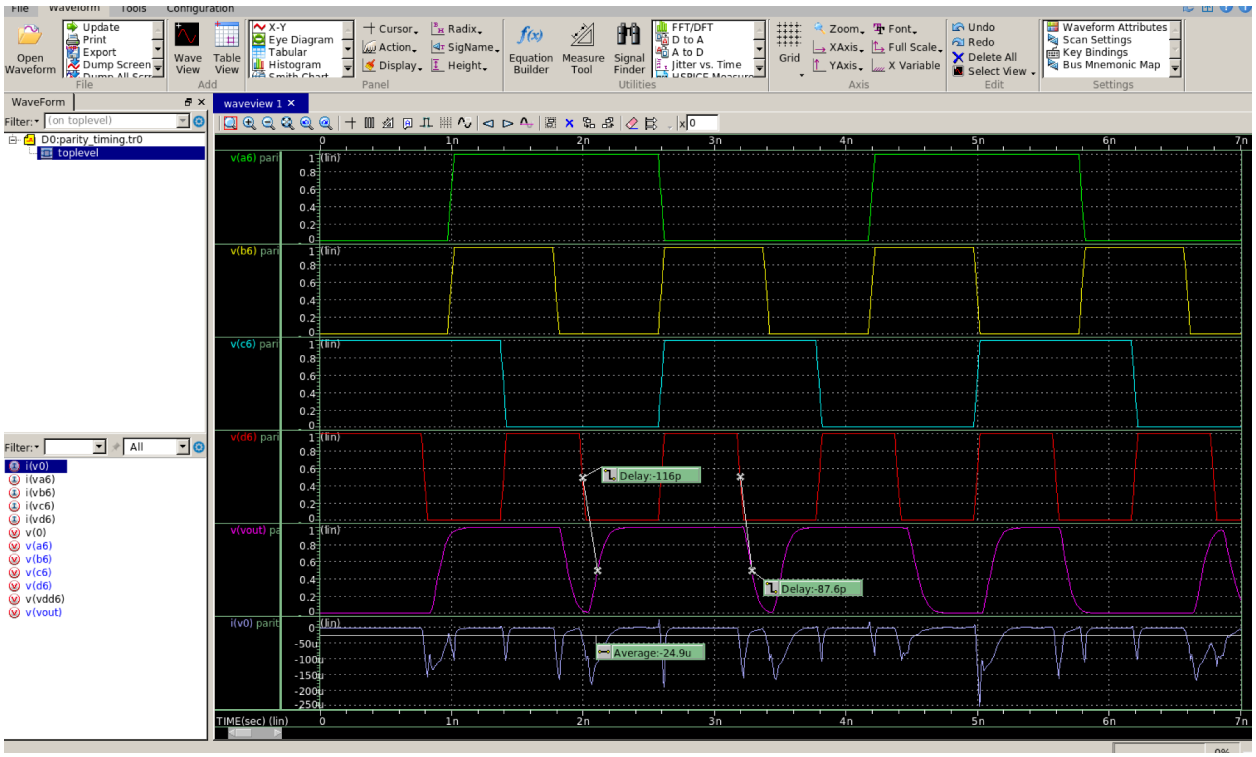


Post-layout simulation data



After observation, the worst case scenario is marked between the 4th input and the output.
Propagation delay for low to high: 116 ps
Propagation delay for high to low: 87.6 ps

Average propagation delay: **101.8 ps** (less than the given constraint, 200 ps)



Average current is plotted on the graph which is **24.9 uA.**
Dynamic power = Vdd * average current = 1.1 * 24.9 = **27.39 micro watts.**
Power delay product = dynamic power * average propagation delay
= 27.39 micro * 101.8 pico = **2.7883 femto watt sec**