ESE 555 CAD ASSIGNMENT 1
Due September 28, 11:59 pm

Should be submitted via Brightspace Only

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Assume a CMOS inverter designed in a 45 nm technology with the following transistor sizes.

a. (W/L)n = 100 nm / 50 nm
b. (W/L)p = 200 nm / 50 nm

1. Assuming that this inverter drives a capacitive load of 2 fF (C_{load} = 2 fF), calculate the low-to-high and high-to-low propagation delays using the following parameters. Note that the nominal power supply voltage for this technology is 1 Volt. Assume that the input is a step function.

   a. $(V_{th})n$ = 0.4106 Volts
   b. $(V_{th})p$ = -0.3842 Volts
   c. μ_n = 270 cm^2 / (V-s)
   d. μ_p = 70 cm^2 / (V-s)
   e. $\varepsilon_{ox} = 3.97 \times \varepsilon_0$
   f. $\varepsilon_0 = 8.85 \times 10^{-12}$ (F/m)
   g. $T_{ox,\ nmos} = 1.14 \times 10^{-9}$ (m)
   h. $T_{ox,\ pmos} = 1.26 \times 10^{-9}$ (m)

2. Start Cadence and open a new schematic window named "inverter" under the main library. Design this inverter using Cadence schematic view. Generate a symbol. Next, start another schematic window named "inverter_test" under the same library to simulate (transient analysis) the inverter. Provide a pulse waveform as the input with a period of 2 nm and 50% duty cycle. Verify correct functionality. Next, simulate (perform transient analysis for 5 clock cycles, equal to 10 ns) the schematic netlist and determine both the low-to-high and high-to-low propagation delays for the following two cases:

   a. Rise/fall times of the input signal is 1 ps (practically step input)
   b. Rise/fall times of the input signal is 200 ps
   c. Compare the simulation results with the calculation results in Step 1 (Discuss the differences)

3. Obtain the DC transfer characteristic of the inverter by performing a DC analysis in Spectre. In DC analysis, a large signal at the input node will be swept from VSS to VDD and output will be analyzed for each input value. From the DC characteristics, determine if the inverter operation is symmetric. If not, resize the transistors to ensure that the DC transfer curve is symmetric (e.g., Vin=Vout line intersects the transfer function curve at half VDD). Re-perform the transient analysis to determine both low-to-high and high-to-low propagation delays again.

   In the remaining parts, set the rise/fall time to 200 ps (except step 7).

4. After adjusting the sizes in the previous step, sweep the load capacitance from 0.5 fF to 5 fF in steps of 0.5 fF. Perform transient analysis to determine low-to-high and high-to-low propagation delays. Plot average propagation delay ({low-to-high+high-to-low}/2) versus output load capacitance.

5. Keep the output load constant at 2 fF. Also keep the Wp/Wn ratio you found in Step 3 constant. Sweep Wn until 1.5 um (with step size of 200 nm) while keeping Wp/Wn ratio constant, so for each Wn, Wp also changes. Perform transient analysis to determine low-to-high and high-to-low propagation delays. Plot average propagation delay ({low-to-high+high-to-low}/2) versus Wn.

6. Change Wp and Wn back to the values determined in Step 3. Draw a physical layout of the final inverter using Cadence Virtuoso. Successfully pass DRC and LVS.

7. Extract the layout and simulate (perform transient analysis for 5 clock cycles) in HSPICE the extracted netlist to verify functionality. Also simulate both the low-to-high and high-to-low propagation delays for the following two cases:

   a. Rise/fall times of the input signal is 1 ps (practically step input)
   b. Rise/fall times of the input signal is 200 ps
   c. Compare the simulation results (transient analysis) of the extracted netlist with that of the schematic netlist

REPORT: Your report should answer each question above. For each step except Step 1, you should include screen snapshots showing your schematic design, input/output transient simulation results with the marked delay values, DC transfer curve, layout, successful DRC and LVS results, and post layout simulation data.

Calculation required in Step 1 should be readable.