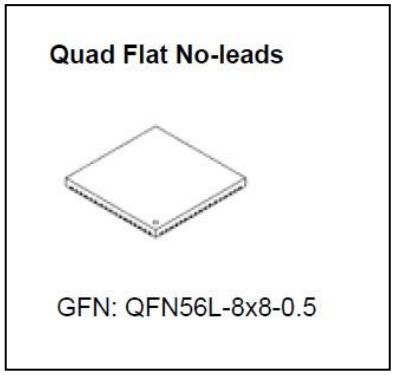
48-Channel PWM Constant Current LED Driver for 1:32 Time-Multiplexing Applications

Features



- 3V-5.5V supply voltage
- 48 constant current output channels
- Constant output current range:
  - 0.5~20mA @ 5V supply voltage
  - 0.5~10mA @ 3.3V supply voltage
- Excellent output current accuracy:
  Between channels:：<±2.5%(Max.)
  Between ICs: <±3%(Max.)
- Built-in 48K-bit SRAM to support time-multiplexing for 1 ~ 32 scans
- Flexible PWM control to improve visual refresh rate,
  -16/15/14/13 bit grayscale mode with programmable scrambling
- Global current gain control:
  - Gain range: 100%~200%, step increment: 14.3%
- 128 steps R/G/B/ individual current gain control
- Integrating ghost elimination circuit
- Premium low grayscale improvement technique
- LED failure isolation
  - LED failure induced cross elimination
- LED status monitoring:
  - LED open detection with programmable threshold levels
  - LED short detection with programmable threshold levels
- Smart power saving mode
- DCLK double edge (rising & falling edge) triggered to improve data transmit capacity
- GCLK multiplier technology
- Maximum DCLK frequency: 30MHz @VDD=5V
- Package MSL Level : 3

Product Description

MBI5353 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 16 /15 /14 / 13-bit color depth. MBI5353 features a 48-bit shift register which converts serial input data into each pixel's gray scale of the output port. The forty-eight regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of V_F variations. The output current can be preset through an external resistor. The innovative architecture with embedded SRAM is designed to support up to 1:32 time-multiplexing applications. Users only need to send the whole frame data once and to store in the embedded SRAM of the LED driver, instead of sending every time when the scan line is changed. It helps to save the data bandwidth and to achieve high grayscale with very low data clock rate. With scan-type Scrambled-PWM (S-PWM) technology, MBI5353 enhances PWM by scrambling the "on" time of each scan line into several "on" periods and sequentially drives each scan line for a short "on" period. The enhancement equivalently increases the visual refresh

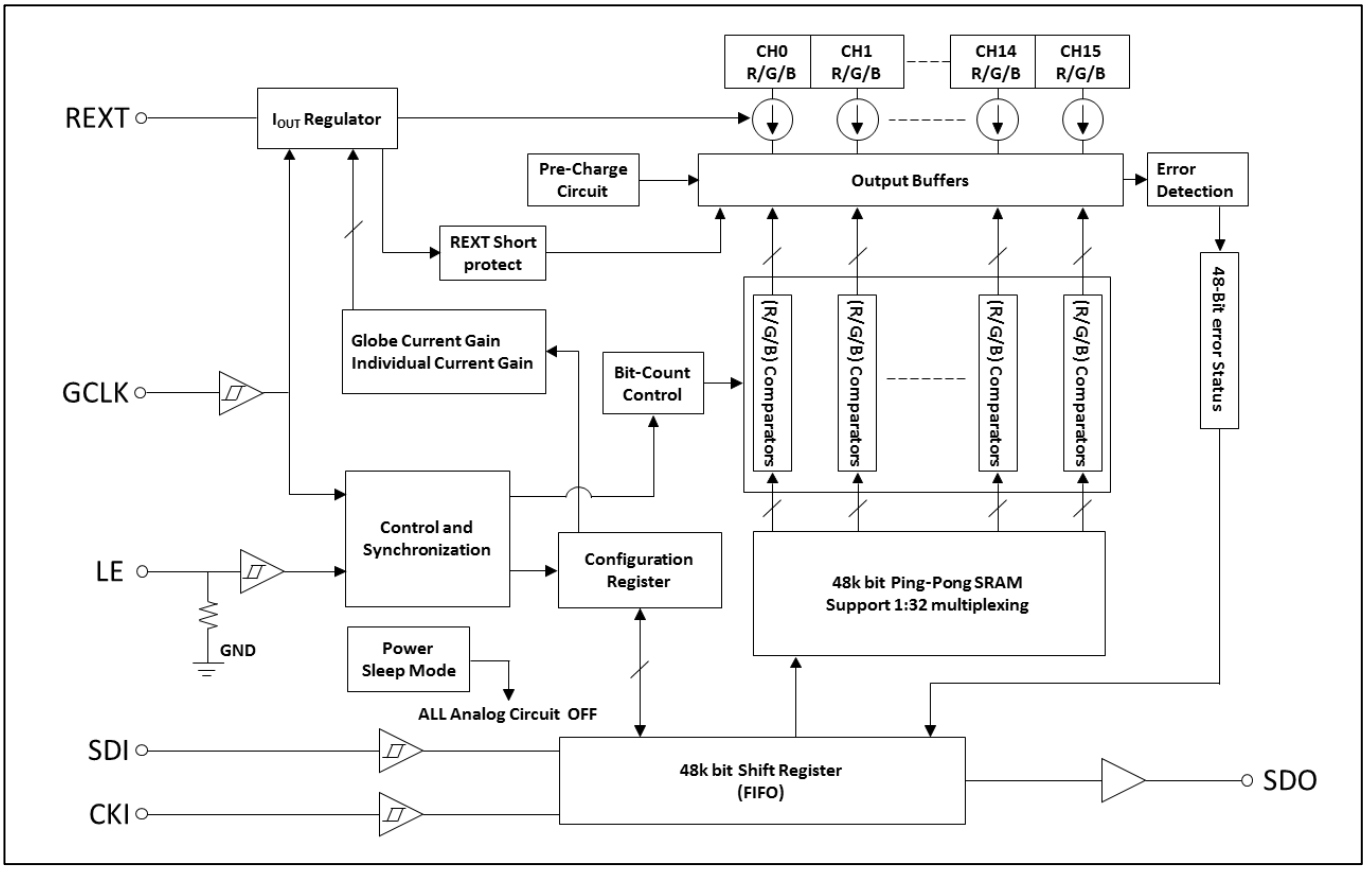
Floor 6-4, No.18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-7534 E-mail: info@mblock.com.tw

rate of scan-type LED displays. In addition, the innovative GCLK multiplier technique doubles visual refresh rate.

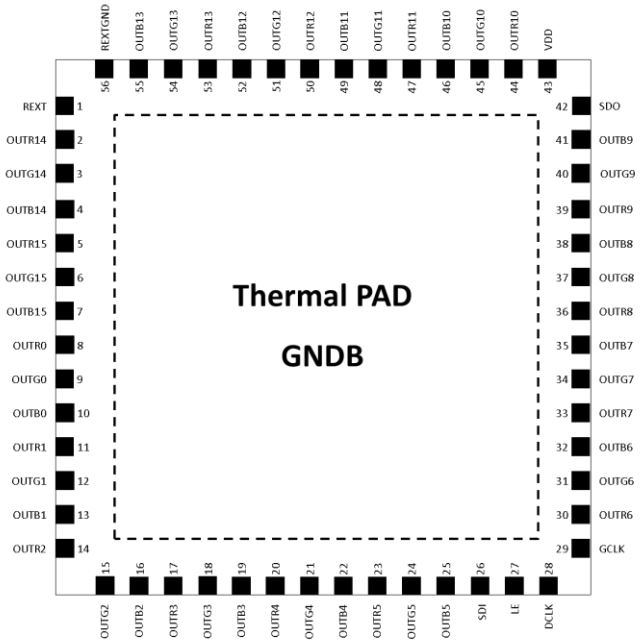
MBI5353 drives the corresponding LEDs to the brightness specified by image data. With MBI5353, all output channels can be built with 16-bit color depth (65,536 gray scales). When building a 16-bit color depth video, S-PWM technology reduces the flickers and improves the image fidelity.

Through compulsory error detection, MBI5353 detects individual LED for open-circuit errors without extra components. MBI5353 equips an innovative cross elimination function, and it solves the cross phenomenon induced by failure LEDs. Besides, integrated ghost elimination circuit eases the ghost problems. To further reduce power consumption of LED display, a built-in smart power saving mode will shut driver IC down when grayscale data is zero.

Block Diagram



Pin Configuration



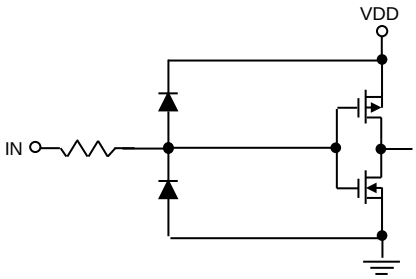
MBI5353GFN

Terminal Description

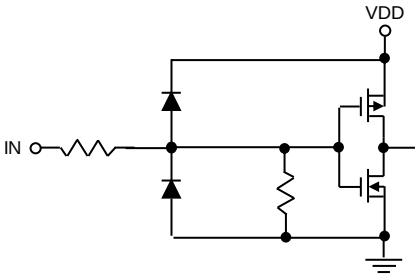
Pin Name	Pin Number	Function
VDD	43	3.3V/5V supply voltage terminal
GNDB	Thermal Pad	Ground terminal for control logic and current sink
SDI	26	Serial-data input to the shift register
DCLK	28	Clock input terminal used to shift data on rising or falling edge and carries command information when LE is asserted
LE	27	Data strobe terminal and controlling command with DCLK
GCLK	29	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock compared with input data.
SDO	42	Serial-data output to the receiver-end SDI of next LED driver
REXT	1	Input terminal used to connect an external resistor for setting up output current for all output channels
REXTGND	56	Ground pin for the external resistor. This pin should be connected to analog ground trace which is connected to power ground near the common GND point of board.
$\overline{OUTR0}$-$\overline{OUTR15}$	2, 5, 8, 11, 14, 17, 20, 23, 30, 33, 36, 39, 44, 47, 50, 53	Constant current output terminals for RLED
$\overline{OUTG0}$-$\overline{OUTG15}$	3, 6, 9, 12, 15, 18, 21, 24, 31, 34, 37, 40, 45, 48, 51, 54	Constant current output terminals for GLED
$\overline{OUTG0}$-$\overline{OUTB15}$	4, 7, 10, 13, 16,19, 22, 25, 32, 35, 38, 41, 46, 49, 52, 55	Constant current output terminals for BLED

Equivalent Circuits of Inputs and Outputs

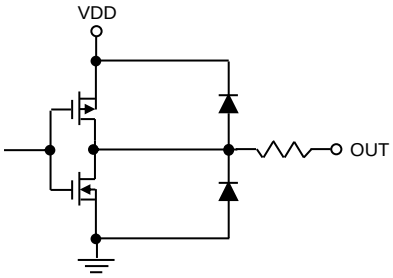
GCLK, DCLK, SDI terminal



LE Terminal



SDO Terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~5.5	V
Input Pin Voltage (SDI, DCLK, GCLK, LE)		V_{IN}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at OUT Port		V_{DS}	-0.5~17	V
Output Current		I_{OUT}	+22	mA
GND Terminal Current		I_{GND}	1100	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GFN Type	P_D	3.45	W
Thermal Resistance (On 4 Layer PCB, Ta=25°C)*	GFN Type	$R_{th(j-a)}$	29	°C/W
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM (MIL-STD-883G Method 3015.7, Human Body Mode)	HBM	Class 3B (8KV)	-
	MM (JEDEC EIA/JESD22-A115, Machine Mode)	MM	Class M4 (450V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTR0}$ ~ $\overline{OUTB15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	20	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}=1.4KΩ@10mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V R_{ext}=1.4KΩ@10mA		-	±1.0	±2.0	% / V
LED Open Detection Threshold		$V_{OD,TH}$	-		-	0.5	-	V
LED Short Detection Threshold		$V_{SD,TH}$	-		-	2.4	-	V
R_{EXT} short Detection Threshold		$V_{reshort}$	V_{REXT}<0.25V,Channel=OFF					V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off" (SDI=DCLK=GCLK =0Hz)	I_{DD}(off) 1	R_{ext}=open $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =Off; ICG & GCG are set to default value		-	6.5	-	mA
		I_{DD}(off) 2	R_{ext}=2.65 KΩ, $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =Off; ICG & GCG are set to default value		-	10	-	
		I_{DD}(off) 3	R_{ext}=890 KΩ, $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =Off; ICG & GCG are set to default value		-	15	-	
	"On" (SDI= 5MHz DCLK=2.5MHz, GCLK=20MHz)	I_{DD}(on) 1	R_{ext}=2.65 KΩ, $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =On; ICG & GCG are set to default value		-	10	-	
		I_{DD}(on) 2	R_{ext}=890 KΩ, $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =On; ICG & GCG are set to default value		-	15	-	

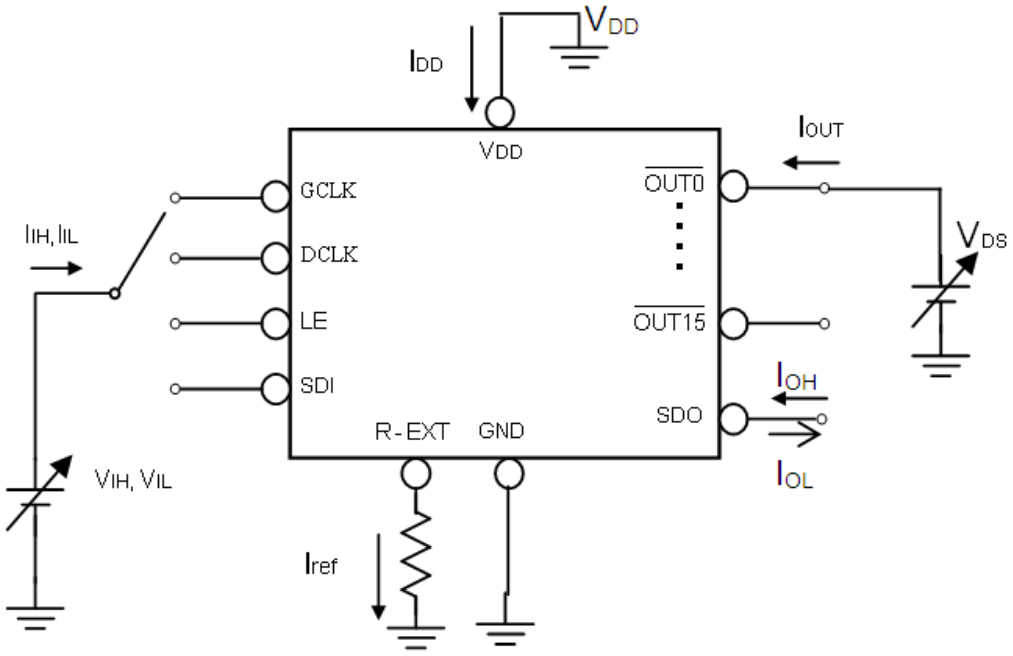
* One channel on.
** ICG: Individual Current Gain, please refer to R/G/B individual configuration register 1[8:2]
*** GCG: Global Current Gain, please refer to global configuration register 2[A:6]

Electrical Characteristics (V_{DD}=3.3V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTR0}$ ~ $\overline{OUTB15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	20	Ma
		I_{OH}	SDO		-	-	-1.0	Ma
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	Ma
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=1.4KΩ@10mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.5V and 5.5V R_{ext}=1.4KΩ@10mA		-	±1.0	±2.0	% / V
LED Open Detection Threshold		$V_{OD,TH}$	$V_{OD,TH}$ is programmable as 0.5V/1.0V/1.5V/2.0V		-	0.5	-	V
LED Short Detection Threshold		$V_{SD,TH}$	$V_{OS,TH}$ is programmable as 2.4V/3.0V/4.0V/4.4V		-	2.4	-	V
R_{EXT} short Detection Threshold		$V_{reshort}$	V_{REXT} <0.25V,Channel=OFF					V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off" (SDI=DCLK=GCLK =0Hz)	I_{DD}(off) 1	R_{ext}=open $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =Off; ICG & GCG are set to default value		-	6.5	-	mA
		I_{DD}(off) 2	R_{ext}=2.65 KΩ, $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =Off; ICG & GCG are set to default value		-	10	-	
		I_{DD}(off) 3	R_{ext}=890 KΩ, $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =Off; ICG & GCG are set to default value		-	15	-	
	"On" (SDI= 5MHz DCLK=2.5MHz, GCLK=20MHz)	I_{DD}(on) 1	R_{ext}=2.65 KΩ, $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =On; ICG & GCG are set to default value		-	10	-	
		I_{DD}(on) 2	R_{ext}=890 KΩ, $\overline{OUTR0}$ ~ $\overline{OUTB15}$ =On; ICG & GCG are set to default value		-	15	-	

*One channel on.
** ICG: Individual Current Gain, please refer to R/G/B individual configuration register 1[8:2]
*** GCG: Global Current Gain, please refer to global configuration register 2[A:6]

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=880Ω V_{DS}=1.0V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4V ICG(Dec)=127 GCG (Dec)=8 *IOUT=10mA	7	-	-	ns
	LE↑ – DCLK↑	t_{SU1}		10	-	-	ns
	LE↓(vsync) – GCLK	t_{SU2}		1200			ns
	LE↓ – DCLK↑	t_{su3}***		50			ns
Hold Time	DCLK↑ - SDI	t_{H0}		6	-	-	ns
	DCLK↑ - LE	t_{H1}		8	-	-	ns
	GCLK – LE↓(vsync)	t_{H2}		300			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	25	28	ns
	GCLK –/OUT2n*	t_{PD1}		-	35	-	ns
	LE – SDO	t_{PD2}***		-	30	40	ns
Pulse Width	LE	$t_{w(LE)}$		15			ns
Command to command		tcc		50	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	15	MHz
Gray Scale Clock Frequency*****		F_{GCLK}		-	-	33	MHz
Gray Scale Clock Frequency (when GCLK multiplier is enabled)		F_{GCLK}		-	-	16.6	MHz
Min Clock(GCLK) pulse width*****		$t_{W(GCLK)}$		12	-	-	ns
Min Clock(DCLK) pulse width******		$t_{W(DCLK)}$		24			ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		40	-	-	%
Compulsory error detection operation time****		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports(OUT-R)		t_{OR}			15	25	ns
Output Fall Time of Output Ports(OUT-R)		t_{OF}			15	25	ns
Dead time		tdth		300			ns
Dead time Low state		tdtl		1200			ns

*Output waveforms have good uniformity among channels.

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7

***In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.

****Users have to leave more time than the maximum error detection time for the error detection.

*****The Gray Scale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

******The DCLK Clock period must be 50% duty cycle.

Switching Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=880Ω V_{DS}=1.0V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4V ICG(Dec)=127 GCG (Dec)=8 *IOUT=10mA	9	-	-	ns
	LE – DCLK↑	t_{SU1}		12	-	-	ns
	LE↓(vsync/swrst) – GCLK	t_{SU2}		1200			ns
	LE↓ – DCLK↑	t_{su3}***		52			ns
Hold Time	DCLK↑ - SDI	t_{H0}		8	-	-	ns
	DCLK↑ - LE	t_{H1}		10	-	-	ns
	GCLK – LE↓(vsync/swrst)	t_{H2}		300			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	30	33	ns
	GCLK –/OUT2n*	t_{PD1}		-	45	-	ns
	LE – SDO	t_{PD2}***		-	40	50	ns
Pulse Width	LE	$t_{w(LE)}$		16			ns
Command to command		tcc		52	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	12.5	MHz
Gray Scale Clock Frequency*****		F_{GCLK}		-	-	20	MHz
Gray Scale Clock Frequency (when GCLK multiplier is enabled)		F_{GCLK}		-	-	10	MHz
Min Clock(GCLK) pulse width*****		$t_{W(GCLK)}$		13			ns
Min Clock(DCLK) pulse width******		$t_{W(DCLK)}$		26			
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		40		-	%
Compulsory error detection operation time****		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports(OUT-R)		t_{OR}			25	35	ns
Output Fall Time of Output Ports(OUT-R)		t_{OF}			25	35	ns
Dead time		Tdth		300			ns
Dead time (Low state)		tdtl		1200			ns

*Output waveforms have good uniformity among channels

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7

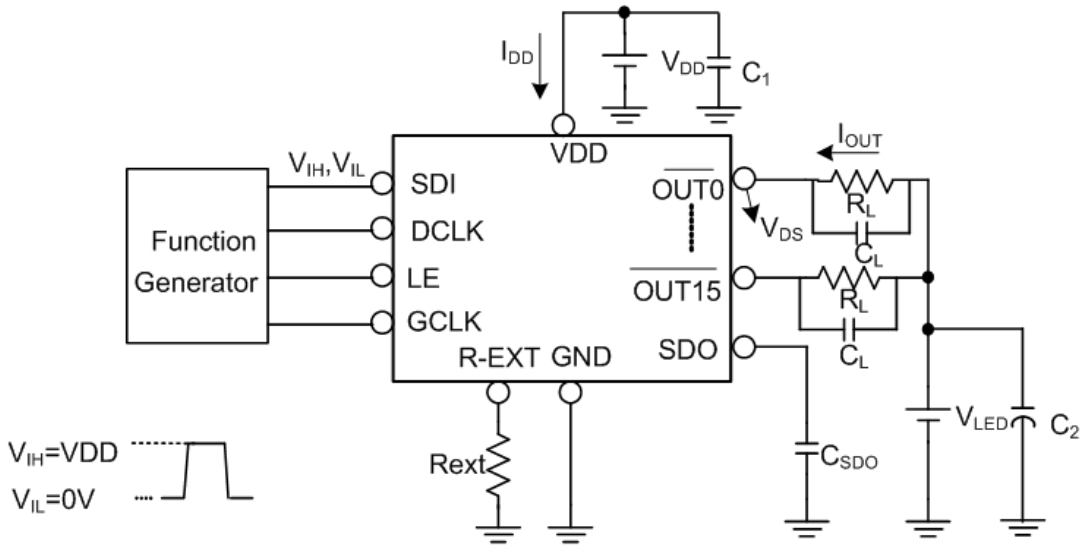
***In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.

****Users have to leave more time than the maximum error detection time for the error detection.

*****The Gray Scale Clock period must 50% duty cycle when the function of GCLK multiplier is enabled.

******The DCLK Clock period must be 50% duty cycle.

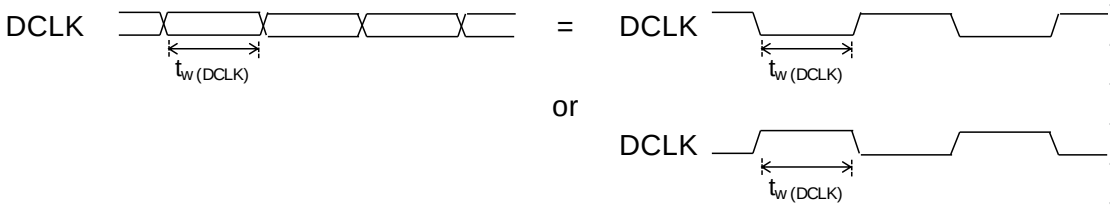
Test Circuit for Switching Characteristics



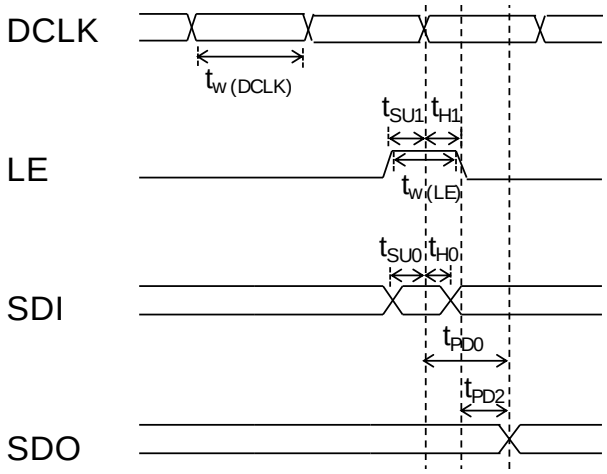
Timing Waveform

(1)

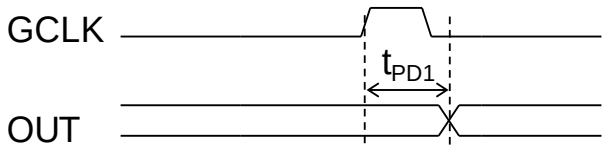
(Note : The figure means that DCLK can be a rising or falling level edge start point)



(2)



(3)



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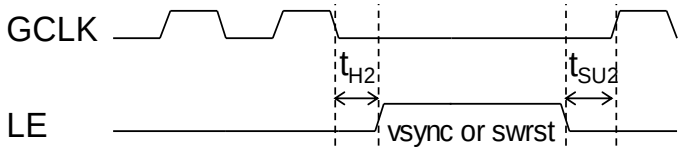

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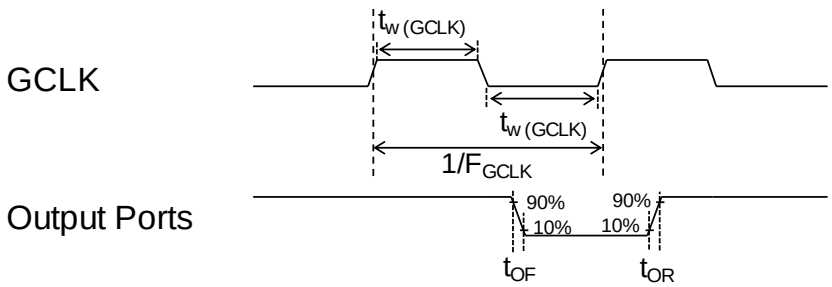

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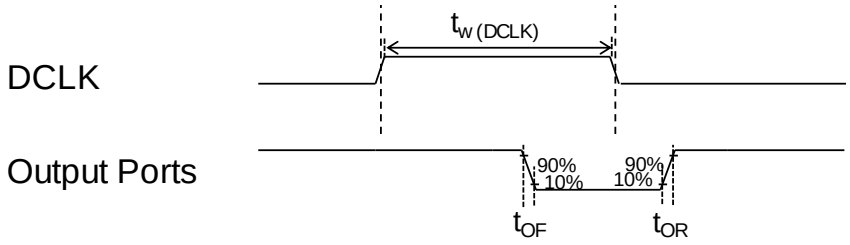
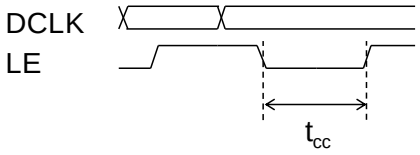
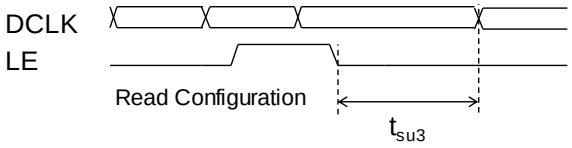

DCLK
Output Ports
$t_{W(DCLK)}$
90%
10%
90%
10%
t_{OF}
t_{OR}

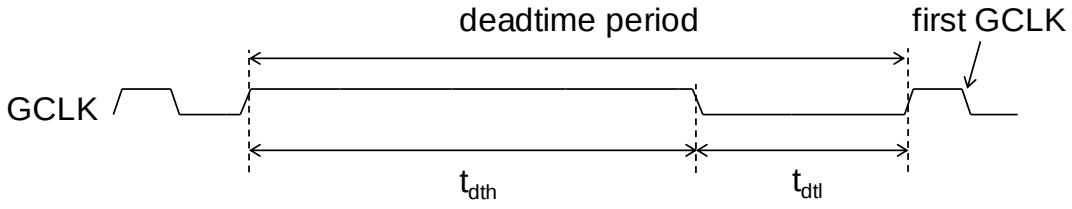
(7)


DCLK
LE
t_{cc}

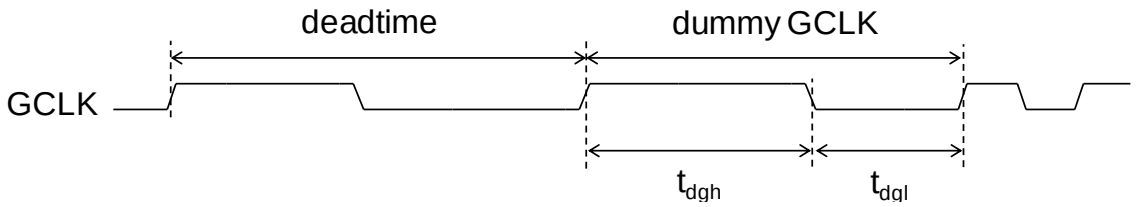
(8)


DCLK
LE
Read Configuration
t_{su3}

(9)


deadtime period
first GCLK
GCLK
t_{dth}
t_{dtl}

(10)


deadtime
dummy GCLK
GCLK
t_{dgh}
t_{dgl}

Control Command

	Signals Combination		Description
Command Name	**LE**	**The Sum of DCLK Rising and Falling Edge Number when LE is asserted**	**The Action after a Falling Edge of LE**
stop compulsory error detection	High	1	Stop compulsory error detection.
Individual Latch	High	1	Serial data are transferred to the buffers
Vertical Sync	High	2 or 3	Display frame will be updated
Write Configuration*	High	4	Serial data are transferred to the “configuration register”
Read global configuration	High	5	Serial data are transferred from the “global configuration register”
Read R configuration reg	High	6	Serial data are transferred from the “R configuration reg”
Read G configuration reg	High	7	Serial data are transferred from the “G configuration reg”
Read B configuration reg	High	8	Serial data are transferred from the “B configuration reg”
Compulsory error detection(open error)	High	9	Start compulsory error detection(open error detection)
Software reset	High	10	Reset all the digital part (not including configure registers)
Enable all outputs*	High	11	All 16 channel turn-on
Disable all outputs*	High	12	All 16 channel turn-off
Compulsory error detection(short error)	High	13	Start compulsory error detection(short error detection)
Confirm command	High	14	Confirm command needs to be sent before “write configure, enable all outputs, disable all outputs and test mode” commands.

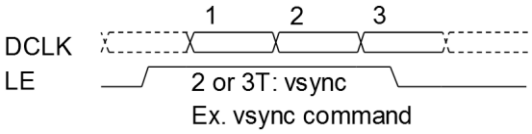
*Those commands can only be activated after Confirm command; otherwise, they will be invalid.

Waveform of Commands

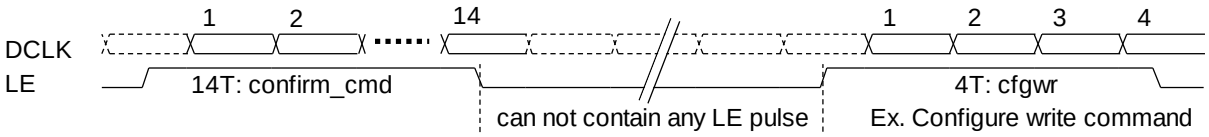
The following figures show the waveforms of each command.

Note: for all following waveforms, "T" means a **rising or falling edge** number of DCLK

Commands which need no confirm-command ahead



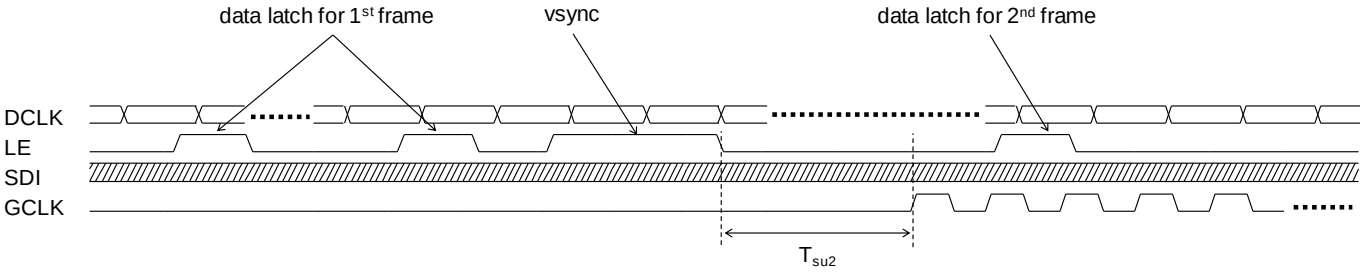
Commands which need to have confirm-command ahead



Initialization Sequence

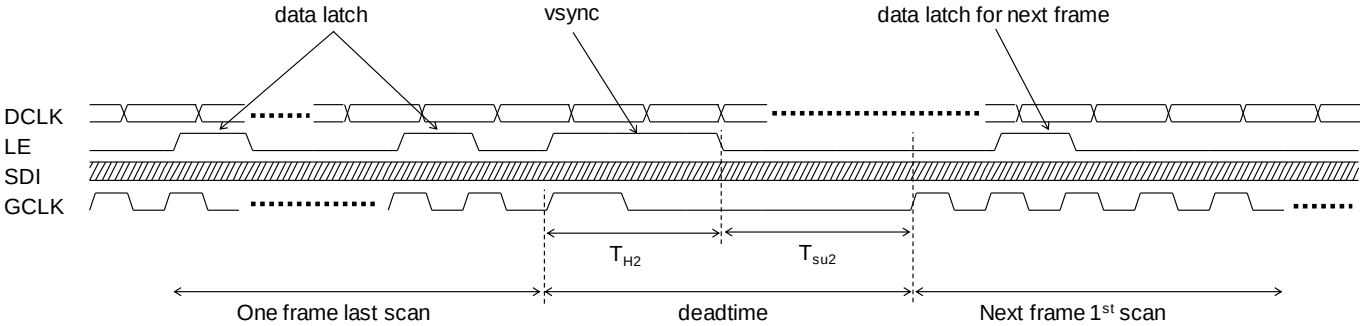
At initialization, users need to program the configuration register, if the default value of the register is not what they want. Then, the users need to send the gray scale data by the number of "Data Latch" commands (16 x number of scan lines), and then send one VSYNC command to start to display.

For the initial sequence, users should send VSYNC command after one frame "Data Latch" command as shown in the below waveform. The display data will not start until first VSYNC command is ready. The GCLK must be stopped before first VSYNC command is set



VSYNC Command Operation

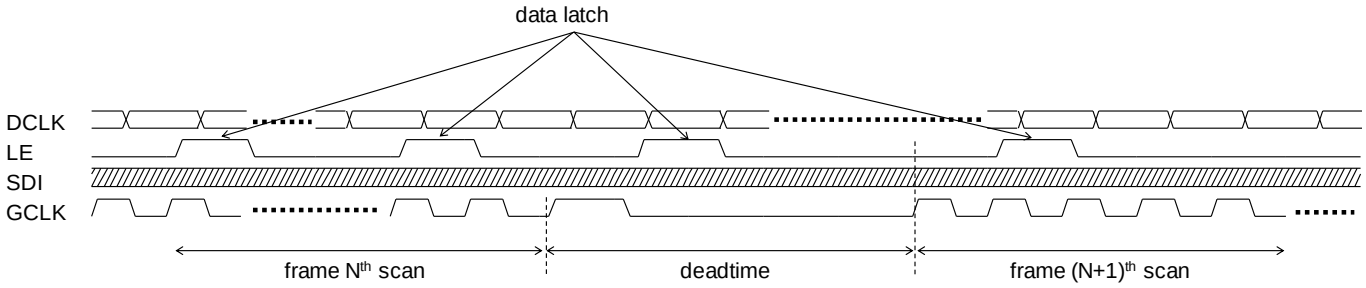
"VSYNC" command is set when users want to update the image frame. Waveforms below derived how the VSYNC command updates the frame data.



T_{H2} is generated of delta and gclk extend function.

Data latch Command Operation

"data latch" command can be set during dead-time(when changing scan line)



There are limitations for users to follow:

a.) It is suggested for controller to keep one GCLK counter (from 0~1024), which will preset to 1024 at the falling edge of LE of VSYNC command and restart from 0 at next GCLK.

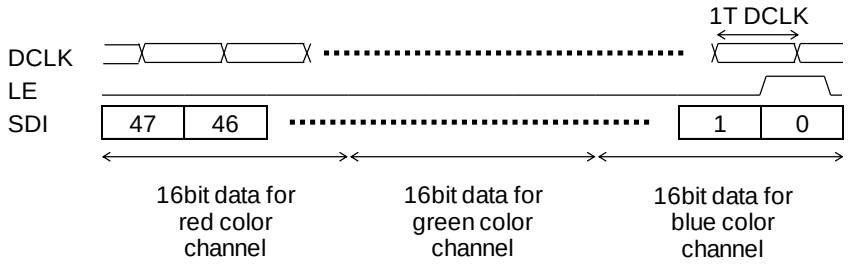
b.) Since VSYNC is the LE clock domain, there is a timing limitation between LE and GCLK. The GCLK should stop before VSYNC command is sent. The setup and hold time between LE's falling edge and GCLK's rising edge must meet the T_{SU2} and T_{H2}, respectively (The period of T_{H2} must greater than 300 ns and T_{SU2} must greater than 1200ns).

c.) The GCLK also needs to stop for dead time. The dead time is the time interval between scan lines, and is controlled by stopping GCLK. When VSYNC command is set, the frame will be updated. The scan line needs to be switched (by controller) from scan line k to scan line 0, too.

d.) DCLK can either stop or not when there is no command.

e.) The new data will be loaded to internal display buffer at VSYNC command. It will start to display after dead time is finished.

Data Latch



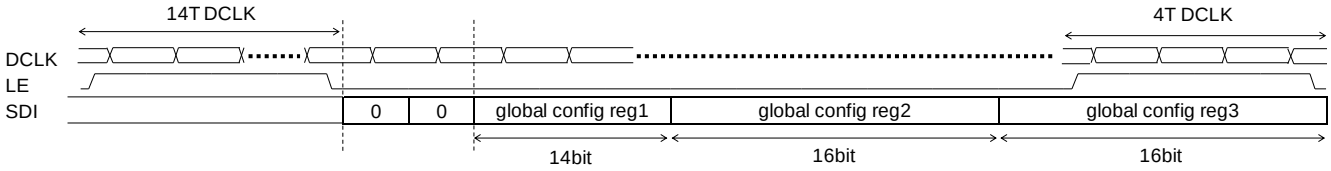
Data Latch command is used to latch the 48-bit shift register from SDI to internal SRAM buffer. When this command is received, the last 48 bits data before the falling edge of LE will be latched into SRAM, as shown in the above waveform, and MSB bit needs to be sent first.

Write Configuration

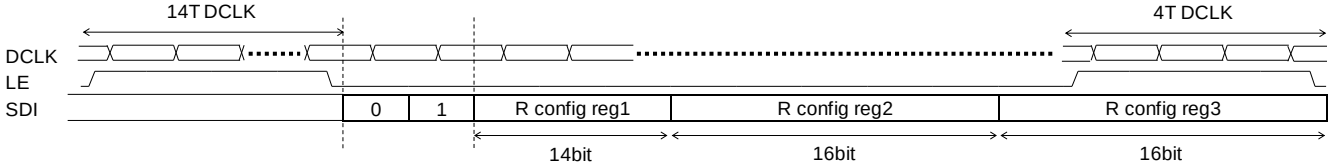
"Write configuration" command is used to program the configuration register of MBI5353. The "Pre-Active" command must be sent in advance. When this command is received, the last 48 bits data before the falling edge of LE will be latched into configuration register, as shown in the above waveform, and MSB bit needs to be sent first.

Note: "T" means a **rising or falling edge** number of DCLK

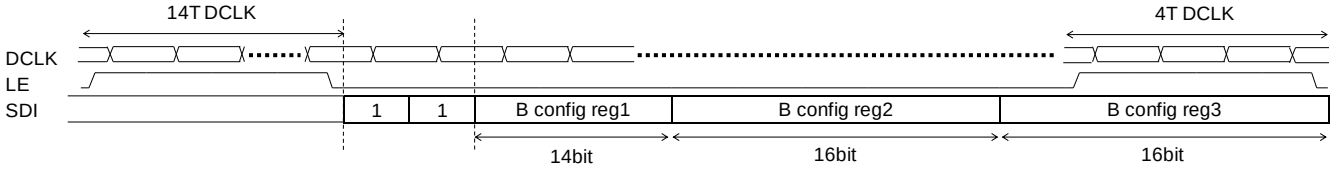
- **Write global configuration register**



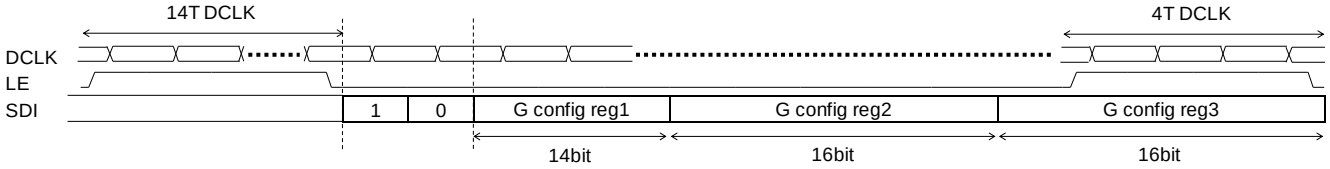
- **Write red color configuration register**



- **Write green color configuration register**



- **Write blue color configuration register**

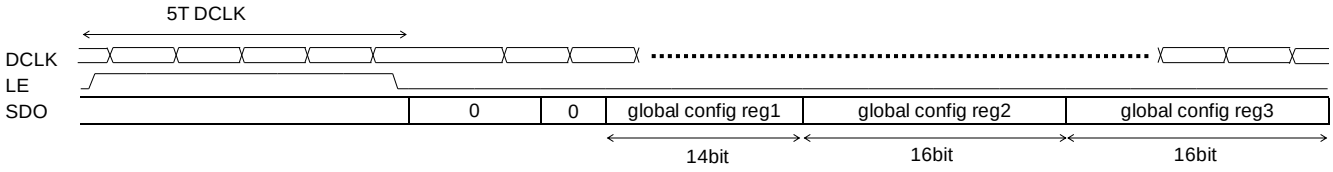


Read Configuration

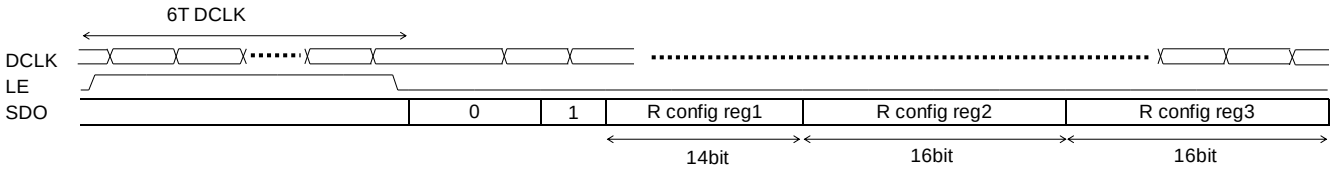
"Read configuration" command is used to read the configuration register of MBI5353. When this command is received, the 48-bit data of configuration register will be shifted out from SDO pin, as shown in the above waveform, and MSB bit will be shifted out first.

Note: "T" means a **rising or falling edge** number of DCLK

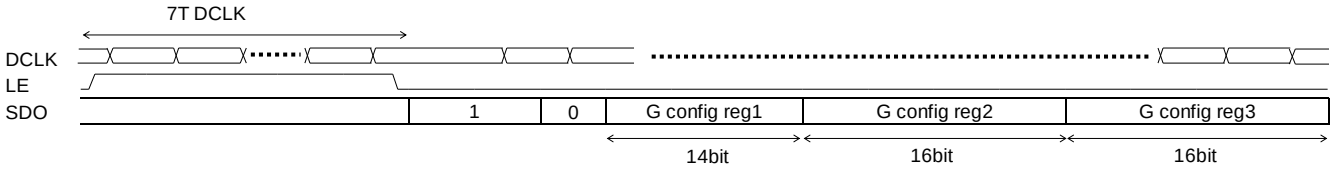
- **Read global configuration register**



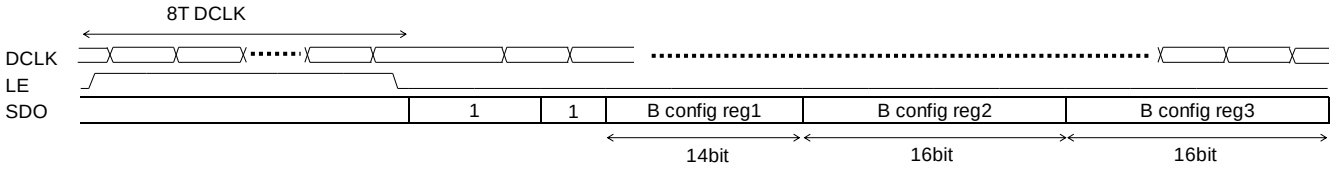
- **Read red configuration register**



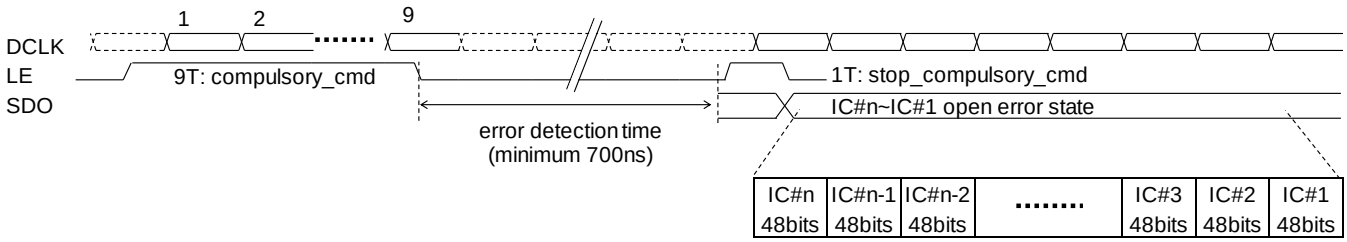
- **Read green configuration register**



- **Read blue configuration register**

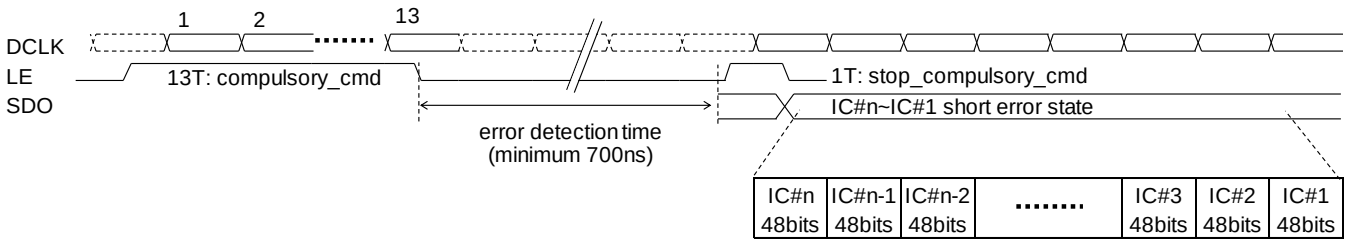


Compulsory LED open detection



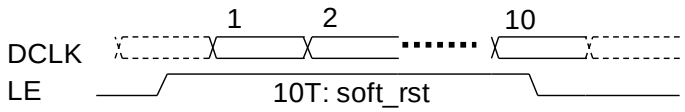
IC#n 48bits is { $\overline{OUTR15}$, $\overline{OUTG15}$, $\overline{OUTB15}$, $\overline{OUTR14}$, $\overline{OUTG14}$, $\overline{OUTB14}$, …, $\overline{OUTR0}$, $\overline{OUTG0}$, $\overline{OUTB0}$ }

Compulsory LED short detection



IC#n 48bits is { $\overline{OUTR15}$, $\overline{OUTG15}$, $\overline{OUTB15}$, $\overline{OUTR14}$, $\overline{OUTG14}$, $\overline{OUTB14}$, …, $\overline{OUTR0}$, $\overline{OUTG0}$, $\overline{OUTB0}$ }

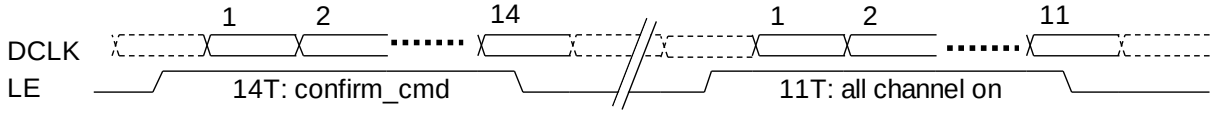
Software reset Command Operation



Software reset command makes MBI5353 go back to the initial state except configuration register value. After this command is received, the output channels will be turned off and will display again with last gray-scale value after new “VSYNC” command is received.

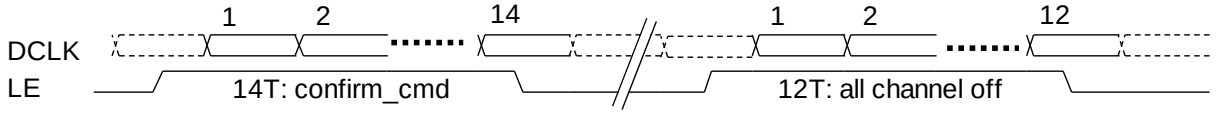
Enable all outputs Command Operation

This command can only be activated after Confirm command; otherwise, they will be invalid.



Disable all outputs Command Operation

This command can only be activated after Confirm command; otherwise, they will be invalid.



Definition of Global Configuration Register 1

MSB LSB

D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	1	0	0	0	0	0

Default setting of configuration register is 16'h032B

Bit	Attribute	Definition	Value	Function
D~C	Read/Write	Grayscale mode select	00 (Default)	Grayscale PWM is 16bit mode, each PWM cycle is 65536 GCLKs
			01	Grayscale PWM is 15bit mode, each PWM cycle is 32768 GCLKs User should still send 16bit data with 1 bit 0 in LSB bits. Ex., {15'h1234, 1'h0}.
			10	Grayscale PWM is 14bit mode, each PWM cycle is 16384 GCLKs User should still send 16bit data with 2 bit 0 in LSB bits. Ex., {14'h1234, 2'h0}.
			11	Grayscale PWM is 13bit mode, each PWM cycle is 8192 GCLKs User should still send 16bit data with 3 bit 0 in LSB bits. Ex., {13'h1234, 3'h0}.
B~A	Read/Write	S-PWM mode	00 (Default)	If grayscale PWM 16bit mode is asserted, PWM cycle is divided into 64 sections If grayscale PWM 15bit mode is asserted, PWM cycle is divided into 32 sections If grayscale PWM 14bit mode is asserted, PWM cycle is divided into 16 sections If grayscale PWM 13bit mode is asserted, PWM cycle is divided into 8 sections, each section has 1024 GCLKs.
			01	If grayscale PWM 16bit mode is asserted, PWM cycle is divided into 128 sections If grayscale PWM 15bit mode is asserted, PWM cycle is divided into 64 sections If grayscale PWM 14bit mode is asserted, PWM cycle is divided into 32 sections If grayscale PWM 13bit mode is asserted, PWM cycle is divided into 16 sections, each section has 512 GCLKs.
			10	If grayscale PWM 16bit mode is asserted,PWM cycle is divided into 256 sections If grayscale PWM 15bit mode is asserted,PWM cycle is divided into 128 sections If grayscale PWM 14bit mode is asserted,PWM cycle is divided into 64 sections If grayscale PWM 13bit mode is asserted,PWM cycle is divided into 32 sections, each section has 256 GCLKs.
			11	If grayscale PWM 16bit mode is asserted,PWM cycle is divided into 512 sections If grayscale PWM 15bit mode is asserted,PWM cycle is divided into 256 sections If grayscale PWM 14bit mode is asserted,PWM cycle is divided into 128 sections If grayscale PWM 13bit mode is asserted,PWM cycle is divided into 64 sections, each section has 128 GCLKs.

9~5	Read/Write	Number of scan lines	00000 00001 00010 00011 (**Default**) ~ 11111	00000: 1 lines; 01000: 9 lines; 10000: 17 lines; 00001: 2 lines; 01001: 10 lines; 10001: 18 lines; 00010: 3 lines; 01010: 11 lines; 10010: 19 lines; 00011: 4 lines; 01011: 12 lines; . 00100: 5 lines; 01100: 13 lines; . 00101: 6 lines; 01101: 14 lines; . 00110: 7 lines; 01110: 15 lines; . 00111: 8 lines; 01111: 16 lines; 11111: 32 lines;
4	Read/Write	GCLK multiplier	0 (Default)	GCLK multiplier disable
			1	GCLK multiplier enable
3~0	Read/Write	Reserved	0000 (Default)	Reserved

Default setting of configuration register is 16'h0060

Definition of Global Configuration Register 2

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~C	Read/Write	Reserved	0000 (default)	Reserved
B	Read/Write	R_{EXT} short detection enable	0 1 (Default)	R_{EXT} short detection enable
A~9	Read/Write	Global current gain (Constant gain) *	00~ 11(default)	00: Reserved 01: Current ratio=15.8* 10: Reserved 11: Current ratio=47.6*
8~6	Read/Write	Global current gain (Adjustable gain) *	000 (default) ~ 111	000~111: Current ratio=100%~200% 1 step=14.3%
5	Read/Write	Reserved	0 (Default)	Reserved
4~3	Read/Write	Stagger delay	00 (Default)	No stagger
			01~11	Stagger delay enable 01: Red color group lead Green color group 25ns Green color group lead Blue color group 25ns 10: Red color group lead Green color group 50ns Green color group lead Blue color group 50ns 11: Red color group lead Green color group 75ns Green color group lead Blue color group 75ns
2~1	Read/Write	Reserved	00 (default)	Reserved
0	Read/Write	Power saving mode enable	0 (Default)	Power saving mode disabled
			1	IC enter power saving mode when all gray data in SRAM are all zero

Default setting of configuration register is 16'h0e00

* Refer to "Setting Output Current" section

Definition of Global Configuration Register 3

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~B	Read/Write	reserve	00000 (Default)	
10	Read/Write	Black screen precharge	0(Default)	0:disable 1:enable
9~0	Read/Write	reserve	0000000000 (Default)	

Default setting of configuration register is 16'h0000

Definition of R/G/B Individual Configuration Register 1

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

		D	C	B	A	9	8	7	6	5	4	3	2	1	0
		0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bit	Attribute	Definition	Value	Function
D~A	Read	Reserved	0000	0000
9	Read/Write	Reserved	1(default)	Reserved
8~2	Read/Write	Current gain adjustment*	0000000~ 1111111	7'b1111111 (Default) Allow 128-step programmable current gain, and the gain range is from 100%-0.78%.
1~0	Read/Write	Reserved**	11(default)	Reserved

Default setting of configuration register is 16'h03FF

* Refer to "Setting Output Current" section

** Please assign "00" as a suggested value

Gray Scale Mode and Scan-type S-PWM

MBI5353 provides a selectable 16 / 15 / 14 / 13-bit gray scale by setting the global configuration register1 bit [D:C] and [B:A], the default value is set to '00' and '00', so the grayscale PWM is asserted as 16-bit mode, PWM cycle is divided into 64 sections.

MBI5353 has a smart S-PWM technology for scan type. With S-PWM, the total PWM cycles can be divided into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles. The MSB information can be broken down into many refresh cycles to achieve overall same high bit resolution.

Number of Scan Line

MBI5353 supports 1 to 32 scan lines. Please set the global configuration register1 bit [9:5] according to the application. The default value '00011' is 4 scan lines.

Data Input Sequence

The sequence of input data starts from scan line 0 first, and then scan line 1 ,and so on.

During each scan line, grayscale data of $\overline{OUTR15}$ / $\overline{OUTG15}$ / $\overline{OUTB15}$ needs to be sent first, and then $\overline{OUTR14}$ / $\overline{OUTG14}$ / $\overline{OUTB14}$, continuously to channel $\overline{OUTR0}$ / $\overline{OUTG0}$ / $\overline{OUTB0}$.

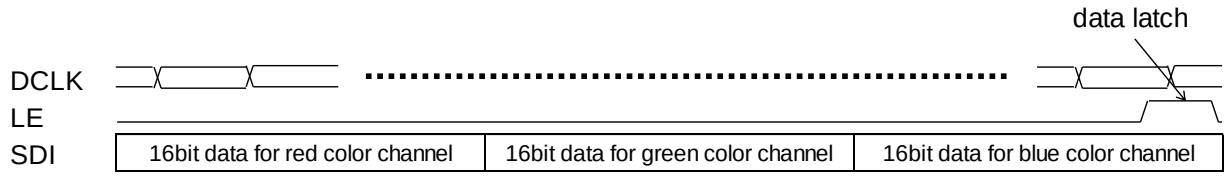
Please refer to the section of scan type application structure for scan type scheme.

The following examples are the waveforms with 1 LED driver and 2 cascaded LED drivers respectively.

For one channel, at 14-bit mode, the MSB 14 bits are valid, the other LSB bits are invalid. The data format is as following:

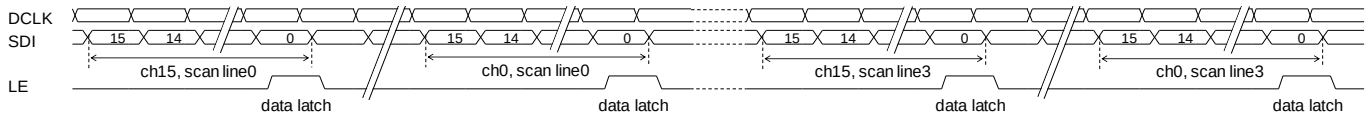
bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	invalid	invalid
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Each data latch includes one pixel gray data, that is $\overline{OUTR\#}$ / $\overline{OUTG\#}$ / $\overline{OUTB\#}$ gray data, #=15~0.



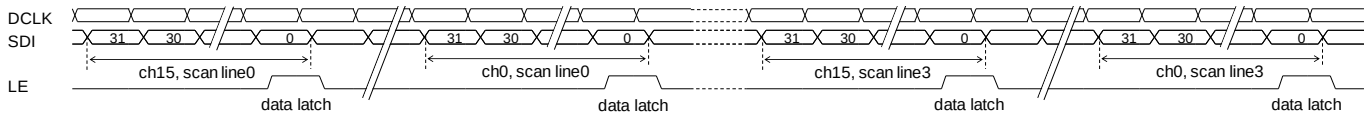
1x IC, 4 scan lines

For only one LED driver used, there are 48 bits for each pixel, and note that MSB bit is sent first.



2x ICs, 4 scan lines

For two LED drivers cascaded, there are 48 bits for each LED driver, so there are 96 bits for each pixel, first 48 bits (bit95 ~ bit48) is for 2nd LED driver, and last 48 bits (bit47 ~ bit0) is for 1st LED driver, please note that MSB bit is sent first, too.



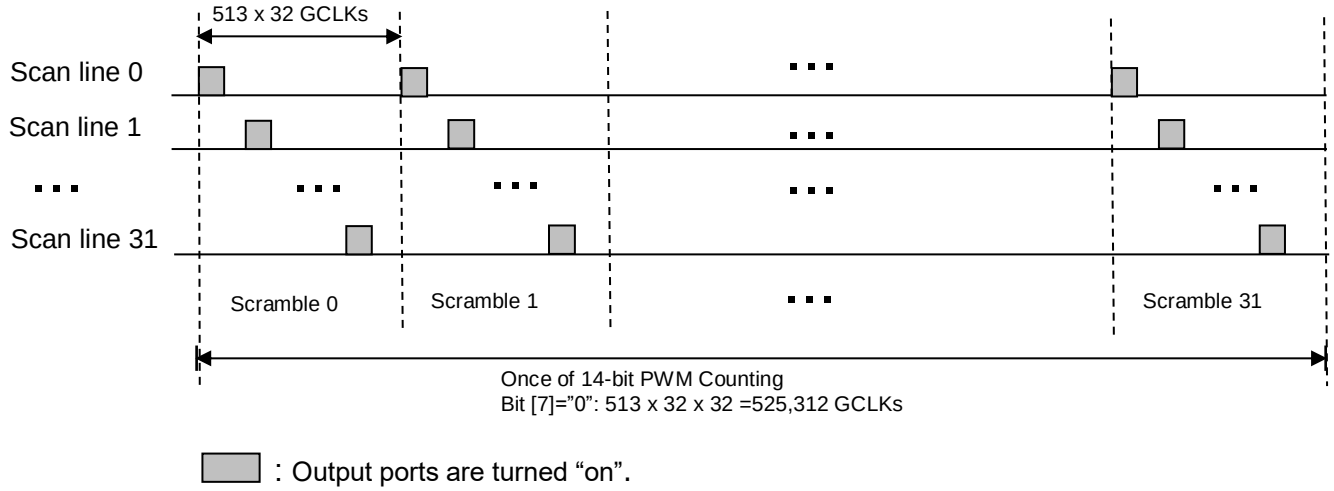
GCLK multiplier

MBI5353 provides a GCLK multiplier function by setting the global configuration register1 bit [4]. The default value is set to ’0’ for GCLK multiplier disabled.

GCLK multiplier disabled (global configuration register1 bit [4] = 0), take grayscale PWM 14-bit mode. PWM cycle is divided into 32 sections as an example,

GCLK multiplier disabled (configuration register1 bit [6] = 0)

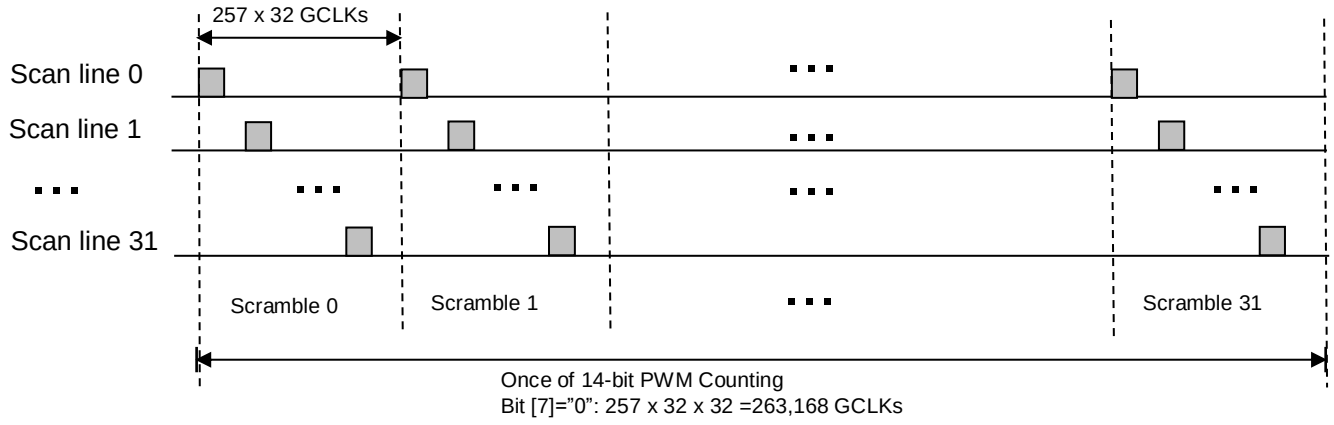
Display sequence of 32 scrambles



: Output ports are turned “on”.

GCLK multiplier enabled (configuration register1 bit [6] = 1)

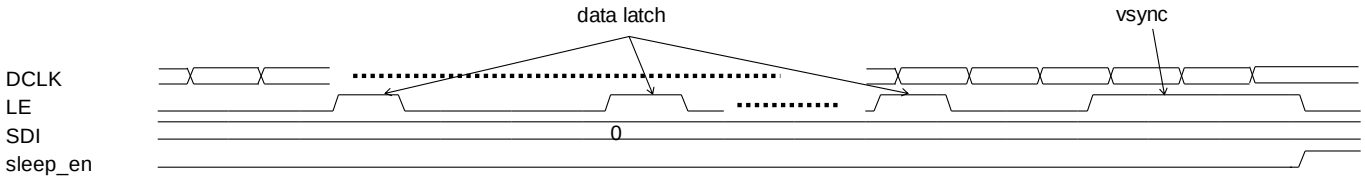
Display sequence of 32 scrambles



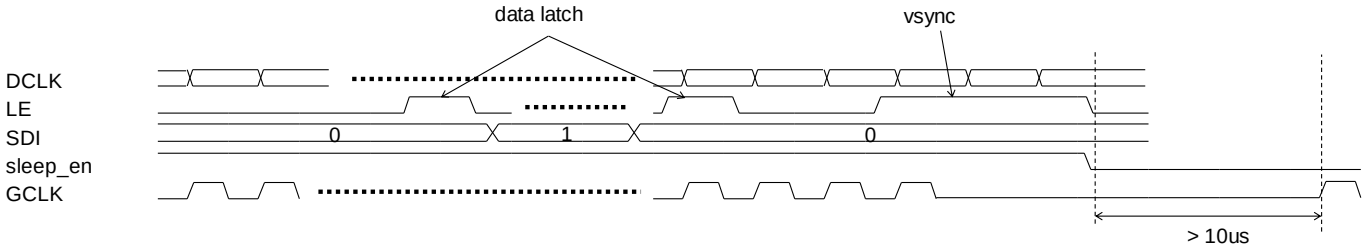
: Output ports are turned “on”.

Power saving mode

If all grayscale data of one frame are all zero, then MBI5353 will enter power saving (sleep_en) mode after VSYNC.

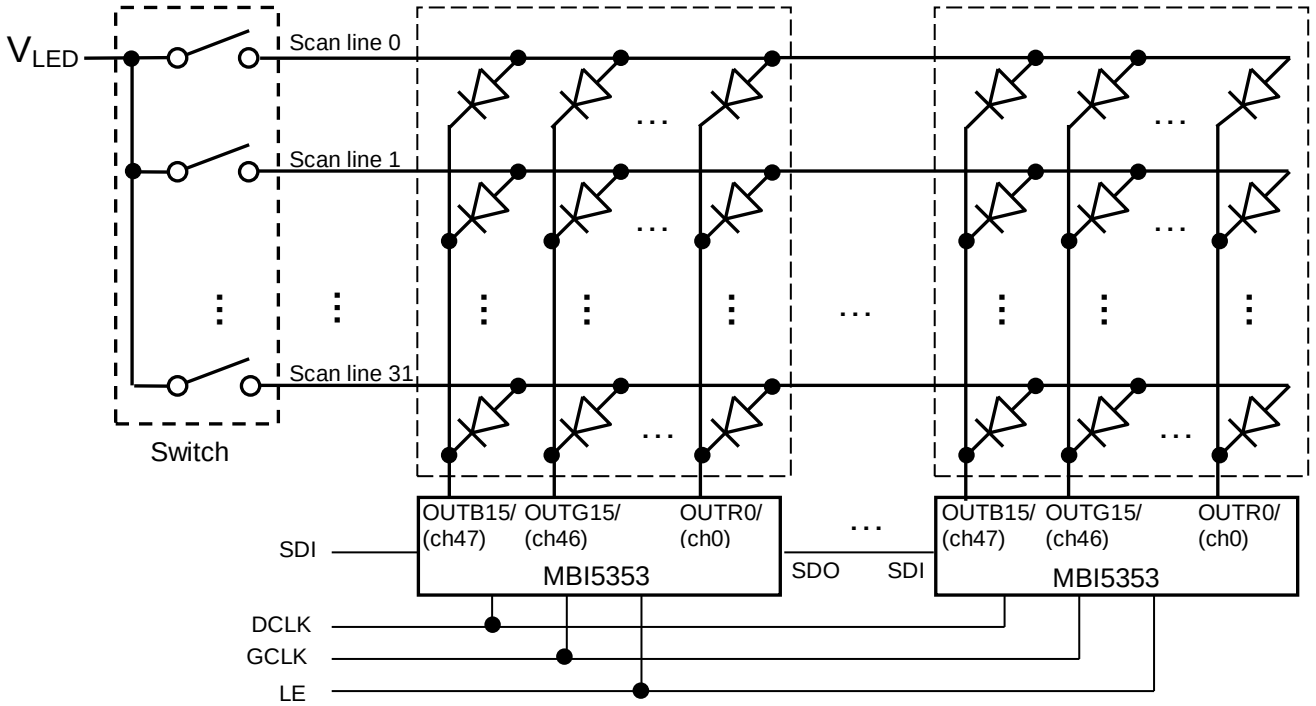


If any grayscale data of one frame is non-zero, MBI5353 will exit power saving mode after VSYNC. The suggested duration of returning from power saving mode should be greater than 1 millisecond to ensure normal operation.



Operation Principle

Scan type application structure



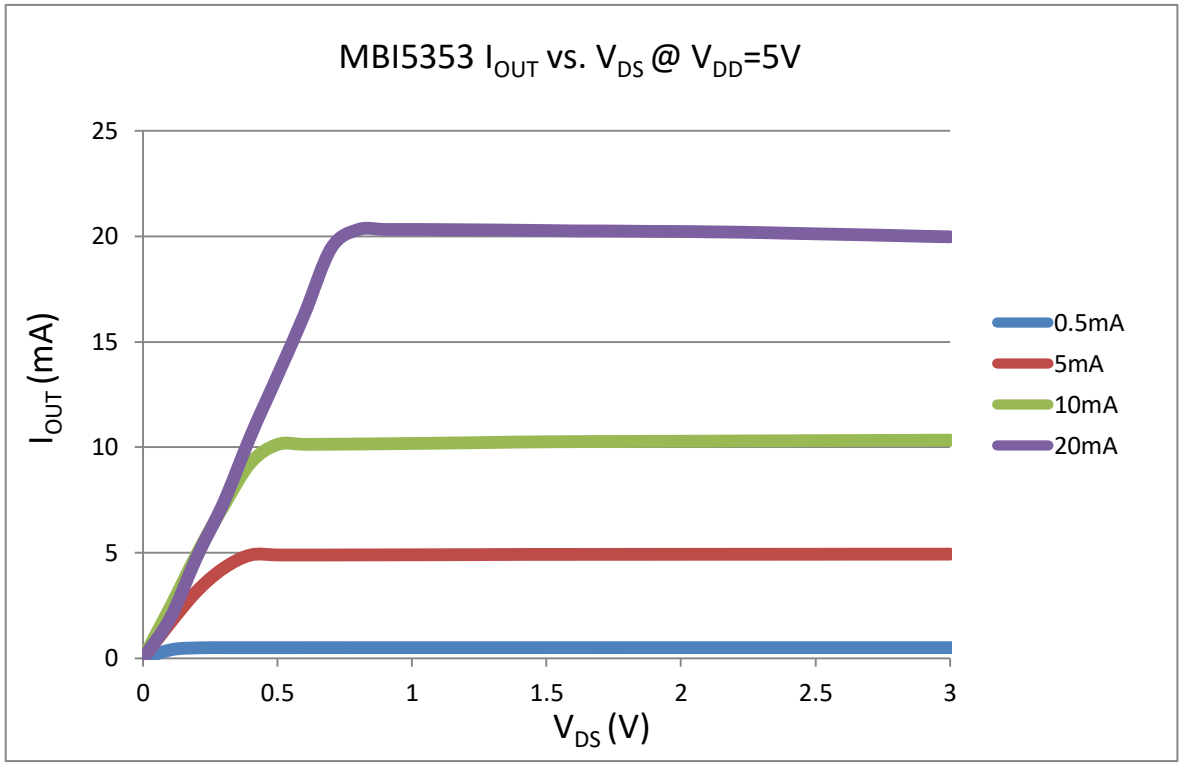
The above figure shows the suggested application structure of scan type scheme with 32 scan lines. The gray-scale data are sent by pin “SDI and SDO” with the commands formed by pin “LE” and “DCLK”. The output ports from 48 channels ($\overline{OUTR15}$ / $\overline{OUTG15}$ / $\overline{OUTB15}$,…, $\overline{OUTR0}$ / $\overline{OUTG0}$ / $\overline{OUTB0}$) will output the PWM result for each scan line at different time, so there must be one “Switch” to multiplex for each scan line. The switching sequence and method and the command usage will be described in the application note.

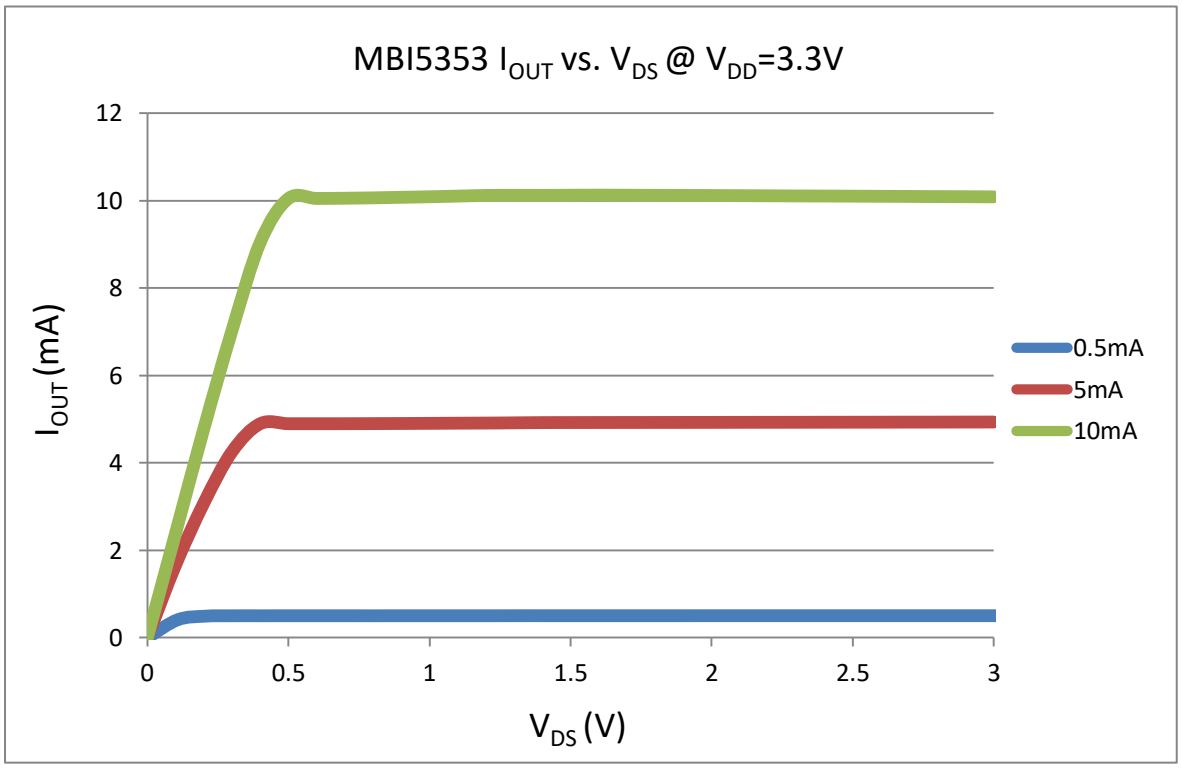
Constant Current

In LED display application, MBI5353 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximum current variation between channels is less than 2.5%, and that between ICs is less than ±3%

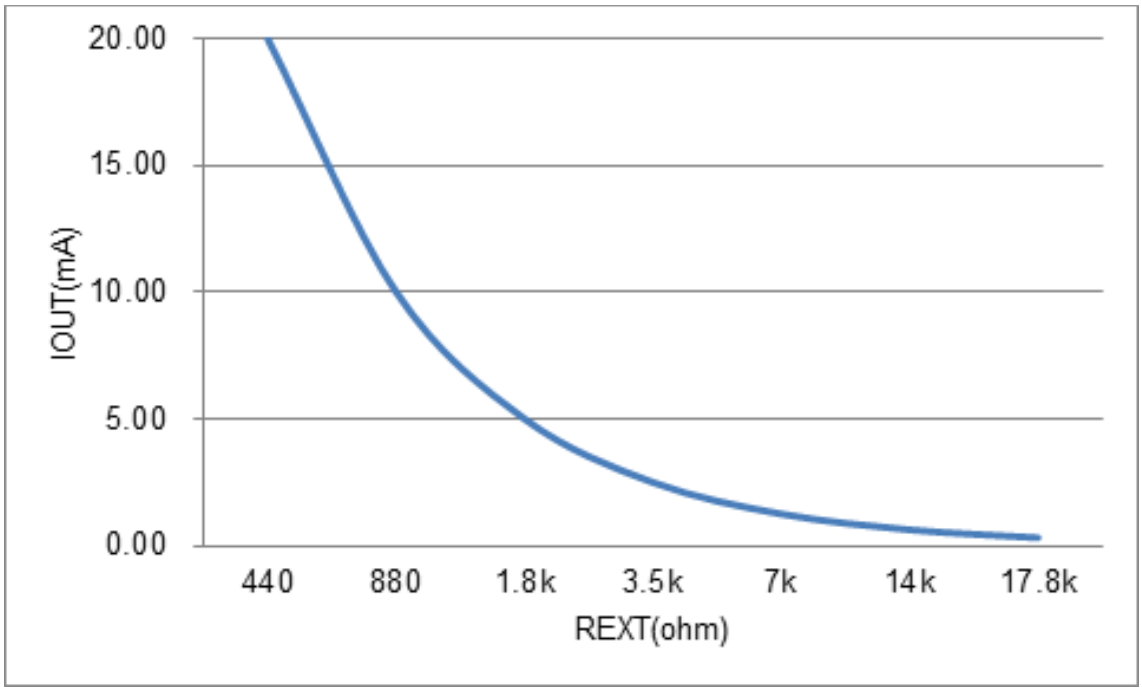
2) In addition, the current characteristic of output stage is flat and user can refer to the figure below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.





Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{EXT}. The default relationship between I_{OUT} and R_{EXT} is shown in the following figure.



Users can follow the below formulas to calculate the target output current I_{OUT}.

$$IOUT_{GCG} = \frac{1}{REXT} * 0.556 * Gain1 * Gain2$$

Whereas REXT is the resistance of the external resistor connected to REXT terminal and ground.
Gain1 and Gain2 is the digital current gain, which is set by the bit 5 to 0bit of the configuration register.

The formula and the setting for Gain1, Gain2 are described in the “Current Gain Adjustment” section.

Current Gain Adjustment

Global Current Gain Adjustment

GCG(Global Current Gain) is in global configuration register 2, and GCG[A:9] is set by global configuration register 2[A:9], similarly, GCG[8:6] is set by global configuration register 2[8:6]; Gain1 and Gain2 are the digital current gain, which is set by GCG[A:9] and GCG[8:6].

The default value of GCG[A:6]=8(dec), which means Gain1=47.6 and Gain2=1.

When global current gain adjustment is applied, users can follow the formulas below to calculate the target output current, $I_{OUT, GCG}$,

$$IOUT_{GCG} = \frac{1}{REXT} * 0.556 * Gain1 * Gain2$$

$$Gain1 = (GCG[A:9])$$
$$Gain2 = GCG[8:6] * 14.3\%+1$$
$$Def.1.Set: GCG[A{\sim}6] = [01000]$$
$$ICG[9:0] = 127(Dec)$$

For your information, the output current is about 10mA when R_{EXT}=880Ω if Gain1 and Gain2 is set to default values.

GCG[A:6] in Global Configuration Register 2

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	GCG4	GCG3	GCG2	GCG1	GCG0	-	-	-	-	-	-

Bit A to 9 set coarse adjustment to current gain

GCG[A:9]-Code	[01]	[11]*
Gain1	15.875	47.625

* Default GCG[A:9]=[11]

Bit 8 to 6 set fine adjustment to current gain

GCG[8:6] -Code	[000]*	[001]	[010]	[011]	[100]	[101]	[110]	[111]
Gain2	1.000	1.144	1.288	1.432	1.576	1.720	1.864	2.008

* Default GCG[8:6]=[000]

R/G/B Individual Current Gain Adjustment

Definition of R/G/B Individual Configuration Register 1

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	0	0	0	0	ICG7	ICG6	ICG5	ICG4	ICG3	ICG2	ICG1	ICG0	0	0

When R/G/B individual current gain adjustment is applied, users can follow the below formulas to calculate the target output current $I_{OUT, ICG}$,

$$IOUT_{ICG} = IOUT_{GCG} * \frac{Code}{127}$$

Where smallest Code is 1.

The output current of R/G/B can be adjusted with individual current gain by 127 steps.

Package Power Dissipation (PD)

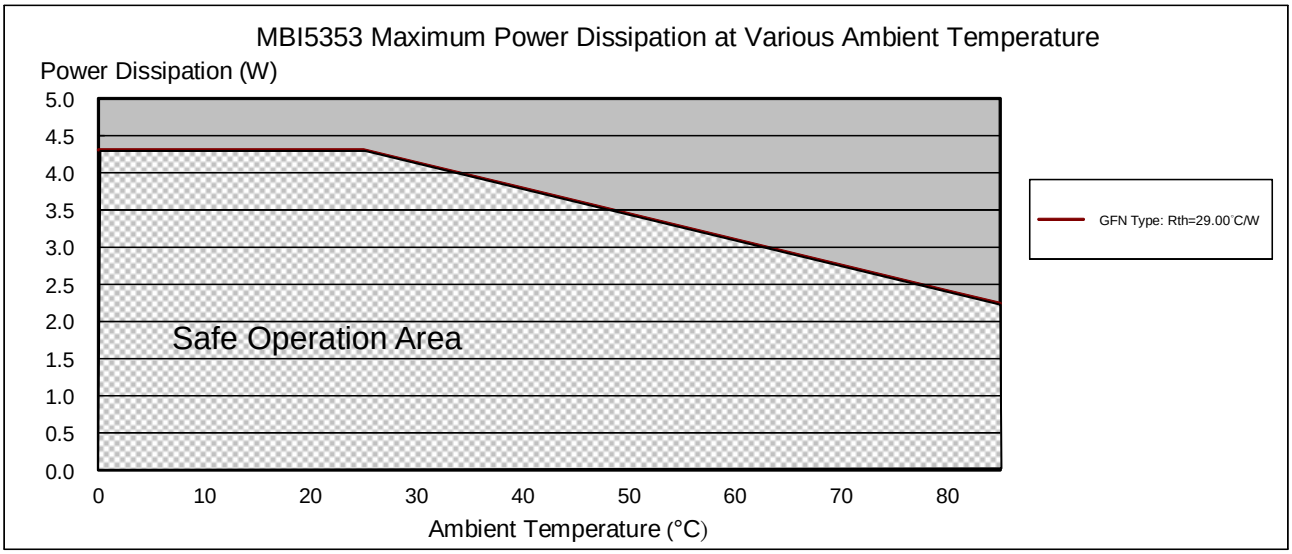
The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 48 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x48)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/48$, where Tj=150°C.

Please see the follow table for P_D and $R_{th(j-a)}$ for different packages:

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GFN	29	3.45

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.

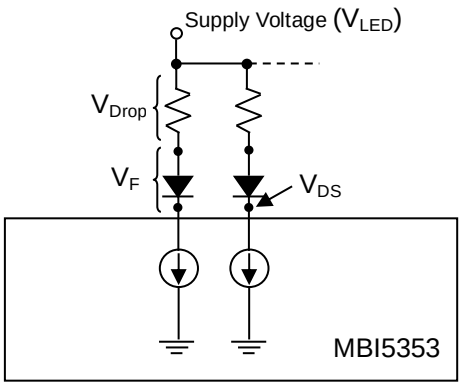


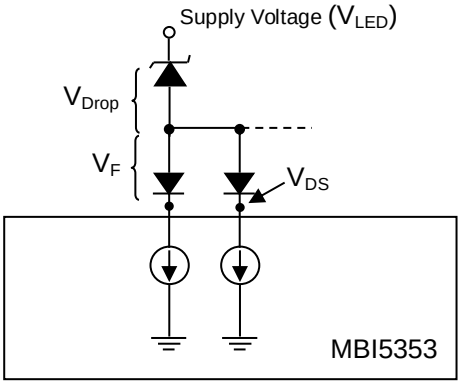
LED Supply Voltage (V_{LED})

MBI5353 is designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=0.5~20mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.





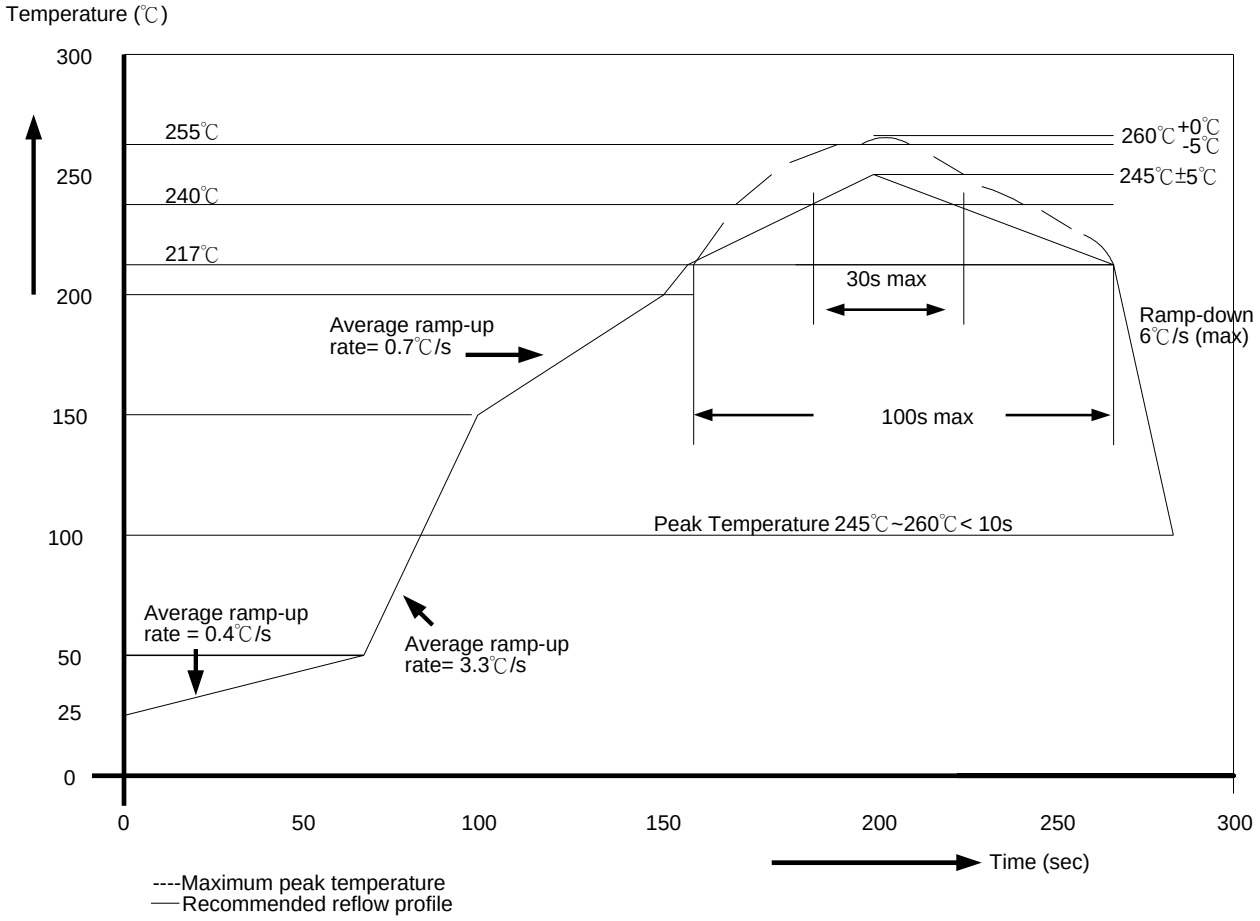
Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below. .

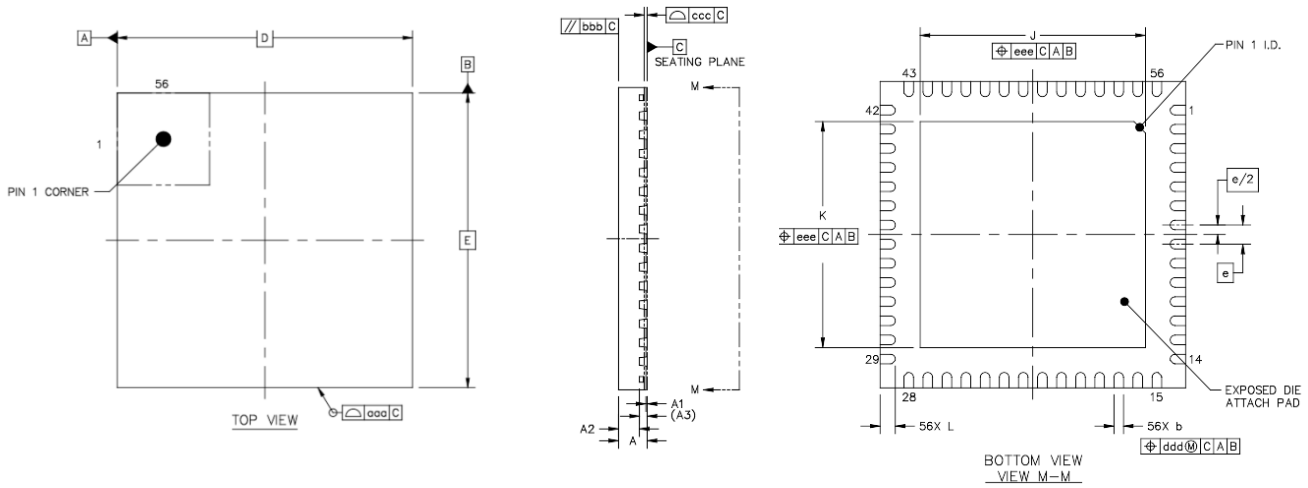
For managing MSL3 Package, it should refer to JEDEC J-STD-020C about floor life management & refer to JEDEC J-STD-033C about re-bake condition while IC's floor life exceeds MSL3 limitation.



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline

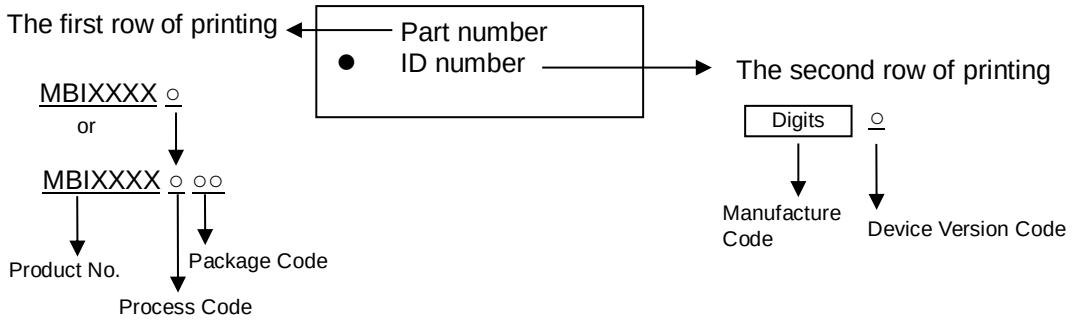


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.85	5.9	5.95
	Y	K	5.85	5.9	5.95
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

MBI5353GFN Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top Mark Information



Product Revision History

Advance Information Version	Devise Version Code
V1.01	B

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5353GFN-B	QFN56L-8*8-0.5	0.15885

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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