Computer Architecture

Final-Term Exam (2/4/2024)

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Place for submission: The submission form in Google Classroom

In this problem, we will look at how variations on Tomasulo algorithm perform when running the loop shown below. (This loop is the so-called DAXPY.)

```
        DADDIU  R4,R1,#800     ; R1 = upper bound for X
Foo:    L.D     F2,0(R1)       ; F2 = X(i)
        MUL.D   F4,F2,F0       ; F4 = a*X(i)
        L.D     F6,0(R2)       ; F6 = Y(i)
        ADD.D   F6,F4,F6       ; F6 = a*X(i) + Y(i)
        S.D     F6,0(R2)       ; Y(i) = a*X(i) + Y(i)
        DADDIU  R1,R1,#8       ; increment X index
        DADDIU  R2,R2,#8       ; increment Y index
        DSLTU   R3,R1,R4       ; test: continue loop?
        BNEZ    R3,foo         ; jump to “Foo” if needed
```

The functional units (FUs) are described in the table below.

FU type	Cycles in EX	Number of FUs	Number of reservation stations
Integer	1	1	5
FP adder	10	1	3
FP multiplier	15	1	2

Assume the followings:

- ✧ Functional units are not pipelined.
- ✧ There is no forwarding between functional units; results are communicated by the common data bus (CDB)
- ✧ The execution stage (EX) does both the effective address calculation and the memory access for loads and stores. Thus, the pipeline is fetch/decode/issue/execute/writeback.

- ✧ Loads require one clock cycle.
- ✧ Each of the issue and writeback stages requires one clock cycles.
- ✧ There are five load buffer slots and five store buffer slots.
- ✧ Assume that the branch on not equal to zero (BNEZ) instruction requires one clock cycle.

Problem:

(a) In a single-issue MIPS pipeline by Tomasulo algorithm, how many cycles does each loop iteration take? Show the number of stall cycles for each instruction and what a clock cycle each instruction begins execution (i.e., enters its first EX stage) for three iterations of the loop. Report your answer in the form of a table with the following column headers (See also Slide 55 of Chapter 5):

- ✧ Iteration (loop iteration number)
- ✧ Instruction
- ✧ Issues (cycle when instruction issues)
- ✧ Executes (cycle when instruction executes)
- ✧ Memory access (cycle when memory is accessed)
- ✧ Write CDB (cycle when a result is written to CDB)
- ✧ Comment (description of any event on which the instruction is waiting)

Show three iterations of the loop in your table. You may ignore the first instruction.

(b) This time assumes a two-issue pipeline by Tomasulo algorithm and a fully pipelined floating-point unit. In this case, how many cycles does each loop iteration take? Report your answer in the same form of Problem (a).

(c) Tomasulo algorithm has a disadvantage: Only one result can compute per clock per CDB. Find a code sequence of no more than 10 instructions where Tomasulo algorithm must stall due to CDB contention. Indicate where this occurs in your sequence.

(d) Show the loop code after applying the register renaming. You may use new registers for renaming floating-point registers (fp0, fp1, fp2, ⋯) and integer registers (rp0, rp1, rp2, ⋯) and do not need to consider the limit of the number of renaming registers.