



* Assignment No. 2 *

Q.1] Explain different addressing modes of 8086 microprocessor

- i) The way of specifying data to be operated by an instruction is known as addressing mode.
- ii) This specifies that the given data is an immediate data or an address.
- iii) Types of addressing mode are:-

a) Register mode:- In this type of addressing mode both the operands are registers.

e.g:- MOV Ax, Bx
 XOR Ax, Dx.

b) Immediate mode:- In this type of addressing mode the source operand is 8-bit or 16-bit data. Destination operand can never be immediate data.

e.g:- MOV Ax, 2000
 AD AL, 45.

c) Displacement / Direct mode:- In this type of addressing mode the effective address is directly given in the instruction as displacement.

e.g:- MOV Ax, [DISP]
 MOV Ax, [0500]



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d) Register Indirect mode:- In this addressing mode the effective address is in SI, DI
or BX.

e.g:-

MOV AX, [DI]

MOV AL, [BX]

e) Based Indexed mode:- In this the effective address is sum of based register and index register.

e.g:- Base register: BX, BP.

Index register :- SI, DI

e.g:- MOV AL, [BP+SI]

MOV AX, [BX + DI]

f) Indexed mode:- In this type of addressing mode the effective address is sum of index register and displacement.

e.g.: MOV AX, [SI + 2000]

MOV AL, [DI + 3000]



(Q2)

Explain the following instructions.

i) DAA : (Decimal adjust after addition)

Decimal adjust after addition it works only on AL register.

- It is used when we want to perform addition of two decimal number (BCD addition)

- We first enter the two decimal numbers. We add them using a normal ADD instruction.

- Then we perform DAA instruction. DAA will adjust the addition to appear as a decimal addition.

- The logic of DAA is as follows:-
if the lower nibble of AL is > 9 or Auxiliary flag is '1' then add 60 to AL.

- if the higher nibble of AL is > 9 or Carry flag is '1' then add 60 to AL.

ii) AAA :- [ASCII Adjust for addition]

- It makes the result is unpacked BCD form.

- In ASCII codes 0....9 are represented as 30....39.

- When we add ASCII codes. we need to mask the higher byte.

- This can be avoided if we use AAA instruction. after the addition is performed.

- AAA updates the AF & the CF; But OF, PF, SF, ZF are undefined after instruction.

iii) XLAT:-

- Here, we can specify the name of look-up table in the instruction.



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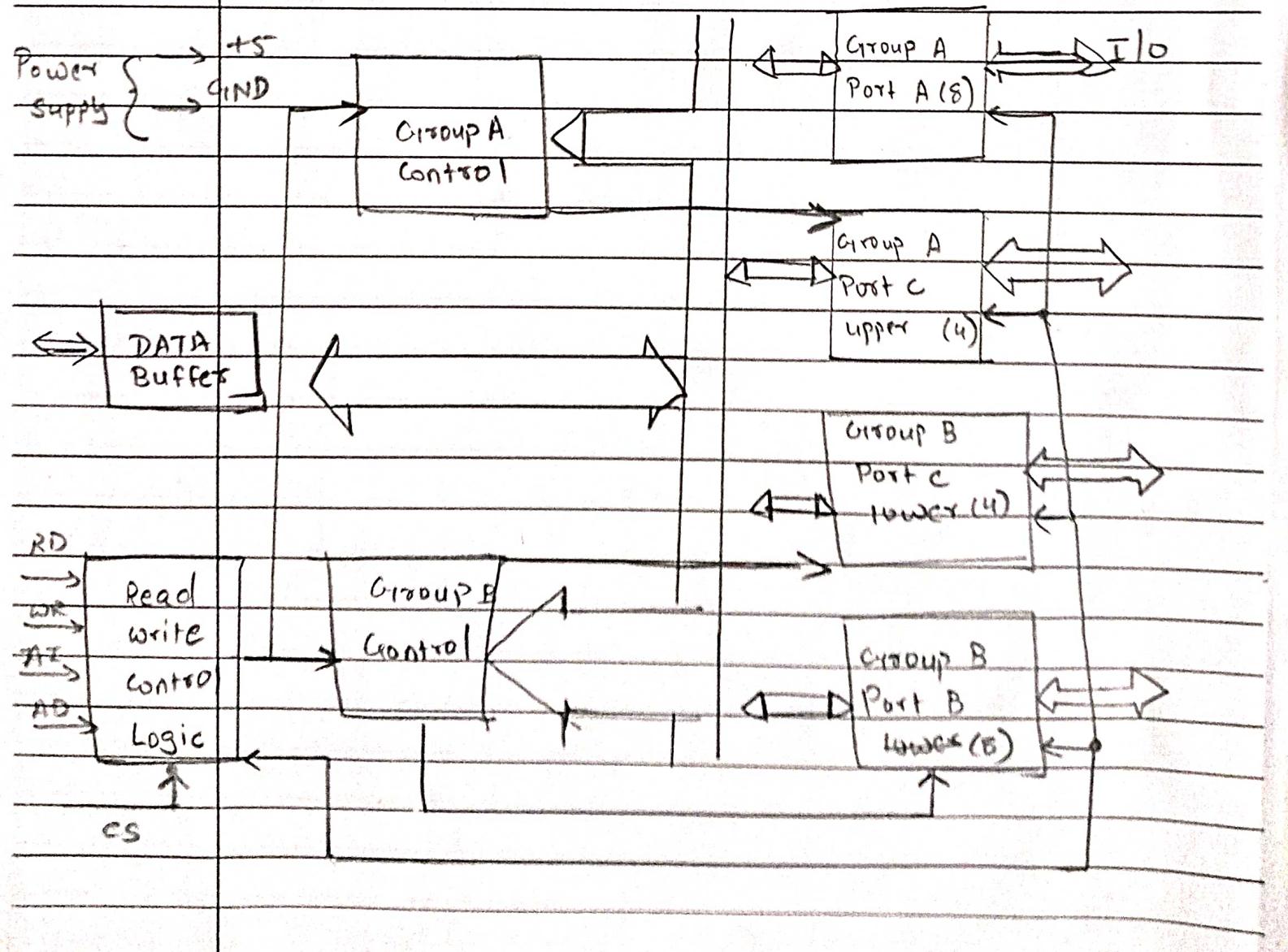
- This will do the translation from the look up table called reverse seg.
 - In any case, the base address of the lookup table must be given by BX.
 - XLAT replaces a byte in AL register with a byte 256 byte lookup table beginning at [BX].
- (iv) LAHF :-
- This instruction copies the values of SF, ZF, AF, PF and CF into bits of 7, 6, 4, 2, 0 respectively of AH register. This instruction was provided to make conversion of assembly language program written for 8080 and 8085 to 8086 easier.
 - It loads AH with lower bytes of the flag register.



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Q5] Explain PPI 8255 with block diagram. [10]

- i) PPI 8255 is a general purpose programmable I/O device designed to interface the CPU with its outside world such as ADC, DAC, keyboard, etc.
- ii) We can program it according to the given condition.
- iii) It can be used with almost any microprocessor.
- iv) It consists of three 8-bit bidirectional I/O ports i.e. PORT A, PORT B, and PORT C
- v) Block diagram for PPI 8255 is:-





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- ii) It consists of 40 pins and operates in +5V regulated power supply.
- vii) Port C is further divided into 4-bit ports i.e. port C lower and port C upper.
- viii) Port B can work in either mode 0 or mode 1 of input - output mode.
- ix) Port A can work in mode 0, mode 1 or mode 2 of input - output mode.



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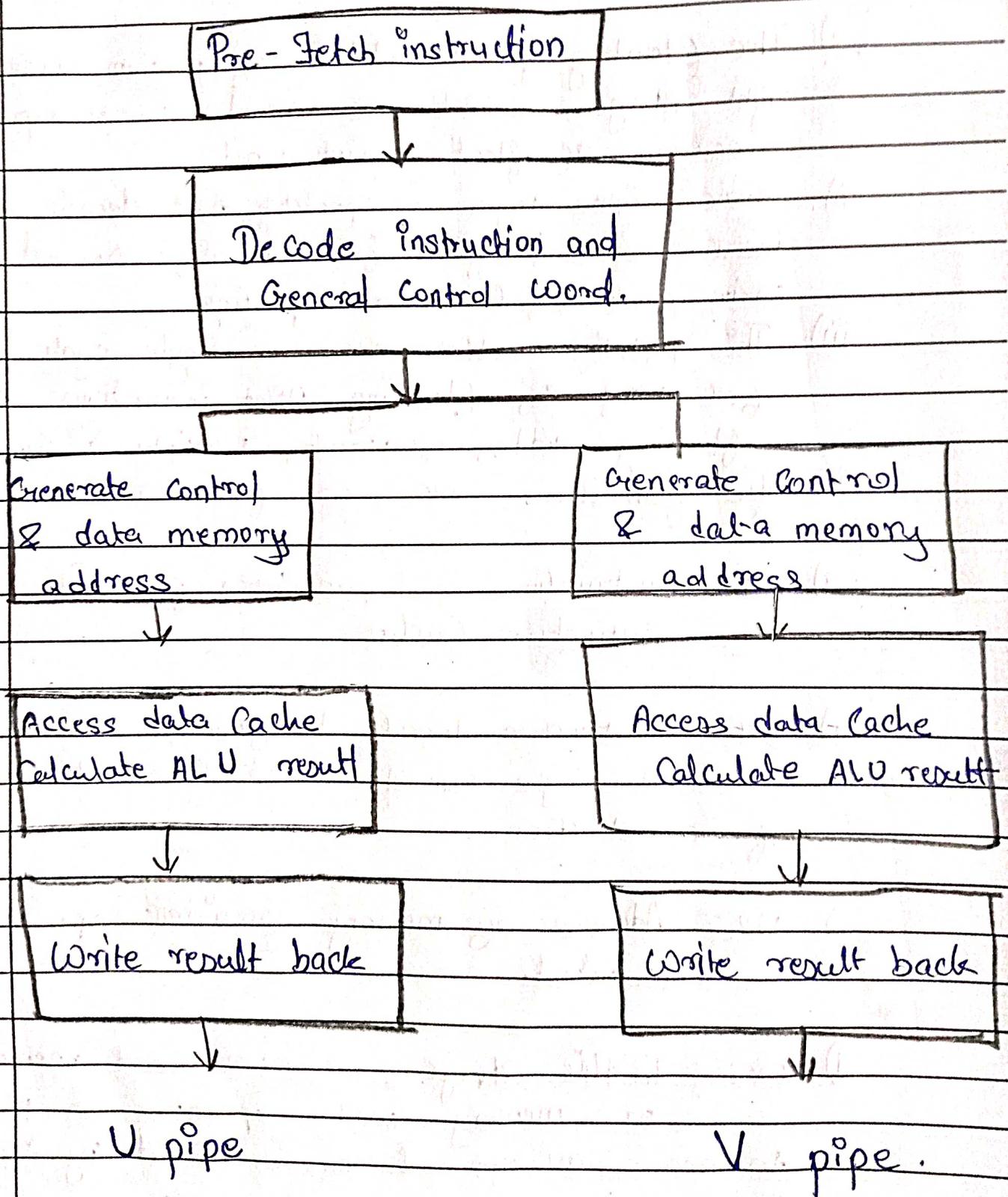
Q6] Draw and explain floating point pipeline for pentium processor.

- i) The floating point pipeline of pentium consist of eight stages which are used to speedup the execution of floating point unit.
- ii) These eight stages are prefetch, first decode, second decode, operand fetch, first execute, second execute, write float and error reporting.
- iii) This pipeline which gives a single cycle execution for many of floating point instructions such as floating adds, subtract, multiply & compare.
- iv) The functions are as follows:
 - a) PF: Instruction are prefetched from the On chip Instruction Cache.
 - b) D1: Instruction decode to generate control word.
A single control word causes direct execution of an instruction.
 - c) D2: Address of memory resident operand are calculated.
 - d) Ex: In this stage, register read, memory read or memory write operation is performed to access an operand as required by instruction.



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- v) The diagram for pipeline is as follows:-





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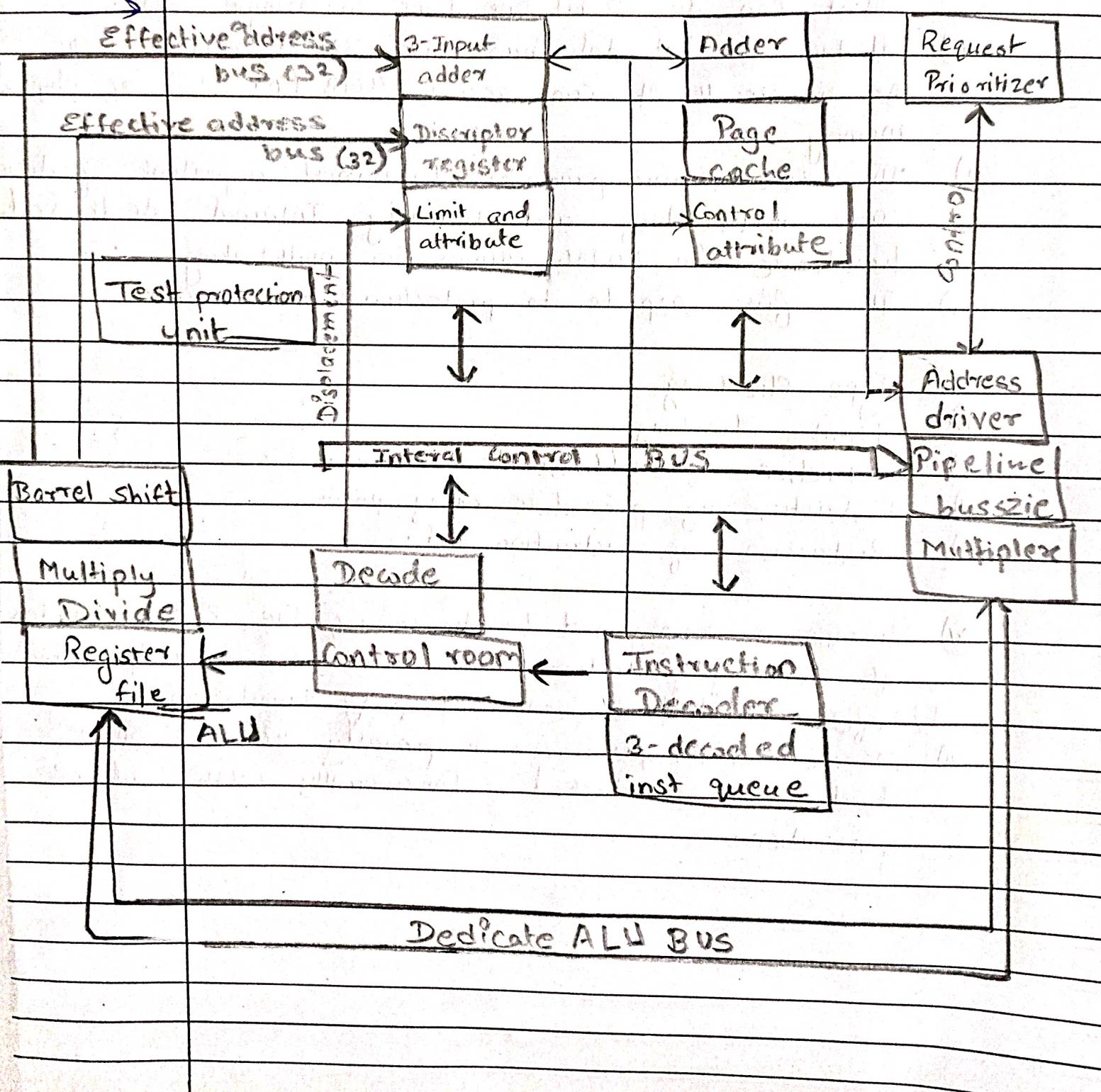
Q7] Discuss in brief protection mechanism of 80386 :-

- i) The 80386 microprocessor is 32-bit microprocessor that can do 32-bit operations in single cycle.
- ii) It has 32-bit data bus and 32-bit address bus. As a result it can access 4 GiB (or 2³²) of physical memory.
- iii) The 80386 microprocessor's two most important features are multitasking and security. Internal dedicated hardware in 80386 allows for multitasking.
- iv) The five aspects to protection in 80386:-
 - a) Type Checking
 - b) Limit Checking
 - c) Restriction of addressable domain.
 - d) Restriction of procedure entry points.
 - e) Restriction of instruction set.
- v) The memory management hardware of the 80386 includes the memory protection circuitry. The term "protection" refers to both segment and page translation.
- vi) There is no performance penalty because the checks are conducted concurrently with address generation.



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Q8. Draw and explain architecture of 80386.





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i) The internal architecture of 80386 is divided into 3 sections.

Q) Central processing unit (CPU)

- Execution unit.
- Instruction unit.

b) Memory management unit (MMU)

- Segmentation unit.
- Paging unit.

c) Bus interface unit (BIU)

Central processing unit (CPU)

- i) Execution unit :- Reads the instruction from the instruction queue and execute the instruction. Consist of three subunits : control, data, protection unit.
- ii) Control unit contains microcode and special hardware allows processor to reduce time required for execution of multiply & divide instruction.
- iii) Data unit is responsible for data operation requested by the control unit. It contains ALU, eight 32 bit general purpose register and 64 bit shifted.
- iv) Protection unit checks for segmentation violation under the control of microcode.
- v) Instruction decode unit takes instruction byte



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from code prefetch queue and translates them into microcode. The decoded instruction are stored in the queue.

- vi) Bus Control unit is the 80386 communication with outside world. It provide a full 32 bit bidirectional data and 32-bit address bus. Responsible for following operations.

Q. 9. Explain memory management in details in 80386 processor.

→ The memory management in 80386, has two separate units in itself.

- a) Segmentation unit.
- b) Paging unit.

- i) Segmentation unit plays a vital role in the 80386 microprocessor. It offers a protection mechanism in order to protect the data or code present in memory from application programs.
- ii) Every information in the memory is assigned a privilege from PL0 to PL3. (PL0 highest priority & PL3 is lowest priority).
- iii) Paging unit unit operates only in protected mode and it changes the linear address into a physical address.
- iv) As the programer only provides the virtual address and not the physical address.

- v) The segmentation unit control the action of the Paging unit, as the Segmentation unit has the ability to convert the logical address into the linear address at the time of executing an instruction.
- vi) It allows handling of tasks in form of pages rather than segments.

Q10] Explain and Draw block diagram of pentium processor.

→ Block diagram for pentium processor :-

