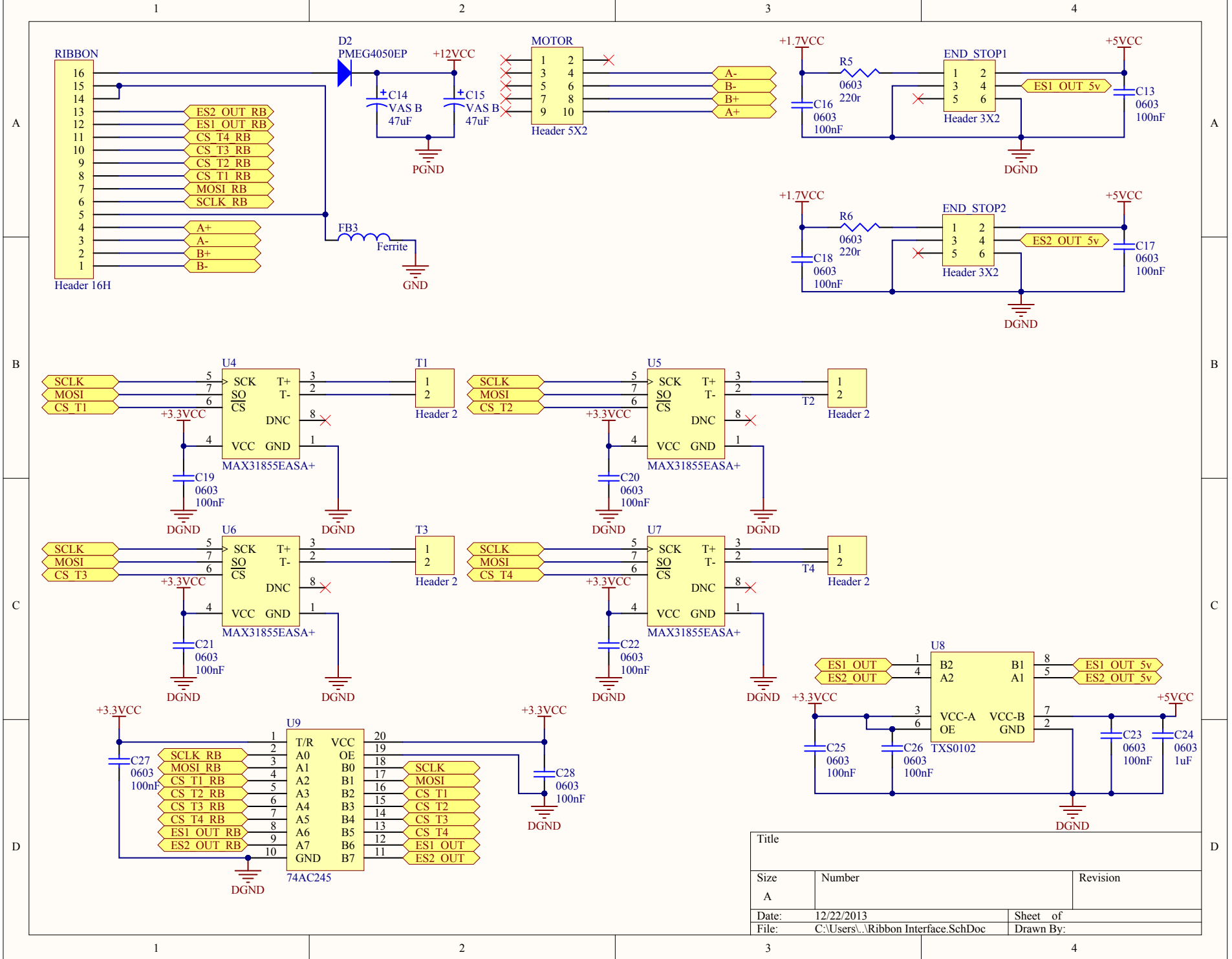
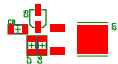
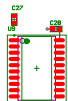


Title			
Size	Number		Revision
A			
Date:	12/22/2013		Sheet of
File:	C:\Users\...\Power.SchDoc		Drawn By:



Title		
Size	Number	Revision
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Date:	12/22/2013	Sheet of
File:	C:\Users\...\Ribbon Interface.SchDoc	Drawn By:



Bill of Materials

<Parameter Title not found>

Source Data From: Cavro Ribbon Interface.PrjPcb
 Project: Cavro Ribbon Interface.PrjPcb
 Variant: None

Creation Date: 12/22/2013 11:39:57 PM
 Print Date: 41630 41630.98612

Footprint	Comment	LibRef	Designator	Description	Quantity
Panasonic VS B	VAS B	Cap Pol1	C1, C5, C9, C14, C15	Polarized Capacitor (Radial)	5
C1206	1206 Tantulum	Cap Semi	C2, C3, C4, C6, C7, C8, C10, C11, C12	Capacitor (Semiconductor SIM Model)	9
1608[0603]	0603	Cap Semi	C13, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28	Capacitor (Semiconductor SIM Model)	14
SM 0805 polarized	LED2	LED2	D1, D3	Typical RED, GREEN, YELLOW, AMBER GaAs LED	2
PMEG4050EP	PMEG4050EP	Diode	D2	Default Diode	1
HDR2X3	Header 3X2	Header 3X2	END_STOP1, END_STOP2	Header, 3-Pin, Dual row	2
SM 0805 - gap trimmed	Ferrite	Inductor	FB1, FB2, FB3	Inductor	3
HDR2X5	Header 5X2	Header 5X2	MOTOR	Header, 5-Pin, Dual row	1
SM 0805 - gap trimmed	Res3	Res3	R1, R2, R3, R4	Resistor	4
J1-0603	0603	Res3	R5, R6	Resistor	2
HDR1X16H	Header 16H	Header 16H	RIBBON	Header, 16-Pin, Right Angle	1
HDR1X2	Header 2	Header 2	T1, T2, T3, T4	Header, 2-Pin	4
TLV117112	TLV117113	TLV117112	U1	Linear Regulator	1
DPAK-3	LM7805-ST	LM708-ST	U2		1
	800ma	800ma			
TPS73101	TPS73101	TPS73101	U3	Ti TPS73101 Adjustable LDO	1
MAXM-S8+4_N	MAX31855EAS A+	MAX31855EAS A+	U4, U5, U6, U7	Cold Junction Compensated Thermocouple to Digital Converter, 14 Bits Temperature Resolution, -40 to 125 degC, 8-Pin SOIC (S8+4), Pb-Free	4
TXS0102	TXS0102	TXS0102	U8	TXS0102	1
74AC245	74AC245	74AC245	U9		1
					57

Approved	Notes