KOCAELI UNIVERSITY ENGINEERING FACULTY

CMOS Folded Cascode OTA Design

ANALOG CIRCUIT DESIGN ESSENTIALS

150208042 CETIN KAYA

130208079 Resul AKAYDIN

Depart:Electoronic and Communication Engineering

Advisor: Dr.Engin AFACAN

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1 Introduction

The evolution of the microelectronics industry is distinguished by the raising level of integration and complexity. It aims to decrease exponentially the minimum feature sizes used to design integrated circuits. The cost of design is a great problem to the continuation of this evolution. To fulfil the given requirements, the designer must choose the suitable circuit architecture. Designing high-performance baseband analog circuits is still a hard task toward reduced supply voltages and increased frequency. Our target is to design a Folded Cascode OTA that is cost-effective, low-size, highly efficient and can deliver the desired outputs within the restricted parameters given to us.

2 CIRCUIT AND INITIAL PARAMETERS

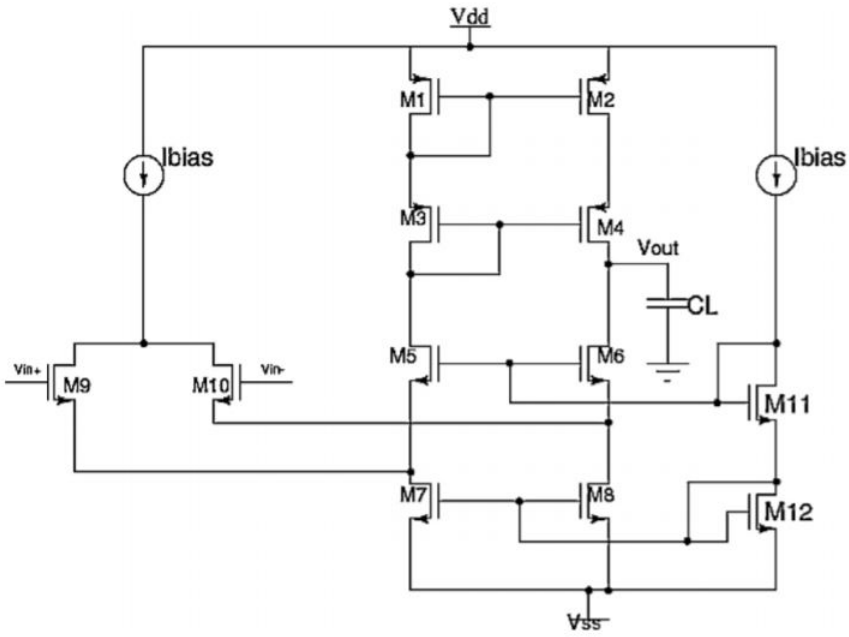

Figure 2.1: Reference circuit

Design Specifications and Constraints		
Technology node: 130nm	DC Gain$\geq 70dB$	CMRR $\geq 90dB$
Power Supply: 1.2V	Ft$\geq 10MHz$	PSRR $\geq 70dB$
0.12m$\leq L \leq 6m$	PM $\geq 60^{\circ}$	SR$\geq 50V/s$
0.16m$\leq W \leq 150m$	Power$\leq 0.5mW$	Input Offset$\leq 1mV$
Current Source: Basic Current Mirror	PArea$\leq 1500\mu^2 m$	Cload=1pF

Table 1.1: Initial parameters

3 THEORETICAL CALCULATION

Element	M2	M4	M6	M1
Model Name	PFET	PFET	NFET	PFET
region	Cutoff	Cutoff	Saturation	Cutoff
id	-2.0305e-005	-2.0305e-005	2.0305e-005	-2.0305e-005
ibs	-0.0000e+000	-0.0000e+000	0.0000e+000	-0.0000e+000
ibd	5.5458e-017	5.5458e-017	-1.4464e-016	5.5458e-017
vgs	-4.1260e-001	-4.1260e-001	3.3079e-001	-4.1260e-001
vds	-4.1260e-001	-4.1260e-001	1.1206e+000	-4.1260e-001
vbs	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000
vth	-2.6312e-001	-2.6312e-001	2.3567e-001	-2.6312e-001
vdsat	-1.4594e-001	-1.4594e-001	1.2299e-001	-1.4594e-001
beta	1.8697e-003	1.8697e-003	2.9938e-003	1.8697e-003
gam eff	4.6252e-001	4.6252e-001	4.1025e-001	4.6252e-001
gm	2.2645e-004	2.2645e-004	2.9331e-004	2.2645e-004
gds	7.5225e-007	7.5225e-007	2.2451e-006	7.5225e-007
gmb	4.7108e-005	4.7108e-005	3.9304e-005	4.7108e-005
cdtot	2.6715e-014	2.6715e-014	5.5393e-015	2.6715e-014
cgtot	3.2262e-013	3.2262e-013	1.0329e-013	3.2262e-013
cstot	3.3249e-013	3.3249e-013	1.0285e-013	3.3249e-013
cbtot	1.0697e-013	1.0697e-013	2.7828e-014	1.0697e-013
cgs	2.9791e-013	2.9791e-013	9.2230e-014	2.9791e-013
cgd	8.6629e-015	8.6629e-015	2.6140e-015	8.6629e-015

Element	M11	M12	M3	M5
Model Name	NFET	NFET	PFET	NFET
region	Saturation	Saturation	Cutoff	Saturation
id	4.0000e-005	4.0000e-005	-2.0305e-005	2.0305e-005
ibs	0.0000e+000	0.0000e+000	-0.0000e+000	0.0000e+000
ibd	-1.4464e-016	-1.4464e-016	5.5458e-017	-1.4464e-016
vgs	3.9250e-001	3.9250e-001	-4.1260e-001	3.3079e-001
vds	3.9250e-001	3.9250e-001	-4.1260e-001	1.1206e+000
vbs	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000
vth	2.3567e-001	2.3567e-001	-2.6312e-001	2.3567e-001
vdsat	1.7032e-001	1.7032e-001	-1.4594e-001	1.2299e-001
beta	2.9461e-003	2.9461e-003	1.8697e-003	2.9938e-003
gam eff	4.1025e-001	4.1025e-001	4.6252e-001	4.1025e-001
gm	4.1828e-004	4.1828e-004	2.2645e-004	2.9331e-004
gds	5.1367e-006	5.1367e-006	7.5225e-007	2.2451e-006
gmb	5.5894e-005	5.5894e-005	4.7108e-005	3.9304e-005
cdtot	6.8630e-015	6.8630e-015	2.6715e-014	5.5393e-015
cgtot	1.0911e-013	1.0911e-013	3.2262e-013	1.0329e-013
cstot	1.0837e-013	1.0837e-013	3.3249e-013	1.0285e-013
cbtot	2.8305e-014	2.8305e-014	1.0697e-013	2.7828e-014
cgs	9.8894e-014	9.8894e-014	2.9791e-013	9.2230e-014
cgd	2.8333e-015	2.8333e-015	8.6629e-015	2.6140e-015

Element	M9	M8	M10	M7
Model Name	PFET	NFET	PFET	NFET
region	Cutoff	Saturation	Cutoff	Saturation
id	-2.0000e-005	4.0305e-005	-2.0000e-005	4.0305e-005
ibs	-0.0000e+000	0.0000e+000	-0.0000e+000	0.0000e+000
ibd	1.0736e-016	-1.4464e-016	1.0736e-016	-1.4464e-016
vgs	-3.5641e-001	3.9250e-001	-3.5641e-001	3.9250e-001
vds	-1.9022e+000	4.5421e-001	-1.9022e+000	4.5421e-001
vbs	0.0000e+000	0.0000e+000	0.0000e+000	0.0000e+000
vth	-2.6317e-001	2.3567e-001	-2.6317e-001	2.3567e-001
vdsat	-1.0655e-001	1.7032e-001	-1.0655e-001	1.7032e-001
beta	3.7202e-003	2.9461e-003	3.7202e-003	2.9461e-003
gam eff	4.6251e-001	4.1025e-001	4.6251e-001	4.1025e-001
gm	2.9892e-004	4.2138e-004	2.9892e-004	4.2138e-004
gds	8.1398e-007	4.7899e-006	8.1398e-007	4.7899e-006
gmb	6.2042e-005	5.6295e-005	6.2042e-005	5.6295e-005
cdtot	3.9515e-014	6.5601e-015	3.9515e-014	6.5601e-015
cgtot	5.7921e-013	1.0899e-013	5.7921e-013	1.0899e-013
cstot	5.9521e-013	1.0840e-013	5.9521e-013	1.0840e-013
cbtot	1.9949e-013	2.8185e-014	1.9949e-013	2.8185e-014
cgs	5.2040e-013	9.8856e-014	5.2040e-013	9.8856e-014
cgd	1.6278e-014	2.7452e-015	1.6278e-014	2.7452e-015

Figure 3.1: MOSFETS regions

Element	VIN+	VDD	VSS	VIN-
volts	8.0000e-001	1.2000e+000	-1.2000e+000	8.0000e-001
current	-1.1894e-014	-1.2061e-004	1.2061e-004	-1.1894e-014
power	9.5151e-015	1.4473e-004	1.4473e-004	9.5151e-015

Figure 3.2: Power consuption

$$Ft = \frac{Gm9}{2 * \pi * CL} \tag{1.1}$$

$$Ft = 48.979MHz \quad CL = 1pf \tag{1.2}$$

$$Gm9 = Ft * (2 * \pi * CL) \tag{1.3}$$

$$Gm9 = 3.07e-4 \tag{1.4}$$

The result of the hand calculation [Equation: 1.4] and the practical result [Figure: 3.1] were found to be almost the same.

4 GRAPHICAL RESULTS AND CONCLUSIONS

4.1 DC gain,Ft and PM

4.1.1 Netlist

```
*Analog Circuit Design Essentials

.INC 130nm.txt



M1 3 2 1 1 PFET W=27u L=1.5u
M2 2 2 1 1 PFET W=27u L=1.5u
M3 4 4 3 3 PFET W=27u L=1.5u
M4 5 4 2 2 PFET W=27u L=1.5u
M5 4 6 7 7 NFET W=9u L=1.5u
M6 5 6 8 8 NFET W=9u L=1.5u
M7 7 9 10 10 NFET W=9u L=1.5u
M8 8 9 10 10 NFET W=9u L=1.5u
M9 7 12 11 11 PFET W=52.5u L=1.5u
M10 8 13 11 11 PFET W=52.5u L=1.5u
M11 6 6 9 9 NFET W=9u L=1.5u
M12 9 9 10 10 NFET W=9u L=1.5u

VDD 1 GND DC 1.2V
VSS 10 GND DC -1.2V
CL 5 GND 1p
*Vin 12 0 0

Vin+ 12 GND DC 0.8V AC 1
Vin- 13 GND DC 0.8V AC 0

Ibias1 1 11 40u
Ibias2 1 6 40u
*Ibias3 16 1 13u
.AC dec 10 1 3000Meg
.tran 0.01u 1u
.OP
.options post


.end
```

Figure 4.1: DC gain and PM netlist

4.1.2 Graph

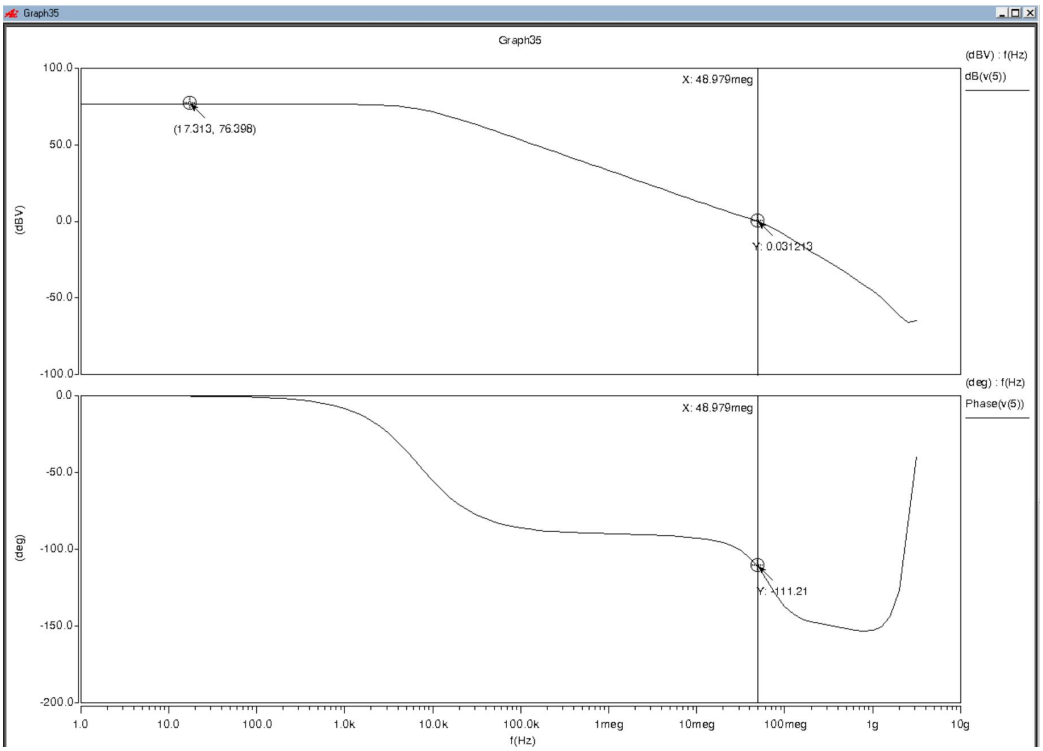

Figure 4.2: DC gain, Ft and PM graph

When we look at the graph, firstly the gain and pm results are suitable for the desired design parameters. It has been observed that changes in current, load capacitor and differential input voltage cause three related parameters to change.

4.2 CMRR

4.2.1 Netlist

```
*Analog Circuit Design Essentials

.INC 130nm.txt



M1 3 2 1 1 PFET W=27u L=1.5u
M2 2 2 1 1 PFET W=27u L=1.5u
M3 4 4 3 3 PFET W=27u L=1.5u
M4 5 4 2 2 PFET W=27u L=1.5u
M5 4 6 7 7 NFET W=9u L=1.5u
M6 5 6 8 8 NFET W=9u L=1.5u
M7 7 9 10 10 NFET W=9u L=1.5u
M8 8 9 10 10 NFET W=9u L=1.5u
M9 7 12 11 11 PFET W=52.5u L=1.5u
M10 8 12 11 11 PFET W=52.5u L=1.5u
M11 6 6 9 9 NFET W=9u L=1.5u
M12 9 9 10 10 NFET W=9u L=1.5u

*VDD 1 GND DC 1.2V
*VSS 10 GND DC -1.2V
CL 5 GND 1p
Vin 12 0 0.8V AC 1

*Vin+ 12 GND DC 0.8V AC 1
*Vin- 13 GND DC 0.8V AC 0

Ibias1 1 11 40u
Ibias2 1 6 40u
*Ibias3 16 1 13u
.AC dec 10 1 3000Meg
.tran 0.01u 1u
.OP
.options post


.end
```

Figure 4.3: CMRR netlist

4.2.2 Graph

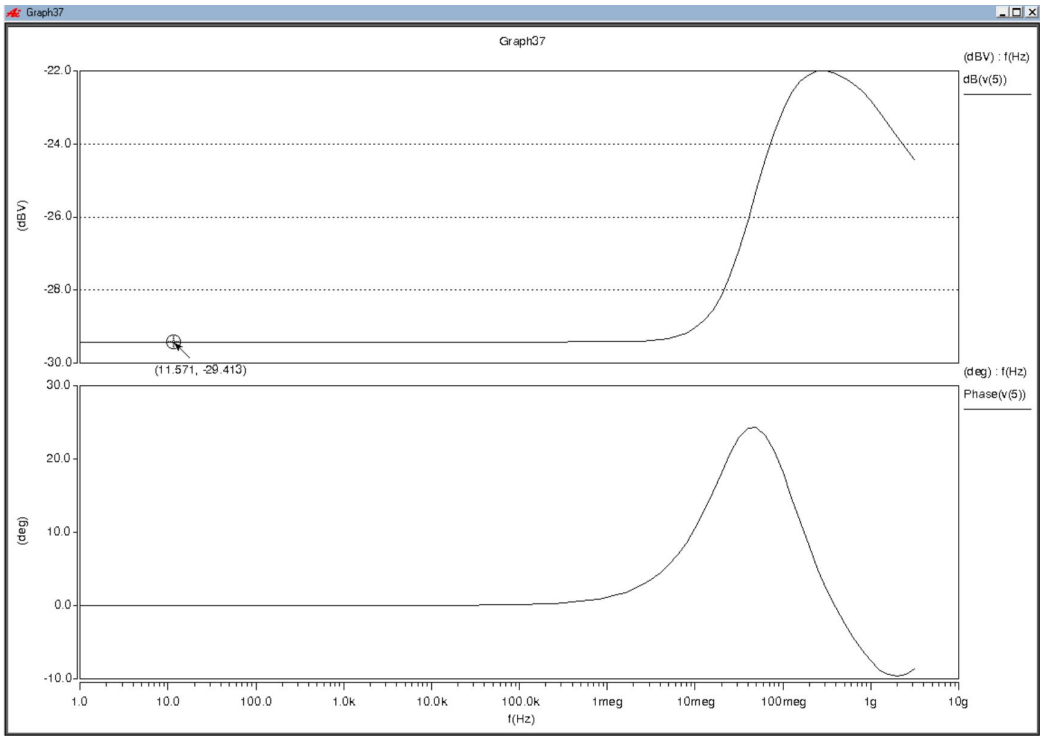

Figure 4.4: CMRR graph

Common mode response rate (CMRR) is the ability to reject them when the same signal is applied to both input terminals of an op-amp. This value is equal to the ratio of a signal applied simultaneously to the phase inverting and non-phase inverting input to the output signal. The unit of CMRR is dB (decibel). In order to observe this output in the circuit, the gates of the input MOSFETs are connected to each other and DC voltage and AC 1V source voltage are supplied and the circuit feeds are disabled. The node V5 on the output is checked. As it is understood from the netlist, the factors affecting CMRR graph appear to be Vin +, W and L values, Cl output capacity and bias currents. First of all, let's start by decreasing this value since we select Vin + maximum. When we decreased the Vin + value, no change in CMRR value was observed in the graph. The change

of total area did not cause any change in the CMRR graph. When we increased the Cl output capacity by 10 times, the CMRR increased approximately 2-fold. When we decreased 10 times, CMRR showed 4 times decrease. Thus, we can say that the capacity has a significant effect on the CMRR value. When we increase the bias currents by about 6 times, we can say that the CMRR value decreases by about 3 times.

4.3 PSRR

4.3.1 Netlist

```
*Analog Circuit Design Essentials


.INC 130nm.txt



M1 3 2 1 1 PFET W=27u L=1.5u
M2 2 2 1 1 PFET W=27u L=1.5u
M3 4 4 3 3 PFET W=27u L=1.5u
M4 5 4 2 2 PFET W=27u L=1.5u
M5 4 6 7 7 NFET W=9u L=1.5u
M6 5 6 8 8 NFET W=9u L=1.5u
M7 7 9 10 10 NFET W=9u L=1.5u
M8 8 9 10 10 NFET W=9u L=1.5u
M9 7 GND 11 11 PFET W=52.5u L=1.5u
M10 8 GND 11 11 PFET W=52.5u L=1.5u
M11 6 6 9 9 NFET W=9u L=1.5u
M12 9 9 10 10 NFET W=9u L=1.5u

VDD 1 GND AC 1

VSS 10 GND AC 0
CL 5 GND 1p
*Vin 12 0 0

*Vin+ 12 GND DC 0.8V AC 1
*Vin- 13 GND DC 0.8V AC 0

Ibias1 1 11 40u
Ibias2 1 6 40u
*Ibias3 16 1 13u
.AC dec 10 1 3000Meg
.tran 0.01u 1u
.OP
.options post


.end
```

Figure 4.5: PSRR netlist

4.3.2 Graph

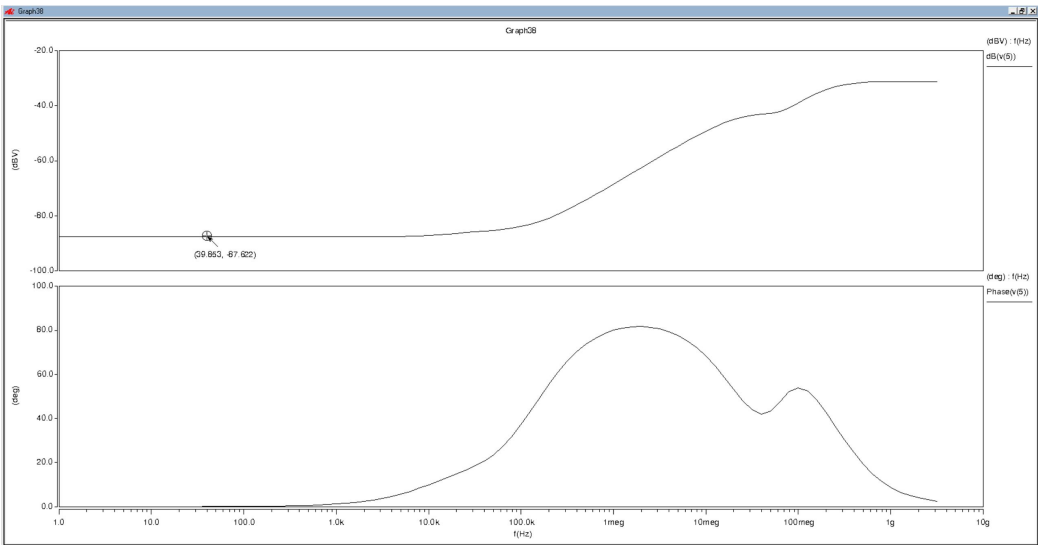

Figure 4.6: PSRR graph

PSRR is the ratio of the change in input offset voltage with respect to the change in power supply voltage. The standard used in the datasheet is DC Variation. PSRR=20log(Power Supply Variation)/(Input Offset Voltage Variation)[dB]. Generally, PSRR is frequency dependent, and decreases as the frequency increases.

In order to observe this output in the circuit, the gates of the input MOSFETs are made GND and only AC1V VSS from VDD, AC 0V is given. Vin inputs are disabled.

4.4 SR

4.4.1 Netlist

```
*Analog Circuit Design Essentials

.INC 130nm.txt



M1 3 2 1 1 PFET W=27u L=1.5u
M2 2 2 1 1 PFET W=27u L=1.5u
M3 4 4 3 3 PFET W=27u L=1.5u
M4 5 4 2 2 PFET W=27u L=1.5u
M5 4 6 7 7 NFET W=9u L=1.5u
M6 5 6 8 8 NFET W=9u L=1.5u
M7 7 9 10 10 NFET W=9u L=1.5u
M8 8 9 10 10 NFET W=9u L=1.5u
M9 7 12 11 11 PFET W=52.5u L=1.5u
M10 8 5 11 11 PFET W=52.5u L=1.5u
M11 6 6 9 9 NFET W=9u L=1.5u
M12 9 9 10 10 NFET W=9u L=1.5u

VDD 1 GND DC 1.2V
VSS 10 GND DC -1.2V
CL 5 GND 1p
Vin 12 0 pulse(0.01 0.8 0 0.1n 0.1n 499.0n 1u)

*Vin+ 12 GND DC 0.8V AC 1
*Vin- 13 GND DC 0.8V AC 0

Ibias1 1 11 40u
Ibias2 1 6 40u
*Ibias3 16 1 13u
.AC dec 10 1 3000Meg
.tran 0.01u 1u
.OP
.options post


.end
```

Figure 4.7: SR netlist

4.4.2 Graph

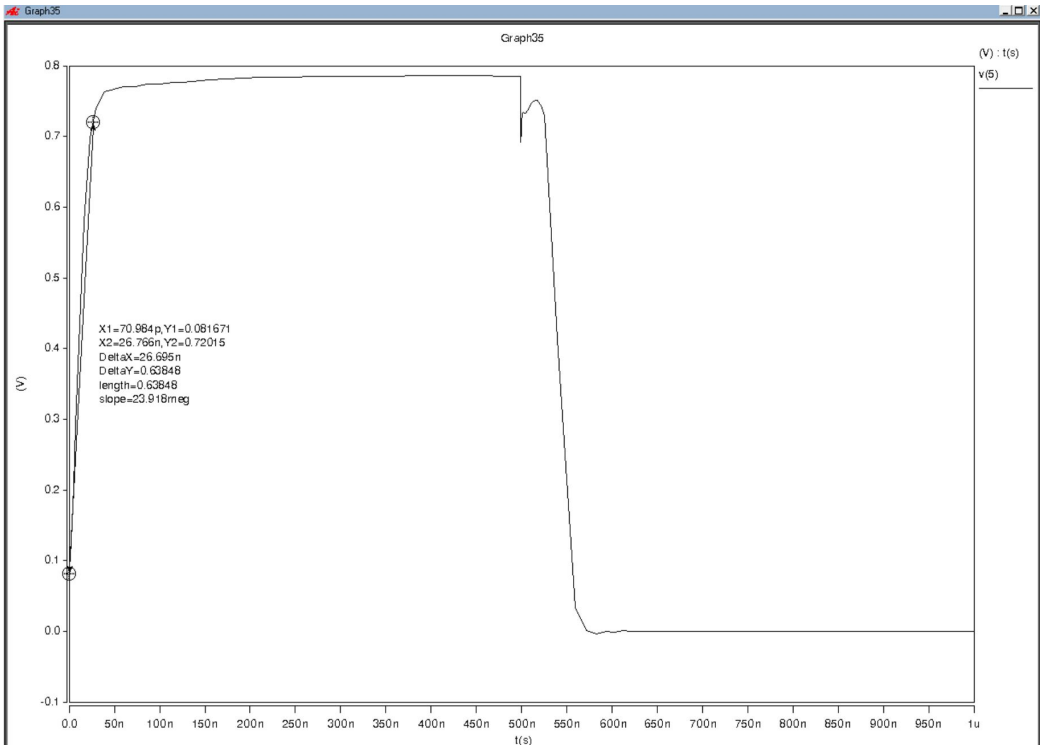

Figure 4.8: SR graph

Op amp slew rate limit the performance of op-amp based amplifiers and designs need to take account of this.

The output of an operational amplifier can only change by a certain amount in a given time. This limit is called the slew rate of the op-amp, and although slew rate is not often mentioned, it can be a critical factor in ensuring that an amplifier is able to provide an output that is a faithful representation of the input..

The gate of the Vin- is connected to the output. The Vin+ input is also given a square wave. to measure the slope of the voltage between the points 0.1 * Vdd and 0.9 * Vdd.

4.5 Input offset

4.5.1 Netlist

```
*Analog Circuit Design Essentials

.INC 130nm.txt



M1 3 2 1 1 PFET W=27u L=1.5u
M2 2 2 1 1 PFET W=27u L=1.5u
M3 4 4 3 3 PFET W=27u L=1.5u
M4 5 4 2 2 PFET W=27u L=1.5u
M5 4 6 7 7 NFET W=9u L=1.5u
M6 5 6 8 8 NFET W=9u L=1.5u
M7 7 9 10 10 NFET W=9u L=1.5u
M8 8 9 10 10 NFET W=9u L=1.5u
M9 7 12 11 11 PFET W=52.5u L=1.5u
M10 8 5 11 11 PFET W=52.5u L=1.5u
M11 6 6 9 9 NFET W=9u L=1.5u
M12 9 9 10 10 NFET W=9u L=1.5u

VDD 1 GND

VSS 10 GND
CL 5 GND 1p
Vin 12 0 0

*Vin+ 12 GND DC 0.8V AC 1
*Vin- 13 GND DC 0.8V AC 0

Ibias1 1 11 40u
Ibias2 1 6 40u
*Ibias3 16 1 13u
.AC dec 10 1 3000Meg
.tran 0.01u 1u
.OP
.options post


.end
```

Figure 4.9: Input offset netlist

4.5.2 Graph

Figure 4.10: Input offset graph

The input offset voltage is defined as the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output. Ideally the output of the op amp should be at zero volts when the inputs are grounded.

The negative input is connected to the output and no voltage is supplied to the circuit. Check the V5 node for the result.

5 GENERAL CONCLUSION

Design Parameters Results		
Technology node: 130nm	DC Gain=76.398 dB	CMRR = 105.811dB
Power Supply: 1.2V	Ft = 48.979Mhz	PSRR = 87.622dB
0.12m$\leq L \leq 6m$	PM = 68.79°	SR= 23.918 V/s
0.16m$\leq W \leq 150m$	Power$\leq 0.288mW$	Input Offset = 38.3mV
Current Source: Basic Current Mirror	PArea$\leq 400.5\mu^2m$	Cload=1pF
MOSFET W and L Values		
MOSFET	Wμm	L μm
M1	27	1.5
M2	27	1.5
M3	27	1.5
M4	27	1.5
M5	9	1.5
M6	9	1.5
M7	9	1.5
M8	9	1.5
M9	52.5	1.5
M10	52.5	1.5
M11	9	1.5
M12	9	1.5

Table 1.2: Result parameters and MOSFET dimensions

We have tried to design Folded Cascode OTA, which is our goal, cost effective, low size, highly efficient and capable of providing the best possible outputs within the limited parameters given to us. We encountered various difficulties in designing this circuit. Some of these challenges include making field adjustments, putting mosfets into the Saturation state and selecting the appropriate current. When we determined these variables in accordance with each other, we were able to obtain values close to the desired results. As a result, we designed the OTA we aimed and carried out their analysis.