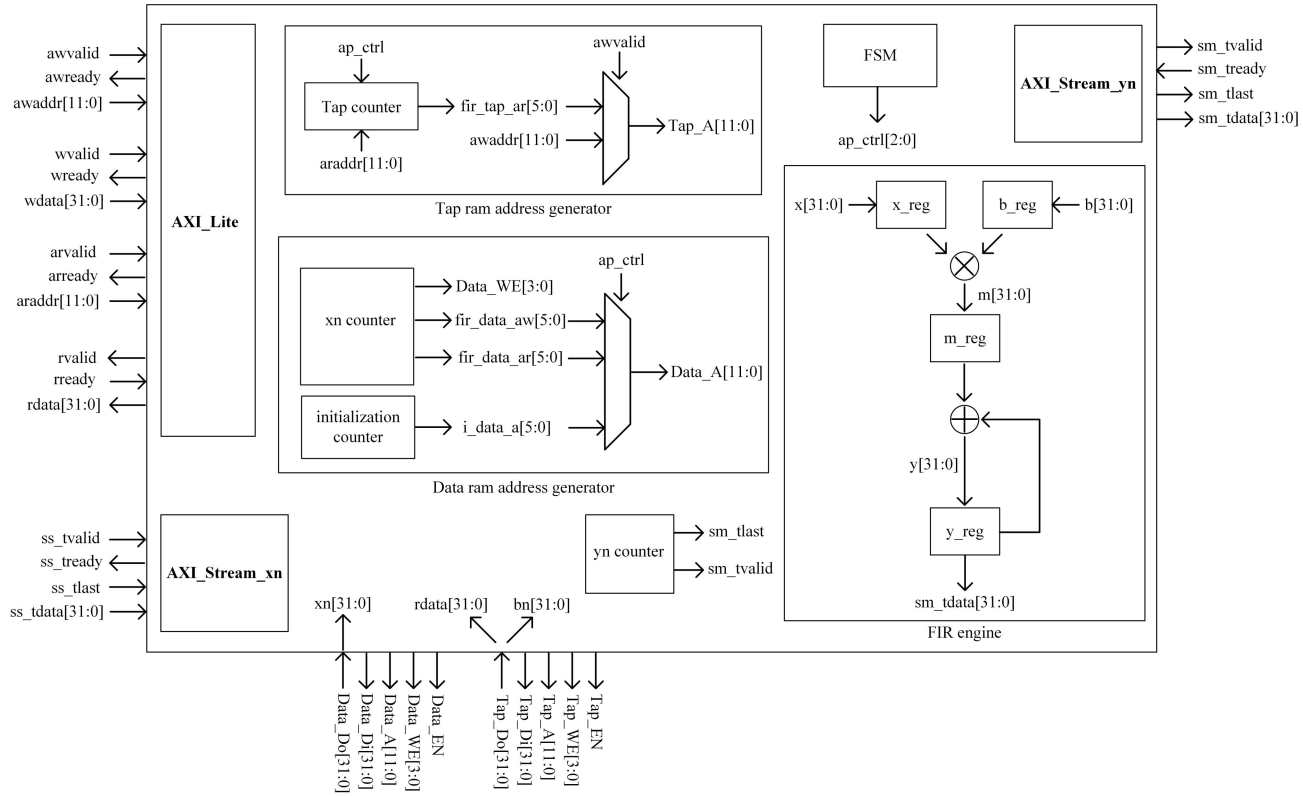
SOC Design

Lab3 FIR

21106974 SHEN Zijun

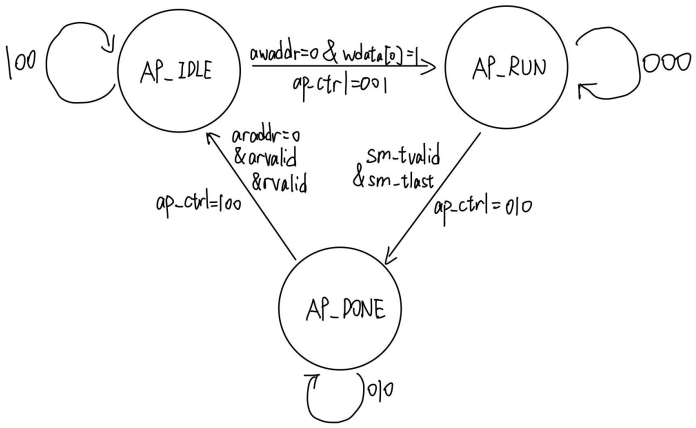
A. Block Diagram



The designed FIR contains 7 sub-blocks:

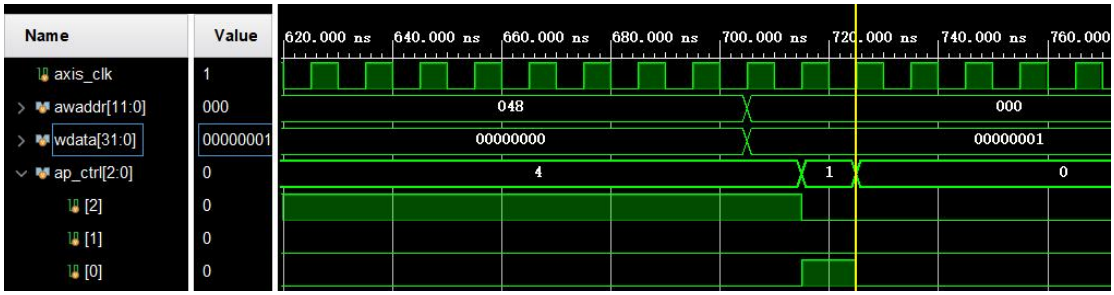
1. AXI_Lite interface between master and Tap_RAM
2. AXI_Stream interface between master and Data_RAM
3. AXI_Stream interface between master and output data Yn
4. Finite state machine to generate ap_ctrl signals to control other blocks
5. Tap_RAM read/write address generator/controller
6. Data_RAM read/write address generator/controller
7. FIR operation Engine

B. FSM design



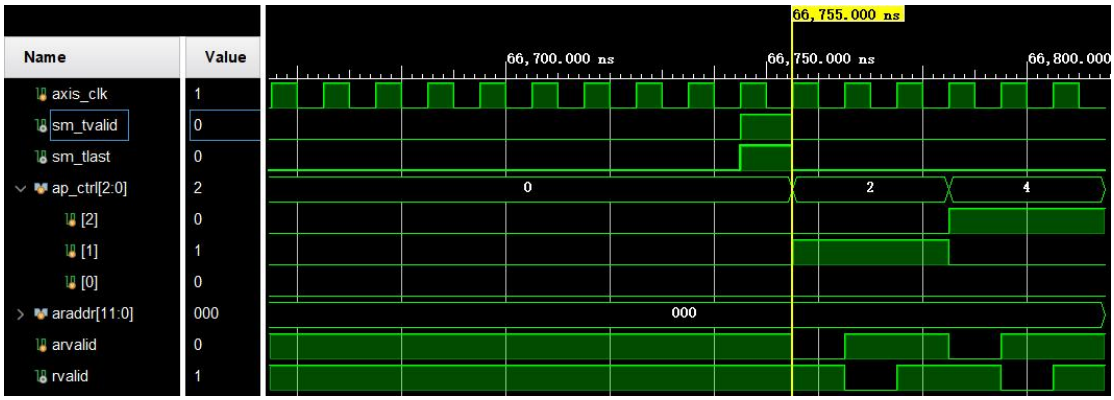
(1) At the beginning, master is executing configuration read/write to the Tap_RAM, so FIR engine is in AP_IDLE state (ap_ctrl=100)

(2) When configuration read/write is finished, awaddr will be programmed by master as 0x000 and wdata[0] will be programmed as 1, then FIR engine will turn to AP_RUN state, ap_ctrl will be programmed as 001 to indicate that FIR engine starts to process data.



(3) Then FIR engine will continuously process data, so it will hold at AP_RUN state and ap_ctrl=000 to indicate that FIR engine is not IDLE.

(4) Until the last Yn finish calculation and output through AXI_Stream to the master (when both sm_tvalid and sm_tlast rise up), then FIR engine will turn to AP_DONE state and ap_ctrl =010 to indicate that FIR engine finish processing data.

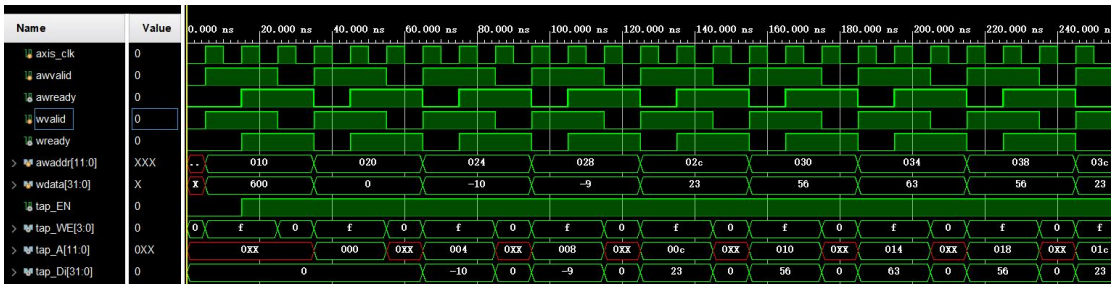


(5) After processing data, FIR engine will turn to AP_IDLE again. master will starts to enquire the state of FIR engine, araddr is 0x000. arvalid and rvalid are high. ap_ctrl will be programmed as 100 to indicate that FIR engine is in IDLE state.

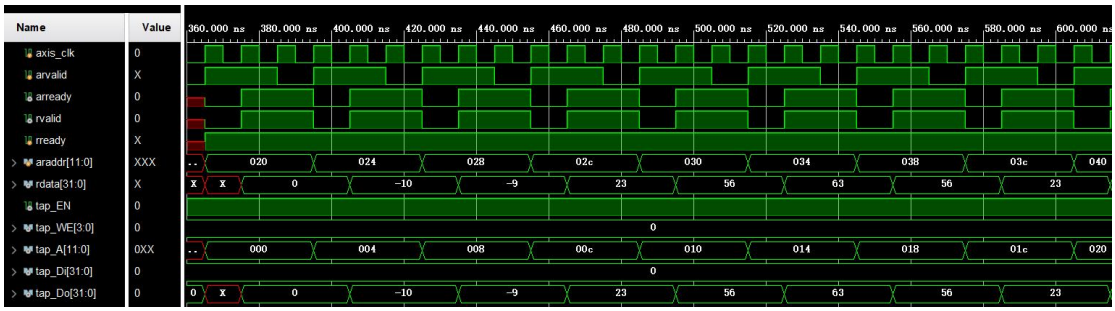
C. Operation Description

(1) AXI_Lite:

Configure write:



Configure read:

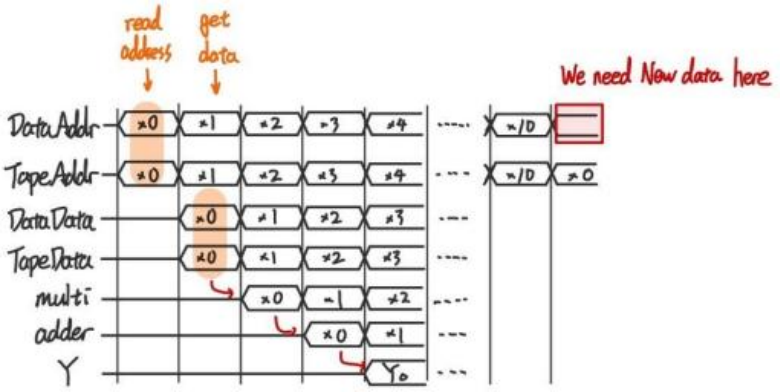


(2) AXI_Stream and fir operation:

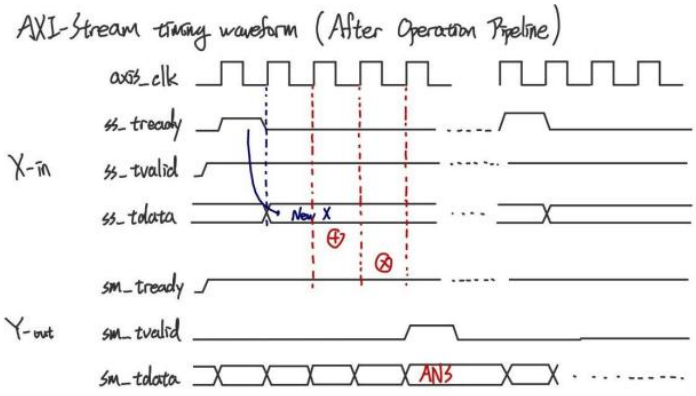
The Data RAM can only store 11 words.

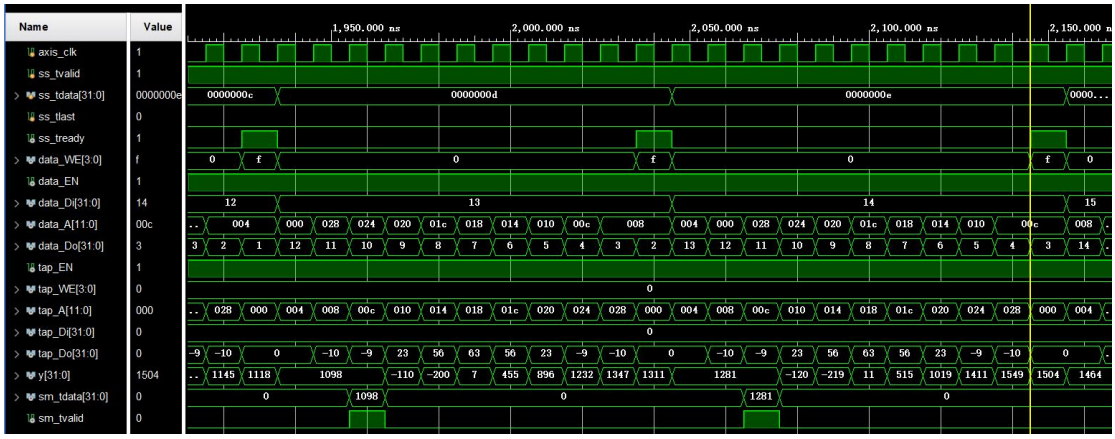
For Tap RAM, it reads out 11 tap numbers in sequence and then repeat in cycle.

For Data RAM, it needs to read out 11 numbers and write 1 new data in a cycle, the new data will wait at the input of the RAM until WE signal pull up, then write into the RAM. WE signal is controlled by the counter in the address generator.



For yn, as we use pipeline structure, it needs 3 cycles (read, add, multiply) to get the calculation result. The accumulation result will be sent to AXI_stream once each cycle. sm_tvalid and sm_tlast are controlled by 2 yn counter.





D. Resource usage

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
8	Yes	-	Set
215	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

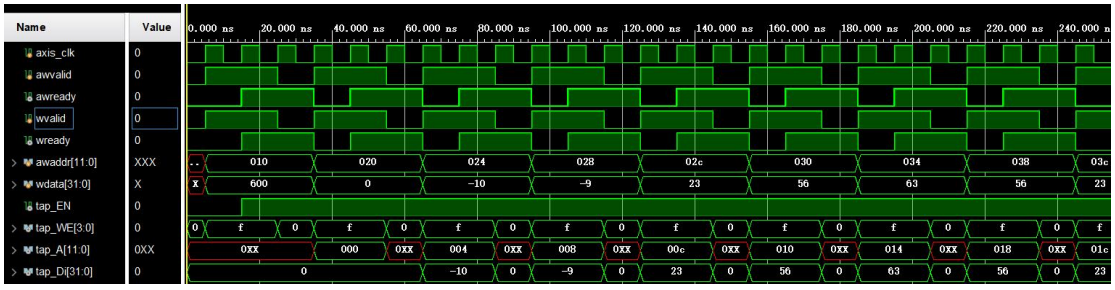
Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

E. Timing report

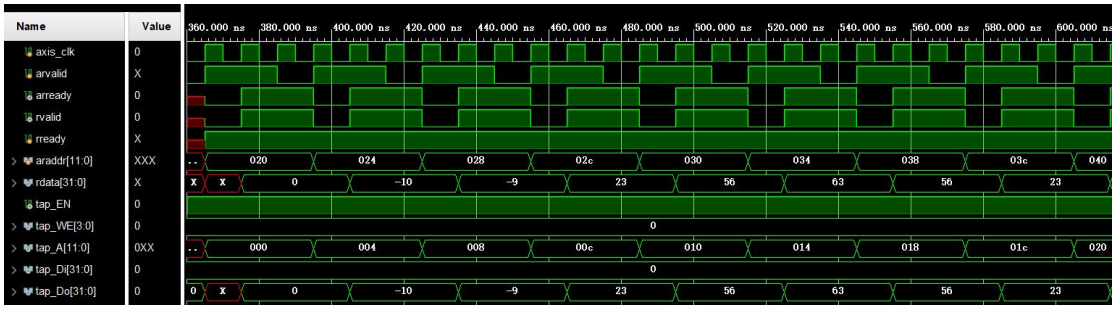
Attatched in github lab3/timing_report.txt

F. Simulation waveforms

Coefficient write:



Coefficient read:



Data in/out