EESM 6000C System on chip laboratory

Lab-3 FIR Report

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- **Function specification**

  • y[t] = Σ (h[i] * x[t - i])

  In signal processing, a finite-impulse-response, or finite impulse response models are generally linear dynamic models characterized by finite-order moving average representations, implying that their responses to impulse inputs go to zero after a finite number of time steps, equal to the model's memory length.

  FIR filters can be discrete-time or continuous-time, and digital or analog.

$$y[n] = b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N] = \sum_{i=0}^{N} b_i \cdot x[n-i],$$

  Where:

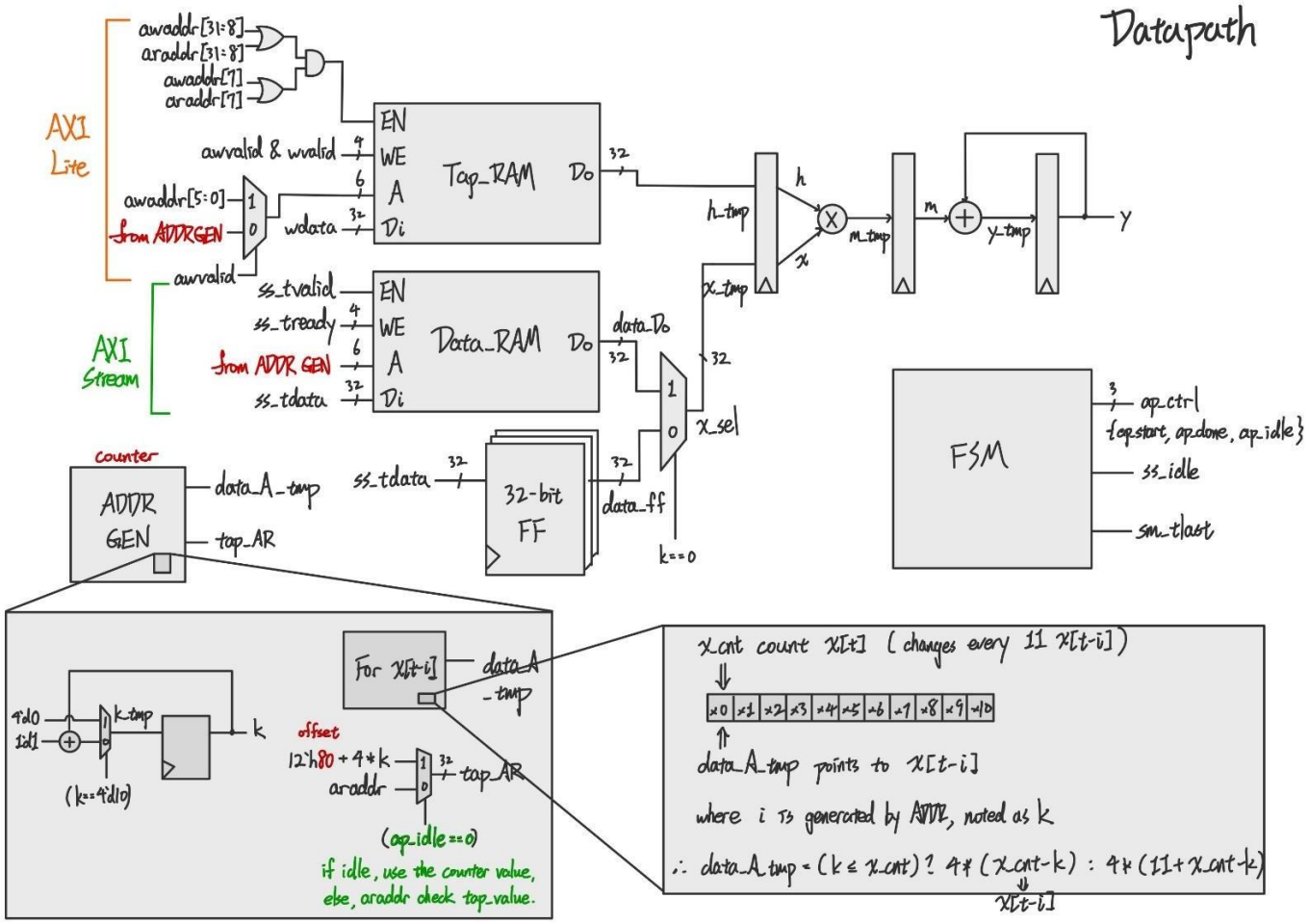
  . x[n] is the input signal,

  . y[n] is the output signal,

  . N is the filter order; an N_{th}-order filter has N + 1 terms on the right-hand side

  . b_i is the value of the impulse response at the i_{th} instant for 0 <= I <= N of an Nth-order FIR filter. If the filter is a direct form FIR filter, then b_i is also a coefficient of the filter.

- **Block Diagram**

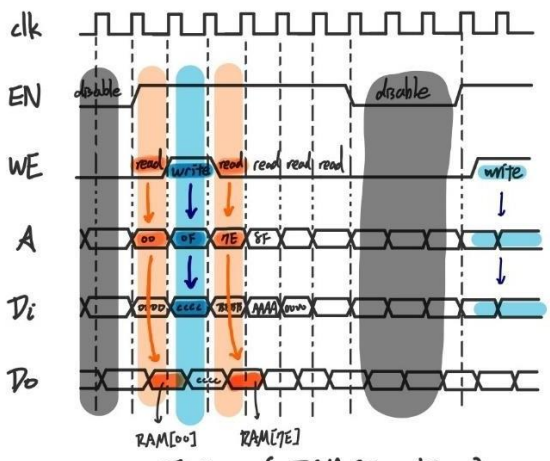


Tap_RAM / Data_RAM

32-bit ↔ 4 byte

reg [3:0] RAM [depth] ⇒ RAM [A>>2] (÷4)

A[10:0] → in order to access byte



Timing of RAM (Tape/Data)

TapeRAM:

Tape address: 8'b10000000 0x80 - 0xFF

EN = (AW[31:8] == 0) | (AR[31:8] == 0) & (AW[7] | AR[7])

Check if read/write address belongs to TapeRAM

WE = (AWvalid && Wvalid == 1) ? 4'b1111 : 4'b0000; Check if address/data write is valid

A = AW[5:0] AW will >>2, 4-bit left, still can represent the address of 11 tapes

Di = Wdata Data-in equals to wdata of AXI-Lite (h[i] flow through TapeRAM by axilite)

Awready = 1 (RAM 尚有空間)

wready = 1 (Data Buffer 尚有 space)

DataRAM:

EN = ss_tvalid (ss_tlast = 0)

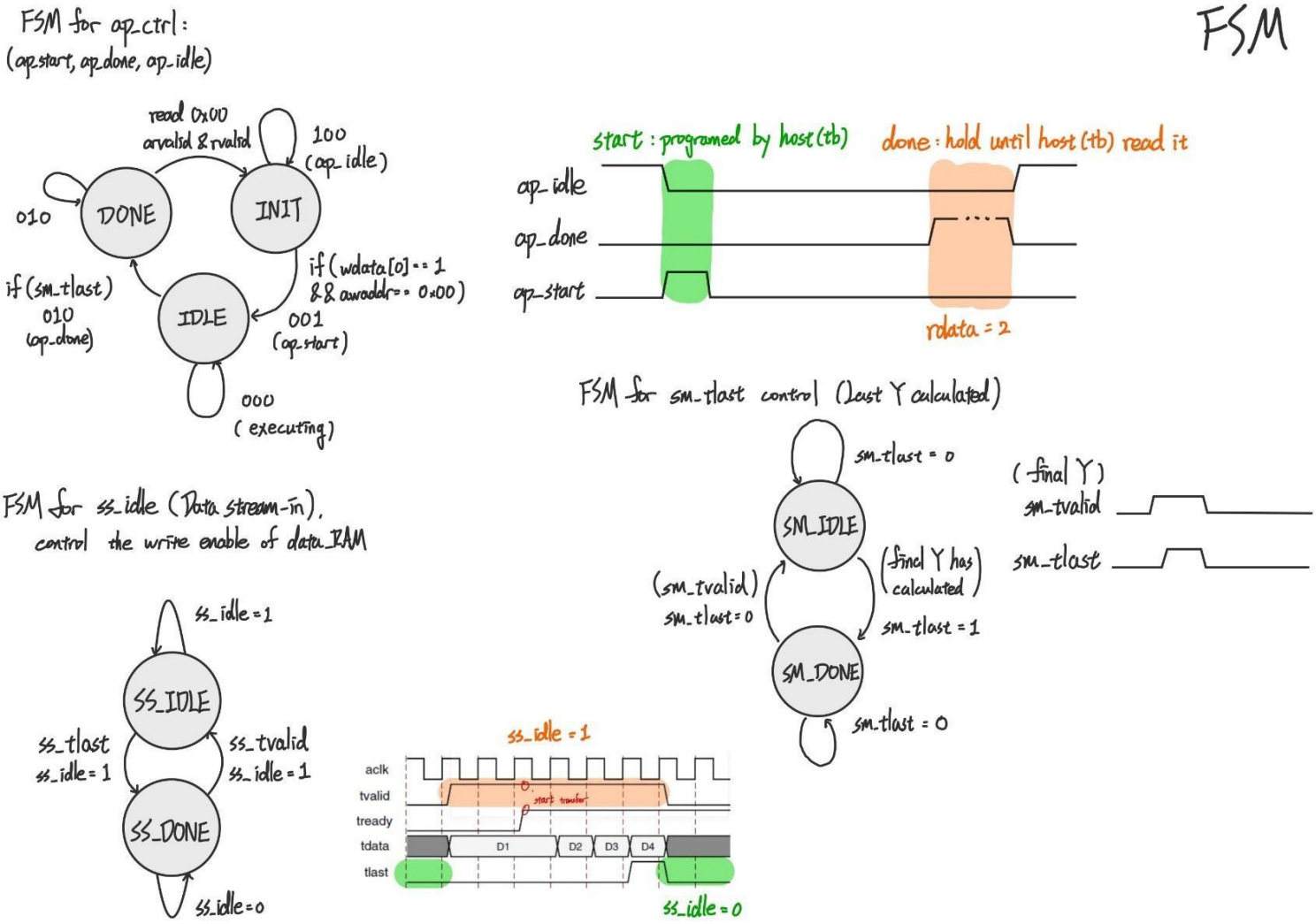
WE = (ss_tready & ss_idle) ? 4'b1111 : 4'b0000; (Ready to write "New value" & not finish)

A = (ap_ctrl[2] && init_addr < 6'd44) ? init_addr : data_A_tmp;

If ap_idle == 1, initialize the value in dataRAM.

Di = ss_tdata

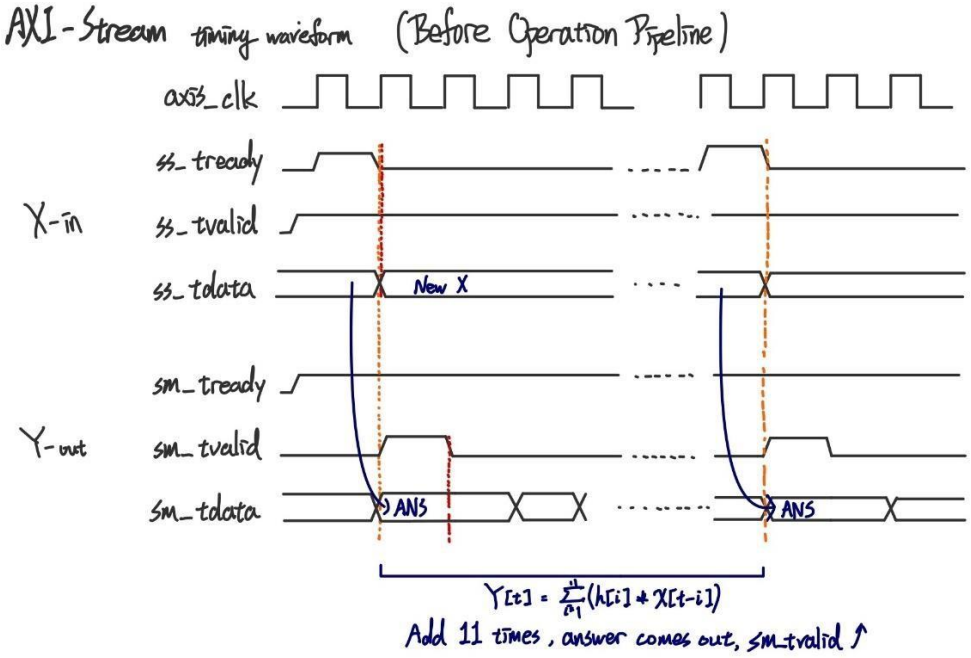
FSM

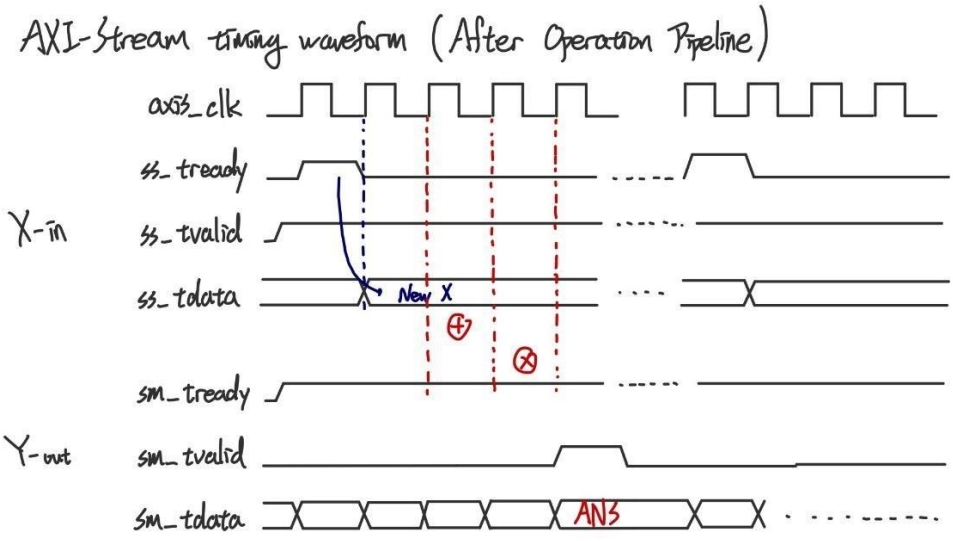


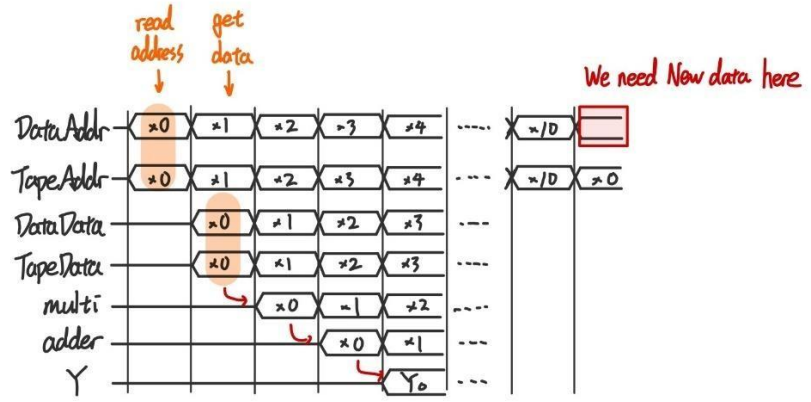
1. The FSM in the top left is given to ap_start, ap _ stone, ap _ dle, starting at INIT state, ap_ctrl = {ap_dle, ap_stone, ap_start} = 3'b100, when we Host end (testbench) program ap_start, representing FIR, ap_idle, down to IDLE state, ap_ctrl = {ap_idle, ap_done, ap_start} = 3'b000. When we finish the calculation of the last Y, send it to testbench alignment, and raise sm_tlast, FIR completes the calculation and goes to DONE state, ap_ctrl = {ap_idle, ap_done, ap_start} = 3'b010. Since testbench needs to read the ap_done signal, wait until read address == 0x00 reads to ap_done before returning to the initial state.
2. The FSM in the lower left corner specially produces the signal of ss_iddle to take data _ RAM as write enable, before the ss_tlast, it will be 1, until the ss_tlast, will enter the SS_DONE state, ss_idle = 0, means can not write again.
3. The FSM on the right is producing sm_tlast. When the last Y is calculated, counter reaches data length, it goes to SM_DONE state, and sm_tlast raises a cycle.

- **Operation explaining**

The upper part of the picture is the y-wave graph that will appear before the operation pipeline. Each time ss_tready is pulled high, representing stream-in new x [t] coming in the RAM. The next cycle can be found The sm_tvalid, pulled high, represents that the calculated Y is taken to the testbench for comparison.





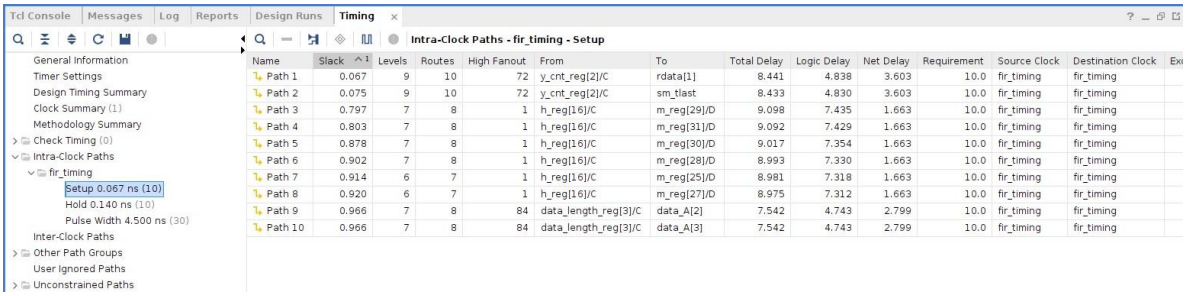


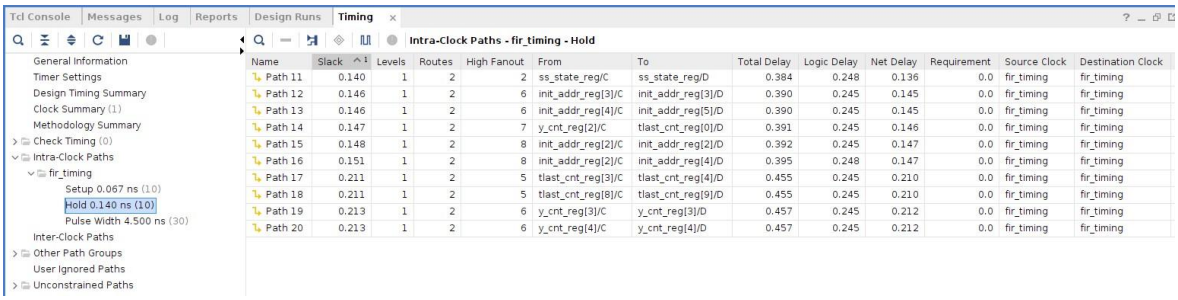
- **Resource usage**

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	190	0	0	53200	0.36
LUT as Logic	190	0	0	53200	0.36
LUT as Memory	0	0	0	17400	0.00
Slice Registers	224	0	0	106400	0.21
Register as Flip Flop	224	0	0	106400	0.21
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

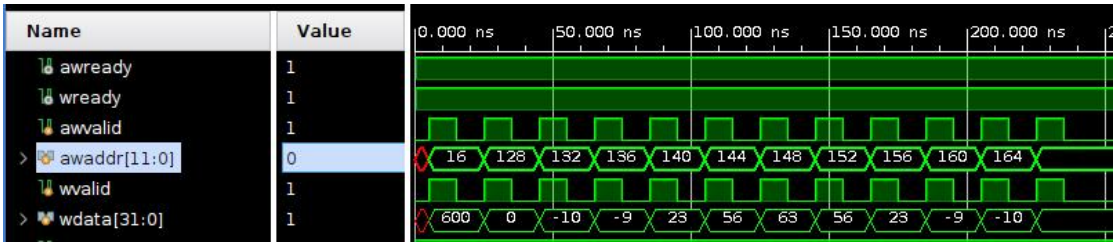
Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

- **Timing report**

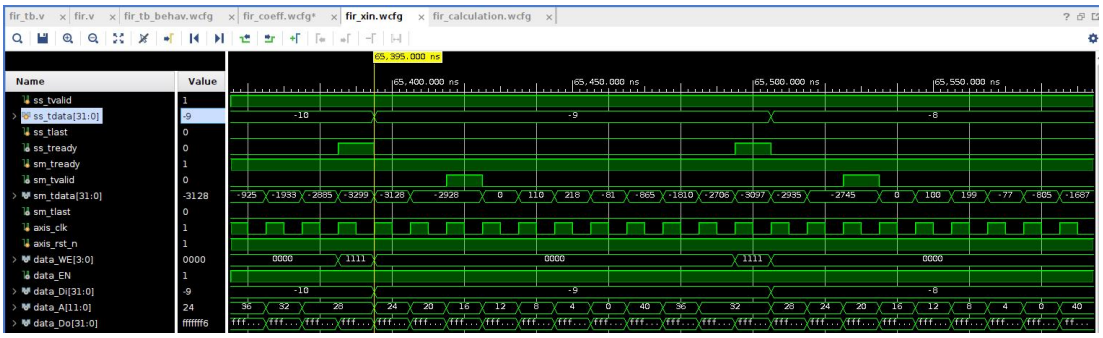




- **Simulation waveforms**
  - Coefficient



  - X-in / Y-out



  - RAM access control