PSoC® Creator™
Project Datasheet for SpiSlave

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Table of Contents

1 Overview

The Cypress PSoC 3 is a family of 8-bit devices with the following characteristics:

- An 8-bit single cycle pipelined 8051 processor, running up to 67 MHz, with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, CAN and I2C
- Analog subsystem that includes configurable switched (SC) and continuous time (CT) blocks, up to 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, op amps, comparators, PGAs, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C38 family member PSoC 3 device. For details on all the systems listed above, please refer to the PSoC 3 Technical Reference Manual .

Figure 1. CY8C38 Device Family Block Diagram

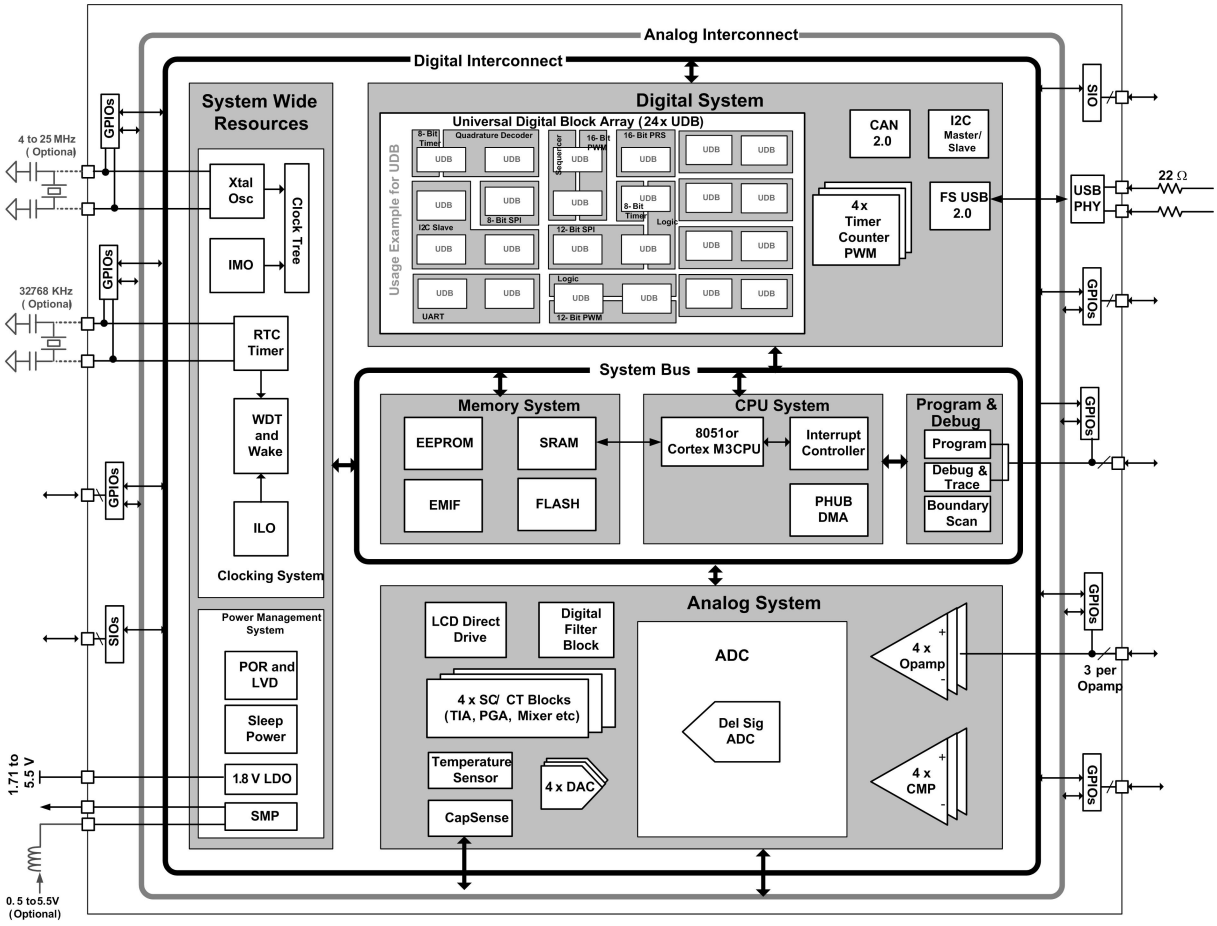


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Architecture	PSoC 3
Family	CY8C38
CPU speed (MHz)	67
Flash size (kBytes)	64
SRAM size (kBytes)	8
EEPROM size (Bytes)	2048
Trace Buffer (kBytes)	4
Vdd range (V)	1.7 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x1E028069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by BUS_CLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

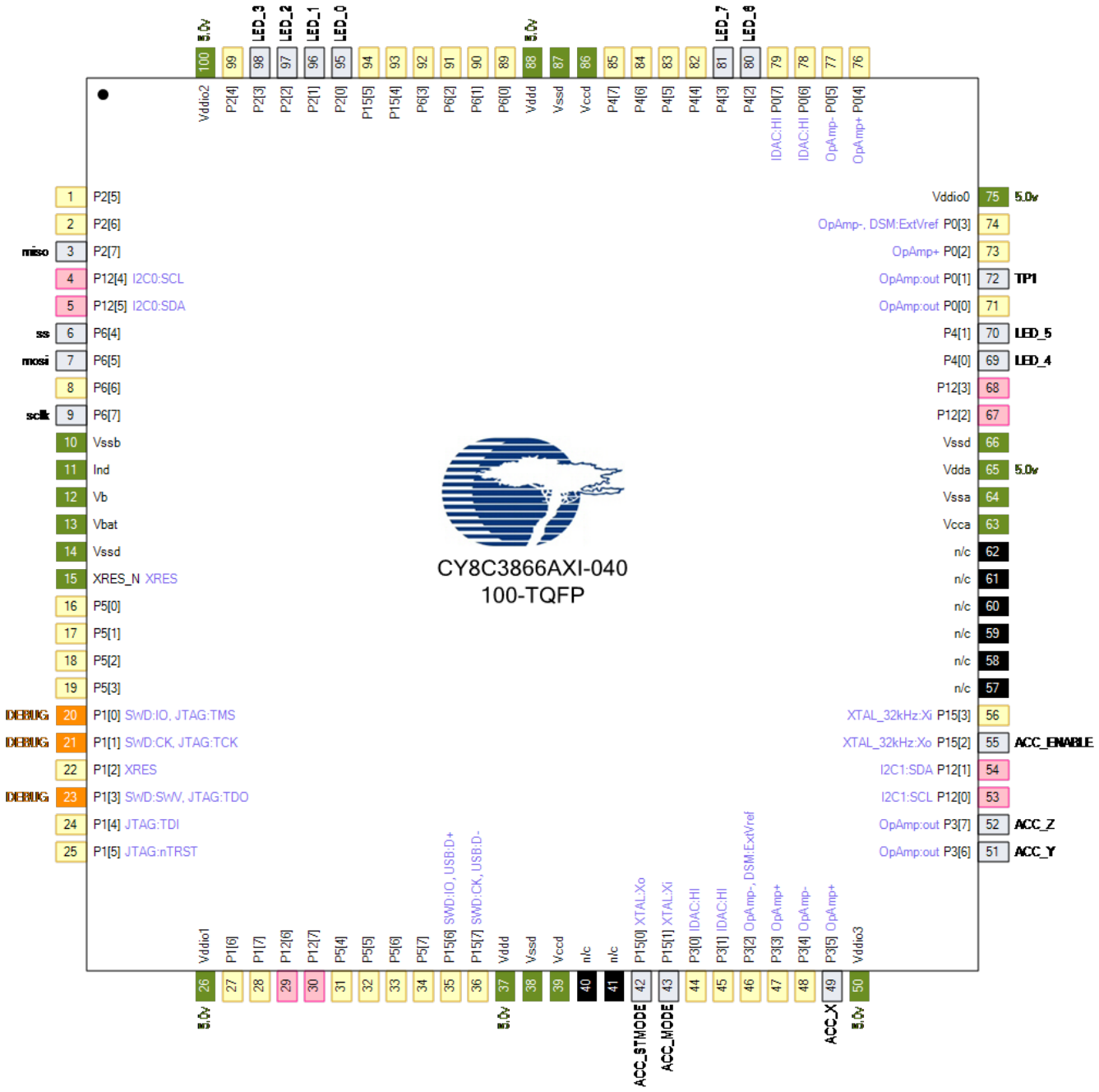
Table 2. Device Resources

Name	Resources in Use	Total Resources Available
Digital domain clock dividers	2 (25.0%)	8
Analog domain clock dividers	2 (50.0%)	4
Pins	22 (30.6%)	72
UDB Macrocells	13 (6.8%)	192
UDB Unique Pterms	17 (4.4%)	384
UDB Datapath Cells	2 (8.3%)	24
UDB Status Cells	3 (12.5%)	24
UDB Control Cells	1 (4.2%)	24
DMA Channels	1 (4.2%)	24
Interrupts	3 (9.4%)	32
DSM Fixed Blocks	1 (100.0%)	1
VIDAC Fixed Blocks	0 (0.0%)	4
SC Fixed Blocks	0 (0.0%)	4
Comparator Fixed Blocks	0 (0.0%)	4
Opamp Fixed Blocks	0 (0.0%)	4
CapSense Buffers	0 (0.0%)	2
CAN Fixed Blocks	0 (0.0%)	1
Decimator Fixed Blocks	1 (100.0%)	1
I2C Fixed Blocks	0 (0.0%)	1
Timer Fixed Blocks	0 (0.0%)	4
DFB Fixed Blocks	0 (0.0%)	1
USB Fixed Blocks	0 (0.0%)	1
LCD Fixed Blocks	0 (0.0%)	1
EMIF Fixed Blocks	0 (0.0%)	1
LPF Fixed Blocks	0 (0.0%)	2

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	GPIO [unused]			HiZ Analog Unb
2	P2[6]	GPIO [unused]			HiZ Analog Unb
3	P2[7]	miso	Dgtl Out	Strong drive	HiZ Analog Unb
4	P12[4]	SIO [unused]			HiZ Analog Unb
5	P12[5]	SIO [unused]			HiZ Analog Unb
6	P6[4]	ss	Dgtl In	HiZ digital	HiZ Analog Unb
7	P6[5]	mosi	Dgtl In	HiZ digital	HiZ Analog Unb
8	P6[6]	GPIO [unused]			HiZ Analog Unb
9	P6[7]	sclk	Dgtl In	HiZ digital	HiZ Analog Unb
10	Vssb	Vssb	Power		
11	Ind	Power			
12	Vb	Vb	Power		
13	Vbat	Vbat	Power		
14	Vssd	Vssd	Power		
15	XRES_N	XRES_N	Power		
16	P5[0]	GPIO [unused]			HiZ Analog Unb
17	P5[1]	GPIO [unused]			HiZ Analog Unb
18	P5[2]	GPIO [unused]			HiZ Analog Unb
19	P5[3]	GPIO [unused]			HiZ Analog Unb
20	P1[0]	GPIO [unused]			HiZ Analog Unb
21	P1[1]	GPIO [unused]			HiZ Analog Unb
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	GPIO [unused]			HiZ Analog Unb
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	GPIO [unused]			HiZ Analog Unb
26	Vio1	Vio1	Power		
27	P1[6]	GPIO [unused]			HiZ Analog Unb
28	P1[7]	GPIO [unused]			HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	SIO [unused]			HiZ Analog Unb
31	P5[4]	GPIO [unused]			HiZ Analog Unb
32	P5[5]	GPIO [unused]			HiZ Analog Unb
33	P5[6]	GPIO [unused]			HiZ Analog Unb
34	P5[7]	GPIO [unused]			HiZ Analog Unb
35	P15[6]	USB [unused]			HiZ Analog Unb
36	P15[7]	USB [unused]			HiZ Analog Unb
37	Vddd	Vddd	Power		
38	Vssd	Vssd	Power		
39	Vccd	Vccd	Power		
42	P15[0]	ACC_STMODE		OD, DL	HiZ Analog Unb
43	P15[1]	ACC_MODE		Strong drive	HiZ Analog Unb
44	P3[0]	GPIO [unused]			HiZ Analog Unb
45	P3[1]	GPIO [unused]			HiZ Analog Unb
46	P3[2]	GPIO [unused]			HiZ Analog Unb
47	P3[3]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
48	P3[4]	GPIO [unused]			HiZ Analog Unb
49	P3[5]	ACC_X	Analog	HiZ analog	HiZ Analog Unb
50	Vio3	Vio3	Power		
51	P3[6]	ACC_Y	Analog	HiZ analog	HiZ Analog Unb
52	P3[7]	ACC_Z	Analog	HiZ analog	HiZ Analog Unb
53	P12[0]	SIO [unused]			HiZ Analog Unb
54	P12[1]	SIO [unused]			HiZ Analog Unb
55	P15[2]	ACC_ENABLE		Strong drive	HiZ Analog Unb
56	P15[3]	GPIO [unused]			HiZ Analog Unb
63	Vcca	Vcca	Power		
64	Vssa	Vssa	Power		
65	Vdda	Vdda	Power		
66	Vssd	Vssd	Power		
67	P12[2]	SIO [unused]			HiZ Analog Unb
68	P12[3]	SIO [unused]			HiZ Analog Unb
69	P4[0]	LED_4		Strong drive	HiZ Analog Unb
70	P4[1]	LED_5		Strong drive	HiZ Analog Unb
71	P0[0]	GPIO [unused]			HiZ Analog Unb
72	P0[1]	TP1		Strong drive	HiZ Analog Unb
73	P0[2]	GPIO [unused]			HiZ Analog Unb
74	P0[3]	GPIO [unused]			HiZ Analog Unb
75	Vio0	Vio0	Power		
76	P0[4]	GPIO [unused]			HiZ Analog Unb
77	P0[5]	GPIO [unused]			HiZ Analog Unb
78	P0[6]	GPIO [unused]			HiZ Analog Unb
79	P0[7]	GPIO [unused]			HiZ Analog Unb
80	P4[2]	LED_6		Strong drive	HiZ Analog Unb
81	P4[3]	LED_7		Strong drive	HiZ Analog Unb
82	P4[4]	GPIO [unused]			HiZ Analog Unb
83	P4[5]	GPIO [unused]			HiZ Analog Unb
84	P4[6]	GPIO [unused]			HiZ Analog Unb
85	P4[7]	GPIO [unused]			HiZ Analog Unb
86	Vccd	Vccd	Power		
87	Vssd	Vssd	Power		
88	Vddd	Vddd	Power		
89	P6[0]	GPIO [unused]			HiZ Analog Unb
90	P6[1]	GPIO [unused]			HiZ Analog Unb
91	P6[2]	GPIO [unused]			HiZ Analog Unb
92	P6[3]	GPIO [unused]			HiZ Analog Unb
93	P15[4]	GPIO [unused]			HiZ Analog Unb
94	P15[5]	GPIO [unused]			HiZ Analog Unb
95	P2[0]	LED_0		Strong drive	HiZ Analog Unb
96	P2[1]	LED_1		Strong drive	HiZ Analog Unb
97	P2[2]	LED_2		Strong drive	HiZ Analog Unb
98	P2[3]	LED_3		Strong drive	HiZ Analog Unb
99	P2[4]	GPIO [unused]			HiZ Analog Unb
100	Vio2	Vio2	Power		

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- OD, DL = Open drain, drives low

- HiZ analog = High impedance analog

2.2 Software Pins

Table 4 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 4. Software Pins

Name	Port	Type	Reset State
ACC_ENABLE	P15[2]		HiZ Analog Unb
ACC_MODE	P15[1]		HiZ Analog Unb
ACC_STMODE	P15[0]		HiZ Analog Unb
ACC_X	P3[5]	Analog	HiZ Analog Unb
ACC_Y	P3[6]	Analog	HiZ Analog Unb
ACC_Z	P3[7]	Analog	HiZ Analog Unb
LED_0	P2[0]		HiZ Analog Unb
LED_1	P2[1]		HiZ Analog Unb
LED_2	P2[2]		HiZ Analog Unb
LED_3	P2[3]		HiZ Analog Unb
LED_4	P4[0]		HiZ Analog Unb
LED_5	P4[1]		HiZ Analog Unb
LED_6	P4[2]		HiZ Analog Unb
LED_7	P4[3]		HiZ Analog Unb
miso	P2[7]	Dgtl Out	HiZ Analog Unb
mosi	P6[5]	Dgtl In	HiZ Analog Unb
Power	Ind		
sclk	P6[7]	Dgtl In	HiZ Analog Unb
ss	P6[4]	Dgtl In	HiZ Analog Unb
TP1	P0[1]		HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 5. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Clear SRAM During Startup	True
Unused Bonded IO	Allow but warn

3.2 System Debug Settings

Table 6. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Require XRES Pin	True
Use Optional XRES	False

3.3 System Operating Conditions

Table 7. System Operating Conditions

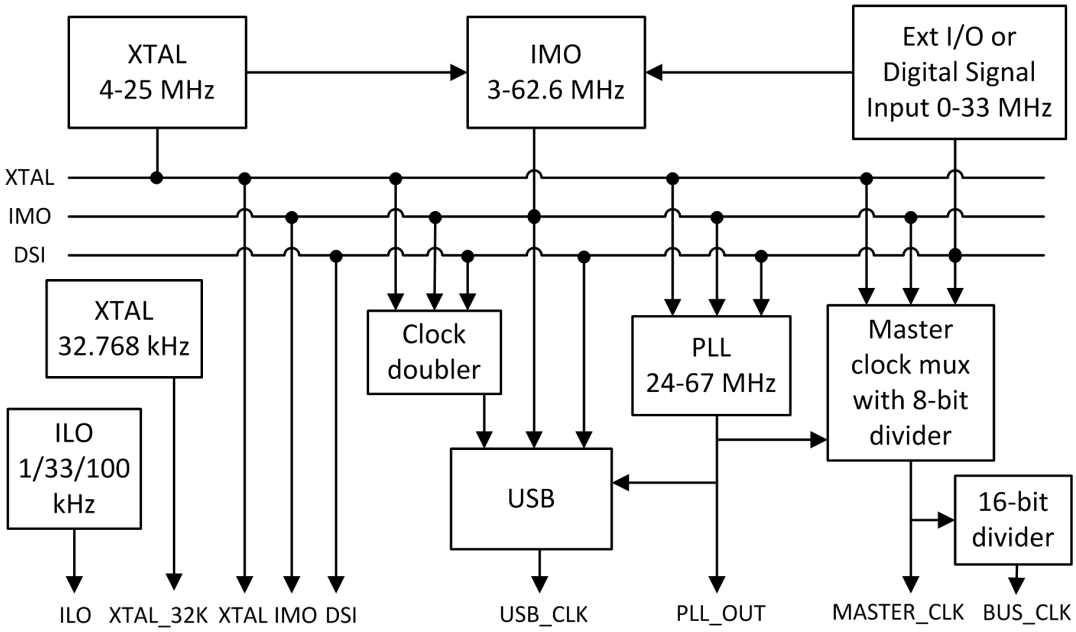
Name	Value
Vddd (V)	5.0
Vdda (V)	5.0
Variable Vdda	False
Vddio0 (V)	5.0
Vddio1 (V)	5.0
Vddio2 (V)	5.0
Vddio3 (V)	5.0
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 62.6 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 67 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 67 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 8 lists the system clocks used in this design.

Table 8. System Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
USB_CLK	DIGITAL	IMO	48	0	±0	False	False
BUS_CLK	DIGITAL	MASTER_CLK	0	24	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	0	24	±1	True	True
Digital Signal	DIGITAL		0	0	±0	False	False
XTAL 32kHz	DIGITAL		0.0328	0	±0	False	False
XTAL	DIGITAL		25	0	±0	False	False
ILO	DIGITAL		0	0.001	-50,+100	True	True
PLL_OUT	DIGITAL	IMO	24	24	±1	True	True
IMO	DIGITAL		3	3	±1	True	True

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

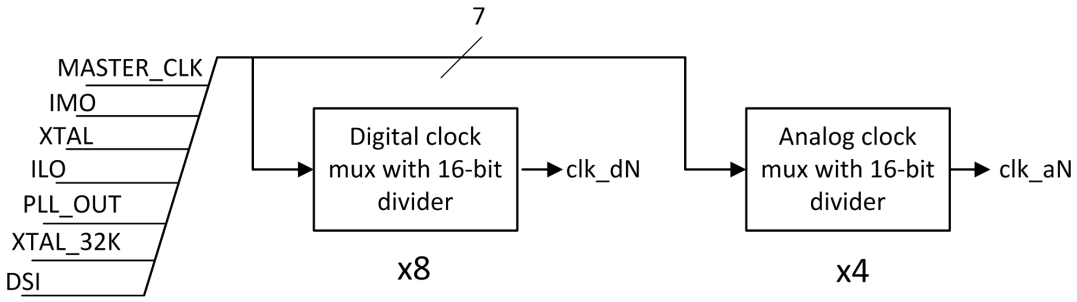


Table 9 lists the local clocks used in this design.

Table 9. Local Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
Clock_1	DIGITAL	MASTER_CLK	12	12	±1	True	True
ADC_DelSig_-1_theACLK	ANALOG	MASTER_CLK	0.67	0.6667	±1	True	True
ADC_DelSig_-1_Ext_CP_Clk	DIGITAL	MASTER_CLK	2.68	2.6667	±1	True	True
Clock_2	ANALOG	IMO	0.0001	0.0001	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 3 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - o CyPLL API routines
  - o CyIMO API routines

- CyILO API routines
- CyMaster API routines
- CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 10. Interrupts

Name	Priority	Vector
rx_isr	5	1
ADC_DelSig_1_IRQ	7	29
dma_isr	7	0

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 3 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 11. DMAs

Name	Priority	Channel Number
DMA_1	2	10

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the PSoC 3 Technical Reference Manual
- DMA chapter in the System Reference Guide
  - DMA API routines and related registers
- Datasheet for cy_dma component

6 Flash Memory

PSoC 3 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0xFFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - External read protect (Factory upgrade)
- R - External write protect (Field upgrade)
- W - Full Protection

For more information on Flash memory and protection, please refer to:

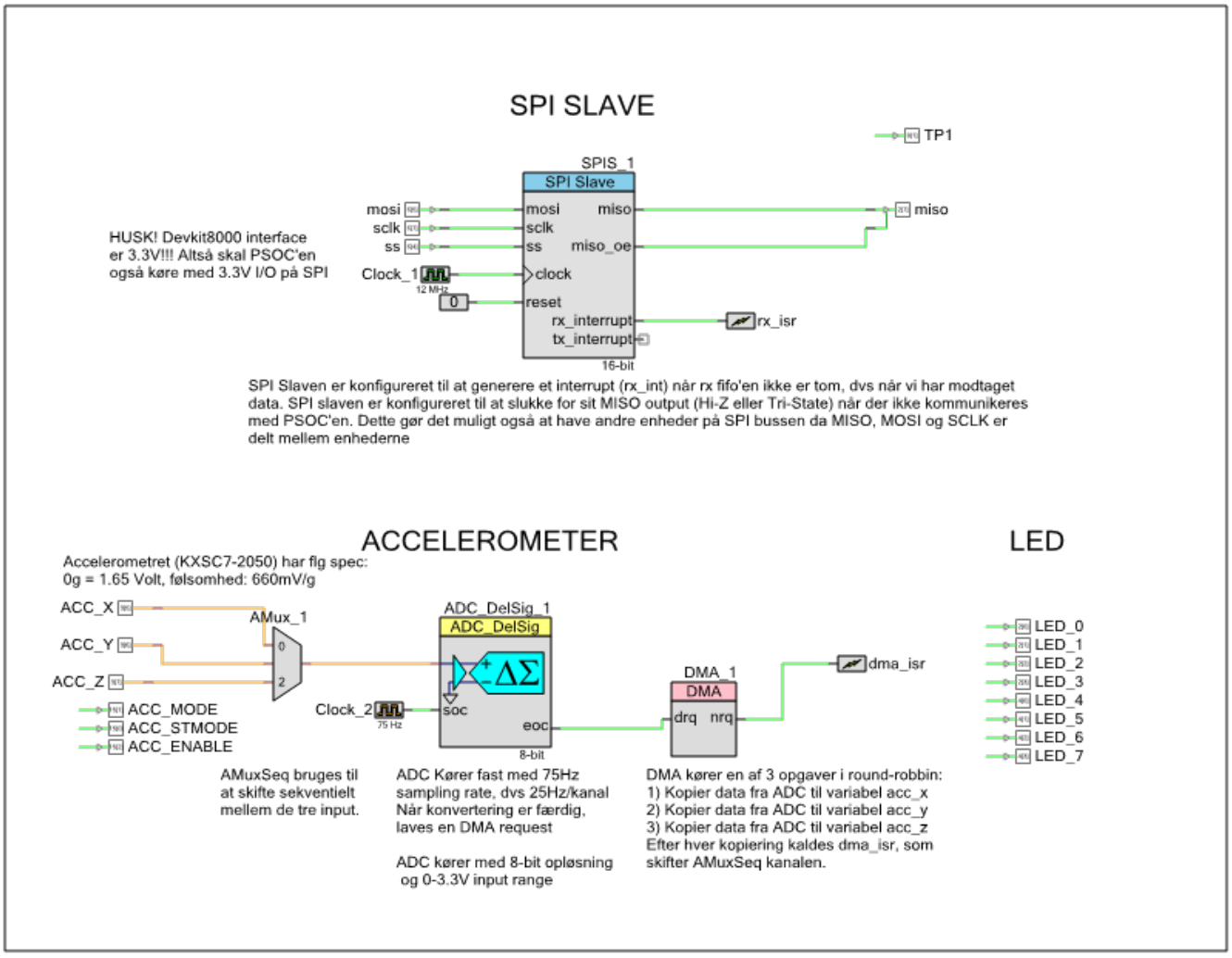
- Flash Protection chapter in the PSoC 3 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyFlash API routines
  - CyWrite API routines

7 Design Contents

This design's schematic content consists of the following 2 schematic sheets:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1

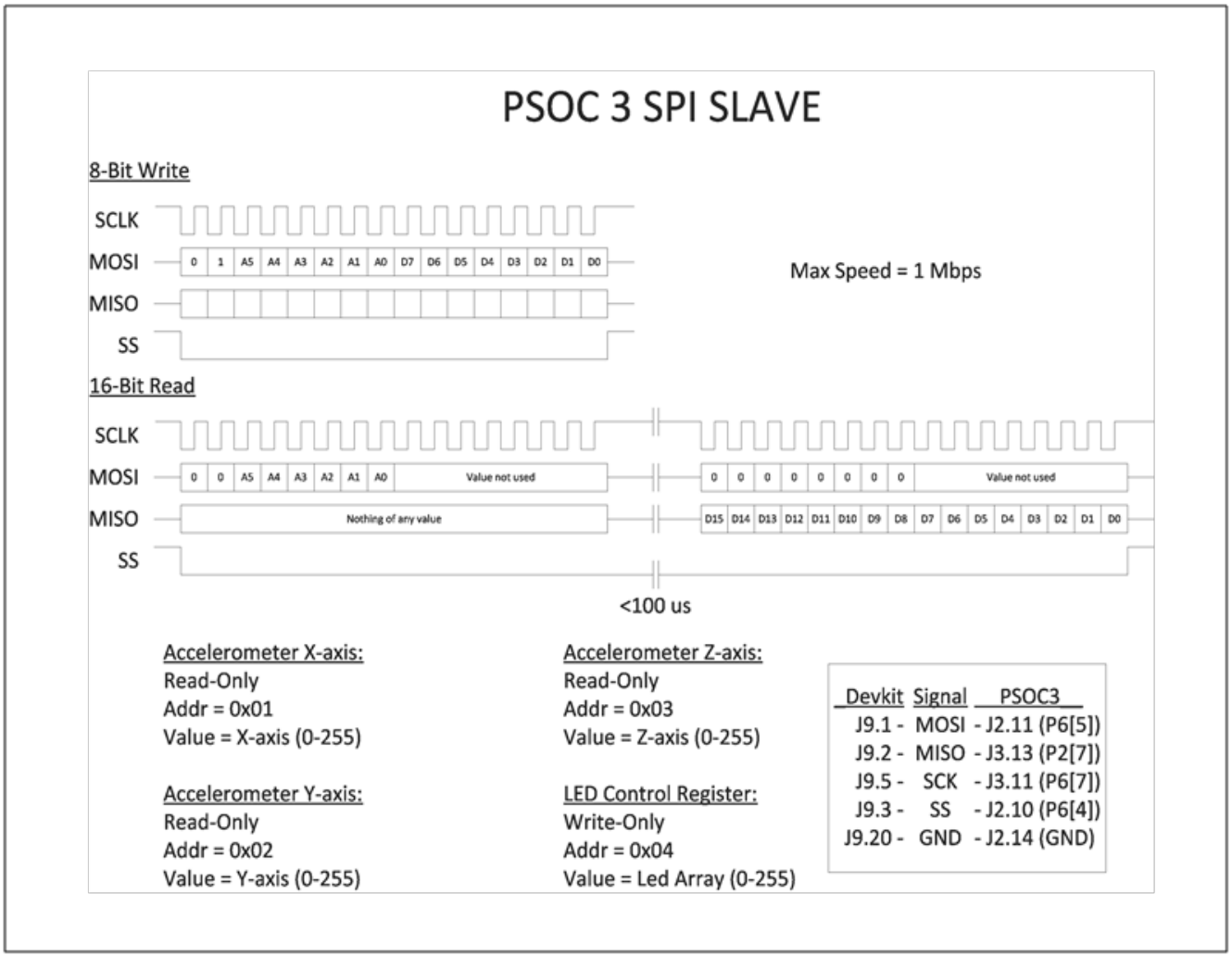


This schematic sheet contains the following component instances:

- Instance ADC_DelSig_1 (type: ADC_DelSig_v2_30)
- Instance AMux_1 (type: AMux_v1_70)
- Instance SPIS_1 (type: SPI_Slave_v2_50)

7.2 Schematic Sheet: Page 2

Figure 6. Schematic Sheet: Page 2



8 Components

8.1 Component type: ADC_DelSig [v2.30]

8.1.1 Instance ADC_DelSig_1

Description: Delta-Sigma ADC
Instance type: ADC_DelSig [v2.30]
Datasheet: online component datasheet for ADC_DelSig

Table 13. Component Parameters for ADC_DelSig_1

Parameter Name	Value	Description
ADC_Charge_Pump_Clock	true	Low power charge pump clock selection
ADC_Clock	Internal	Parameter for selecting the ADC clock type.
ADC_Input_Mode	Single	Differential or Single ended input mode
ADC_Input_Range	Vssa to Vdda	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config2	Vssa to 2.048V (0.0 to 2*Vref)	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config3	Vssa to 1.024V (0.0 to Vref)	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config4	Vssa to 1.024V (0.0 to Vref)	Choose input operating mode that best supports the range of the signals being measured.
ADC_Power	Medium Power	Sets power level of ADC.
ADC_Reference	Internal Vdda/4	Selects voltage reference source and configuration.
ADC_Reference_Config2	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config3	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config4	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Resolution	8	ADC Resolution in bits
ADC_Resolution_Config2	16	ADC Resolution in bits
ADC_Resolution_Config3	16	ADC Resolution in bits
ADC_Resolution_Config4	16	ADC Resolution in bits
Clock_Frequency	64000	Determines the ADC clock frequency.
Comment_Config1	Default Config	Parameter which holds the user comment for the config1.
Comment_Config2	Second Config	Parameter which holds the user comment for the config2.
Comment_Config3	Third Config	Parameter which holds the user comment for the config3.
Comment_Config4	Fourth Config	Parameter which holds the user comment for the config4.

Parameter Name	Value	Description
Config1_Name	CFG1	This parameter is used to create constants in the header file for config 1.
Config2_Name	CFG2	This parameter is used to create constants in the header file for config 2.
Config3_Name	CFG3	This parameter is used to create constants in the header file for config 3.
Config4_Name	CFG4	This parameter is used to create constants in the header file for config 4.
Configs	1	Number of active configurations
Conversion_Mode	1 - Multi Sample	ADC conversion mode
Conversion_Mode_Config2	0 - Single Sample	ADC conversion mode
Conversion_Mode_Config3	2 - Continuous	ADC conversion mode
Conversion_Mode_Config4	2 - Continuous	ADC conversion mode
Enable_Vref_Vss	false	Determines whether or not to connect ADC's reference Vssa to AGL[6].
Input_Buffer_Gain	1	Gain of input amplifier
Input_Buffer_Gain_Config2	1	Gain of input amplifier
Input_Buffer_Gain_Config3	1	Gain of input amplifier
Input_Buffer_Gain_Config4	1	Gain of input amplifier
Input_Buffer_Mode	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config2	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config3	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config4	Rail to Rail	Buffer Mode type selection
Ref_Voltage	1.25	Set reference voltage
Ref_Voltage_Config2	1.024	Set reference voltage
Ref_Voltage_Config3	1.024	Set reference voltage
Ref_Voltage_Config4	1.024	Set reference voltage
Sample_Rate	10000	Sample Rate in Hz
Sample_Rate_Config2	10000	Sample Rate in Hz
Sample_Rate_Config3	10000	Sample Rate in Hz
Sample_Rate_Config4	10000	Sample Rate in Hz
sRate_Err	false	Parameter to hold the Conversion rate error status of ADC configuration.
Start_of_Conversion	Hardware	Continuous conversions or hardware controlled

8.2 Component type: AMux [v1.70]

8.2.1 Instance AMux_1

Description: Multiplexer used to route analog signals.
Instance type: AMux [v1.70]
Datasheet: online component datasheet for AMux

Table 14. Component Parameters for AMux_1

Parameter Name	Value	Description
AtMostOneActive	false	Limit to at most one active channel.
Channels	3	Channel count.
Isolation	Medium	Specify minimum, medium, or maximum switch control; affects channel isolation and switching time.
MuxType	Single	Select between single or differential inputs.

8.3 Component type: SPI_Slave [v2.50]

8.3.1 Instance SPIS_1

Description: Serial Peripheral Interface Slave
Instance type: SPI_Slave [v2.50]
Datasheet: online component datasheet for SPI_Slave

Table 15. Component Parameters for SPIS_1

Parameter Name	Value	Description
BidirectMode	false	Bidirectional mode setting
ClockInternal	false	Defines whether internal clock is used or not
DesiredBitRate	1000000	Desired Bit Rate in Hz
FixedPlacementEnabled	false	
InterruptOnByteComplete	true	Set Initial Interrupt Source to Enable Interrupt on Byte Transfer Complete
InterruptOnDone	false	Set Initial Interrupt Source to Enable Interrupt on SPI Done
InterruptOnRXEmpty	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Empty
InterruptOnRXFull	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO full
InterruptOnRXNotEmpty	true	Set Initial Interrupt Source to Enable Interrupt on RX Not Empty
InterruptOnRXOverrun	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO overrun
InterruptOnTXEmpty	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Empty
InterruptOnTXFull	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO full
InterruptOnTXNotFull	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO not full
Mode	CPHA = 1, CPOL = 1	Allows for setting the SPI Clock Polarity and Clock Phase from one of the four well known modes
MultiSlaveEnable	true	Allows using of the SPI MISO output enable terminal for multislave mode support
NumberOfDataBits	16	Data Width (3-16 bits)

Parameter Name	Value	Description
RxBufferSize	4	RAM size used to store RX Data
ShiftDir	MSB First	Data Shift Direction (MSB First or LSB First)
TxBufferSize	4	RAM size used to store TX Data
UseInternalInterrupt	false	Defines whether internal interrupt is used or not
UseRxInternalInterrupt	false	Defines whether Rx internal interrupt is used or not
UseTxInternalInterrupt	false	Defines whether Tx internal interrupt is used or not

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 3 register map is covered in the PSoC 3 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 3 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 3 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 3 Technical Reference Manual
  - Cache chapter in the System Reference Guide