Nanotextured Solar Cells Using Aluminum as a Catalyst and Dopant

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***Abstract* — A black silicon solar cell fabricated using aluminum as both a catalyst and dopant is demonstrated. A nanowire/nanopyramid black silicon surface texture is grown via aluminum (Al)-catalyzed vapor-liquid-solid growth, and post-growth annealing diffuses the aluminum into the n-type substrate, forming a p-n junction. Devices with nanopyramid surface textures are found to have higher short-circuit currents and open-circuit voltages than nanowire surface textures grown at lower temperatures, and post-growth annealing times of 15-30 minutes are found to promote higher short-circuit current densities. External quantum efficiency measurements show that the highest photoconversion occurs in the red and IR regions for all devices, with low quantum efficiencies at shorter wavelengths even when the p-type silicon surface is passivated with alumina. The quantum efficiency spectra imply that the devices are limited by recombination on the illuminated side of the device. Based on these results and previous data on Al-catalyzed wires and pyramids, excess Al incorporation and Al cluster formation in the emitter are suggested as the primary factors currently limiting device performance.**

I. Introduction

As the next generation of silicon photovoltaics moves to thinner substrates, black silicon texturing using nanoscale surface features has become a popular approach to maximize light-trapping and compensate for the lost material in the substrate. Several methods for black silicon texturing have been reported, including metal assisted chemical etching [1] and reactive ion etching [2]. Devices fabricated using these techniques have reached 22% efficiencies [2], suggesting that black silicon textured solar cells are a viable next generation device structure.

However, current black silicon devices require separate steps for texturing and junction formation – adding processing costs and time to the final device. A technique combining both steps into a single process is therefore desirable to continue to reduce fabrication costs.

Aluminum-catalyzed vapor-liquid-solid (VLS) growth of nanotextured silicon can simultaneously p-type dope the silicon and texture the surface. While gold has been the most widely-studied material for VLS growth, gold is a deep-level trap in silicon while aluminum acts as a natural p-type dopant. In this process, Al is incorporated into wires at concentrations up to $2x10^{20}$ atoms/cm^3 [3,4]. Thus, growth on an n-type substrate allows for formation of a black silicon solar cell with a highly doped p-type emitter (Figure 1). Subsequent post-growth annealing in the same reactor allows for the formation of a planar junction beneath the pyramid texture.

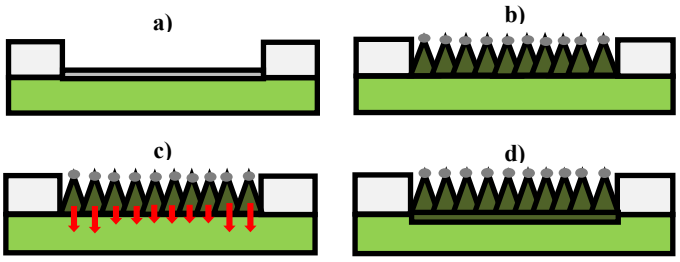

Fig. 1. Schematic of solar cell fabrication process. a) Al catalyst layer deposited on patterned n-type substrate (light green). b) Al-catalyzed growth of p-type silicon nanopyramids (dark green) c) Post-growth annealing to diffuse Al into the substrate surface and form a p-type emitter. d) Formation of a planar p-n junction beneath the textured surface

Our previous report on aluminum-catalyzed VLS growth demonstrated how growth temperatures could be used to control nanotexture morphology and optimize light-trapping in these structures [5]. However, the influence of growth parameters on device performance has not been demonstrated. In this report, we demonstrate the performance of aluminum-catalyzed nanotextured photovoltaics and the effects of different growth parameters on device performance.

II. EXPERIMENTAL

Solar cells were fabricated on lightly-doped (1-10 Ω-cm) n-type CZ Si <111> substrates. First, a back-surface field was formed by thermal diffusion of $POCl_3$ in O_2 at 1000 ^oC for 20 minutes, followed by a 20 minute drive-in at 1000 ^oC. To protect the front surface of the wafer from diffusion, a 200 nm SiO_2 layer was deposited on the surface using PECVD prior to $POCl_3$ diffusion. The surface oxide from the thermal diffusion process was removed in 10:1 BOE, and a 300 nm amorphous SiNx layer was deposited atop the undiffused side of the wafer. Contact lithography was used to define 0.5 cm x 0.5 cm^2 square patterns on the SiNx surface, and reactive ion etching was used to etch through into the substrate to define the device areas. Using electron beam evaporation and base pressures of $1x10^{-6}$ Torr or less, 10 nm Al thin films were evaporated over the etched patterns to form the catalyst layer for pyramid growth. Post deposition liftoff in acetone was performed to remove remaining resist and Al deposited

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between the patterns. Finally, samples were diced into 1 cm x 1cm squares prior to LPCVD growth.

Al-catalyzed VLS growth was performed following conditions described in earlier work by Hainey et al. [5], with a hydrogen ambient, 500 Torr reactor pressure, 5 Torr SiH_4 partial pressure, 700°C growth temperature, and 100 sccm total flow rate. Textures were grown from 650-700°C to study the effect of morphology on device performance. Upon finishing growth, the reactor temperature was increased to 950°C for post-growth annealing to drive aluminum into the substrate and form a planar p-n junction. To study the effect of junction depth on wire performance, anneals were performed for 15, 30, and 60 minutes on pyramid-textured samples. Finally, to study the effects of pyramid dimensions on device performance, samples were fabricated at 700°C with short (9.5 minute) growth times or reduced SiH_4 partial pressures to produce smaller pyramids. Scanning electron microscopy (Leo 1530) was used to visualize the final morphology of these structures.

Upon finishing growth, devices were passivated with a 20 nm alumina layer using a Kurt Lesker 150LE atomic layer deposition system. To activate the passivation layer, samples were annealed for 15 minutes at 400°C in forming gas. Contacts were applied to the p+ emitter surface using Heraeus 4140 solar paste, and were then annealed at 150 °C for 45 minutes to burn out organic binders, then fired at 800 °C for 15 minutes to form ohmic contacts. Indium dots were then used to form ohmic contacts to the back surface.

Dark I-V testing was performed using an Autolab system, scanning from -1V to 1V, while light I-V testing was performed on a Newport Solar Simulator at 1 sun. External quantum efficiency (EQE) measurements were performed using the setup described in Bernardo et al. [6]

III. Results and Discussion

As reported in previous work [5], increasing growth temperature from 650°C to 700°C changes the morphology of the VLS-grown nanostructures from wires to more tapered wires or pyramids. While reflectivities below 8% were realized for wires grown at 650°C, reflectivities below 4% have been realized for nanopyramids grown at 700°C. SEM images showing the changing morphologies for each structure can be seen in Figure 2.

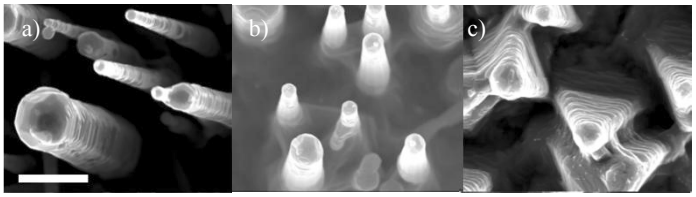

Fig 2. – Top-down SEM of wires grown at a) 650°C and b) 675°C, and c) pyramids grown at 700°C after a 30 min post-growth anneal. Scale bar is one micron for all figures.

Dark IV curves show that all devices are rectifying with relatively low leakage currents (10^{-7} to 10^{-4} A). This behavior is translated into the device performance, as seen in Figure 3. With increasing growth temperature, short-circuit current densities (Jsc) increased from 6 to 7 to 14 mA/cm^2 and external quantum efficiencies increase from 20 to nearly 70%. A summary of device parameters is included in Table 1, which shows that the transition from wire to pyramid also results in a transition to greater open-circuit voltages.

Along with studying the effects of surface texture on device performance, the effect of junction depth was studied by varying annealing times Short-circuit currents were similar for junctions formed after 15 and 30 minute anneals, but were greatly reduced for wires annealed for 60 minutes. With shallow junction depths formed with a 15 minute post-growth anneal, devices can reach efficiencies of greater than 5%.

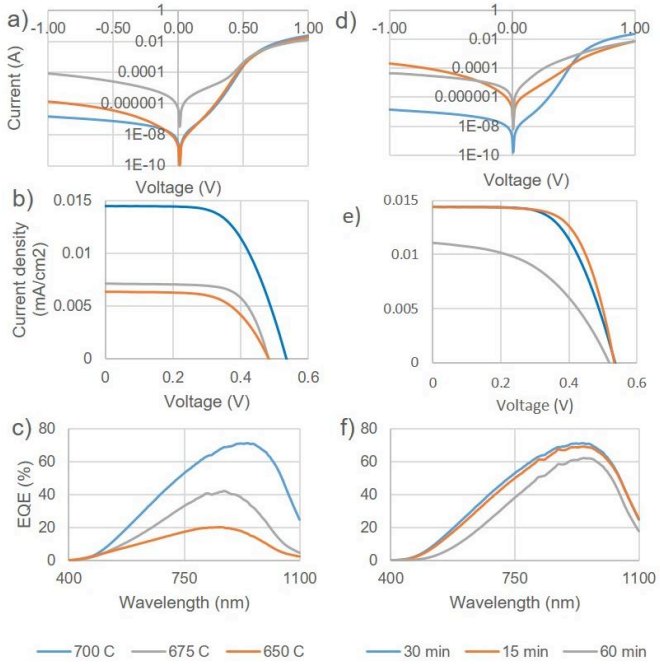

Fig 3. – a,d) Dark I-V, b,e) Light I-V, and c,f) EQE data for growth temperature (left column) and annealing time (right) series

External quantum efficiency (EQE) measurements confirmed the observed behaviors, with lower growth temperatures leading to reduced quantum efficiencies across the spectrum and particularly in the red and IR regions. For samples fabricated with different junction depths, EQE values again show comparable behavior for devices with shallower junctions, with reduced efficiencies as the junction moves further into the device.

TABLE 1: Light I-V Device Parameters

Device	J_{SC}(mA/cm^2)	V_{OC} (V)	FF (%)	Eff (%)
650°C growth	6.34	0.48	62.3	1.90
675°C growth	7.12	0.48	69.6	2.13
700°C/30 min	14.4	0.53	60.9	4.81
15 min anneal	14.4	0.53	65.5	5.04
60 min anneal	8.36	0.51	50.2	2.12

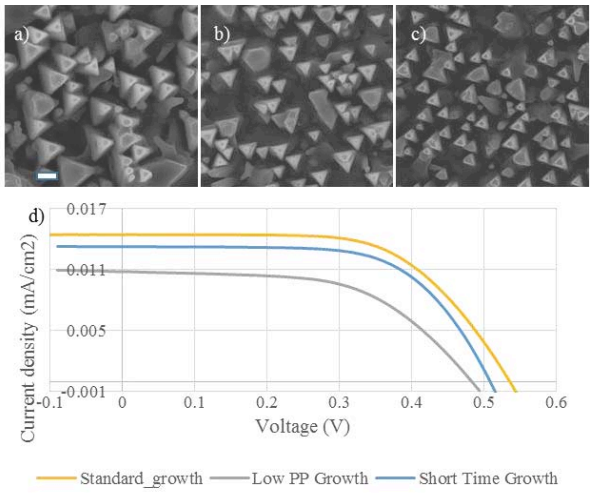

Fig 4. – Top-down SEM of pyramids grown with a) standard conditions, b) short growth times, and c) low partial pressures. Light IV curves d) show the effects of pyramid size on device performance. Scale bar is one micron for all figures.

The effects of the pyramid texture dimensions can be seen in Figure 4. Devices grown for short growth times (838±122nm pyramid bisector length) or with lower SiH_4 partial pressures (606±175nm bisector) have smaller pyramids compared to samples grown following standard conditions (1382±303nm). Samples with smaller pyramids show reduced short-circuit current densities and open-circuit voltages, suggesting that increased aluminum incorporation and light-trapping from more extensive texturing does improve device performance.

These results, particularly the low EQE values at shorter wavelengths, suggest that recombination is occurring in the emitter. Transmission electron microscopy of nanopyramids from previous reports on pyramid growth suggests two possible sources of recombination [5]. Structural defects within the pyramid layer are clearly visible and can serve as recombination sites. More noticeably, visible aluminum clusters can be observed within the p+ region. Cluster formation has been previously reported for aluminum-catalyzed silicon nanowires grown at 550°C, with small (~1nm) clusters reported to be uniformly distributed throughout the wire [3]. The high estimated doping levels in the emitter along with the clusters can combine to form a "dead" layer that has a short carrier lifetime at the top of the p+ emitter. This dead layer may be present across the surface of the emitter, greatly limiting carrier lifetimes and leading to reduced device performance and EQE particularly in the short wavelength region. This effect can also explain the lower current densities observed for low growth temperature devices. Carriers excited in solar cells with high aspect ratio nanowire textures require longer diffusion lengths to reach the junction. Future studies will focus on reducing the impact of this dead layer by decreasing the p+ emitter thickness, decreasing aluminum incorporation through the use of thinner aluminum films and devising alternative cooling procedures to suppress aluminum clustering.

IV. Conclusion

In summary, a black silicon solar cell using aluminum as both a VLS growth catalyst and a p-type dopant has been demonstrated. By growing aluminum-catalyzed silicon nanotextures and diffusing aluminum into the n-type substrate in a post-growth anneal, surface texturing and junction formation can be consolidated into a single process. Dark IV curves show that the devices are rectifying with low leakage currents. Initial studies on the effects of junction depth and texture morphology suggest that nanopyramid textures and 15-30 minute post-growth anneals produce devices with the largest short-circuit currents and open-circuit voltages, with maximum efficiencies of 5%. External quantum efficiency data reveals that photoconversion is most efficient in the red and IR regions of the spectrum, particularly for nanopyramid textures. EQE values at shorter wavelengths remain low, even after devices are passivated. The observed behavior after passivation suggests that recombination is occurring within the emitter, not at the surface. Based on previous reports, the high aluminum concentrations and cluster formation within the wires and pyramids may be creating a dead layer in the emitter which serves as a recombination site. Subsequent experiments will focus on mitigating the effects of excess aluminum in order to reduce recombination.

ACKNOWLEDGEMENTS

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