Digital-electronics-1

gates-01

My github profile

https://github.com/ZukyFresh/Digital-electronics-1

Verifications of basic Boolean postulates

$$f(c,b,a) = \overline{b}\,a + \overline{c}\,\overline{b}$$

$$f(c,b,a)_{\mathrm{NAND}} = \overline{\overline{\overline{b}\,a} \cdot \overline{\overline{b}\,\overline{c}}}$$

$$f(c,b,a)_{\mathrm{NOR}} = \overline{b + \overline{a}} + \overline{c + b}$$

Logical table

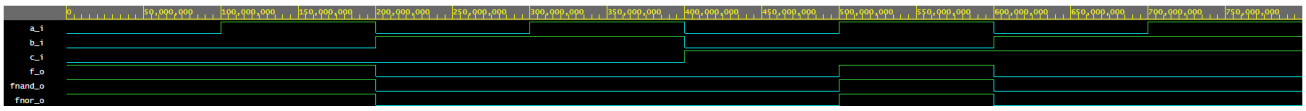
c	b	a	f(c,b,a)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Architecture body for basic gates in VHDL

```
architecture dataflow of gates is
begin
    f_o  <= ((not b_i) and a_i) or ((not c_i) and (not b_i));
    fnand_o <= not (not (not b_i and a_i) and not(not b_i and not c_i));
    fnor_o <= (not (b_i or not a_i)) or (not (c_i or b_i));

end architecture dataflow;
```

Simulated time waveforms



EDA playground example link

https://www.edaplayground.com/x/fmSH

Verification of Distributive laws

Equations

$$x \cdot y + x \cdot z = x \cdot (y + z)$$
$$(x + y) \cdot (x + z) = x + (y \cdot z)$$

Logical table

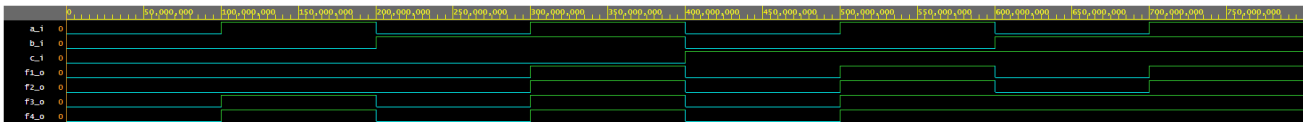
c	b	a	a and b or a and c	a and (b or c)	(a or b) and (a or c)	a or (b and c)
0	0	0	0	0	0	0
0	0	1	0	0	1	1
0	1	0	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	1	1	1	1	1

VHDL code

```
architecture dataflow of gates is
begin
    f1_o <= (a_i and b_i)or(a_i and c_i);
        f2_o <= (a_i and (b_i or c_i));
        f3_o <= (a_i or b_i) and (a_i or c_i);
        f4_o <= a_i or (b_i and c_i);

end architecture dataflow;
```

Simulated time waveforms



EDA playground example link

https://www.edaplayground.com/x/t7nP