

##Table with connection (16 switches & 16 LEDs)

LED	Conn	Switch	Conn
LED0	H17	SW0	J15
LED1	K15	SW1	L16
LED2	J13	SW2	M13
LED3	N14	SW3	R15
LED4	R18	SW4	R17
LED5	V17	SW5	T18
LED6	U17	SW6	U18
LED7	U16	SW7	R13
LED8	V16	SW8	T8
LED9	T15	SW9	U8
LED10	U14	SW10	R16
LED11	T16	SW11	T13
LED12	V15	SW12	H6
LED13	V14	SW13	U12
LED14	V12	SW14	U11
LED15	V11	SW15	V10

Two-bit wide 4-to-1 multiplexer

VHDL architecture (mux_2bit_4to1.vhd)

```
architecture Behavioral of mux_2bit_4to1 is
begin
    f_o <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;

end architecture Behavioral;
```


Click on New Project.



Quick Start

Create Project >

Now click on

Next>. Name your project and click on Next>. Select RTL Project and click on Next>.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ Project is an extensible Vitis platform

Add sources by clicking on Create File and then click on Next>. (type VHDL, location =)

Default Part
Choose a default Xilinx part or board

Parts **Boards**

[Reset All Filters](#)

Vendor:

Search:

Display Name

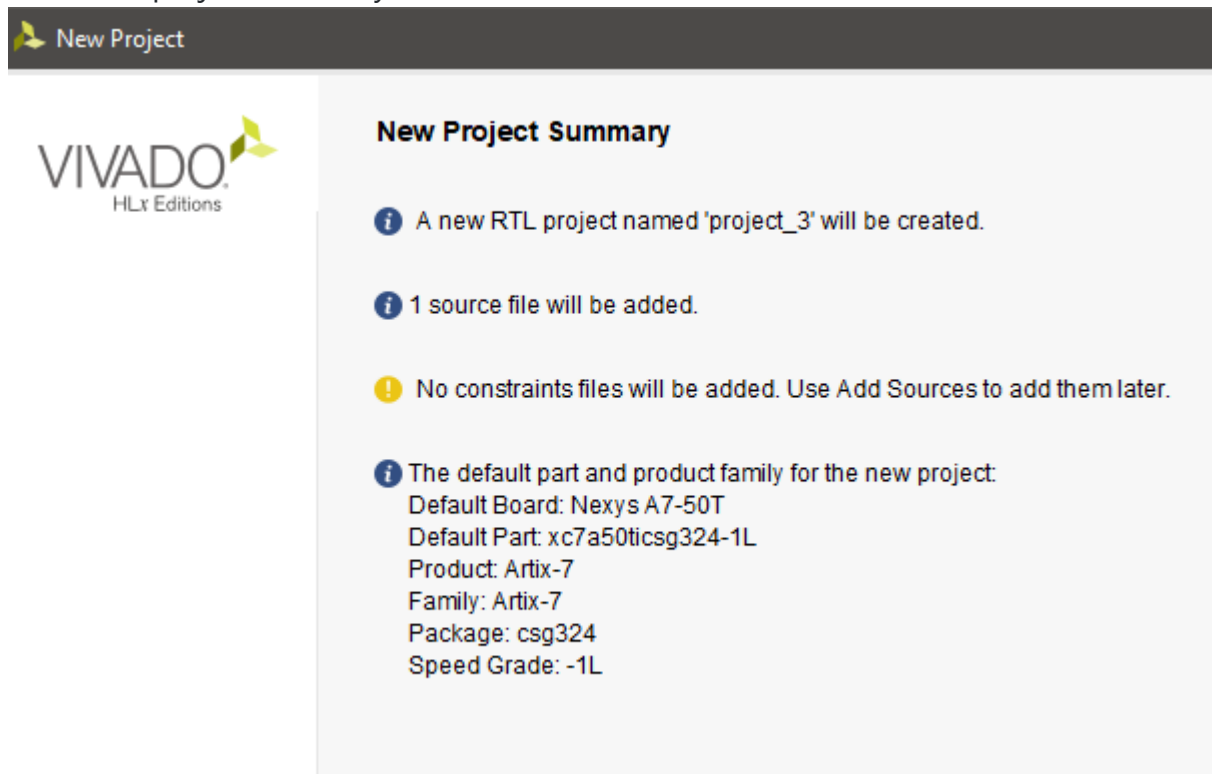
[Genesys ZU-3EG](#)

[Nexys A7-100T](#)

[Nexys A7-50T](#)

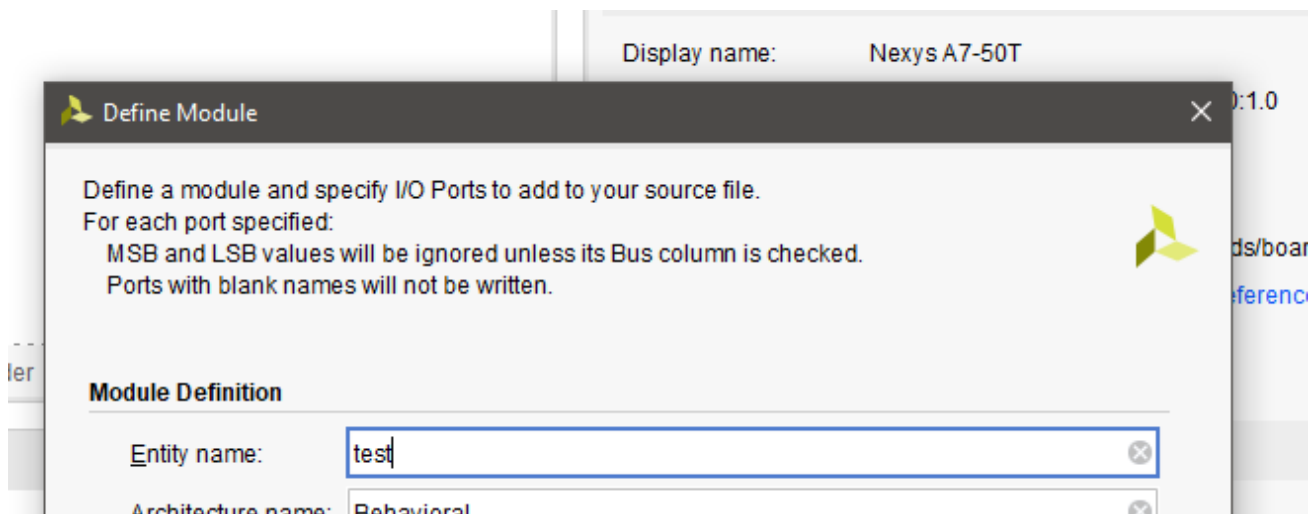
In Boards choose Nexys A7-50T and then click on Next>.

Finish the project summary.



Now

define module.



Add source => Add or create simulation sources and then click on Next>. Create a source

file and then click on Finish. Everything should be ready.

