1. Description

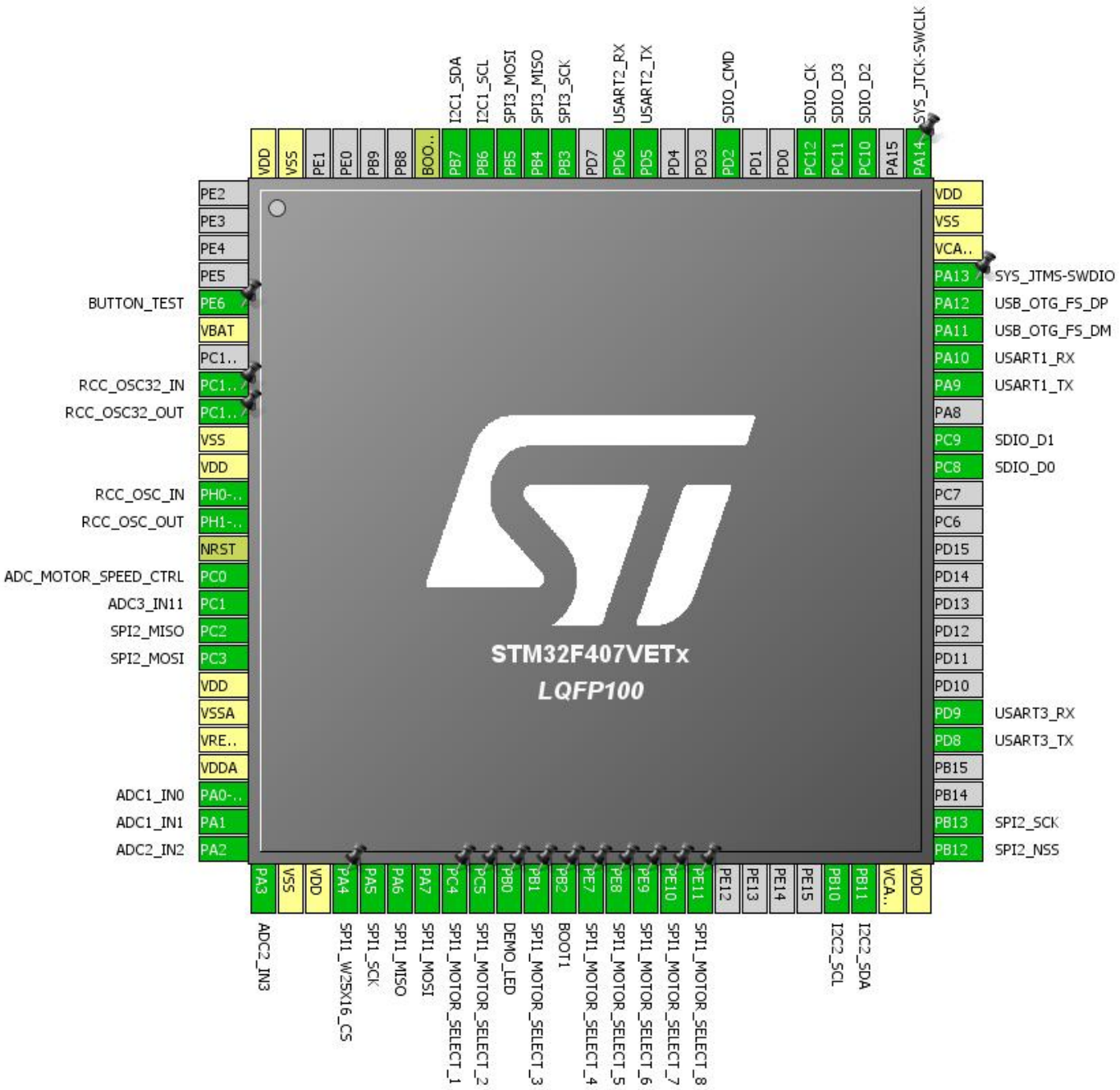
1.1. Project

Project Name	Brain
Board Name	Brain
Generated with:	STM32CubeMX 4.14.0
Date	05/10/2016

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



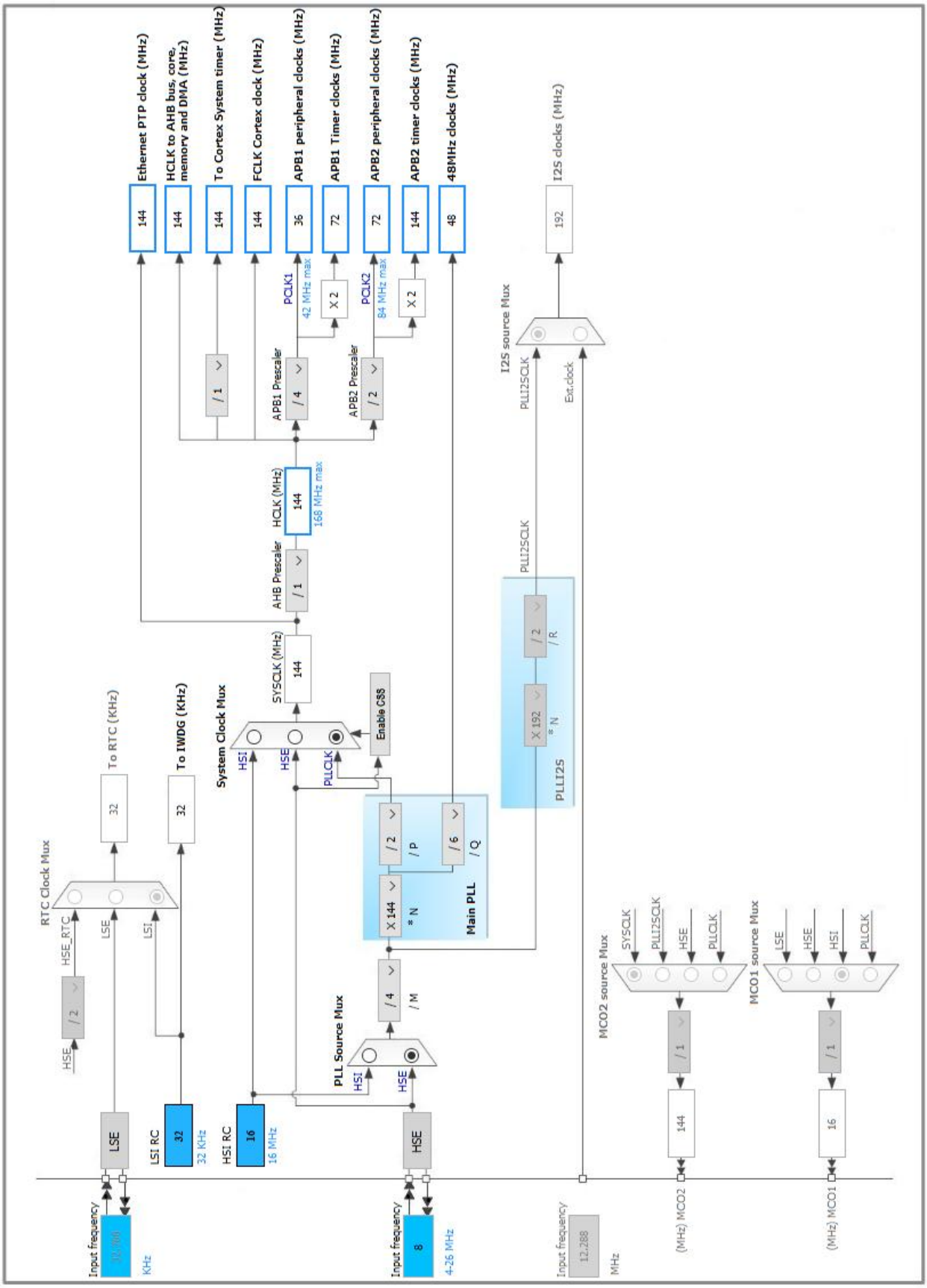
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
5	PE6 *	I/O	GPIO_Input	BUTTON_TEST
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC3_IN10	ADC_MOTOR_SPEED_CTRL
16	PC1	I/O	ADC3_IN11	
17	PC2	I/O	SPI2_MISO	
18	PC3	I/O	SPI2_MOSI	
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	
24	PA1	I/O	ADC1_IN1	
25	PA2	I/O	ADC2_IN2	
26	PA3	I/O	ADC2_IN3	
27	VSS	Power		
28	VDD	Power		
29	PA4 *	I/O	GPIO_Output	SPI1_W25X16_CS
30	PA5	I/O	SPI1_SCK	
31	PA6	I/O	SPI1_MISO	
32	PA7	I/O	SPI1_MOSI	
33	PC4 *	I/O	GPIO_Output	SPI1_MOTOR_SELECT_1
34	PC5 *	I/O	GPIO_Output	SPI1_MOTOR_SELECT_2
35	PB0 *	I/O	GPIO_Output	DEMO_LED
36	PB1 *	I/O	GPIO_Output	SPI1_MOTOR_SELECT_3
37	PB2 *	I/O	GPIO_Input	BOOT1
38	PE7 *	I/O	GPIO_Output	SPI1_MOTOR_SELECT_4
39	PE8 *	I/O	GPIO_Output	SPI1_MOTOR_SELECT_5
40	PE9 *	I/O	GPIO_Output	SPI1_MOTOR_SELECT_6

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
41	PE10 *	I/O	GPIO_Output	SPI1_MOTOR_SELECT_7
42	PE11 *	I/O	GPIO_Output	SPI1_MOTOR_SELECT_8
47	PB10	I/O	I2C2_SCL	
48	PB11	I/O	I2C2_SDA	
49	VCAP_1	Power		
50	VDD	Power		
51	PB12	I/O	SPI2_NSS	
52	PB13	I/O	SPI2_SCK	
55	PD8	I/O	USART3_TX	
56	PD9	I/O	USART3_RX	
65	PC8	I/O	SDIO_D0	
66	PC9	I/O	SDIO_D1	
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	SDIO_D2	
79	PC11	I/O	SDIO_D3	
80	PC12	I/O	SDIO_CK	
83	PD2	I/O	SDIO_CMD	
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
89	PB3	I/O	SPI3_SCK	
90	PB4	I/O	SPI3_MISO	
91	PB5	I/O	SPI3_MOSI	
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

mode: IN1

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 4 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN2

mode: IN3

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 4 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 2
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN10

mode: IN11

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 4 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	**Trigger detection on the rising edge ***
External Trigger Conversion Source	**Timer 2 Trigger Out event ***
Rank	1
Channel	Channel 10
Sampling Time	**28 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. CRC

mode: Activated

5.5. I2C1

I2C: I2C

5.5.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.6. I2C2

I2C: I2C

5.6.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.7. IWDG

mode: Activated

5.7.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

5.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.8.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.9. SDIO

Mode: MMC 4 bits Wide bus

5.10. SPI1

Mode: Full-Duplex Master

5.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**4.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	**Enabled ***
CRC Polynomial	X1+X3
NSS Signal Type	Software

5.11. SPI2

Mode: Full-Duplex Master
Hardware NSS Signal: Hardware NSS Output Signal

5.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

5.12. SPI3

Mode: Full-Duplex Master

5.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.13. SYS

Debug: Serial Wire Debug (SWD)

Timebase Source: TIM1

5.14. TIM2

Clock Source : Internal Clock

5.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**719 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	**Enable (sync between this TIM (Master) and its Slaves (through TRGO)) ***
Trigger Event Selection	**Update Event ***

5.15. TIM13

mode: Activated

5.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2000 ***
Internal Clock Division (CKD)	**Division by 4 ***

5.16. TIM14

mode: Activated

5.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

5.17. USART1

Mode: Asynchronous

5.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.18. USART2

Mode: Asynchronous

5.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.19. USART3

Mode: Asynchronous

5.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.20. USB_OTG_FS

Mode: Device_Only

5.20.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled

5.21. FATFS

mode: User-defined

5.21.1. Set Defines:

Version:

FATFS version	R0.11

Function Parameters:

FS_TINY (Tiny mode)	Disabled
FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FORWARD (Forward function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FASTSEEK (Fast seek function)	Enabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1 (Windows)

USE_LFN (Use Long Filename)	**Enabled with dynamic working buffer on the STACK ***
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	**Unicode ***
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
WORD_ACCESS (Platform dependent access option)	Byte access
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

5.22. FREERTOS

mode: Enabled

5.22.1. Config parameters:

Versions:

CMSIS-RTOS version	1.02
FreeRTOS version	8.2.1

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	**256 ***
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled

IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	**Enabled ***
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4
USE_ALTERNATIVE_API	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

USE_TRACE_FACILITY	Enabled
GENERATE_RUN_TIME_STATS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.22.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled

xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled

5.23. USB_DEVICE

Class For FS IP: Human Interface Device Class (HID)

5.23.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

5.23.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22315
PRODUCT_STRING (Product Identifier)	**Zulolo F Brain ***
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	HID Config
INTERFACE_STRING (Interface Identifier)	HID Interface

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA2	ADC2_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC0	ADC3_IN10	Analog mode	No pull-up and no pull-down	n/a	ADC_MOTOR_SPEED_CTRL
	PC1	ADC3_IN11	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**High ***	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**High ***	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
SPI3	PB3	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB4	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB5	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	
USART2	PD5	USART2_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PD6	USART2_RX	Alternate Function Push Pull	Pull-up	**High ***	
USART3	PD8	USART3_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PD9	USART3_RX	Alternate Function Push Pull	Pull-up	**High ***	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
GPIO	PE6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTTON_TEST
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_W25X16_CS
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_MOTOR_SELECT_1
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_MOTOR_SELECT_2
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEMO_LED
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_MOTOR_SELECT_3
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BOOT1
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_MOTOR_SELECT_4
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_MOTOR_SELECT_5
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_MOTOR_SELECT_6
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_MOTOR_SELECT_7
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_MOTOR_SELECT_8

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC3	DMA2_Stream0	Peripheral To Memory	Low

ADC3: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
Debug monitor	true	0	0
System tick timer	true	15	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
TIM8 update interrupt and TIM13 global interrupt	true	5	0
DMA2 stream0 global interrupt	true	5	0
USB On The Go FS global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
SPI3 global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	022152_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Brain
Project Folder	G:\Geek\Projects\Zulolo_F\Up\Code\ZuloloF_Brain\Brain
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.11.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No