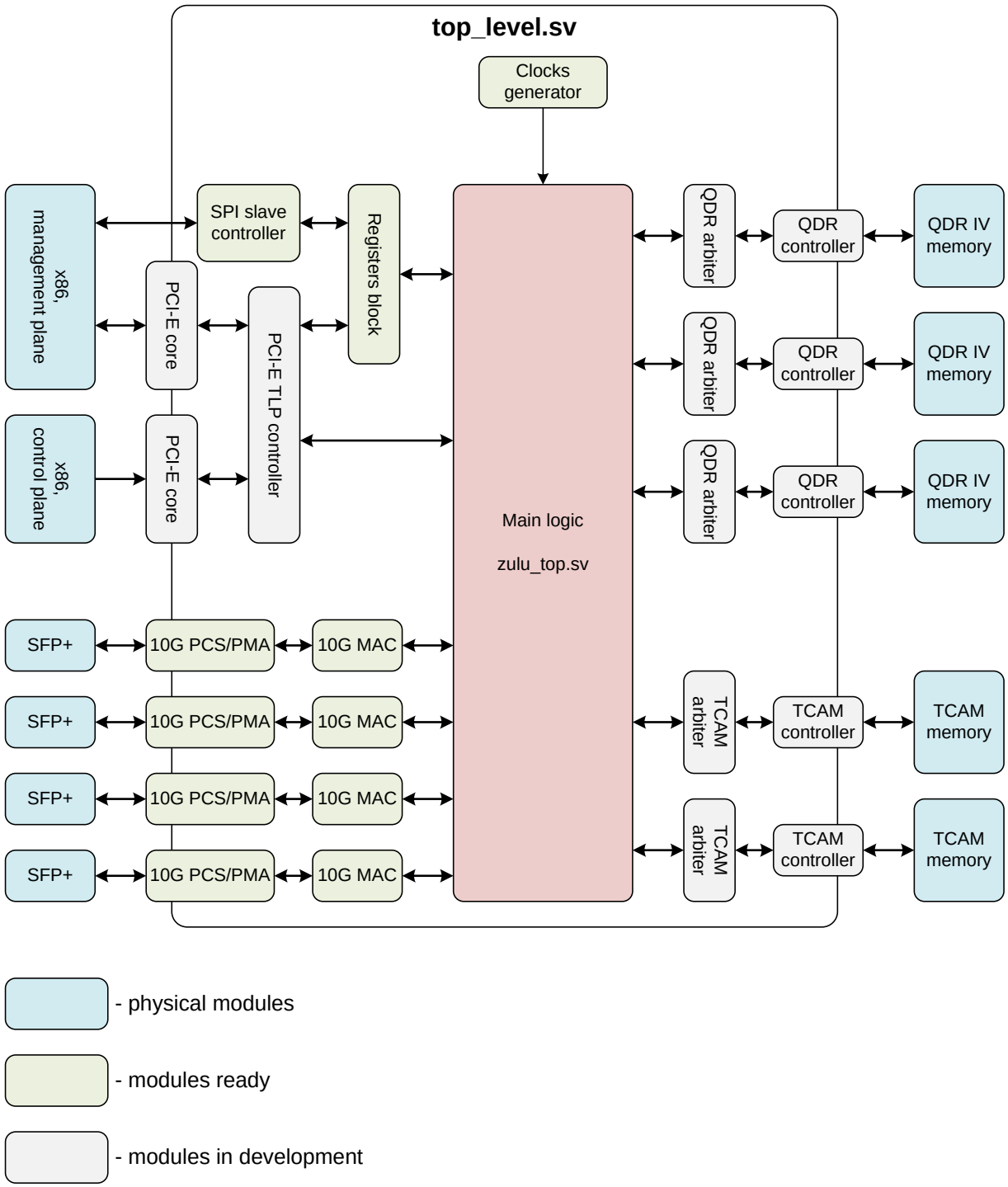
Top level architecture.



Design consists of number of common modules and one unique processing module.

Complete common modules are:

1. **Clocks generator** – provide necessary clocks. In initial design, generate 4 clocks:
   - 50 MHz for control signals.
   - 150 MHz for TCAM memory.
   - 156.25 MHz for 10G modules.
   - 200 MHz for main Zulu logic.

Can be reconfigured for design needs.

2. **SPI slave controller** – provide auxiliary access to control registers.
3. **Registers block** – stores current configuration and status. Support up to 65536 32-bit registers.
4. **10G PCS/PMA** and **10G MAC** – provide access to 10G interface. User interface – 64-bit AXI bus. These modules can be changed to 1G variant with the same interface.

Incomplete common modules are:

1. **PCI-E core** – standard Xilinx IP-core for PCI-E. Used for hi-speed communication with Management Plane and Control Plane.
2. **PCI-E TLP controller** – logic for PCI-E transaction generation with DMA support. Should provide two types of access – one is access to control registers, second is 64-bit AXI bus for data streams.
3. **QDR controller**, **QDR arbiter** – modules for access to QDR-IV memory devices.
4. **TCAM controller**, **TCAM arbiter** – modules for access to TCAM memory devices.

Common modules structure is hidden for main processing module, so development can be done separately for common and for unique modules.

Wrapper for top level of processing module (***zulu_top.sv***) is provided. It held all interface ports and parameters, that available at this moment.