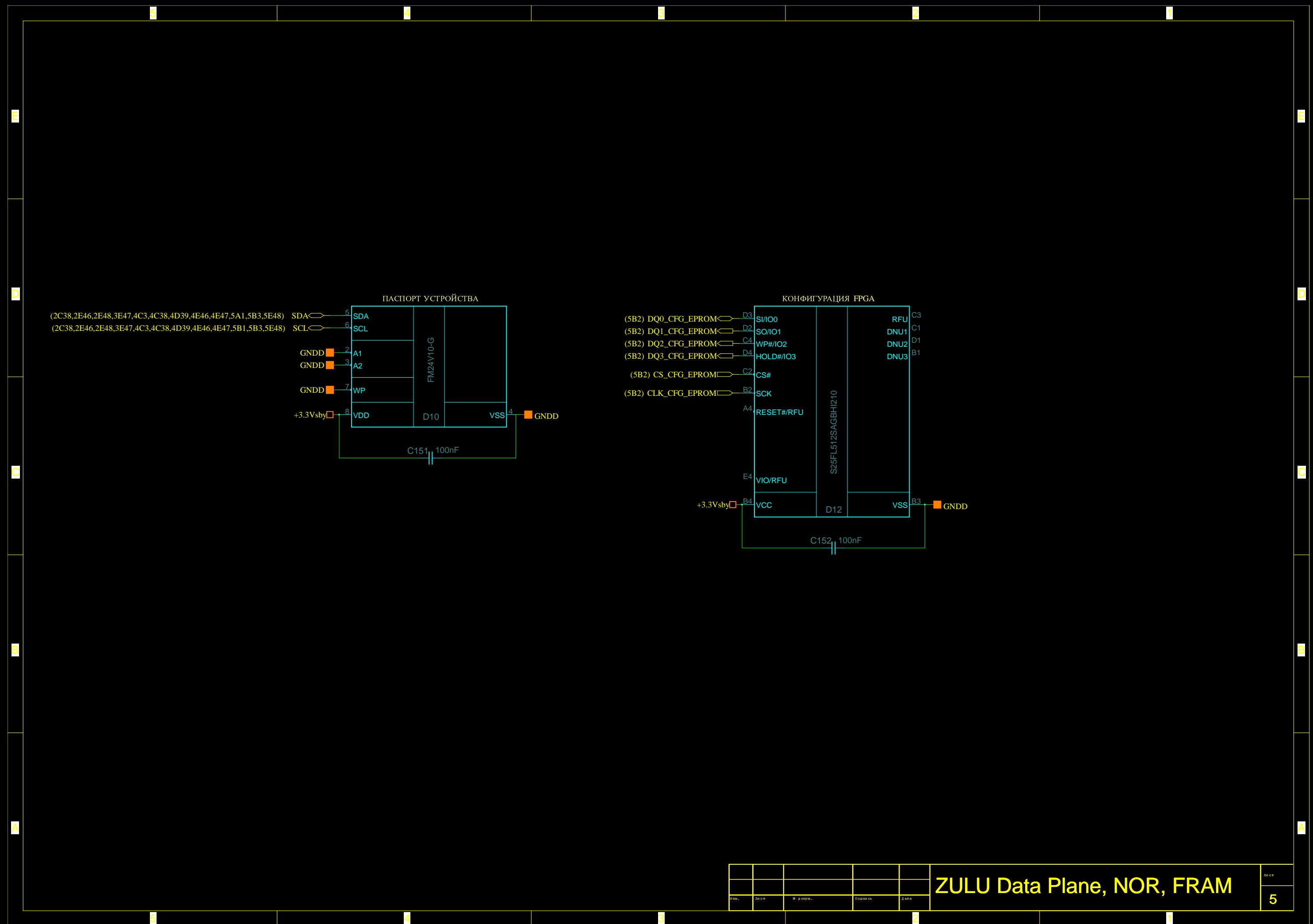
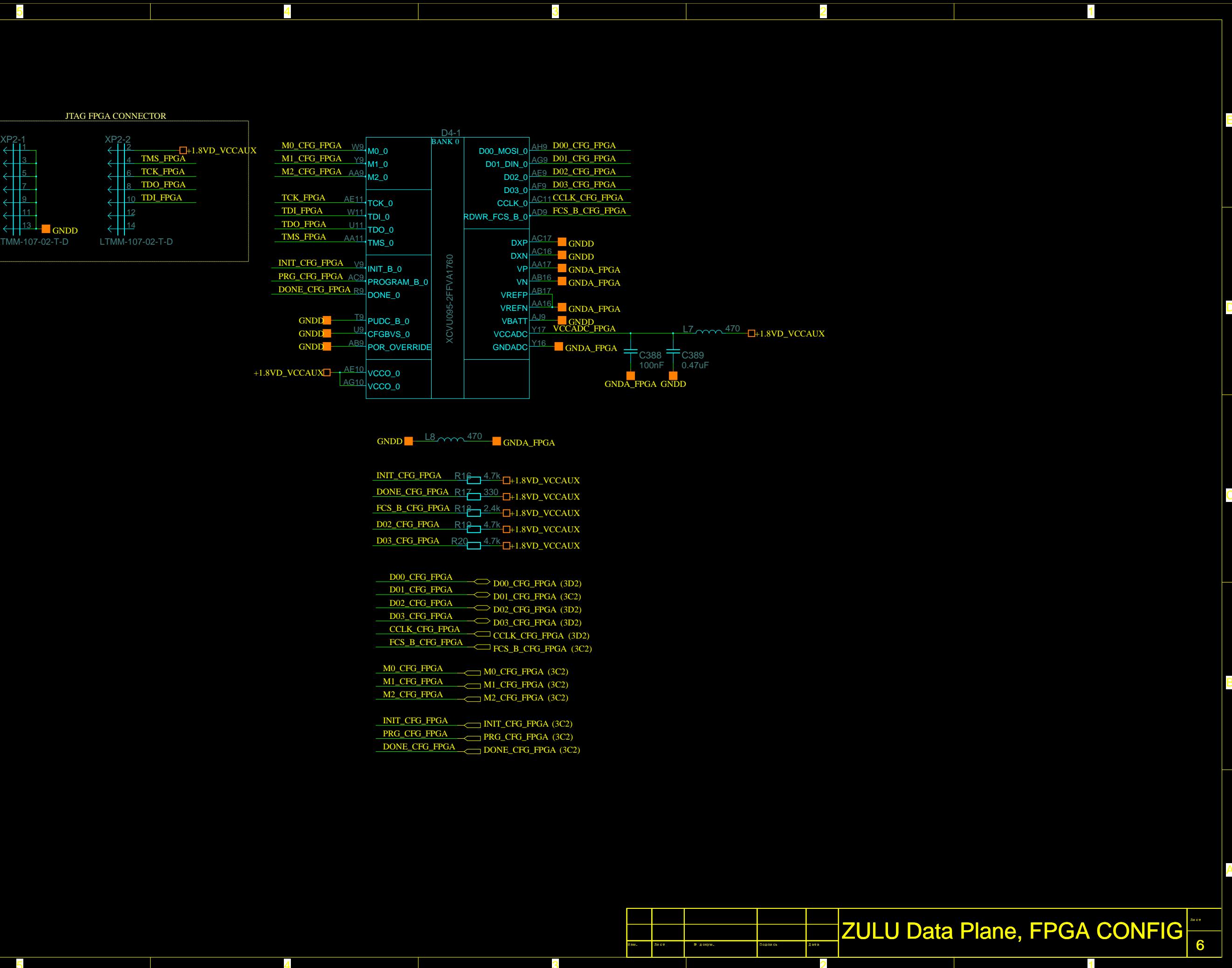


ZULU Data Plane, Oscillators

5 4 3 2 1







5

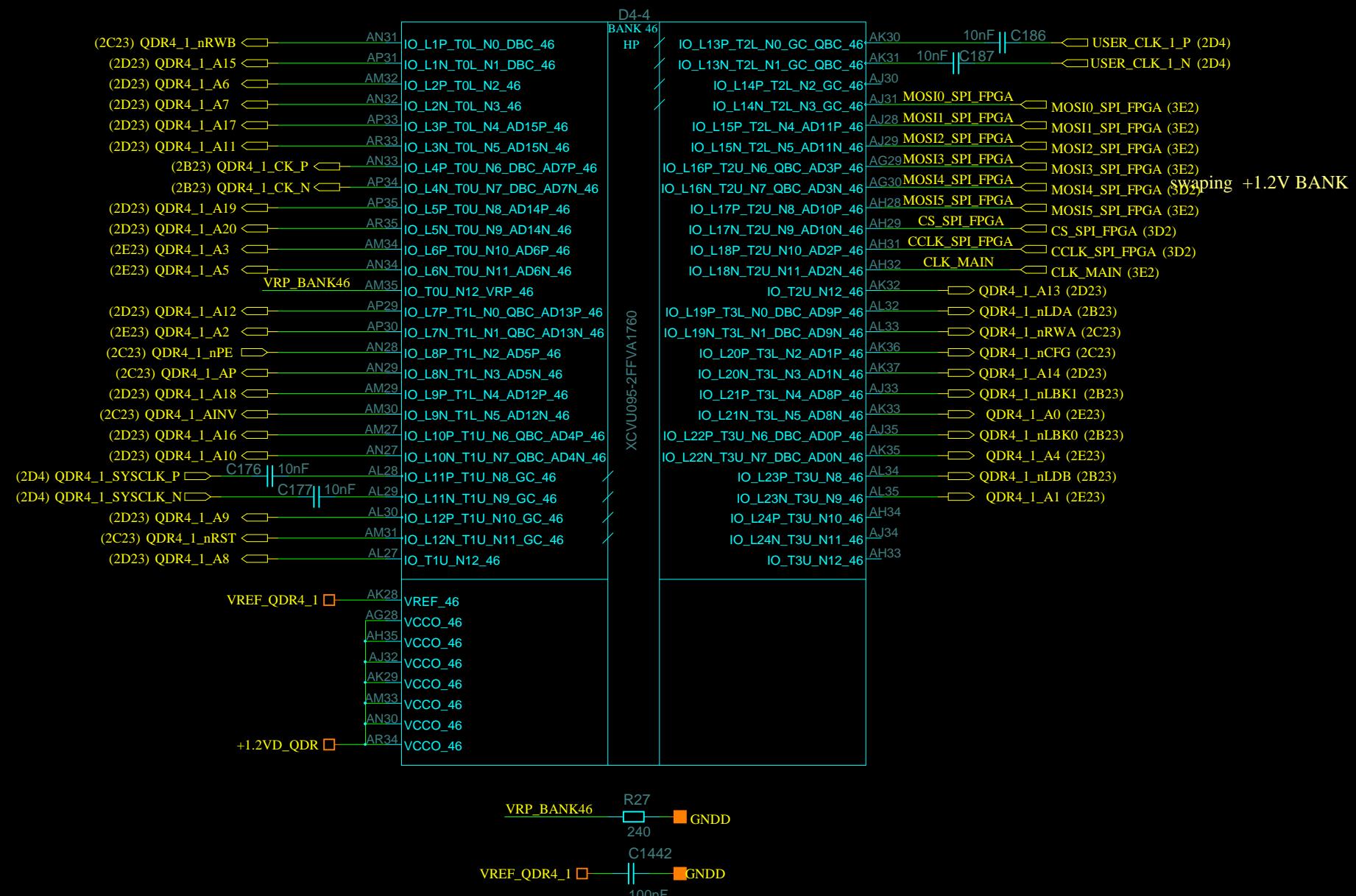
4

3

2

1

FPGA Banks 46  
QDRIV-1 Address/CTRL  
Power: 1.2V



ZULU Data Plane, FPGA QDR1

5

4

3

2

1

5

4

3

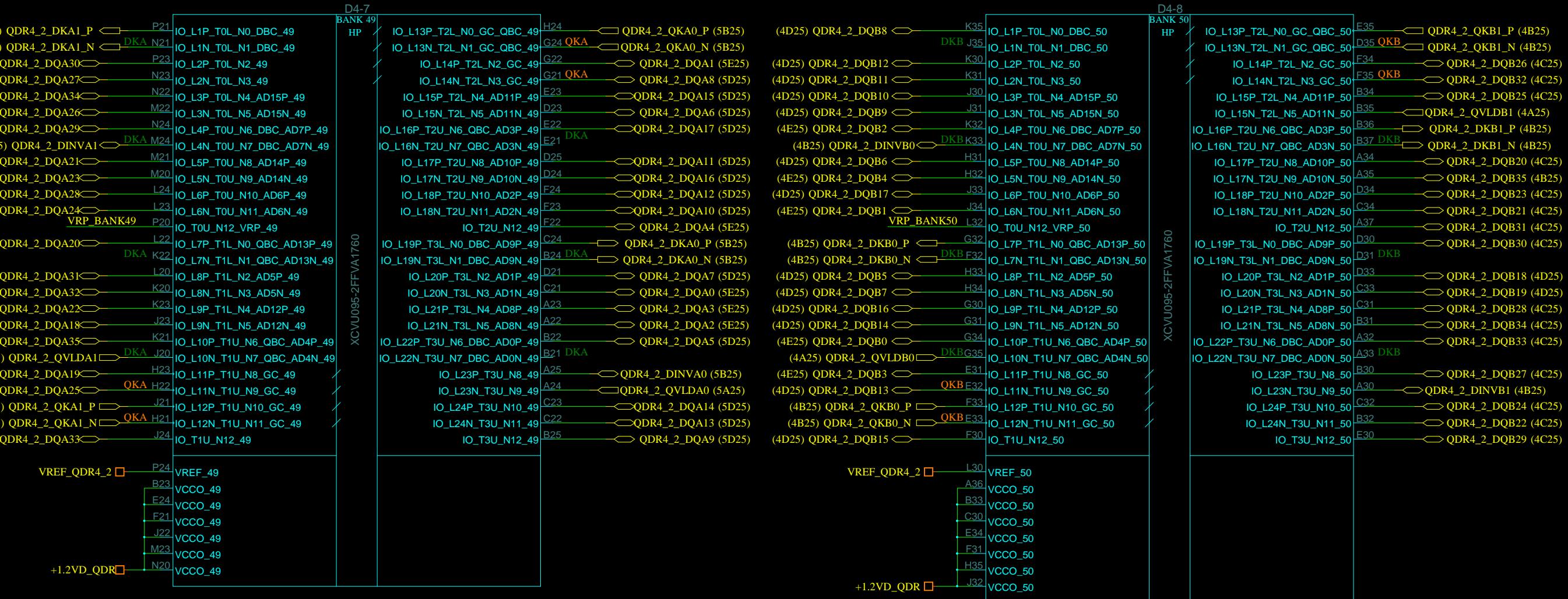
2

1

## FPGA Banks 49/50

QDRIV-2 Data

Power: 1.2V



5	4	3	2	1

ZULU Data Plane, FPGA QDR2

9

5

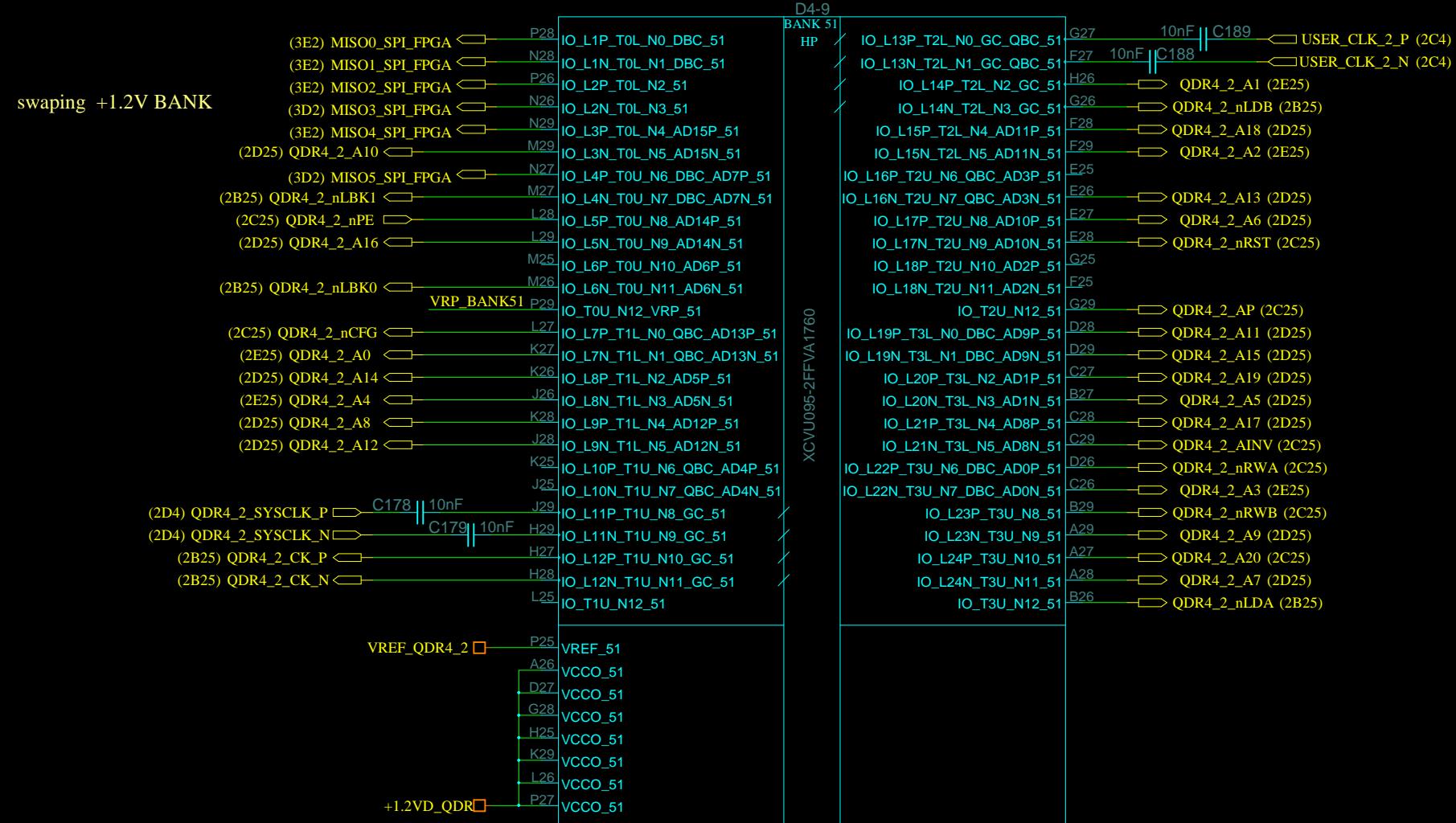
4

3

2

1

FPGA Banks 51  
QDRIV-2 Address/CTRL  
Power: 1.2V



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ZULU Data Plane, FPGA QDR2

10

5

4

3

2

1

FPGA Banks 66/67  
QDRIV-3 Data

Power: 1.2V

E

F



5

4

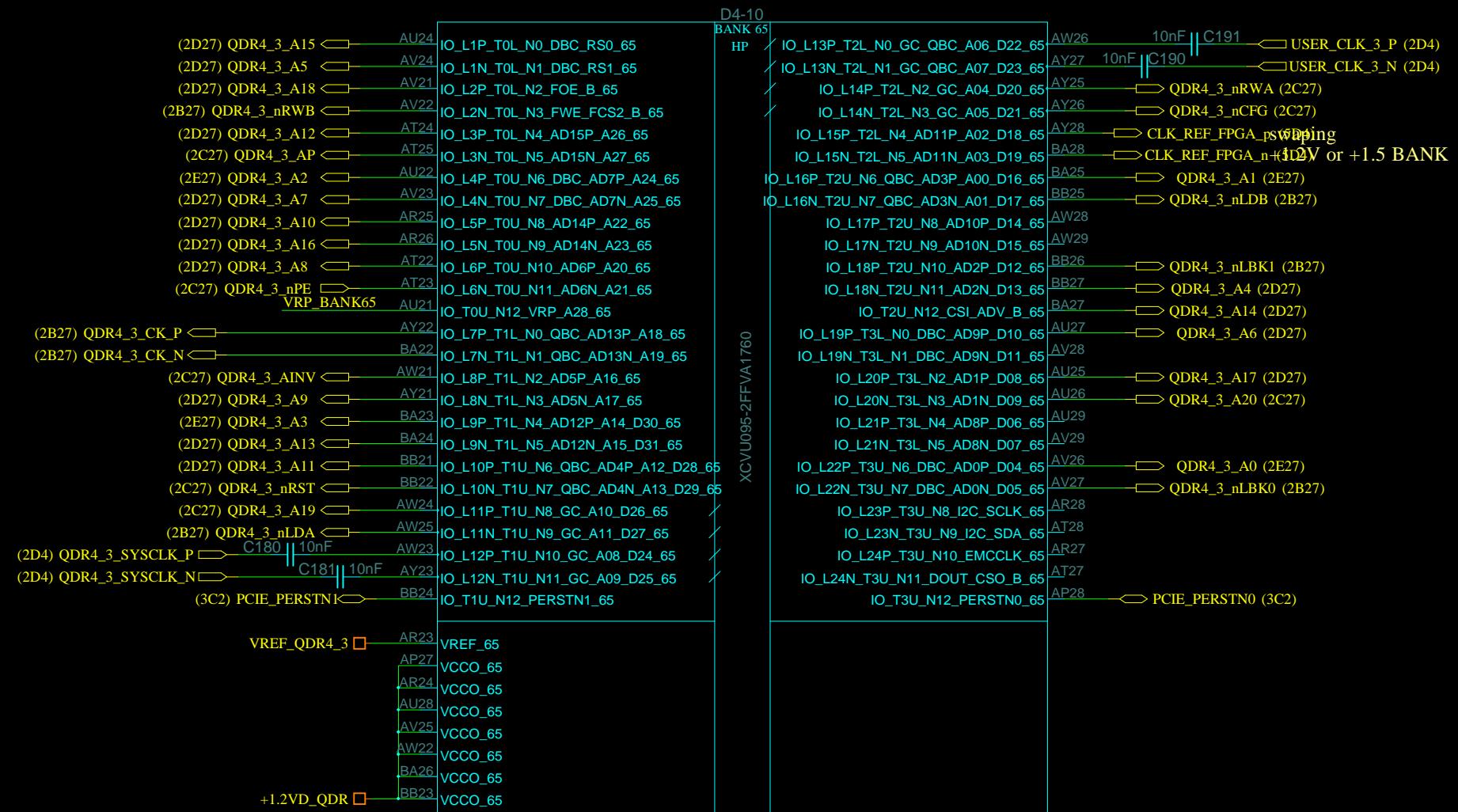
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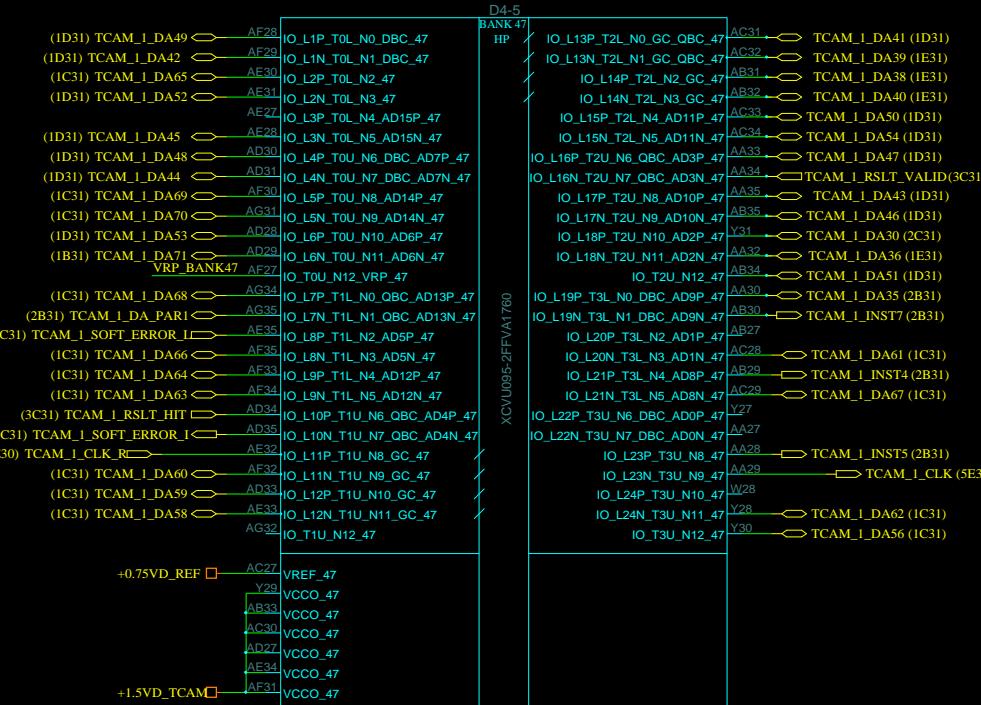
1

FPGA Banks 65  
QDRIV-3 Address/CTRL  
Power: 1.2V

PERSTN[0:1] Default reset pin locations for the integrated block for PCI Express.



FPGA Banks 47/48  
TCAM-1 Block-1  
Power: +1.5V



5

4

3

2

1

FPGA Banks 94  
TCAM-1 Block-2  
Power: +1.5V



C469  
+0.75VD\_REF || GNDD  
100nF

5	4	3	2	1
5	4	3	2	1
5	4	3	2	1
5	4	3	2	1

ZULU Data Plane, FPGA TCAM1

14

5

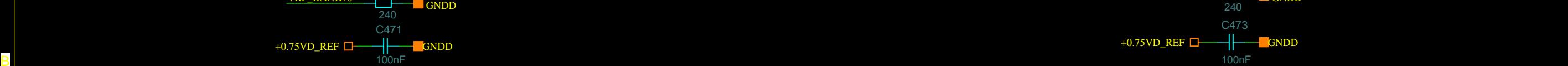
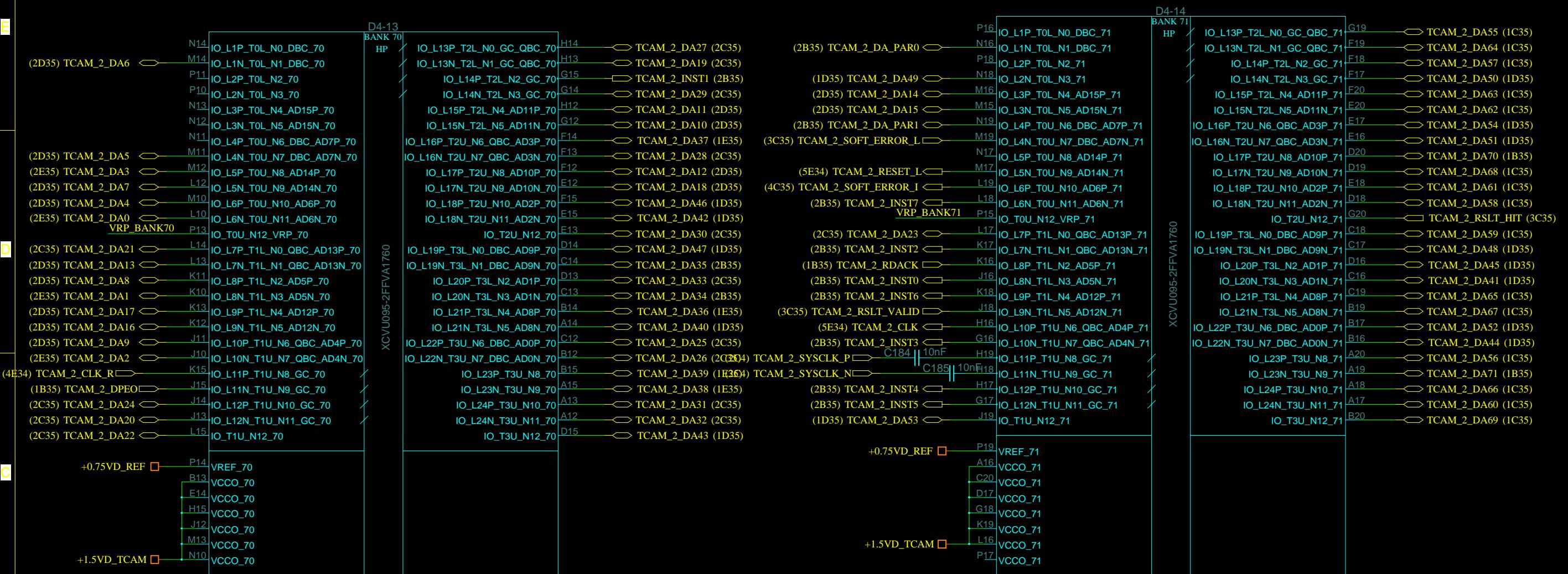
4

3

2

1

FPGA Banks 70/71  
TCAM-2 Block-1  
Power: +1.5V



5	4	3	2	1

ZULU Data Plane, FPGA TCAM2

5

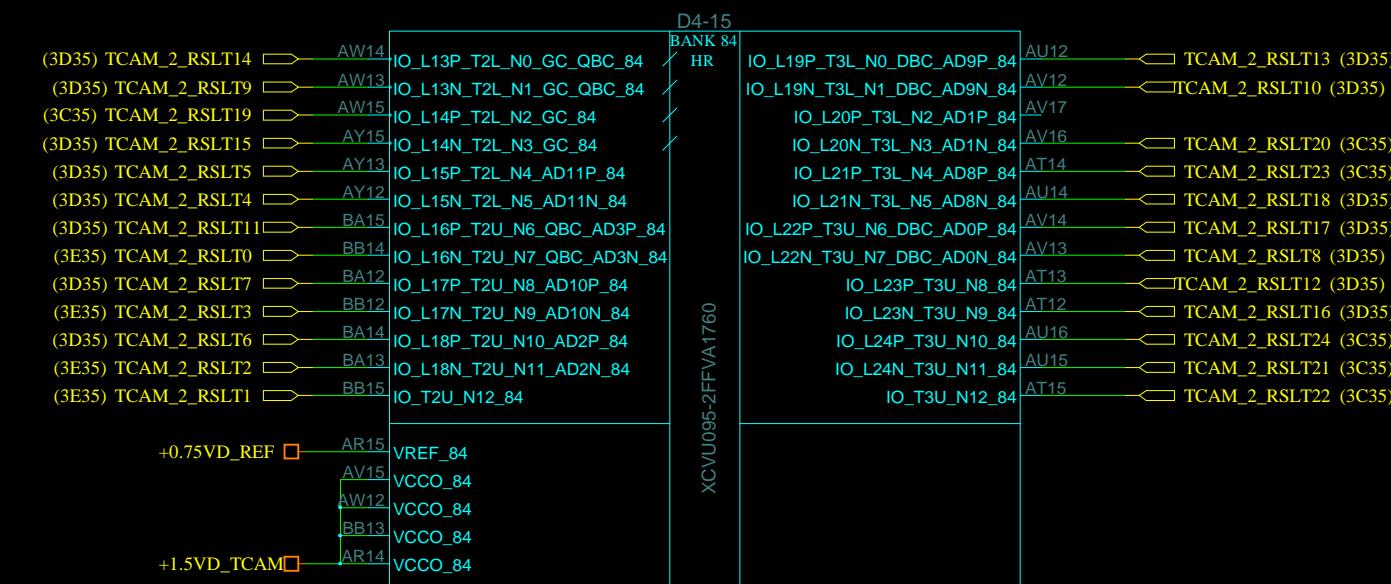
4

3

2

1

FPGA Banks 84  
TCAM-2 Block-2  
Power: +1.5V



C475  
+0.75VD\_REF → GNDD  
100nF

Power	Reset	Sync	Normal	Data

ZULU Data Plane, FPGA TCAM2

16

5

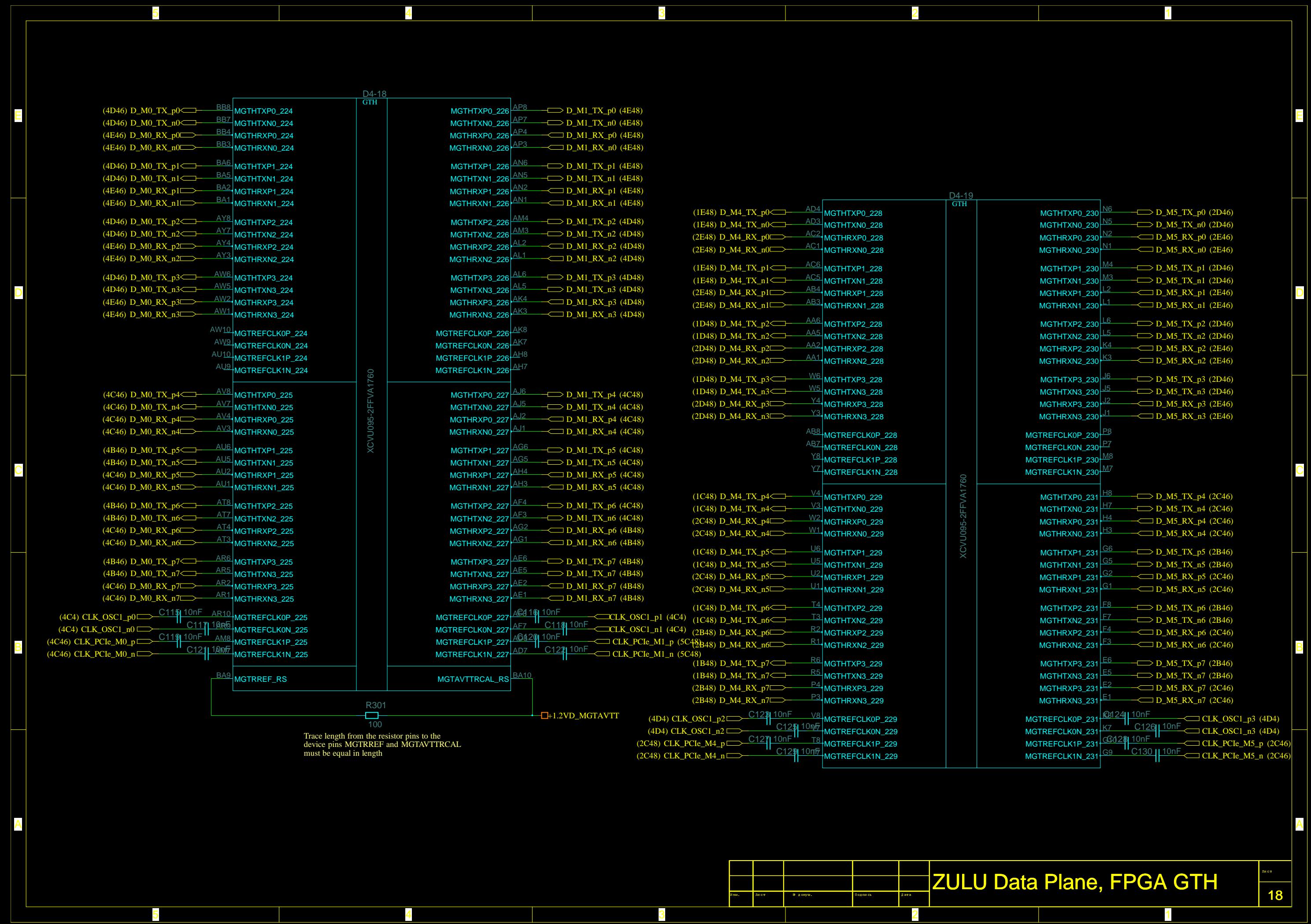
4

3

2

1







5

4

3

2

1

H

D

C

B

A

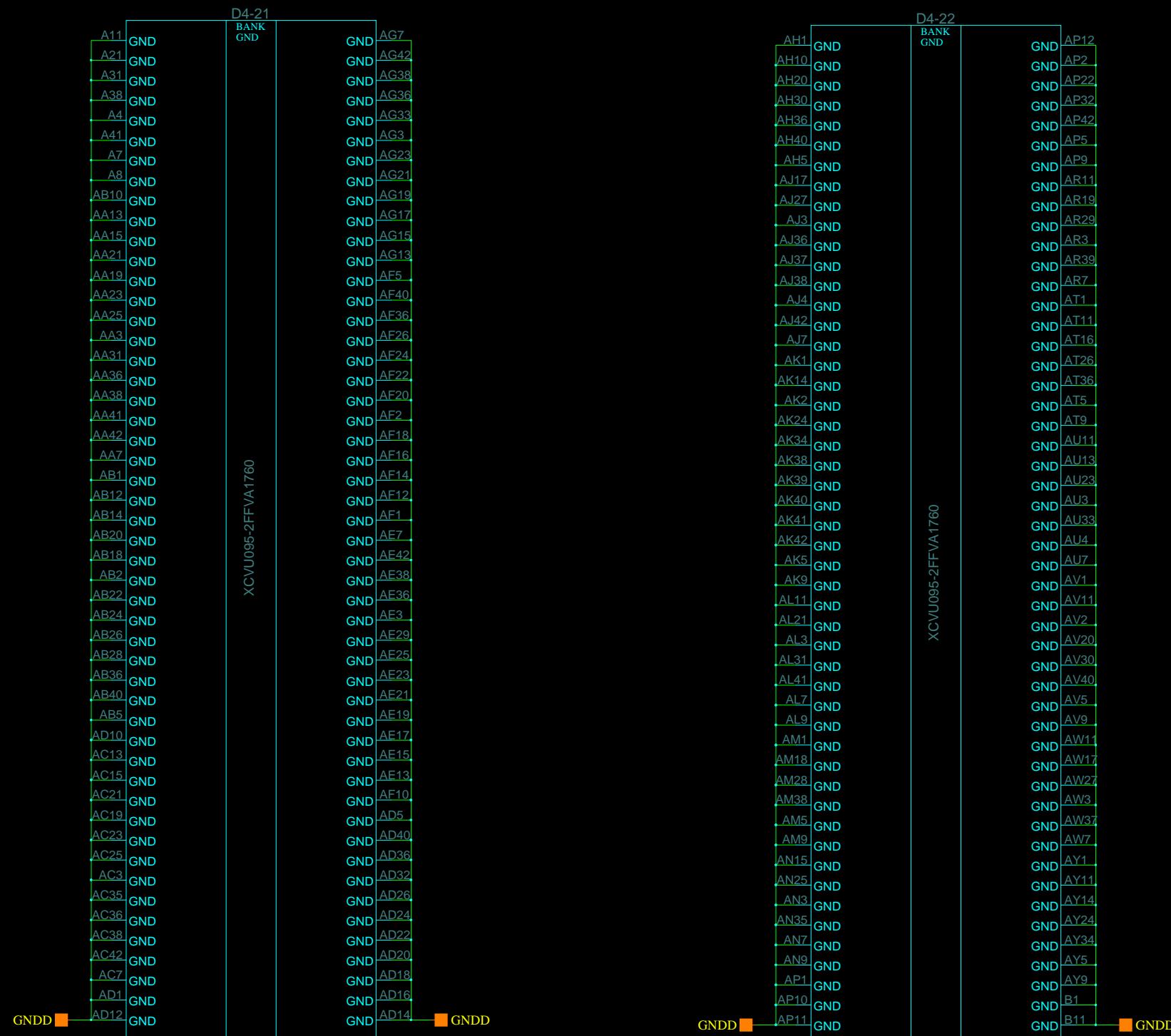
H

D

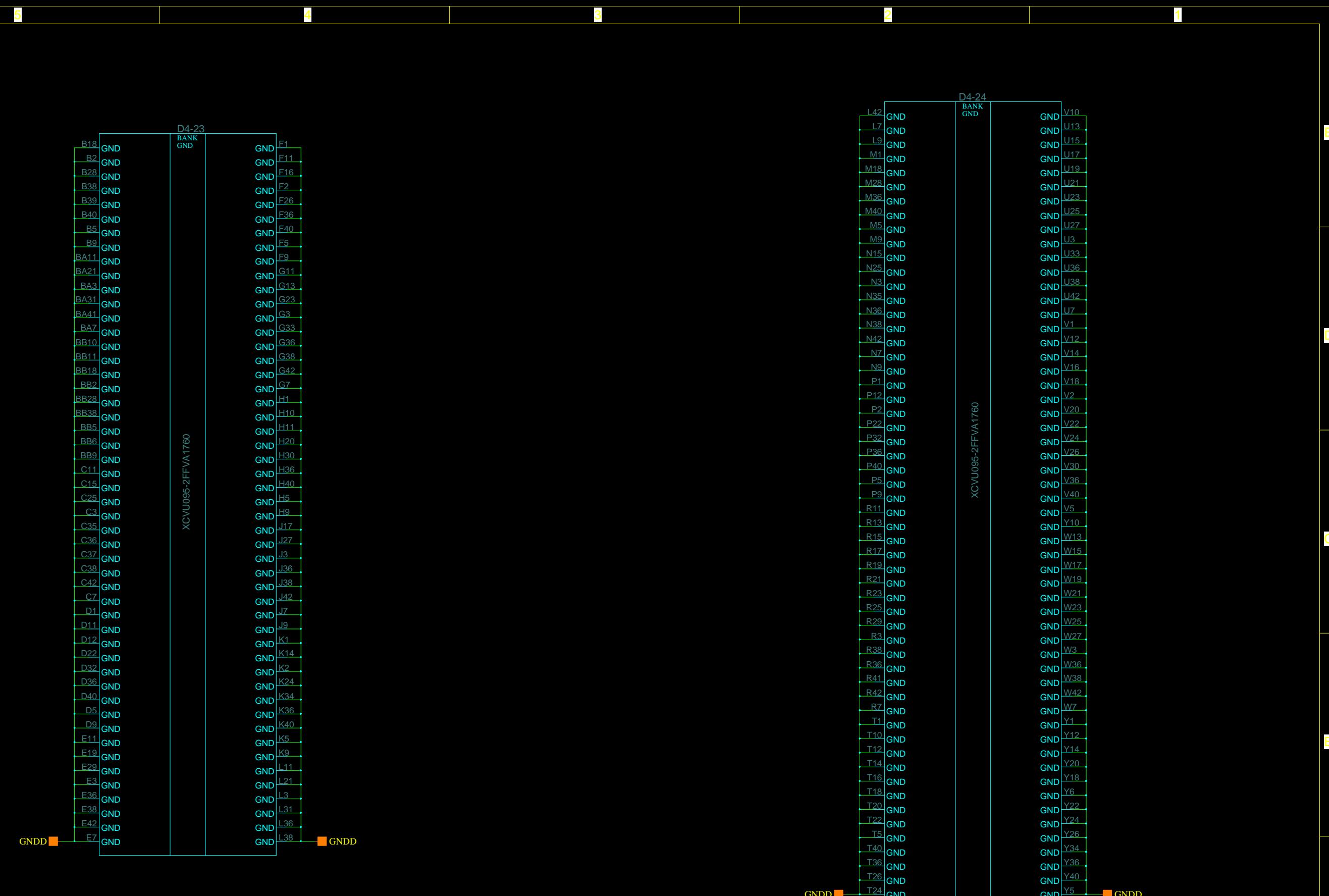
C

B

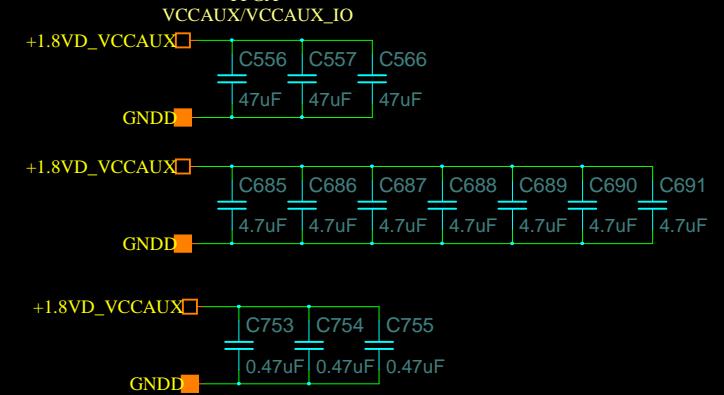
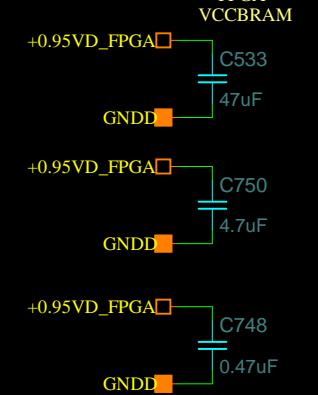
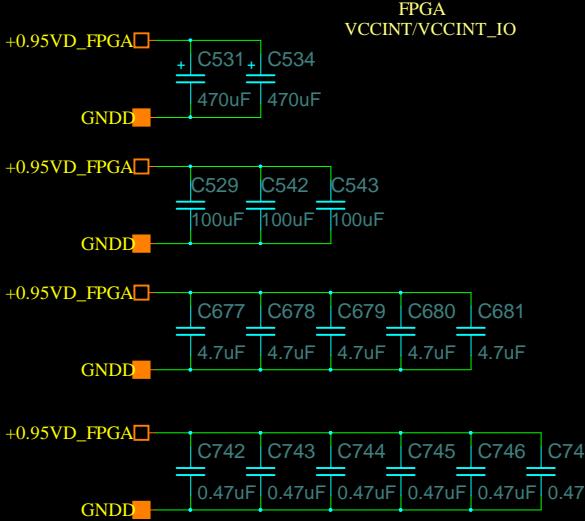
A



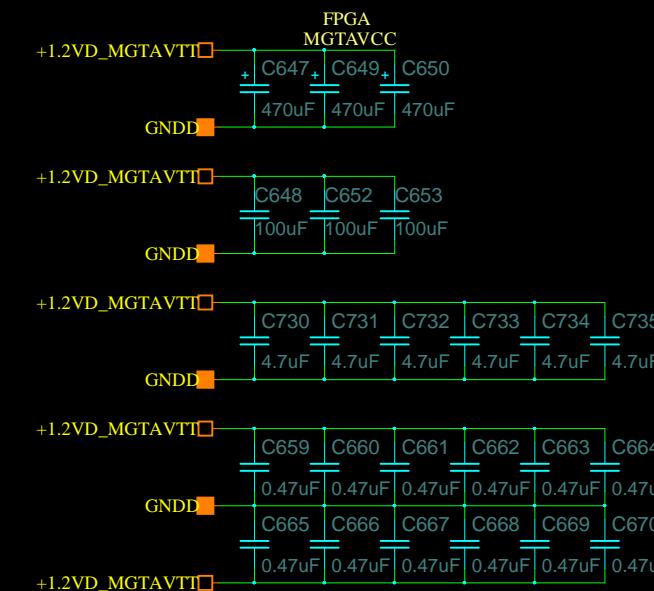
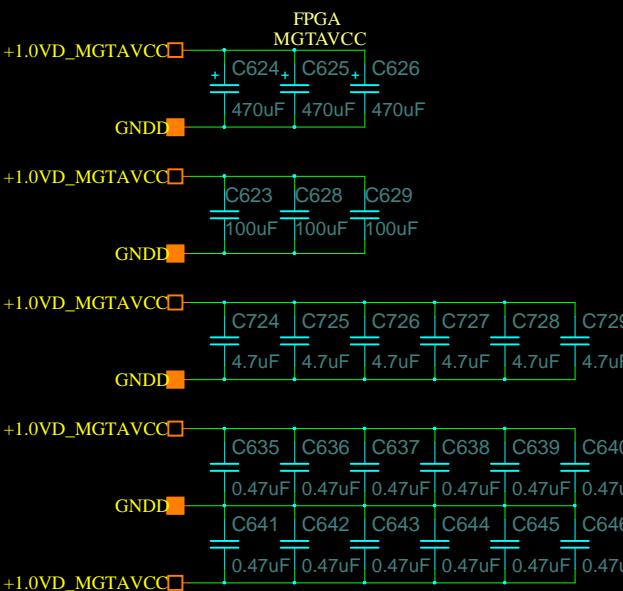
					ZULU Data Plane, FPGA GND	20
5	4	3	2	1		



ZULU Data Plane, FPGA GND



**2**



ZULU Data Plane, FPGA Decoup.

22

5

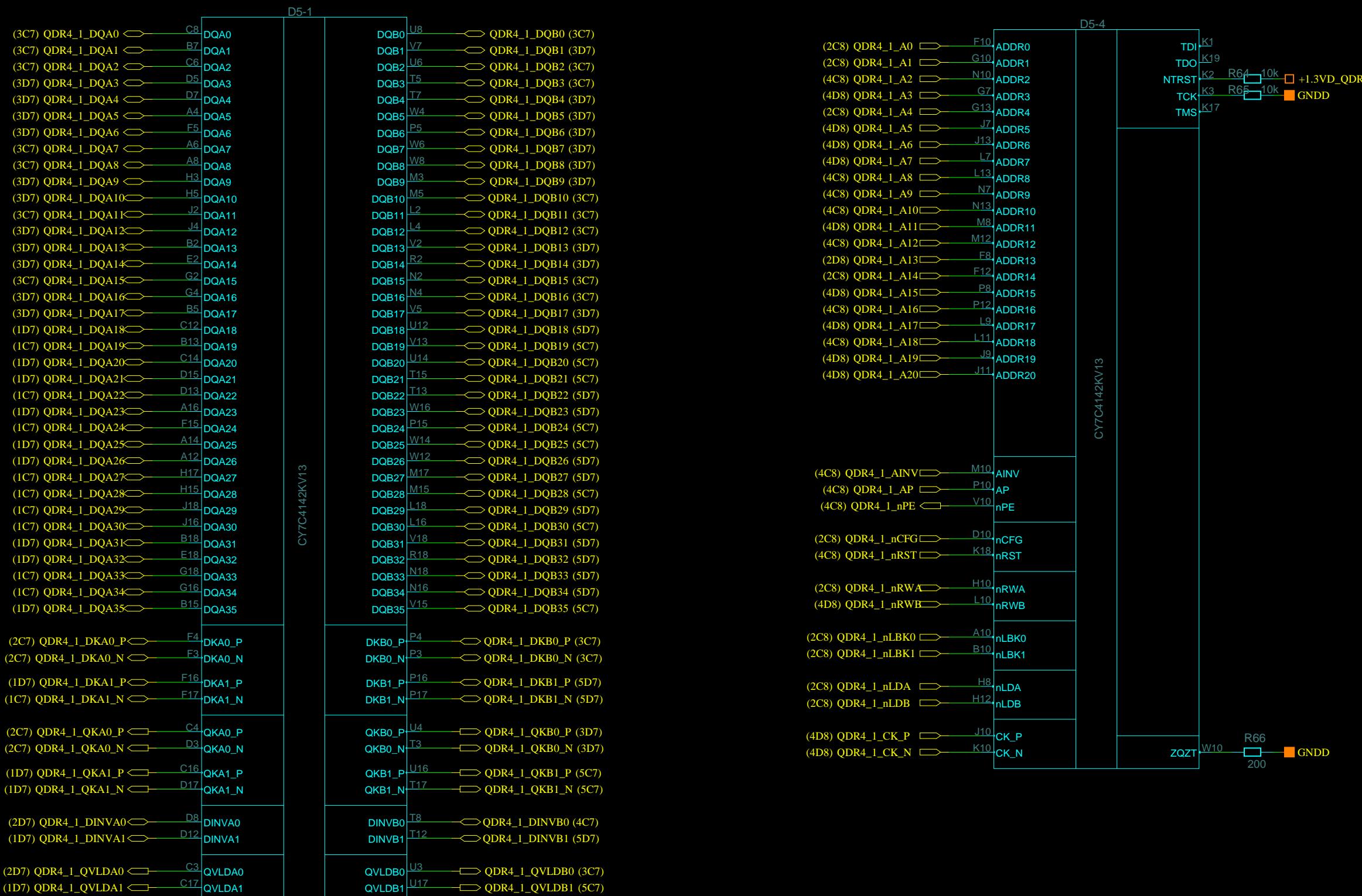
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3

2

1

**QDR IV**  
Memory - 1 Block - 1





5

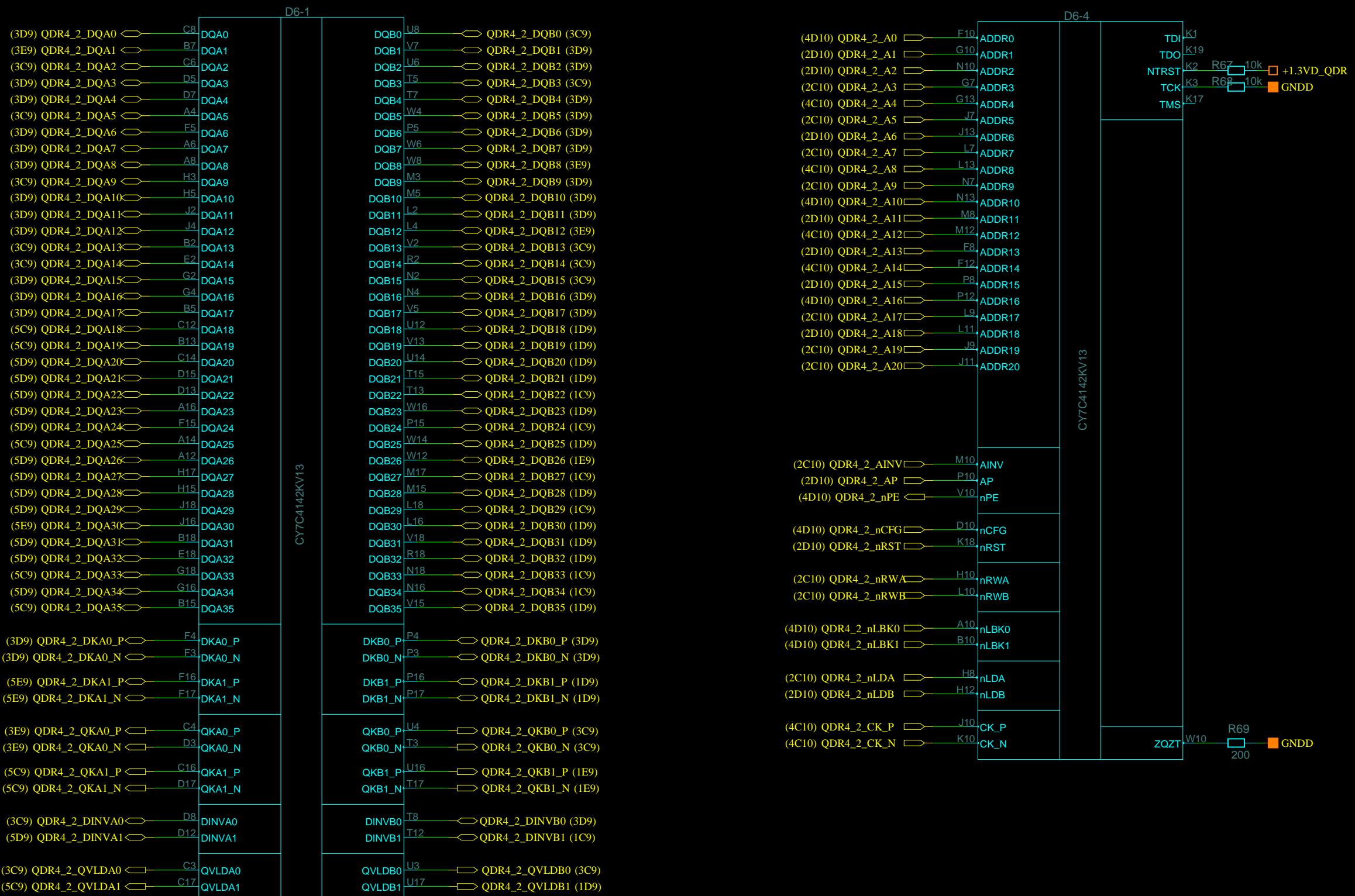
4

3

2

1

QDR IV  
Memory - 2 Block - 1



5	4	3	2	1

**ZULU Data Plane, QDR 2**

5 4 3 2 1

QDR IV  
Memory - 2 Block - 2  
POWER

Power: +1.2V, +1.3V, +1.2/2V

D6-2

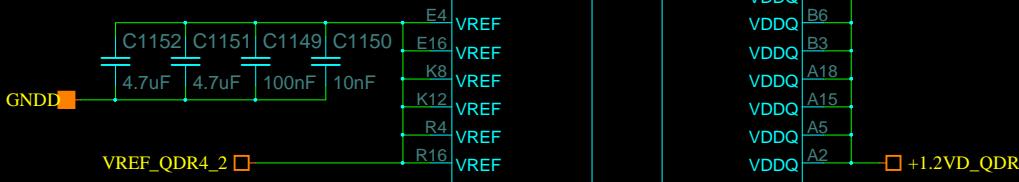
B1	VDD	VDDQ	W18
B9	VDD	VDDQ	W15
B11	VDD	VDDQ	W5
B19	VDD	VDDQ	W2
D1	VDD	VDDQ	V17
D9	VDD	VDDQ	V14
D11	VDD	VDDQ	V12
D19	VDD	VDDQ	V8
E8	VDD	VDDQ	V6
E10	VDD	VDDQ	V3
E12	VDD	VDDQ	U18
F9	VDD	VDDQ	U13
F11	VDD	VDDQ	U10
G6	VDD	VDDQ	U7
G14	VDD	VDDQ	U2
H1	VDD	VDDQ	T16
H19	VDD	VDDQ	T4
J6	VDD	VDDQ	R17
J14	VDD	VDDQ	R14
K5	VDD	VDDQ	R6
K15	VDD	VDDQ	R3
L6	VDD	VDDQ	P19
L8	VDD	VDDQ	P13
L12	VDD	VDDQ	P7
L14	VDD	VDDQ	P1
M1	VDD	VDDQ	N15
M19	VDD	VDDQ	N5
N6	VDD	VDDQ	M11
N14	VDD	VDDQ	M9
P9	VDD	VDDQ	L17
P11	VDD	VDDQ	L3
R8	VDD	VDDQ	K11
R10	VDD	VDDQ	K9
R12	VDD	VDDQ	J17
T1	VDD	VDDQ	J3
T9	VDD	VDDQ	H11
T11	VDD	VDDQ	H9
T19	VDD	VDDQ	G15
V1	VDD	VDDQ	G5
V9	VDD	VDDQ	F19
V11	VDD	VDDQ	F13
V19	VDD	VDDQ	F7
K7	VDD	VDDQ	F1
K13	VDD	VDDQ	E17
+1.3VD_QDR	□		VDDQ

CY7C4142KV13

D6-3

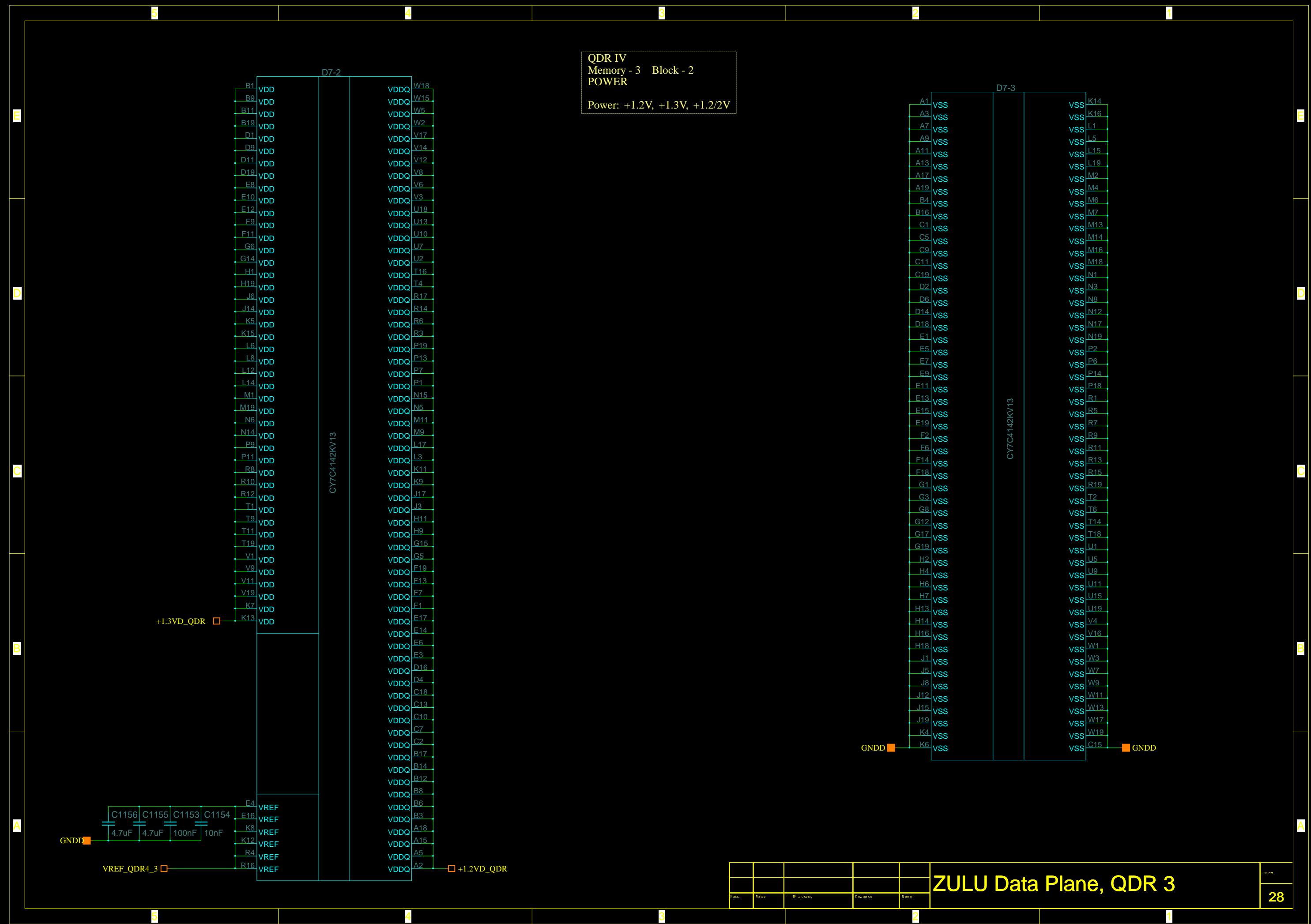
A1	VSS	K14
A3	VSS	K16
A7	VSS	L1
A9	VSS	L5
A11	VSS	L15
A13	VSS	L19
A17	VSS	M2
A19	VSS	M4
B4	VSS	M6
B16	VSS	M7
C1	VSS	M13
C5	VSS	M14
C9	VSS	M16
C11	VSS	M18
C19	VSS	N1
D2	VSS	N3
D6	VSS	N8
D14	VSS	N12
D18	VSS	N17
E1	VSS	N19
E5	VSS	P2
E7	VSS	P6
E9	VSS	P14
E11	VSS	P18
E13	VSS	R1
E15	VSS	R5
E19	VSS	R7
F2	VSS	R9
F6	VSS	R11
F14	VSS	R13
F18	VSS	R15
G1	VSS	R19
G3	VSS	T2
G8	VSS	T6
G12	VSS	T14
G17	VSS	T18
G19	VSS	U1
H2	VSS	U5
H4	VSS	U9
H6	VSS	U11
H7	VSS	U15
H13	VSS	U19
H14	VSS	V4
H16	VSS	V16
H18	VSS	W1
J1	VSS	W3
J5	VSS	W7
J8	VSS	W9
J12	VSS	W11
J15	VSS	W13
J19	VSS	W17
K4	VSS	W19
K6	VSS	C15
GNDD	□	GNDD

CY7C4142KV13



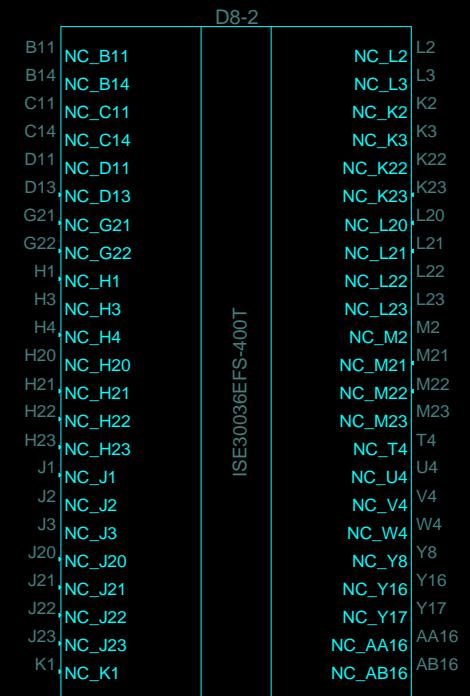
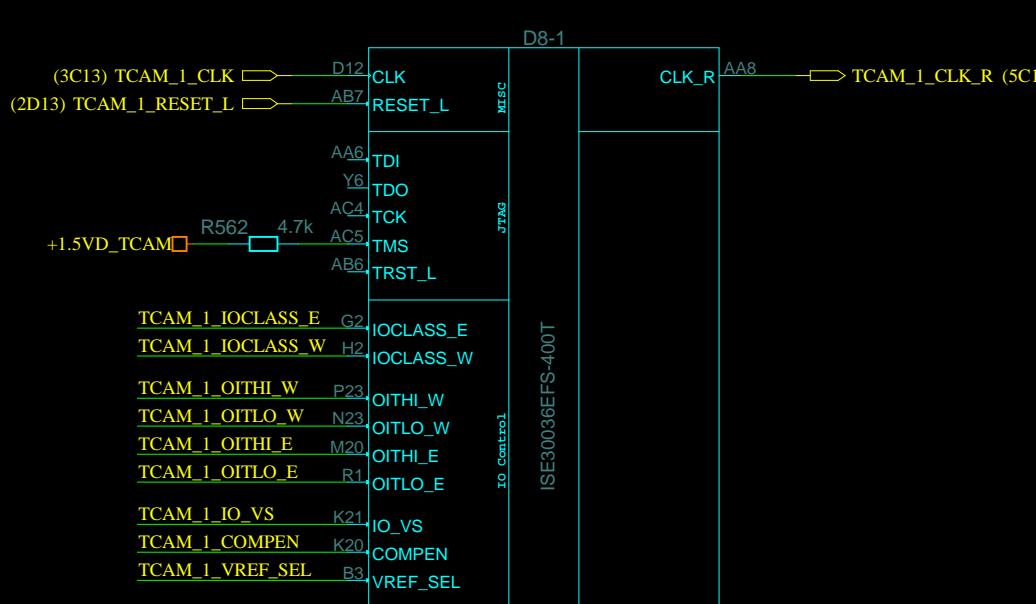
26







Note:  
 For "T" application type device:  
 25 Ohm impedance condition:  
 IOCLASS\_\* = 1 , COMPEN= 1 , OITHI\_\* , OITLO\_\* connect to 50 Ohms  
 50 Ohm impedance condition:  
 IOCLASS\_\* = 0 , COMPEN= 1 , OITHI\_\* , OITLO\_\* connect to 100 Ohms



**TCAM end termination:**

TCAM\_1\_CLK → R526 (100) → GNDD

FPGA end termination:

TCAM\_1\_CLK\_R → R528 (100) → GNDD

**IO class configuration.** Select output drive strength for DA\_BUS, DA\_PAR, RSLT\_BUS, Result Valid and Flags.

TCAM\_1\_IOCLASS\_E → R534 (49.9) → R535 (49.9) → GNDD

TCAM\_1\_IOCLASS\_W → R536 (49.9) → R537 (49.9) → GNDD

**Output Impedance Tuning:** This input signal, along with OITLO\_W is used to tune the device outputs to the system data bus impedance. OITHI\_W's pull-up output impedance is set to 1.0x R0\_W, where R0\_W is a resistor from this pin to ground. We require a 100 or 50 Ohm high precision 1% resistor to be used for R0\_W and R1\_W

TCAM\_1\_OITHI\_W → R538 (100) → 50 or 100 Ohm → GNDD

TCAM\_1\_OITLO\_W → R539 (100) → 50 or 100 Ohm → +1.5VD\_TCAM

**Output Impedance Tuning:** This input signal, along with OITHI\_E is used to tune the device outputs to the system data bus impedance. OITLO\_E's pull-down output impedance is set to 1.0x R1\_E, where R1\_E is a resistor from this pin to ground. We require a 100 or 50 Ohm high precision 1% resistor to be used for R0\_E and R1\_E

TCAM\_1\_OITHI\_E → R540 (100) → 50 or 100 Ohm → GNDD

TCAM\_1\_OITLO\_E → R541 (100) → 50 or 100 Ohm → +1.5VD\_TCAM

**Output Impedance Tuning Configuration:** Configure impedance tuning options: COMPEN=0 selects no impedance tuning COMPEN=1 selects impedance tuning

TCAM\_1\_COMPEN → R543 (49.9) → R542 (49.9) → GNDD

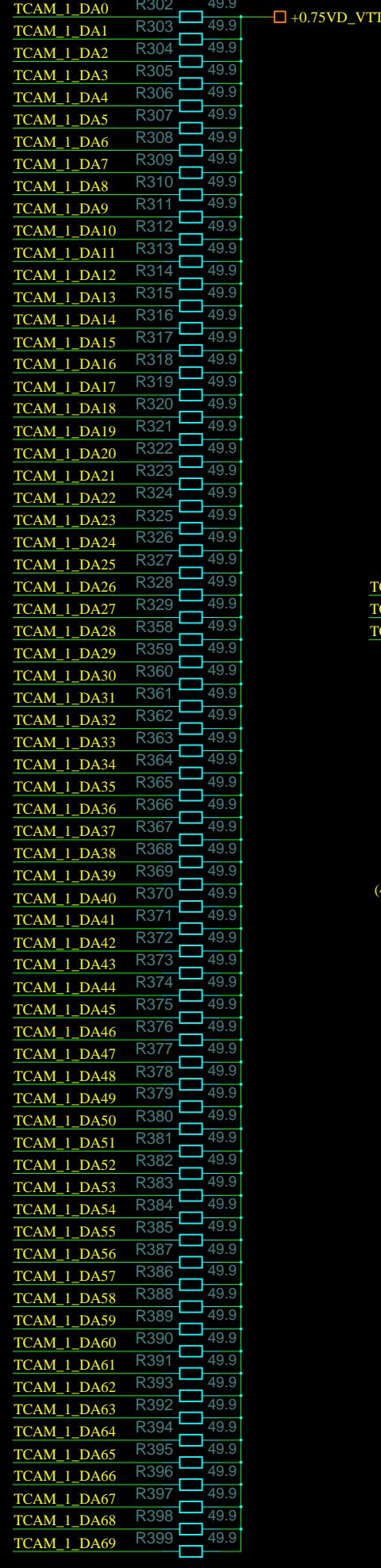
TCAM\_1\_VREF\_SEL → R545 (49.9) → R544 (49.9) → GNDD

**Reference Select:** Select internal or external reference voltage supply for HSTL IOs  
 0: for internal reference voltage  
 1: for external reference voltage

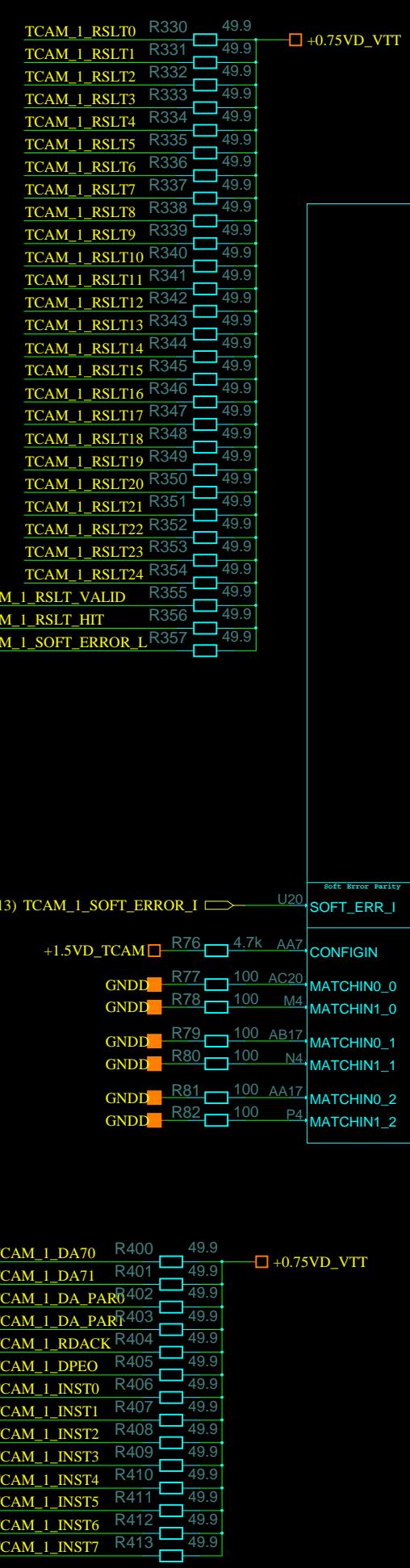
**IO Voltage Control:**  
 0: 1.5V HSTL  
 1: Reserved  
 This pin is required to be pulled down to ground

TCAM\_1\_IO\_VS → R546 (49.9) → GNDD

5



5



4

FPGA end termination:  
TCAM\_1\_RSLT[0:24]  
TCAM\_1\_RSLT\_VALID  
TCAM\_1\_RSLT\_HIT  
TCAM\_1\_SOFT\_ERROR\_L  
TCAM\_1\_RDACK  
TCAM\_1\_DPEO

3

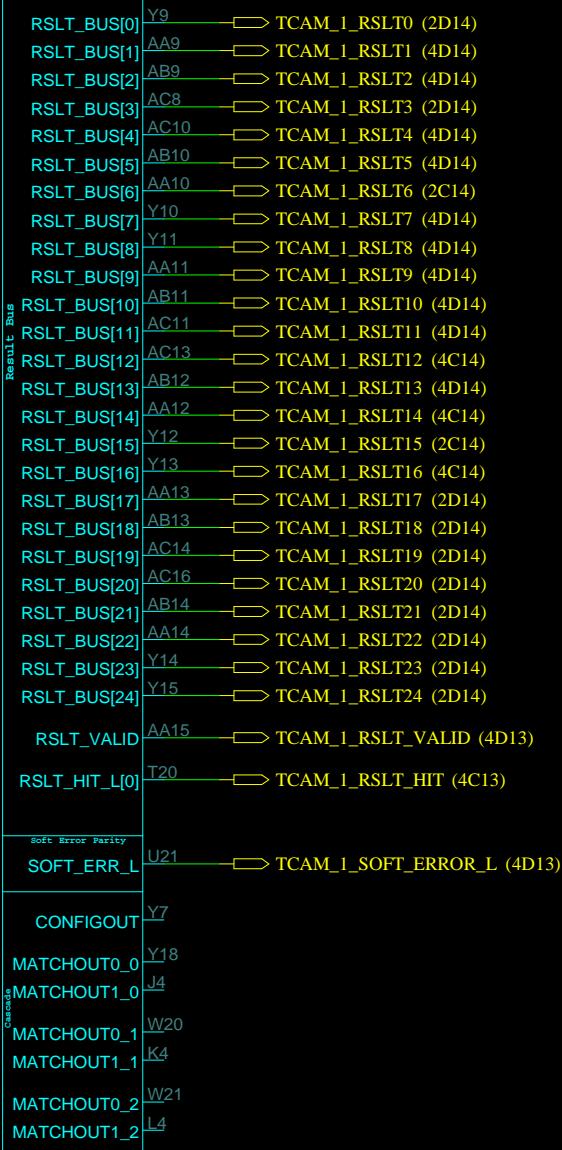
TCAM end termination:  
TCAM\_1\_DA[0:71]  
TCAM\_1\_DA\_PAR[0:1]  
TCAM\_1\_INST[0:7]

2

1

1

D8-4



ISE30036EFS-400T

Cables

Cables

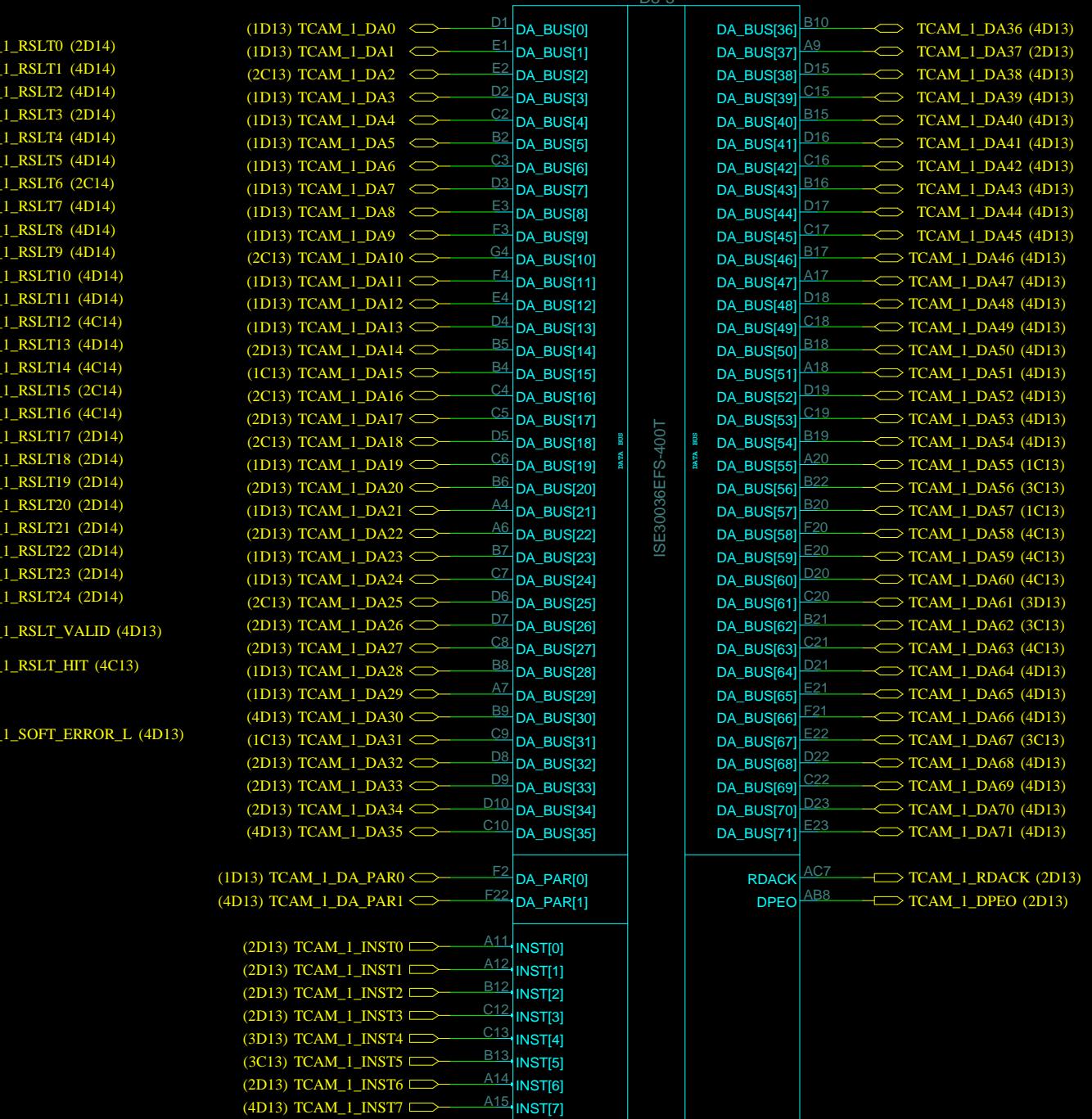
Cables

Cables

Cables

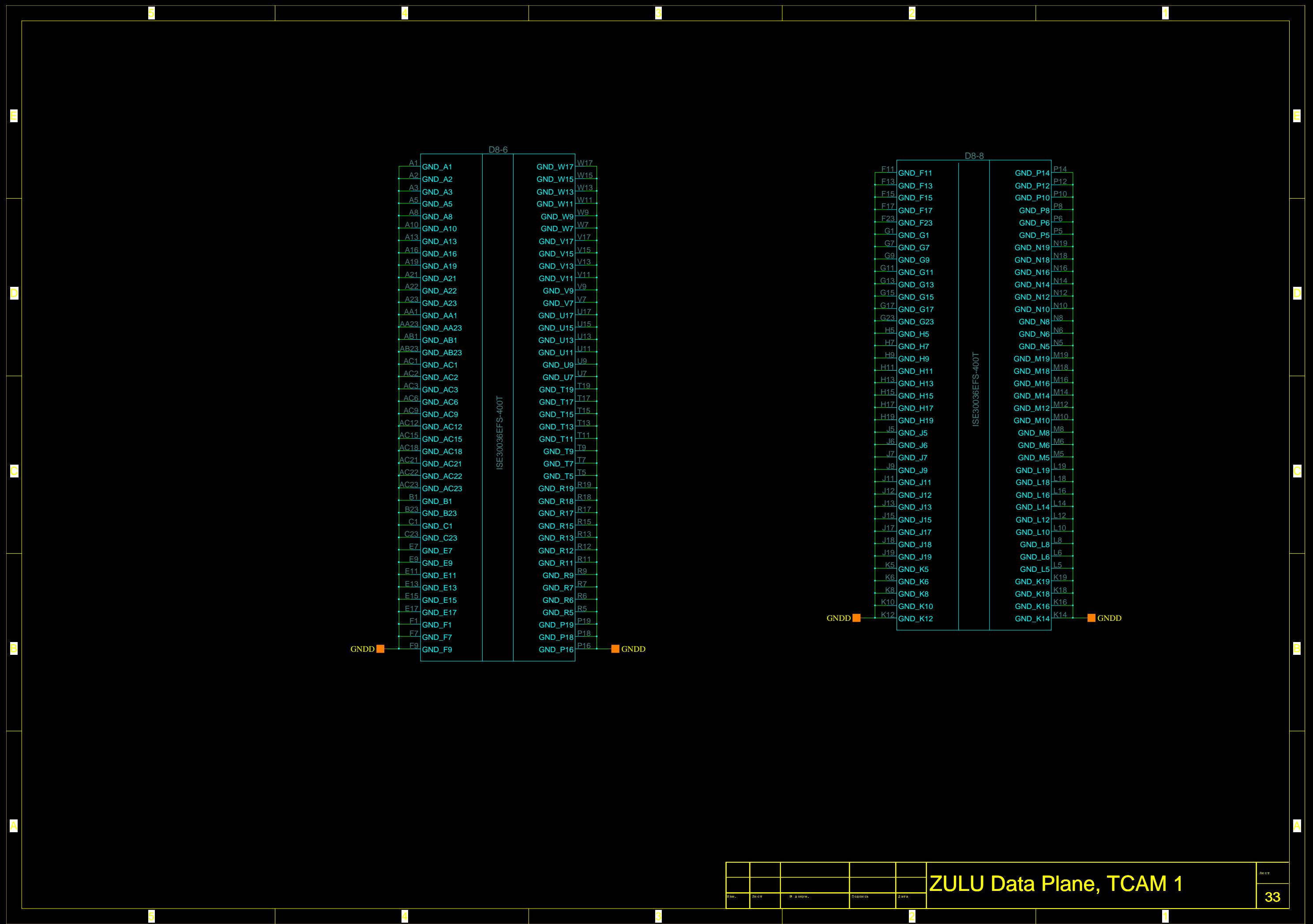
Cables

D8-5





5 4 3 2 1



5 4 3 2 1

Note:

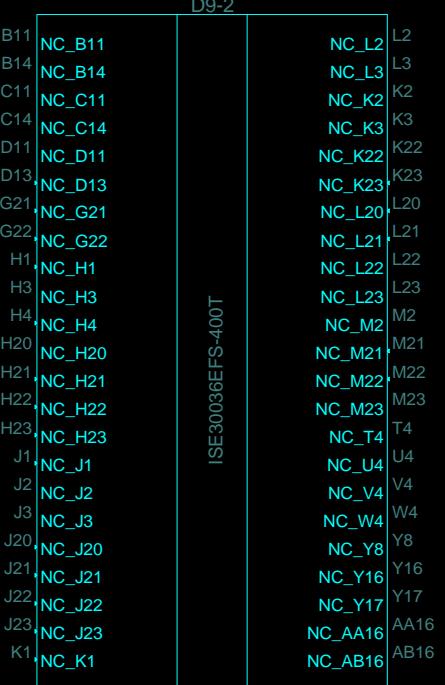
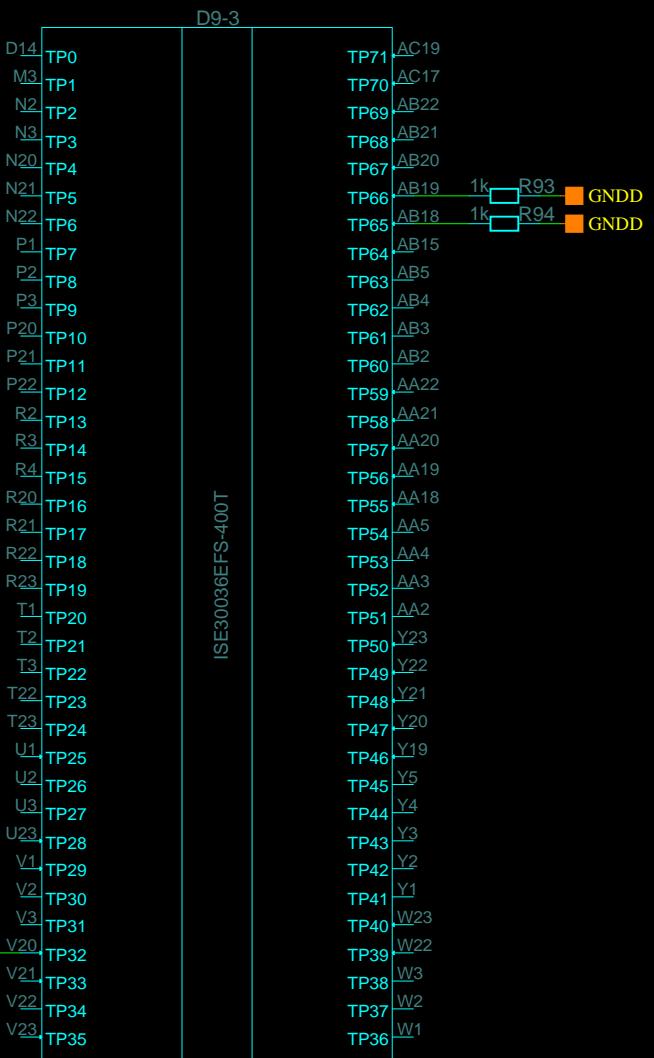
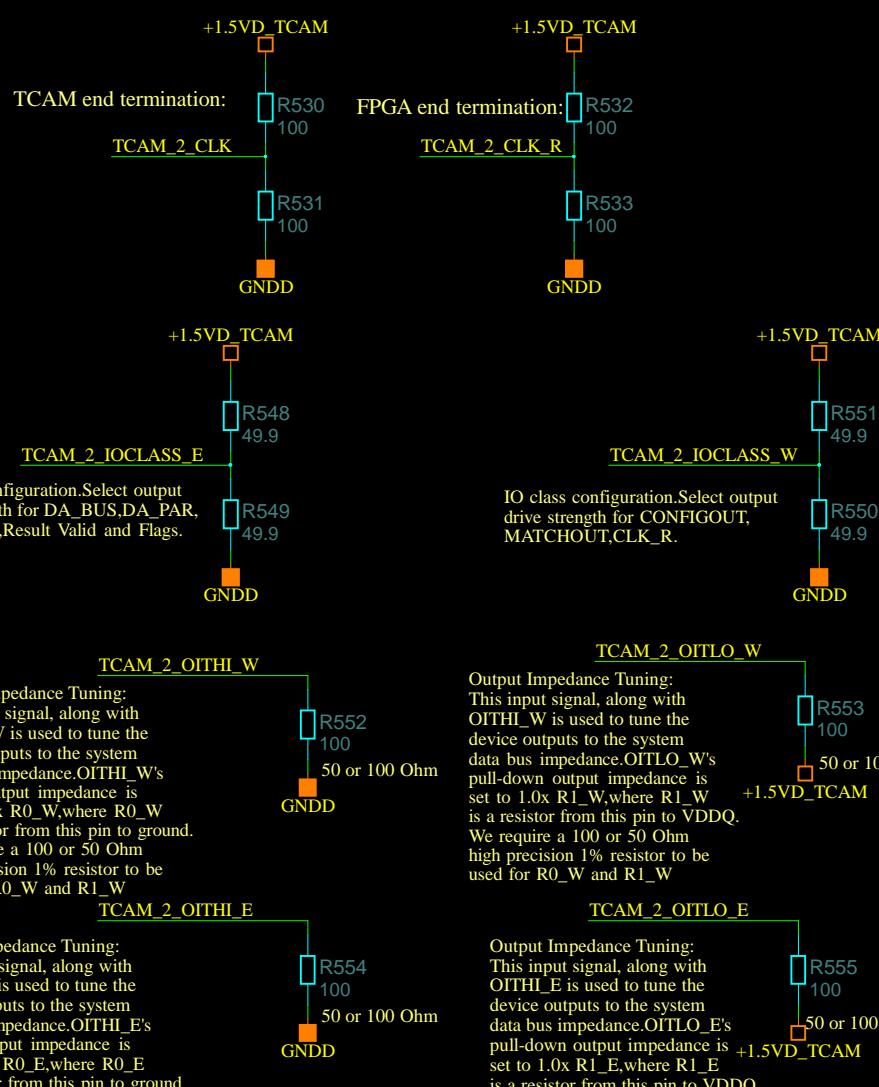
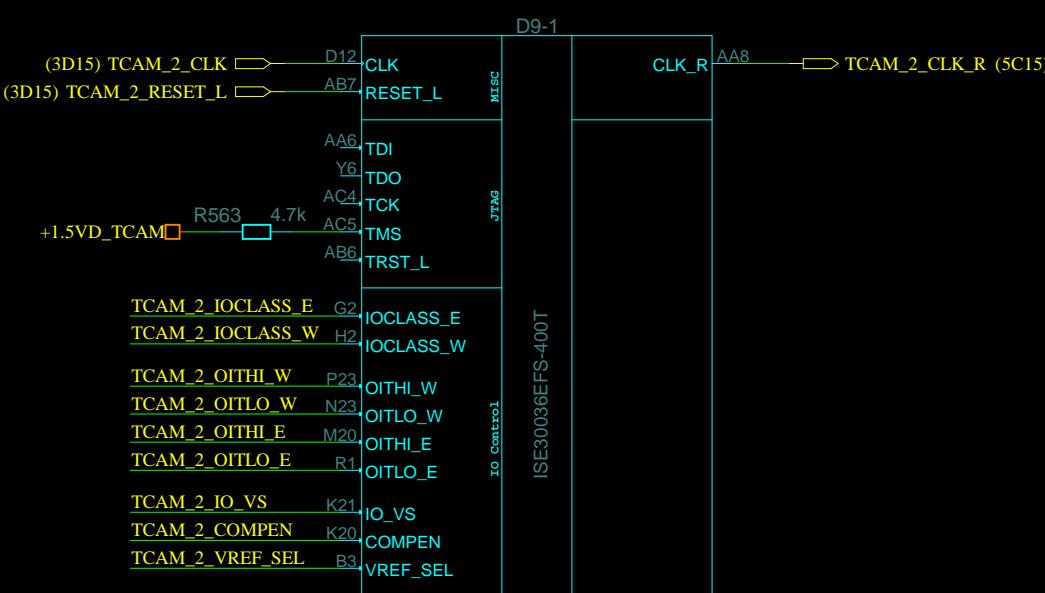
For "T" application type device:

25 Ohm impedance condition:

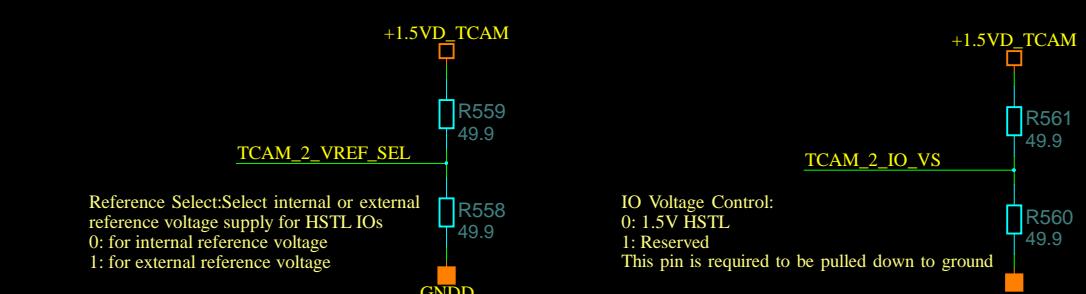
IOCLASS\_\* = 1 , COMPEN= 1 , OITHI\_\* , OITLO\_\* connect to 50 Ohms

50 Ohm impedance condition:

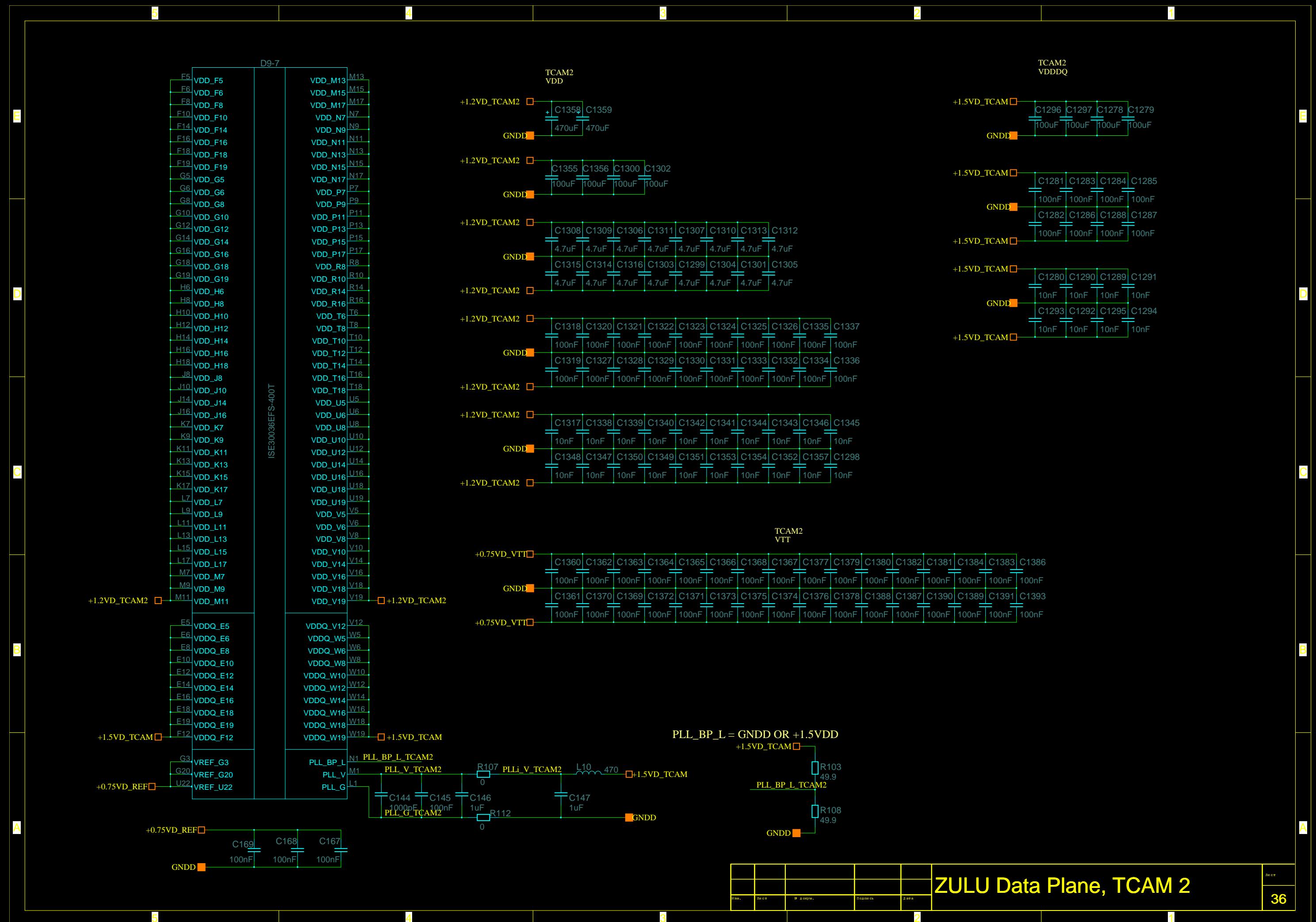
IOCLASS\_\* = 0 , COMPEN= 1 , OITHI\_\* , OITLO\_\* connect to 100 Ohms



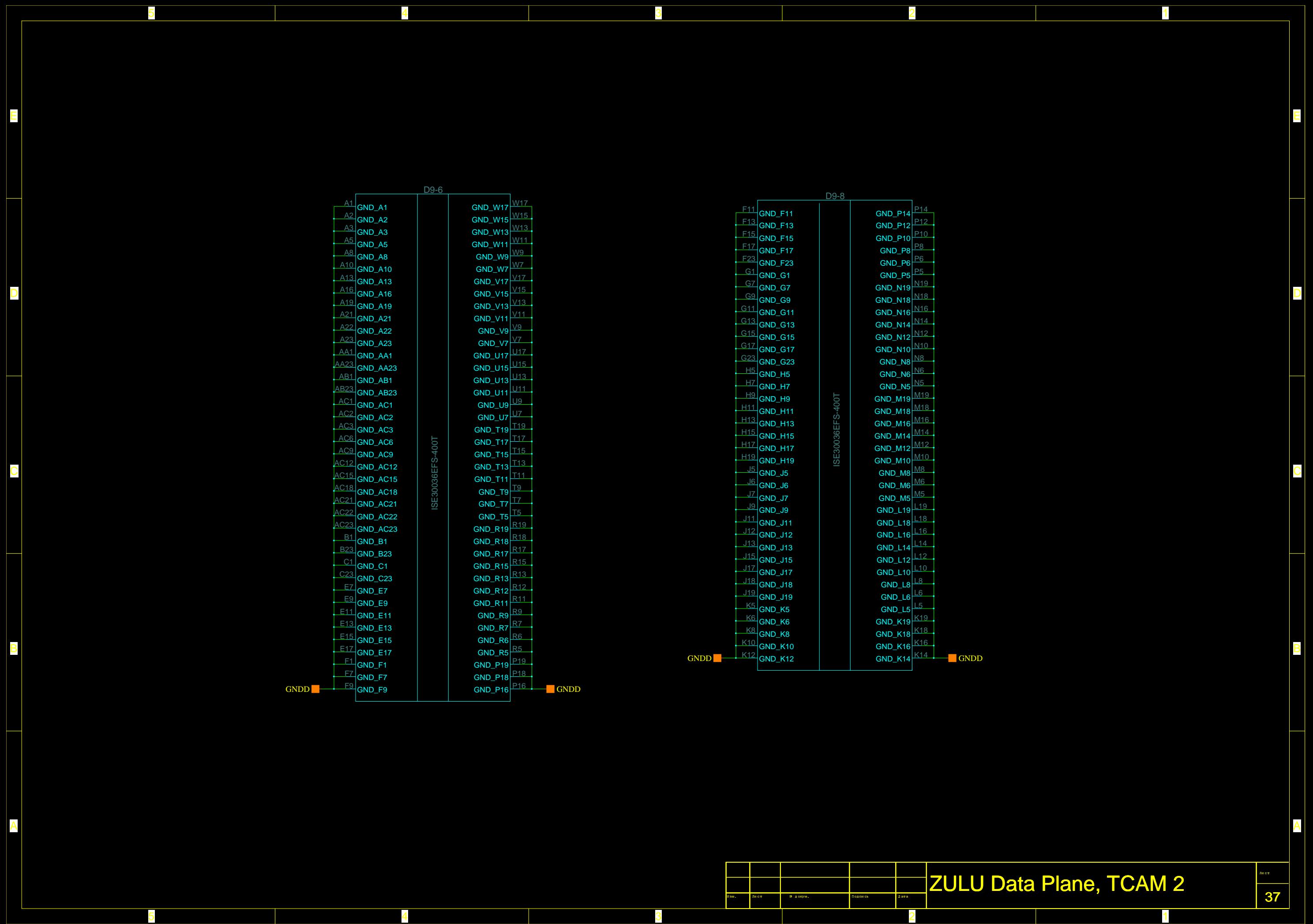
ISE30036EFS-400T

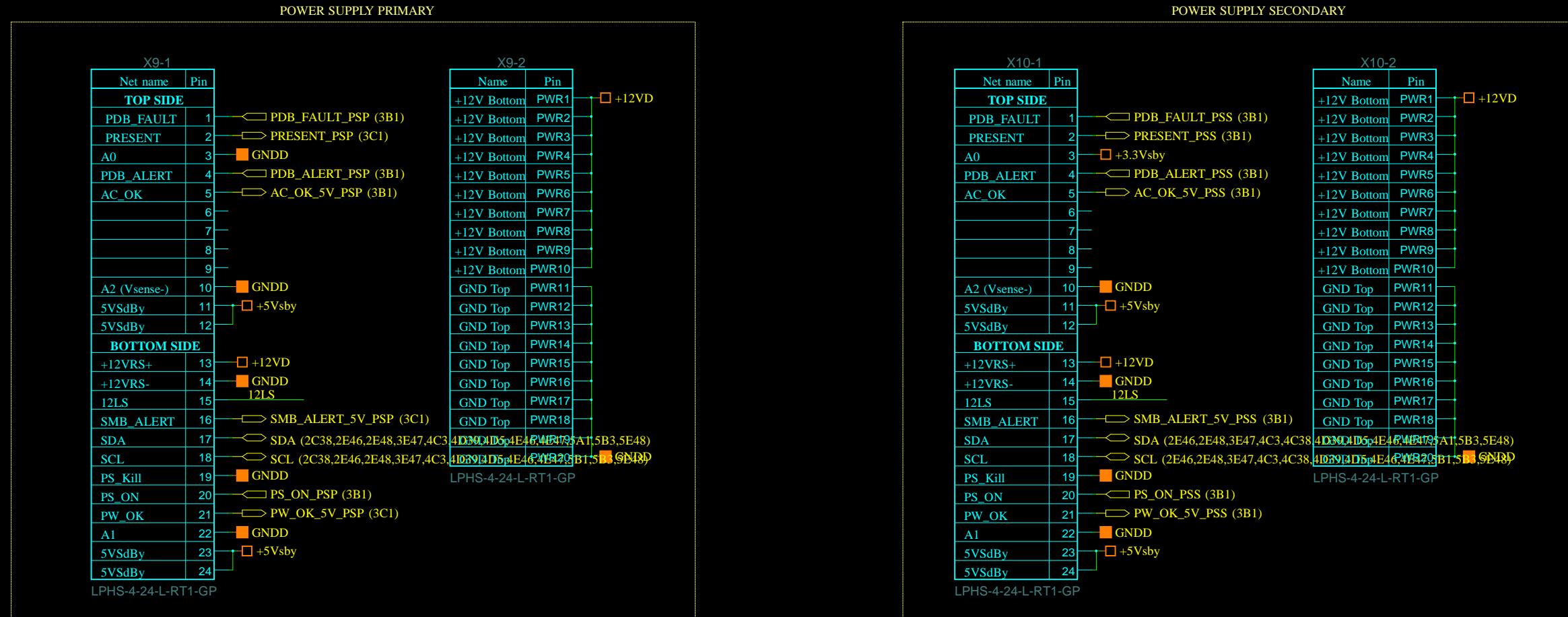


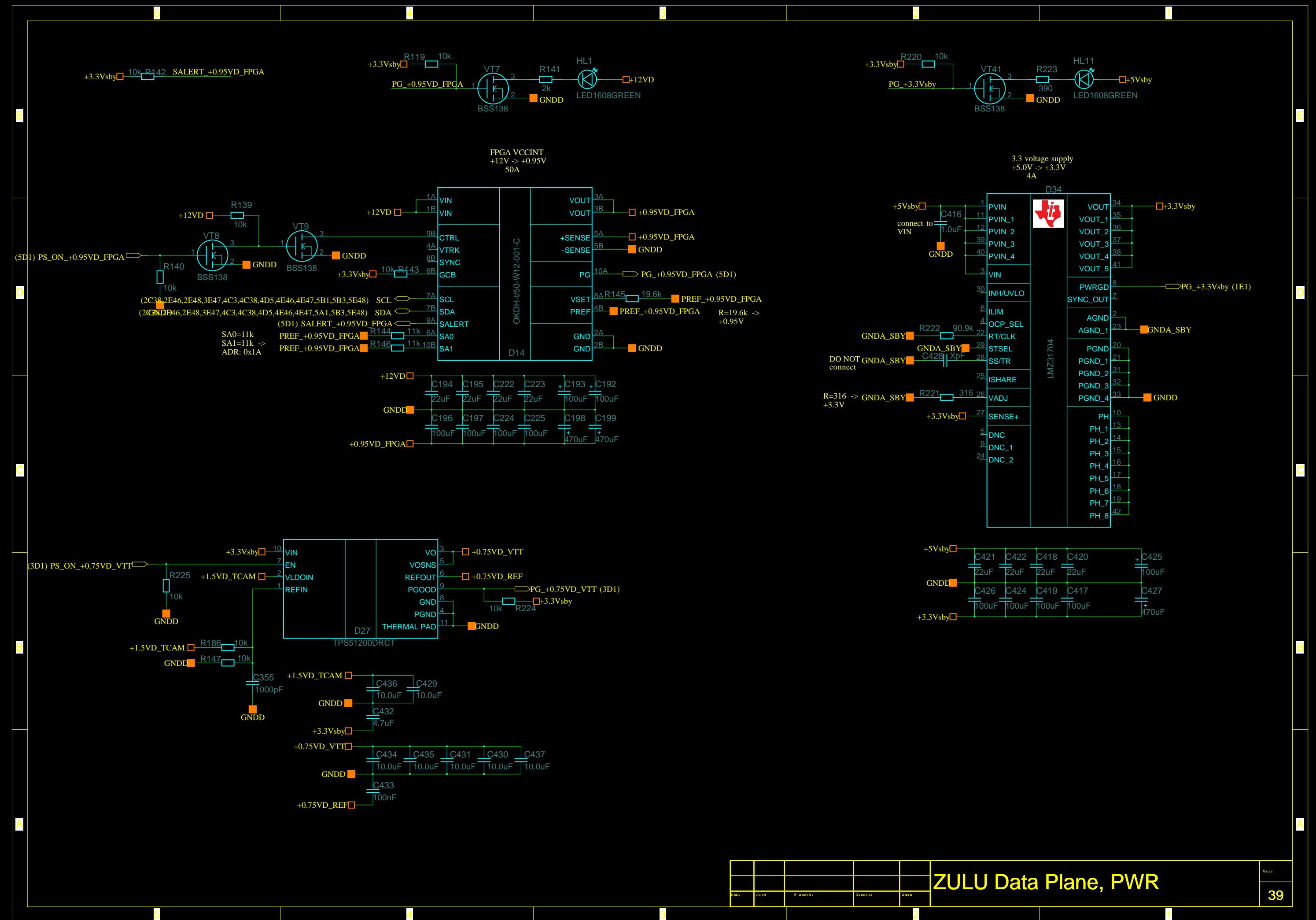


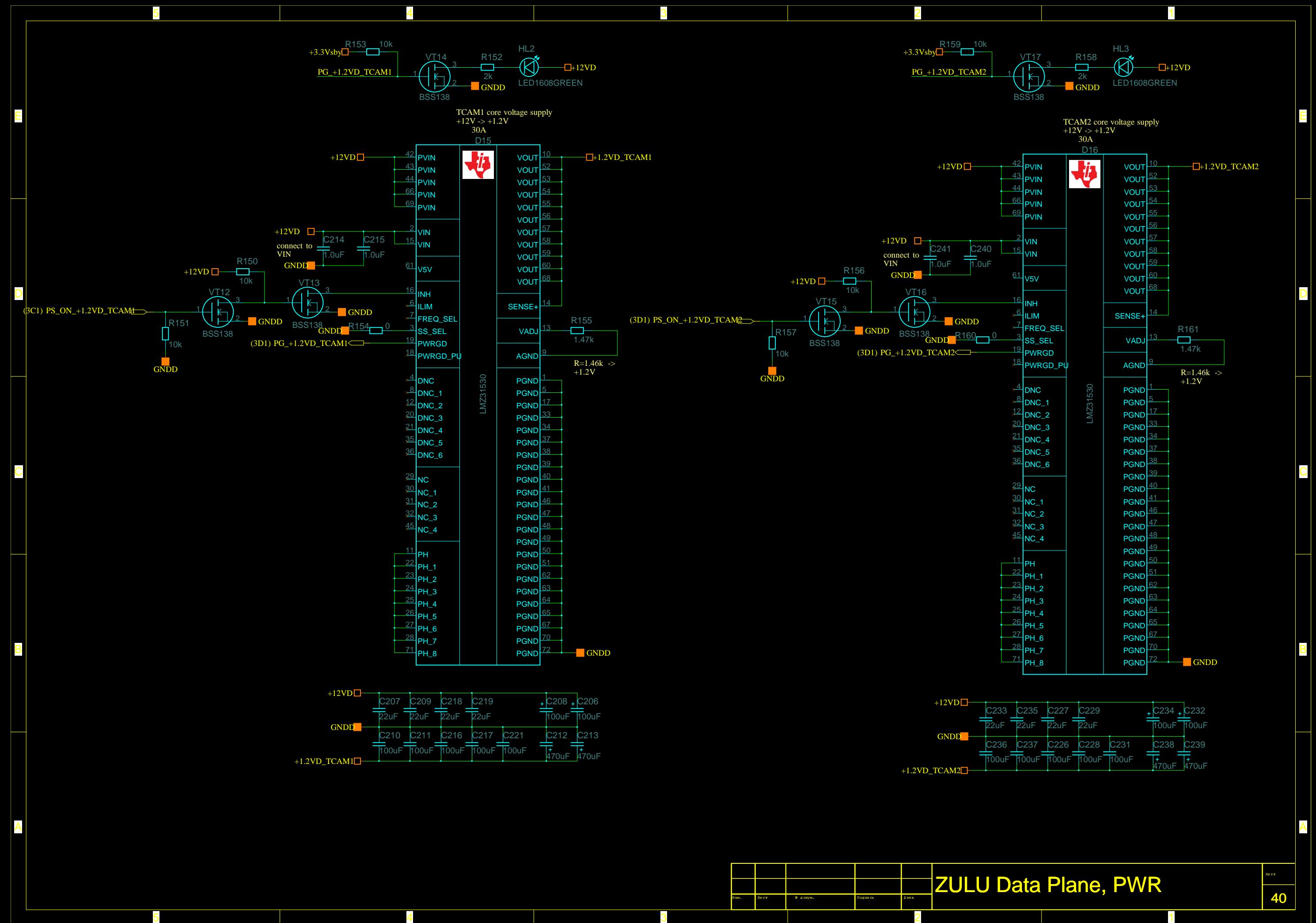


5 4 3 2 1

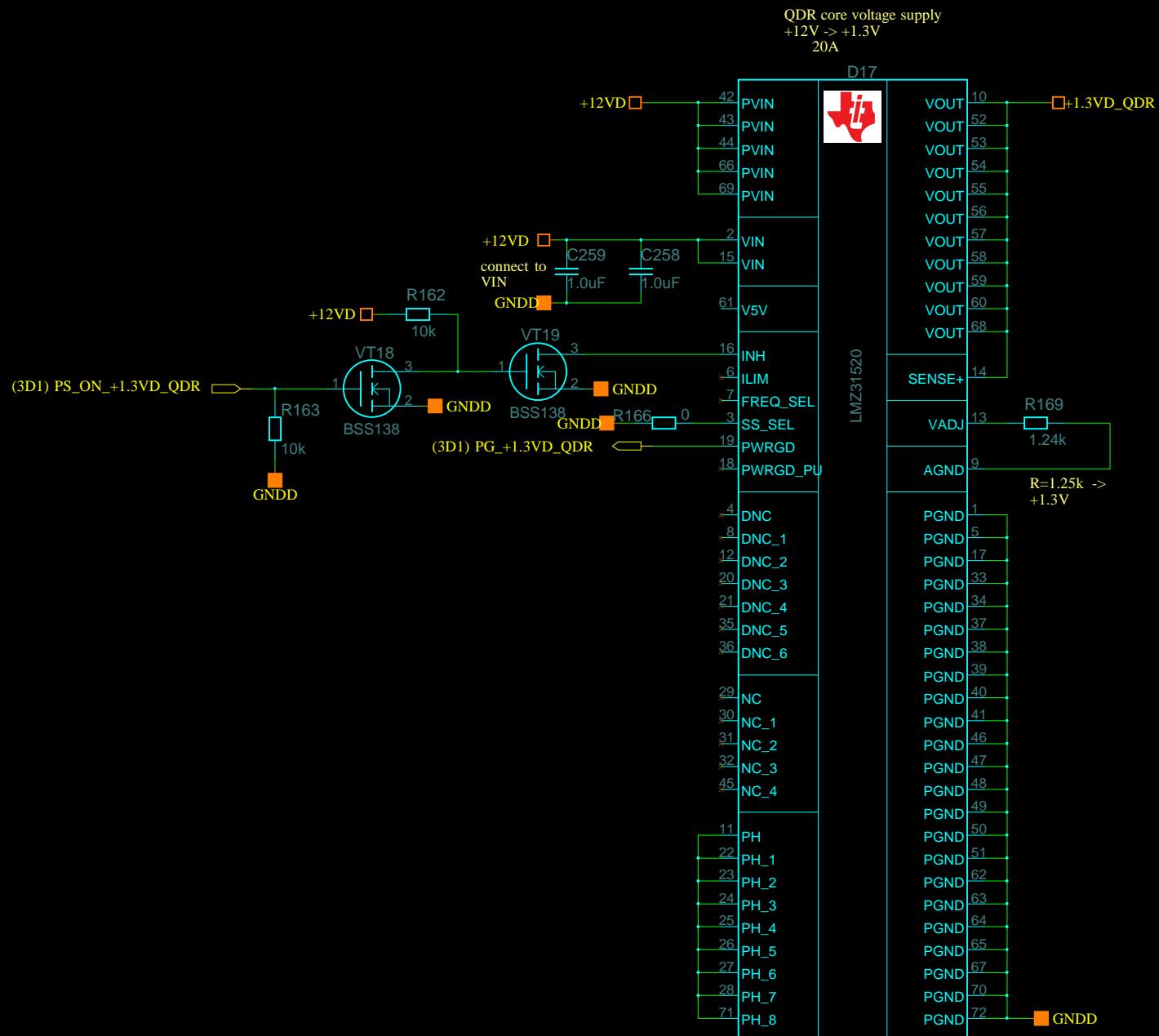
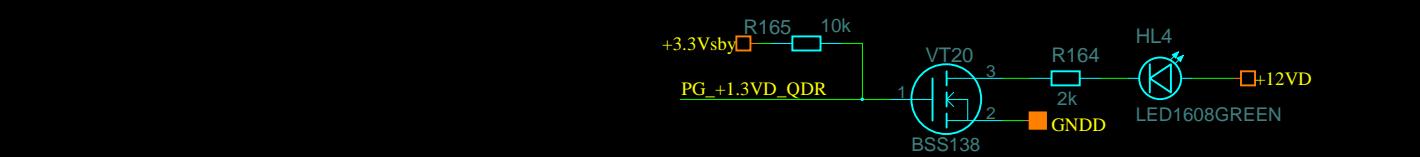




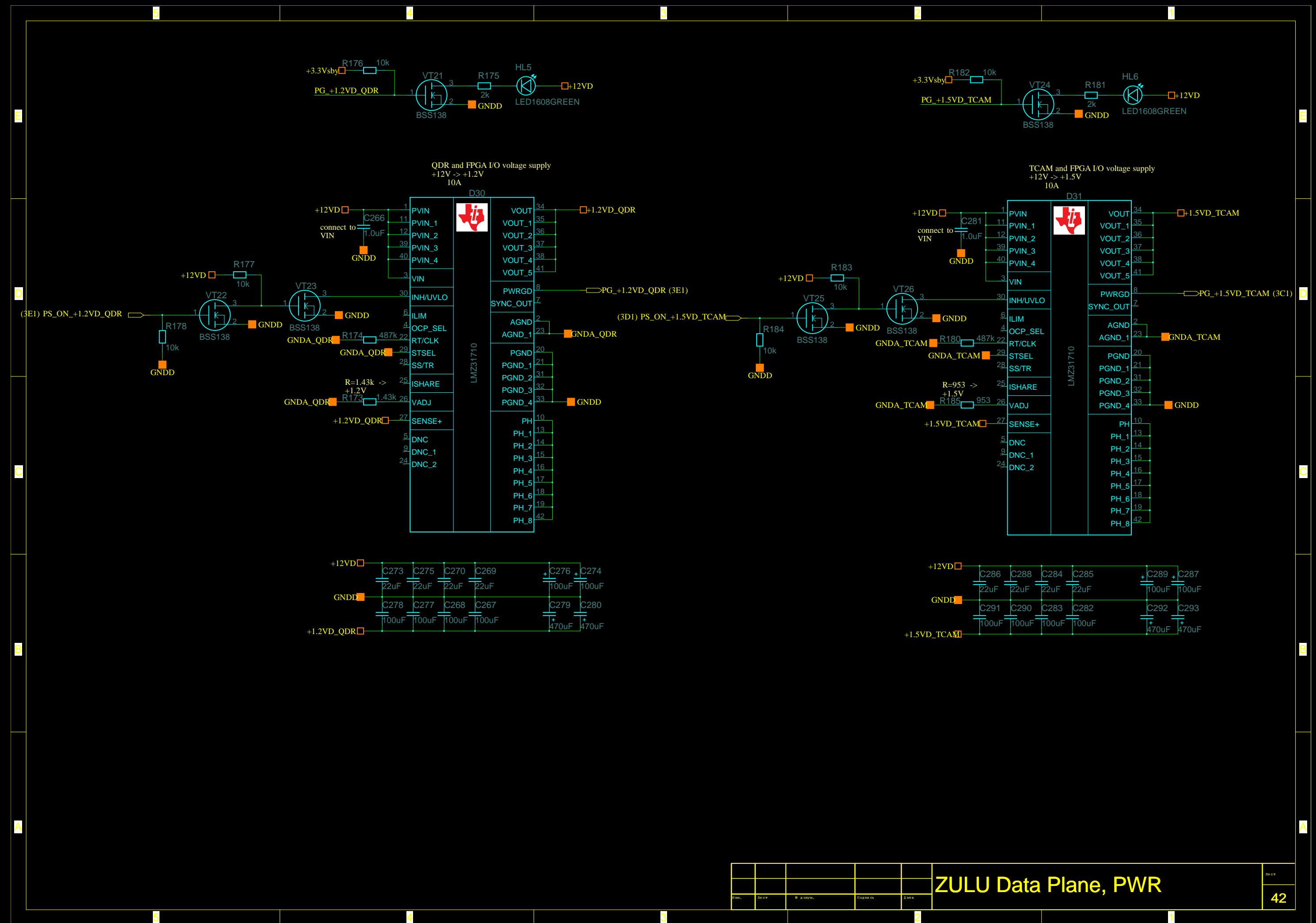


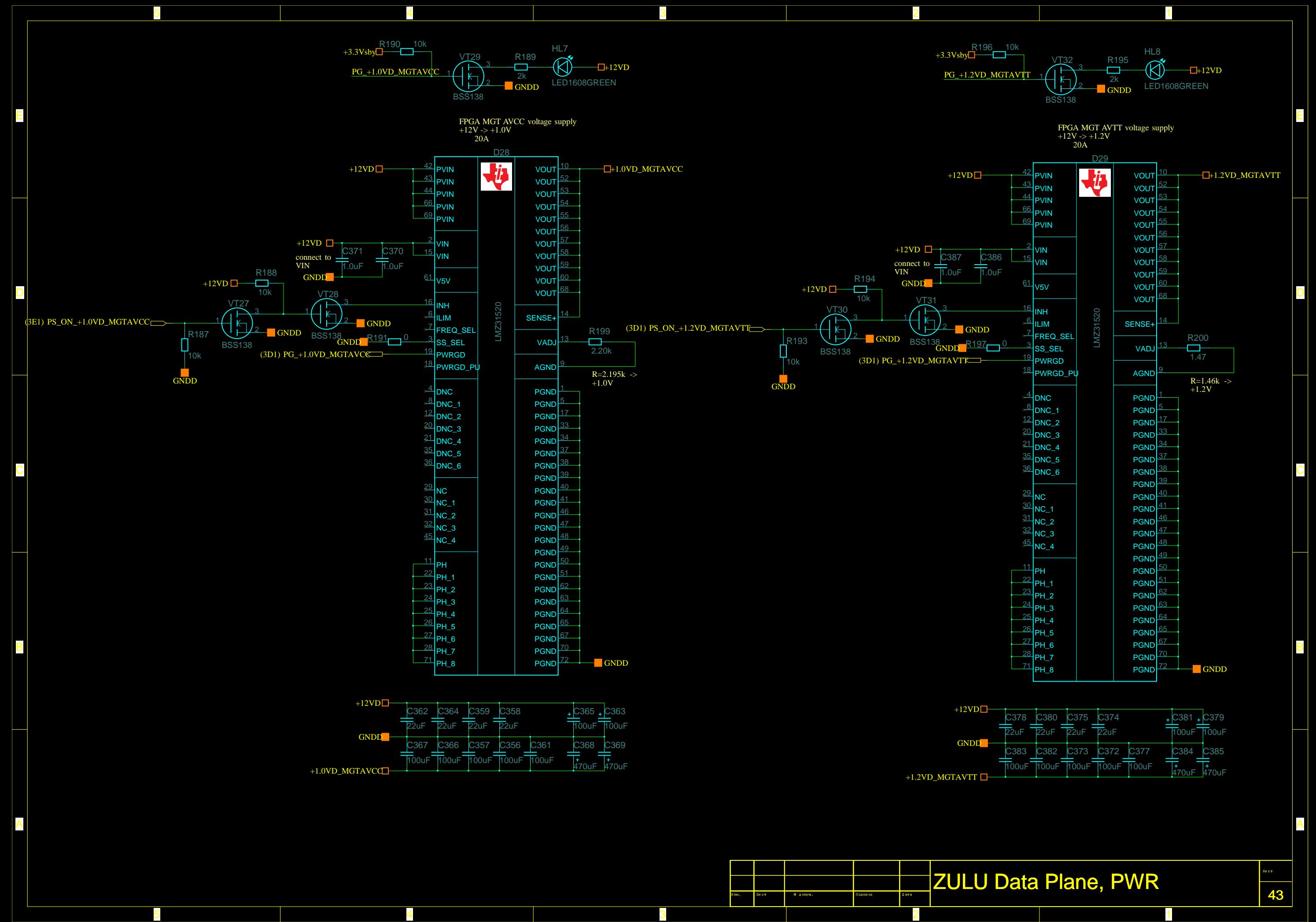


5 4 3 2 1



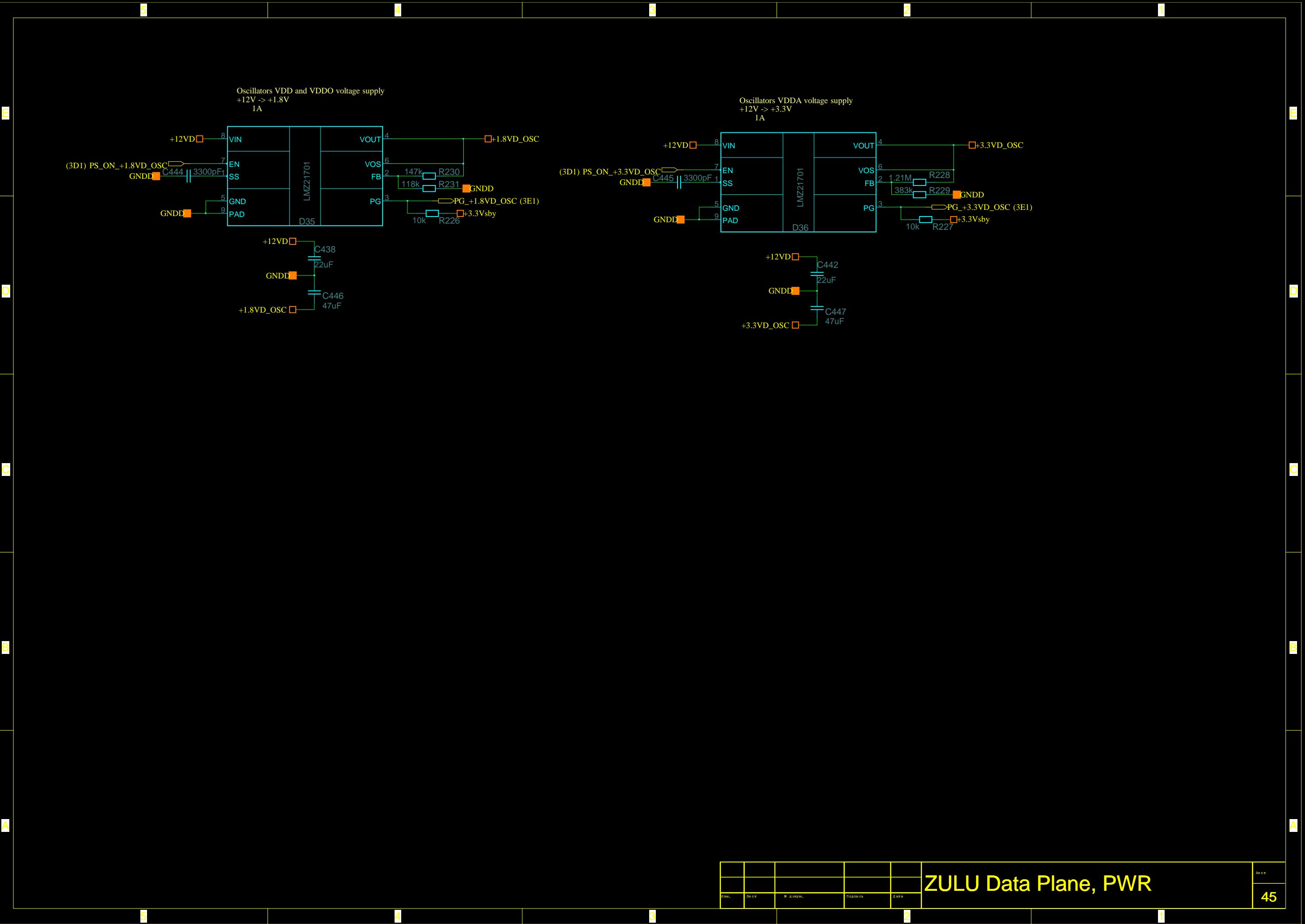
					ZULU Data Plane, PWR	
5	4	3	2	1		41





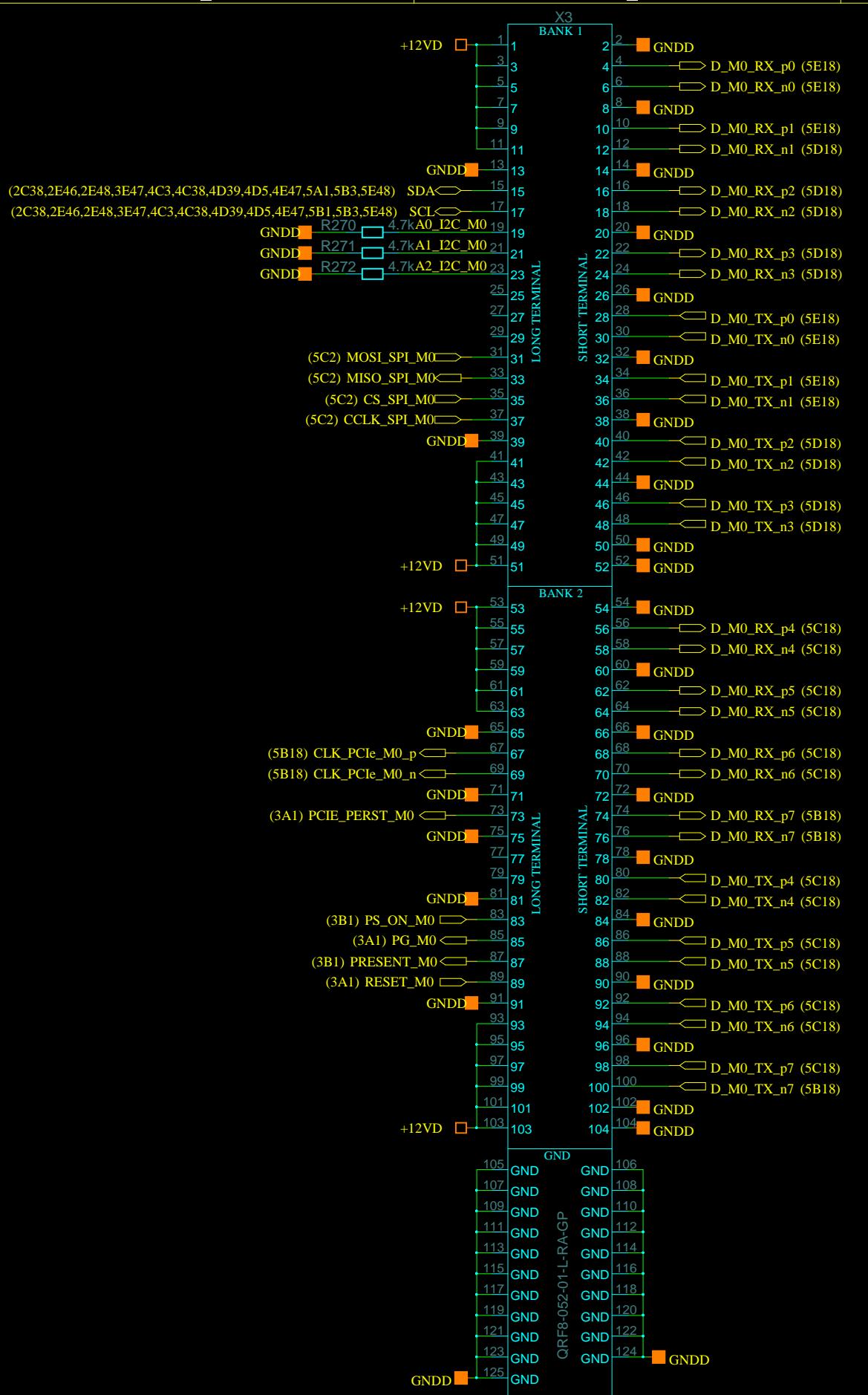


5 4 3 2 1



5            4            3            2            1

GTH Connector  
south-left addr: 0  
south-right addr: 5





PCIe Connector  
north-left addr: 1  
north-right addr: 4



ZULU Data Plane, module conn. 3