AN700.1: Manufacturing Test Guidelines for the EFR32

Most customers have standard product manufacturing test flows, but some do not incorporate RF testing. Document *AN718: Manufacturing Test Overview* provides a high-level overview of the product tests flow and phases – prototype testing, characterization testing, low-volume manufacturing, and high-volume manufacturing. This document's goal is to provide the finer details of these test phases and Silicon Labs' recommended best practices for manufacturing test. This document is intended for Silicon Labs customers developing for the EFR32 product family and who are moving from the early prototype development stage to the manufacturing production environment.

KEY POINTS

- Test flow
- Test definitions
- Test recommendations
- Test architecture and equipment
- Embedded software tools

1 Introduction

Most customers have standard product manufacturing test flows, but some do not incorporate RF testing. This document details the different options for integrating RF testing and characterization into your standard test flows. Document *AN718: Manufacturing Test Overview* provides a high-level overview of the product tests flow and phases – prototype testing, characterization testing, low-volume manufacturing, and high-volume manufacturing. This document's goal is to provide the finer details of these test phases, introduction to the test tools available, and Silicon Labs' recommended best practices for manufacturing test, focusing on the EFR32 family of products. Due to the various options available during prototype testing, this document focuses on the characterization and manufacturing test phases.

Device programming is not discussed in this application note. For information on the programming options available for EFR32 devices, see https://www.silabs.com/products/mcu/programming-options.

If after reading this document you have questions or require assistance with the procedures described, contact a support representative at https://www.silabs.com/support.

2 Test Definitions

To communicate with the device under test (DUT) and control various device test modes by automated test software, Silicon Labs provides embedded software applications to allow for both serial communication as well as Over the Air (OTA) communication to automated test software. Both of these interfaces enable configuring a device for receive or transmit modes, turning on peripherals (if applicable), reading Analog to Digital Conversion (ADC) pins on the micro (if applicable), putting the radio and/or microprocessor to sleep, and similar control functions. See section 3 Embedded Software Tools for a description of these applications.

The tests can be divided into different types of tests— RF testing, DC testing, and peripheral testing.

- RF testing is any test specific to the operation and functionality of the radio (for example, transmitting and receiving packets).
- DC testing is any test related to the voltage and current characteristics of the device or board (for example, active and sleep currents).
- Peripheral testing is any test not specific to RF or DC, like a sensor or an external crystal.

The following sections describe the tests that make up the potential suite of DUT testing.

2.1 Serial Communication Test

The Serial Communication Test verifies valid serial communication with the DUT before testing. This is a basic check that the device has been programmed correctly. If no communication is present, the DUT fails this test and does not proceed with further testing. This test is important because, if there is no serial communication with the DUT, there is no way to interface with the DUT to put the device into test mode or send commands in a standalone test application.

2.2 Supply Current Test

The Supply Current Test verifies that current consumption is valid for each mode of operation for the DUT. The modes of operation are set through the serial interface and include transmit mode, receive mode, and sleep modes (radio sleep and deep sleep). If there is excessive current draw, the DUT fails this test and does not proceed with further testing. This test is especially important for devices that will be used in battery-operated applications, as these measurements are an effective predictor of battery life.

For measuring sleep mode current draw, a multi-meter is required with the ability to measure less than 1 µA.

AN1082: EFR32 Transmit and Receive Current Measurements provides some more insight into the current measurement procedure and configurations.

2.3 Quick Verify of Transmit and Receive Test

The Quick Verify of Transmit and Receive Test quickly verifies that the DUT transmits valid packets to the Reference Node and receives valid packets from the signal generator. This can be tested on any single channel in the available frequency band. If either of these checks fails, the DUT fails this test and does not proceed with further testing. This test identifies hardware that does not require full characterization testing due to a major manufacturing defect.

2.4 Transmitter Tests

2.4.1 Transmit Power Test

The Transmit Power Test verifies that the power level of the transmitter is at the appropriate level and within a specified range. The power output is measured with the power meter at multiple power levels to confirm power output accuracy at various coded settings. The serial command interface can include a function that enables continuous waveform (CW) or unmodulated tone to be transmitted for ease of measuring these power levels. Silicon Labs recommends that this test be performed over a subset of the frequency band to record trends in power output versus frequency.

The transmit power output can be measured with a spectrum analyzer or a power meter.

2.4.2 Transmit Frequency Offset Test

The Transmit Frequency Offset Test verifies the crystal accuracy and valid transmission frequency offset of the DUT. The CW tone is again used for this transmission and the crystal capacitor value is set using software.

The EFR32 38.4MHz crystal does not require external loading caps as there is a tunable capacitor bank in the EFR32 that can be used instead. Different capacitor values can be written to registers to observe the corresponding frequency offset, and the CTUNE manufacturing token is used to store the value for use by the application. The optimal CTUNE value for the DUT can be determined in the design characterization stage by sweeping all CTUNE values at the transmit frequency and measuring the frequency offset with a spectrum analyzer. This value can then be programmed as the CTUNE manufacturing token in volume manufacturing, or each board can be tested for optimal CTUNE value, using the value from the design verification stage as a starting point. Note that the measured frequency offset will differ depending on the frequency band, so Silicon Labs recommends determining CTUNE for each frequency band needed for the device.

Additionally, the test can be performed over a subset of the frequency band to record trends versus frequency.

For information on how to set the CTUNE token, please refer to the applicable software tool application note described in section 3 Embedded Software Tools.

2.4.3 Transmit Error Vector Magnitude Test

The Transmit Error Vector Magnitude (EVM) test verifies that the device's EVM is within specified limits. The EVM is measured with a spectrum analyzer. Either a transmit packet or transmit stream command is used for this transmission, as the spectrum itself is analyzed. Silicon Labs recommends that this test be performed over a subset of the frequency band to record trends versus frequency.

Some spectrum analyzers are able to measure EVM as a standalone instrument, while other spectrum analyzers require a PC software tool to provide EVM measurement details.

2.4.4 Transmit Sweep Test

The Transmit Sweep Test verifies transmission of valid packets from the DUT to the Reference Node at all channels or a subset of channels across the frequency band. The Reference Node is put into receive mode while the DUT transmits 100 packets to the Reference Node for each channel, with an attenuation between nodes that translates to a strong signal, approximately 60 dB attenuation between devices. Please refer to the specific radio chip data sheet for more information.

Packet success rate is measured at each channel. The packet success rate percentage is defined as the number of packets received divided by the number of packets transmitted and then multiplied by 100. For the Transmit Sweep Test, anything below 100% packet success rate is flagged as a failure, as this test is conducted at a signal level where all packets should be received. This test confirms that there are no frequency-dependent issues with transmit mode.

2.4.5 Spurious Emissions Test

The Spurious Emissions test verifies that the transmitter's unwanted emissions outside the channel bandwidth that result from the modulation process and non-linearity are within the applicable limits set by regulatory bodies. A transmit tone from the DUT can be used to measure the out-of-band emission levels in a spectrum analyzer.

2.5 Receiver Tests

2.5.1 Receive Sweep Test

The Receive Sweep Test is similar to the Transmit Sweep Test. It verifies reception of valid packets at the DUT from the signal generator at all channels or a subset of channels across the frequency band and at two receiver input power levels (a strong signal level, approximately -50 dBm, and a level closer to the edge of sensitivity performance, approximately -90 dBm).

The DUT is put into receive mode while the signal generator transmits 100 packets for each channel. Packet success rate is measured at each channel/receive input level. Any packets missed at the strong signal level are considered a failure, while the failure threshold at the lower input level can be at a lower percentage, depending on the expected sensitivity of the radio. Please refer to the data sheet of the radio chip for details related to receive sensitivity. This test should be performed over the full operating band to record trends versus frequency.

Silicon Labs recommends using a signal generator to transmit packets to a DUT, as the signal generator allows for easily configuring the receive input power level at the DUT.

2.5.2 Receive Sensitivity Test

The Receive Sensitivity Test determines the receiver sensitivity of the DUT by measuring the input power level at 0.1% BER (Bit Error Rate) or 1% PER (Packet Error Rate) depending on the radio chip configuration. Please refer to the data sheet for the specific radio chip information on the sensitivity requirements. To measure PER, the DUT is placed in receive mode with 1,000 valid packets being sent from the signal generator for each channel. The power level should begin at some level before the 1% Packet Error Rate (PER) threshold. The PER is measured until the receiver input power level corresponding to 1% PER is determined. This test should be performed over a subset of the operating band to record trends versus frequency. During the characterization testing phase Silicon Labs recommends that the actual sensitivity level be determined, while at high volumes the receive sensitivity specification can be set as the low limit and be used as a single power level for ease of testing.

Similarly, to measure BER, the DUT is placed in receive mode and the signal generator sends valid bits to the DUT for each channel. The BER is measured until the receiver input power level corresponds to 0.1 % BER.

Silicon Labs recommends using a signal generator to transmit packets to a DUT, as the signal generator allows for easily configuring the receive input power level at the DUT.

2.5.3 Receive Waterfall Test

The Receive Waterfall Test determines the receiver sensitivity of the DUT by collecting data to determine the receiver roll-off curve. The DUT is placed in receive mode with 100 valid packets being sent from the signal generator for each channel. The power level should begin at some level before the 1% PER or 0.1% BER threshold. Please refer to the data sheet for the specific radio chip for more information on the sensitivity. The packet success rate is measured for all input powers selected for testing. Silicon Labs recommends that enough input power levels are selected to ensure that the data collected includes both 100% and 0% packets received. This allows for a complete roll-off curve to be observed. This test should be performed over a subset of the operating band to record trends versus frequency. Silicon Labs recommends this test for characterization testing so that the roll-off is quantified and understood but can be omitted at higher volumes.

Silicon Labs recommends using a signal generator to transmit packets to a DUT, as the signal generator allows for easily configuring the receive input power level at the DUT.

2.5.4 Receive Signal Strength Indicator (RSSI) Test

The RSSI Test measures the RSSI value for a single channel and known receiver input power level. The RSSI is determined by receiving a valid packet from the signal generator and reading the RSSI value through the serial command interface. The DUT is placed into receive mode while the signal generator transmits a single packet and the RSSI measurement is averaged to determine RSSI value. This single data point is measured to verify that the RSSI pin for the radio chip is connected and that RSSI is reporting a valid level. The RSSI operation of the chip itself is validated at the chip testing level and is not tested here.

Silicon Labs recommends using a signal generator to transmit packets to a DUT, as the signal generator allows for easily configuring the receive input power level at the DUT.

2.6 External 32kHz Test

The operation of the external 32 kHz crystal (if applicable) should be verified through the LFXO tune manufacturing token.

2.7 Peripherals Test

Various peripherals, if applicable, can be tested through the serial port. These include anything that may be accessed through the ADC or GPIO (general purpose I/O) on the micro. For example, an LED is often tied to a GPIO pin for some status to be alerted. The state of the LED can be modified by changing the level of the GPIO pin. Another example is reading an ADC pin for a particular voltage level that corresponds to the status of a peripheral such as a temperature sensor or an accelerometer. Any peripheral accessible through GPIO or the ADC should be tested to ensure valid functionality.

3 Embedded Software Tools

Silicon Labs supports multiple embedded software tools for manufacturing test for the EFR32. This supports testing with a standalone test application or a test mode within the customer application.

NodeTest

The NodeTest is a pre-built standalone application is provided with the EmberZNet SDK (Software Development Kit). Silicon Labs recommends that NodeTest be used only for radio boards in the kit for evaluation purposes. NodeTest provides a serial command line interface to the Silicon Labs device. Instructions for using NodeTest are provided in *AN1019: Using the NodeTest Application*.

Manufacturing Library

Silicon Labs recommends that customers use the manufacturing library in mature applications, regardless of the testing phase. Customers without mature applications can build a simple Zigbee sample application with the manufacturing library enabled to access this functionality. The manufacturing library provides access to a test mode within the application and removes the need for multiple application bootloads or multiple programming steps within the manufacturing process. The manufacturing library is available as a configurable plugin in the EmberZNet SDK. The guidelines for enabling the manufacturing library plugin and using the manufacturing library CLI commands for manufacturing tests are provided in *AN1162: Using the Manufacturing Library for EmberZNet*.

RAILtest

The RAILtest standalone application is provided with the Flex SDK. It provides customers with a simple tool for testing the radio and the functionality of the RAIL library. For any advanced usage customers should write their own software with a custom radio configuration. RAILtest is documented in *UG409: RAILtest User's Guide, AN972: EFR32 RF Evaluation Guide*, and *INS14283: Bring-up/Test HW Development*.

Direct Test Mode protocol (DTM)

The DTM protocol is defined in the Bluetooth specification as a means for testing the radio performance of Bluetooth low energy products. Bluetooth-enabled Silicon Labs EFR32xG SoCs and the xGM modules support two approaches for RF PHY testing offered by DTM. One approach is where the RF PHY tester controls the DUT over the standardized HCI (host control interface) of the DUT. In another approach, the tester had direct access to the DUT through a dedicated 2-wire connection to control the radio tests on the DUT. More information on DTM testing is described in *AN1046: Bluetooth Radio Frequency Physical Layer Evaluation*.

4 Test Recommendations

This section outlines the various tests that can be run on the hardware product, which of those tests Silicon Labs recommends running, and the channel selection for each test in each phase.

4.1 SoC Test Recommendations

4.1.1 Characterization Testing

Characterization testing is recommended for early production stages. In this phase of testing, the hardware is characterized on all 16 Zigbee channels or a subset of these channels, as well as at various transmit output power levels or receiver input power levels. This phase fully characterizes the hardware that is being developed, determines the tests to be executed in manufacturing test, determines the test limits of these tests, and flushes out any manufacturing or process issues that might be present.

Silicon Labs recommends that the tests outlined in the following table be conducted in the characterization phase of testing. This table, and the similar tables that follow in subsequent sections of this document, list the various tests that could be run on these devices, which of those tests Silicon Labs recommends running, and the channel selection for each test in each phase.

Note: An X in these tables represents a test that is recommended for this phase of testing.

Table 3-1. Characterization Test Recommendations

Test	Run?	Channel			
		Mid	Low Mid High	Subset	All
Serial Communication	X				
Supply Current	X	X			
Transmit/Receive Verify	X	X			
Transmit Power	X		X		
Transmit Frequency Offset	X		X		
Transmit EVM	X		X		
Transmit Sweep	X				X
Spurious Emissions	X				
Receive Sweep	X				X
Receive Sensitivity	X		X		
Receive Waterfall	X		X		
RSSI	X	X			
External 32 kHz Crystal	X				
Peripherals	X				

4.1.2 Low-Volume Manufacturing Test

Low-volume manufacturing test is usually a subset of the characterization testing. A subset of the 16 Zigbee channels or transmit output power levels can be tested to reduce the test time without compromising test coverage. For example, one channel/power level combination (likely mid-band at max power) can be measured for transmit power and frequency. Also, receive waterfall can be omitted and receive sensitivity can be run in its place, where a certain packet-success rate is expected at mid-band for a given input power level.

The results from the characterization phase of testing help determine not only what should be tested in the manufacturing phase but also the test limits to be applied to certain tests. For example, if a particular test does not fail at all during the characterization phase, it can be omitted from the manufacturing phase altogether. Also, if it is determined that a particular test will fail all channels if it fails at all, testing can be reduced from all channels to a single channel, most likely mid-band.

4.1.2.1 Test Recommendations

The following table lists the tests Silicon Labs recommends be conducted in the low-volume manufacturing phase of testing.

Table 3-2. Low Volume Manufacturing Test Recommendations

Test	Run?	Channel			
		Mid	Low Mid High	Subset	All
Serial Communication	X				
Supply Current	X	X			
Transmit/Receive Verify	X	X			
Transmit Power	X	X			
Transmit Frequency Offset	X	X			
Transmit EVM					
Transmit Sweep	X			X	
Spurious Emissions	X				
Receive Sweep	X			X	
Receive Sensitivity	X	X			
Receive Waterfall					
RSSI	X	X			
External 32kHz Crystal	X				
Peripherals	X				

4.1.2.2 Test Times

The typical test time that can be achieved in the low-volume manufacturing test phase is three minutes per board. If the devices are preprogrammed, the overall test time can be reduced to less than three minutes. Program times vary depending on the flash memory size of the microprocessor. Note that programming may be included at both the front end (test application) and back end (final application) of the process.

4.1.2.3 Setting Test Limits

The results of the characterization phase of testing help determine how the limits are set for low-volume manufacturing test. Other factors in setting limits are customer application and manufacturing variation. For example, if an application specifies only a certain amount of dynamic range, perhaps limits will be relaxed to allow for this. Manufacturing variation can also be a factor in setting limits. For example, if the performance of the board is sensitive to particular components, it is important to account for any performance variation that may be seen with these particular components.

4.1.2.4 Full Characterization Sampling

It is important to continue to fully characterize samples from each production run to ensure that nothing in the process has shifted, causing a difference in the overall performance of a production run compared to a previous run. The size of this sample can be determined by the manufacturer, but Silicon Labs recommends this full characterization sampling for additional test coverage and process control at volume testing.

4.1.3 High-Volume Manufacturing Test

High-volume manufacturing testing is much simpler than characterization testing or low volume manufacturing testing. The hardware design and manufacturing process have already been proven, so the product now just requires a quick “go/no go” functional test to verify operation.

4.1.3.1 Test Recommendations

Silicon Labs recommends that the tests in the following table be conducted in the high-volume phase of testing.

Table 4-3. High-Volume Test Recommendations

Test	Run?	Channel			
		Mid	Low Mid High	Subset	All
Serial Communication	X				
Supply Current	X	X			
Transmit/Receive Verify	X	X			
Transmit Power					
Transmit Frequency Offset					
Transmit EVM					
Transmit Sweep					
Spurious Emissions					
Receive Sweep					
Receive Sensitivity	X	X			
Receive Waterfall					
RSSI					
External 32 kHz Crystal	X				
Peripherals	X				

4.1.3.2 Test Times

The typical test time that can be achieved in the high-volume manufacturing test phase is less than one minute per board. This assumes that devices are preprogrammed with the customer application and that the customer application uses the appropriate test tool for invoking test modes.

4.1.3.3 Setting Test Limits

Since the test environment in the high-volume manufacturing phase is different from the test environment in the low-volume phase, setting the limits is also done differently. The test limits for the basic transmit and receive tests are dependent on the fixed attenuation between the Golden Node and the DUT, as well as the variation in over-the-air results. Silicon Labs recommends that customers run a sample size of boards through testing to determine these test limits.

4.1.3.4 Full Characterization Sampling

Even in high-volume testing, it makes sense to fully characterize samples from each production run to ensure that the process has not shifted in any way. The size of this sample can be determined by the manufacturer, but this full characterization sampling is recommended for additional test coverage at high volumes.

4.2 PCB and SiP Module Testing

Silicon Labs offers EFR-based modules that are pre-certified or fully certified. When customers use PCB or SiP modules, the end product will require only limited RF testing depending on the module variant, market region and its compliance to the regulatory standards. Therefore, modules need only a subset of the tests described in Section 2 Test Definitions. For example, modules with an integrated antenna may only need a quick go/no-go test to verify functionality and modules with an external antenna path will need to be evaluated for its radiated RF performance. Please refer to *AN1048: Regulatory RF Module Certifications* for more information on module certifications and the required testing.

5 Test Architecture and Equipment

The following sections detail the recommended test architecture and equipment for each phase of testing, discuss test results and their dependence on test setup, and describe the typical manufacturing faults detected in manufacturing test.

5.1 Characterization Testing

The architecture and test equipment used in the characterization stage of testing is more comprehensive than that of the volume manufacturing stages.

5.1.1 Test Architecture

The following figure shows an example of the interfaces of the test equipment to the DUT. The test equipment can be controlled by test software through the General Purpose Interface Bus (GPIB) or Recommended Standard 232 (RS-232). The DUT may be controlled by utilizing the Wireless Starter Kit Mainboard which contains an on-board J-Link debugger and a Virtual COM port over USB or Ethernet, enabling application development and debugging/testing of custom hardware. For more information on the debug interfaces available, please refer to *AN958: Debugging and Programming Interfaces for Custom Designs*. Any number of DUTs may be tested at once, but this number is dependent on serial ports available and will affect the selection of the power splitter and matrix switch hardware described in the following figure.

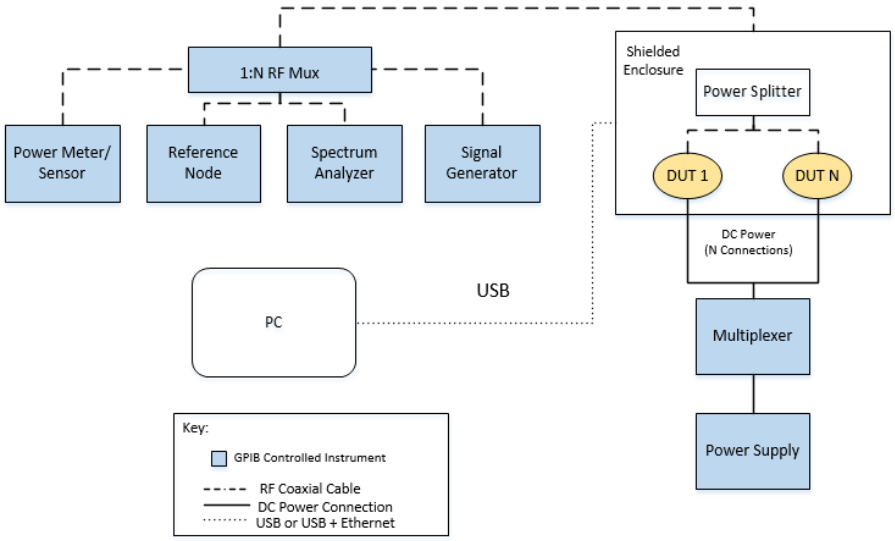


Figure 4.1. High level Architecture Example of the Characterization Test

5.1.2 Recommended Equipment

The recommended characterization test setup uses Agilent test equipment for the basic radio frequency (RF) measurements and current measurements, as well as for supplying power to the DUT and switching the RF connections from the DUT to various types of measurement equipment. A Reference Node, as mentioned in the characterization stage of testing, is any Ember radio communication module (RCM) configured with the same radio chip as the DUT that can be used to verify transmission of packets from the DUT.

The following table lists the basic set of test equipment Silicon Labs has used for characterization testing. Please consult the equipment manufacturer for the appropriate models for these particular instruments.

Table 4-1. Recommended Characterization Test Equipment

Description	Purpose
Power Meter	Used with power sensor to measure transmit power of the DUT
Power Sensor	Used with power meter to measure transmit power of the DUT
Universal Counter	Measures the transmission frequency offset of the DUT
Spectrum Analyzer	Used to verify transmit power, Transmit Frequency Offset accuracy, and EVM of the DUT
Signal Generator	Verifies reception of valid packets at the DUT
Dual Output Power Supply	Powers the DUT and Reference Node
Digital Multimeter	Verifies current consumption of the DUT in various modes of operation
Data Acquisition Switch Unit	Supplies power to the DUT and switches RF connection
3.5 GHz 1:N RF Mux Module	Switches RF connection from the DUT to the Reference Node/Spectrum Analyzer, frequency counter, power meter, or signal generator
1:N Multiplexer Splitter	Splits power from test equipment to N DUTs; alternative parts can be used for more or fewer DUTs
Shielded RF Enclosure	Provides RF isolation for the DUT during testing
Reference Node	Known good radio module that is used as a receiver reference node in DUT transmit tests; manufacturer can be Silicon Labs, a Silicon Labs customer, or a Silicon Labs module partner

Note: A power meter and frequency counter may be used in place of a spectrum analyzer in characterization testing to measure transmit power and transmit frequency offset. In volume manufacturing test, the power meter and frequency counter are a much more cost-effective method of measuring transmit power and transmit frequency offset than the spectrum analyzer.

5.1.3 Configuring Equipment

Some test equipment needs to be configured specifically for 802.15.4/BLE radio communications. For the signal generator, for instance, the specific packet needs to be configured. Silicon Labs recommends contacting the specific test equipment manufacturer for information on configuring the signal generator for valid 802.15.4/BLE packets.

5.1.4 Low-Cost Alternative to Signal Generator (Golden Node)

For some customers, adding a signal generator to manufacturing test is not desired or not possible due to cost concerns. In this case, Silicon Labs recommends using a Golden Node (a known good device that can be used in test for repeatable measurements) with TCXO (temperature controlled/compensated crystal oscillator). The TCXO allows for frequency accuracy when using the Golden Node as a known good transmitter source for DUT receive tests. Using a Golden Node without TCXO would present issues with test accuracy, as the crystal would drift over time and temperature. The Golden Node will have known transmitter performance (0 dBm +/0.5 dBm) across voltage and temperature, allowing for test repeatability.

5.1.5 RF Test Interface Examples

The type of interface to the DUT and the RF shielded test enclosure selected for testing can determine the accuracy and repeatability of the measurements.

It is important to pay special attention to the RF test interface to the DUT because of the sensitivity of these signals. For example, a product with a 50-Ohm terminated Subminiature Type A (SMA) connector populated on the board can be connected directly to a coaxial cable with a known loss. Repeatability in this scenario is very good.

Another example is a product with an embedded antenna that was designed with test points for RF and ground can be connected with a pogo-pin style RF probe. The path loss from the RF test point to the cabled connections of the setup can be calibrated to determine accurate performance. The repeatability of this setup is dependent on the board layout, in the sense that the RF and ground signals should have test points in close proximity to one another. The repeatability is also more dependent on the shielded enclosure in this case, because the RF signal is exposed at the test point rather than enclosed within an SMA connector as in the first example.

As a final example, a product with an embedded antenna can be tested over the air within an enclosure. A reference antenna would be used within the enclosure to feed back the RF signal to the RF Mux. The path loss over the air from the reference antenna to the DUT antenna can be calibrated to determine accurate performance. Fixed position of the DUT and position of the DUT and reference antennas are crucial to getting repeatable results.

5.2 Low-Volume Manufacturing Testing

The architecture and test equipment used in the characterization stage of testing is more comprehensive than that of the volume manufacturing stages.

5.2.1 Test Architecture

The test architecture in the low-volume phase of testing is very similar to that of the characterization phase.

5.2.2 Recommended Equipment

The equipment Silicon Labs recommends for the low-volume manufacturing phase of testing is very similar to that for the characterization phase. Some of the equipment may be removed depending on the tests selected for this phase.

5.2.3 Interference

There are many RF devices in a test environment, such as wireless networks, microwave ovens, and mobile phones. For this reason, it is important to maintain RF isolation of the DUT from these sources of interference. It is also important to maintain RF isolation between multiple stations. For example, the equipment for test station A should be able to communicate only with a DUT from test station A and not with a DUT from test station B. Likewise, the equipment for test station B should be able to communicate only with a DUT from test station B and not a DUT from test station A. If these stations are not isolated from each other, the DUT will not be uniquely configured and multiple boards could share unique configuration information.

5.3 High-volume Manufacturing Testing

The architecture and test equipment used in the characterization stage of testing is more comprehensive than that of the volume manufacturing phases.

5.3.1 Test Architecture

The test architecture in the high-volume phase of testing can be structured any number of ways depending on customer preference. One approach is to develop this test with a Golden Node programmed with an application that allows the DUT to obtain unique configuration information from the Golden Node through packets transmitted and received. This test may be limited to configuring one DUT at a time. The Golden Node initiates communication with the unconfigured DUT and sends unique configuration information to the DUT. The Golden Node can then interface with the PC application to configure the DUT uniquely. Then the DUT can reboot itself and be ready for testing or application operation. A basic transmit/receive test can then be run. The test architecture for this phase of testing is shown in the following figure.

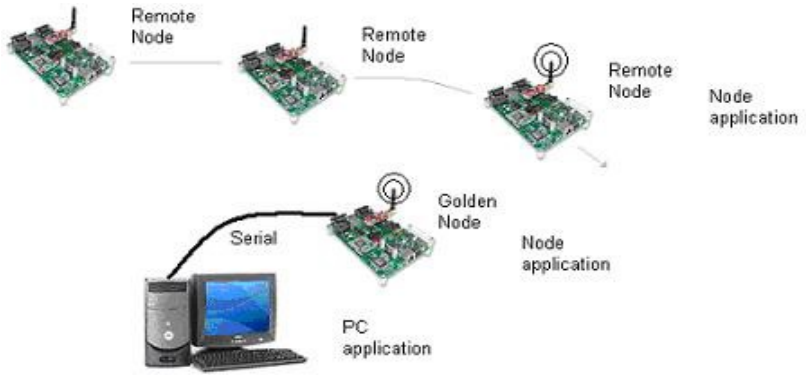


Figure 4.2. Architecture Example of a High-Volume Manufacturing Test

Another approach is to develop a test with a serial interface to both the Golden Node and the DUT. This may be more straightforward to develop but requires a more extensive set up and use of a UART.

5.3.2 Recommended Equipment

The equipment is based on the tests selected for this phase of testing, as well as the preference of the customer. No matter the approach, it is important that, at the very least, the Golden Node (and in some cases the DUT) have an interface to a PC or server so that it can log test information like EUI, test results, and so on.

5.3.3 Interference

A facility running multiple test stations maintains RF isolation among the stations, as previously detailed. In this test phase, the only interface to the DUT is power, as all communication between the Golden Node and the DUT is done through the radio. All of the test equipment used in the characterization testing can be removed from the process, unless a customer decides to continue to test certain functionality on the board that requires test equipment.

5.4 Manufacturing Coverage

Manufacturing testing not only determines the tests that should be included in the manufacturing test phase, but it also helps detect manufacturing failures. The following sections provide some examples of typical manufacturing faults and how they are detected in testing.

5.4.1 IC Manufacturing

5.4.1.1 Insufficient Solder on Ember IC

An insufficient amount of solder will result in any number of failures in test. Insufficient solder will prevent some pins on the device from making contact with the pads on the board. This will result in programming failures, serial communication failures, and RF performance problems, all of which are detected in manufacturing test. Insufficient solder on the ground pad underneath the device will result in degraded RF performance, most likely in the receiver. This type of issue will be detected in either the Receive Waterfall Test or Receive Sensitivity Test. In some drastic cases where there is no solder on the ground pad and thus no ground connection from the device to the board, the device will not function and would either fail to program or fail to calibrate properly.

5.4.1.2 Wrong Component

An incorrect component or component value will alter the performance of the board. For example, if a crystal tuning cap is the incorrect value, the Transmit Frequency Offset Test will detect this failure because the frequency will be outside the specified limits. If a component in the matching network is incorrect, this will affect the transmit power and will be detected in the Transmit Power Test. If a decoupling capacitor is the wrong value, it will affect the receiver performance of the device and will be detected in either the Receive Waterfall Test or the Receive Sensitivity Test.

5.4.1.3 Missing Component

A missing component will also alter the performance of the board. For example, if there is a component missing from the RF path, there will be a major degradation in the transmit output power and overall receive sensitivity of the board. Also, if a component is missing that affects power distributed to the microprocessor or radio chips, the board will not be able to communicate serially in the case of the micro; the microprocessor will not configure the radio to transmit or receive in the case of the radio.

5.4.1.4 Solder Shorts or Opens

A solder short or open on any component or device will cause any number of failures in manufacturing test. Any short or open in the RF circuitry of the board will cause degradation in performance and will be detected in various RF tests. A short or open in the DC circuitry or programming circuitry will prevent the device from programming properly and/or communicate properly with the test interface. For all of these cases mentioned, at least one test will detect a failure and flag this device as defective.

5.4.2 SiP Manufacturing

SiP modules contain system-level components on a substrate inside a package and for this reason they require special guidance and considerations as part of a customer board manufacturing process. Refer to *AN1223: LGA Manufacturing Guidance* for module manufacturing guidance.

6 Conclusions and Summary

As you can see from the descriptions of each test phase within this document, the recommended tests and test flow are different when comparing characterization testing with manufacturing testing.

The following table lists the test recommendations by phase and Table 6-2. Comparison of Test Phases on page 16 compares the test phases.

Note: In the following table, C denotes tests recommended for characterization testing, L denotes tests recommended for low-volume manufacturing testing, and H denotes tests recommended for high-volume manufacturing.

Table 6-1. Test Recommendations by Phase

Test	Run?	Channel			
		Mid	Low Mid High	Subset	All
Serial Communication	CLH				
Supply Current	CLH	CLH			
Transmit/Receive Verify	CLH	CLH			
Transmit Power	CL	L	C		
Transmit Frequency Offset	CL	L	C		
Transmit EVM	C		C		
Transmit Sweep	CL			L	C
Spurious Emissions	CL				
Receive Sweep	CL			L	C
Receive Sensitivity	CLH	LH	C		
Receive Waterfall	C		C		
RSSI	CL	CL			
External 32kHz Crystal	CLH				
Peripherals	CLH				

Table 6-2. Comparison of Test Phases

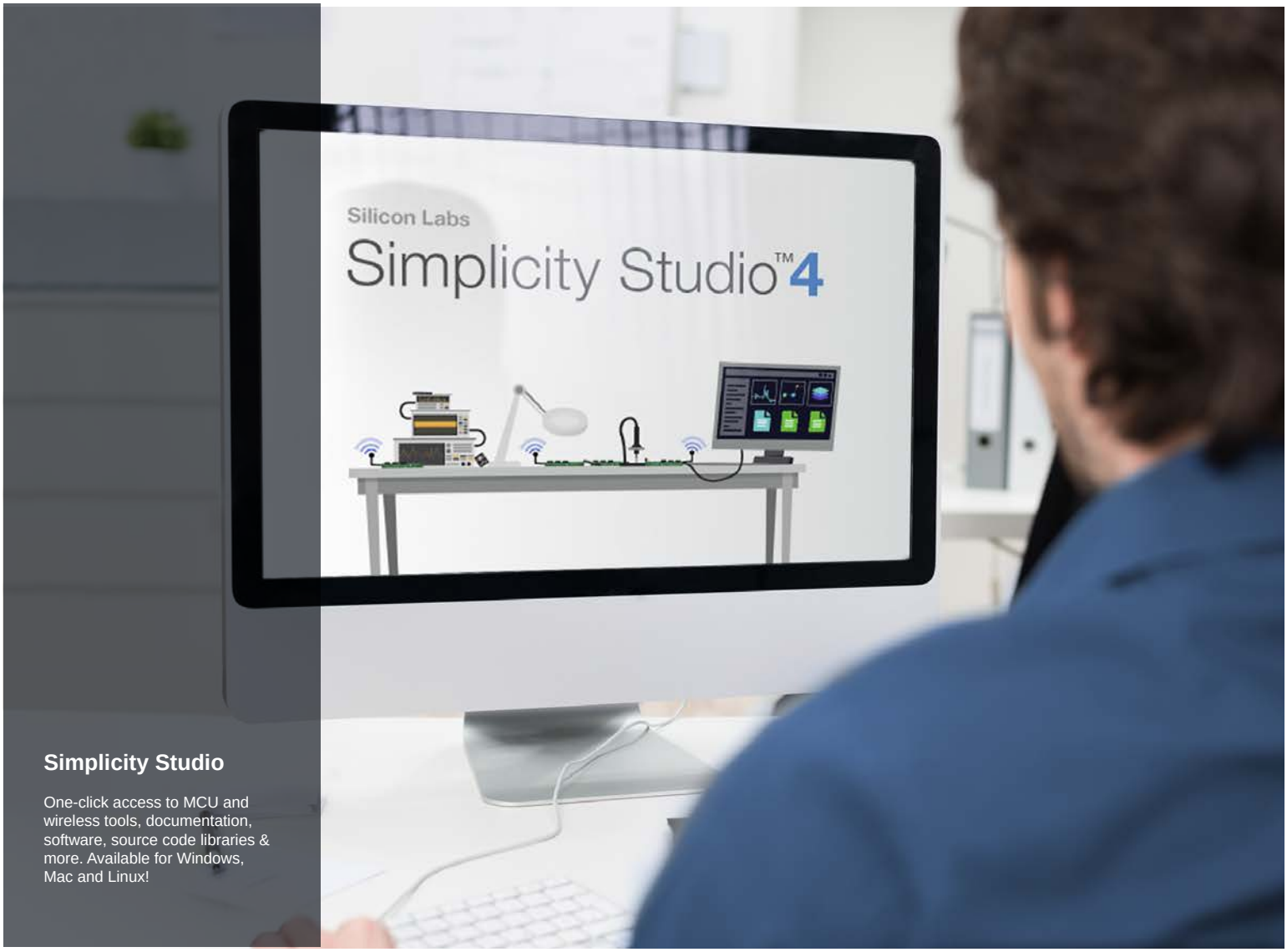
Step	Characterization	Manufacturing Low-Volume	Manufacturing High-Volume
Program bootloader (if applicable)	Functional Test	Functional Test or Preconfigured	Preconfigured
Program/load test application	Functional Test	Functional Test or Preconfigured	Standalone/Test Mode within application
Load stack information	Functional Test	Functional Test or Preconfigured	Preconfigured
Load manufacturing Information	Functional Test	Functional Test	Golden Node application
Load application information	Functional Test	Functional Test	Preconfigured
Verify DUT operation	Functional Test	Functional Test	Golden Node application

Step	Characterization	Manufacturing Low-Volume	Manufacturing High-Volume
Program/load production application	Functional Test	Functional Test	Preconfigured

In the characterization phase of testing, all programming and configuration steps can be automated to occur within the test itself. In the low-volume manufacturing phase, some of these steps can be done before actual manufacturing. For example, the device can be preconfigured with the appropriate bootloader and/or test application. In the case of high-volume manufacturing, the test functions can be included in the production application as a test mode or a standalone test application can be used. The Golden Node application can be developed by the customer to configure the appropriate unique manufacturing information for each DUT.

7 Revision History

Version 0.1: Initial Release.



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