



Learn Git and GitHub without any code!

Using the Hello World guide, you'll start a branch, write comments, and open a pull request.

Read the guide

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Zuzanaczm Update readme.md

🕒 History

👤 1 contributor

Raw

Blame



127 lines (97 sloc) | 3.25 KB

Zuzana Czmelová - Lab assignment 3 (vivado)

<https://github.com/Zuzanaczm/Digital-electronics-1/tree/main/Labs/03-vivado>

Part 1 - Table with connection of 16 slide switches and 16 LEDs on Nexys A7 board

Notice : LEDs are active-high = they are switched with logic value 1

Switches	Pins	LEDs	Pins
00	J15	00	H17
01	L16	01	K15
02	M13	02	J13
03	R15	03	N14
04	R17	04	R18
05	T18	05	V17
06	U18	06	U17
07	R13	07	U16
08	T8	08	V16
09	U8	09	T15
10	R16	10	U14
11	T13	11	T16
12	H6	12	V15
13	U12	13	V14
14	U11	14	V12
15	V10	15	V11

<https://github.com/Digilent/digilent-xdc/blob/master/Nexys-A7-50T-Master.xdc>

Part 2 - Two-bit wide 4-to-1 multiplexer

Listing of VHDL architecture from source file mux_2bit_4to1.vhd

```

architecture Behavioral of mux_2bit_4to1 is
begin

    f_o  <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;

end architecture Behavioral;

```

Listing of VHDL stimulus process from testbench file tb_mux_2bit_4to1.vhd

```

p_stimulus : process
begin

    report "Stimulus process started" severity note;
    s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "00" ;
    s_sel <= "00" ; wait for 10ns;

    s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "00" ;
    s_sel <= "00" ; wait for 10ns;

    s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "11" ;
    s_sel <= "00" ; wait for 10ns;

    s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "00" ;
    s_sel <= "01" ; wait for 10ns;

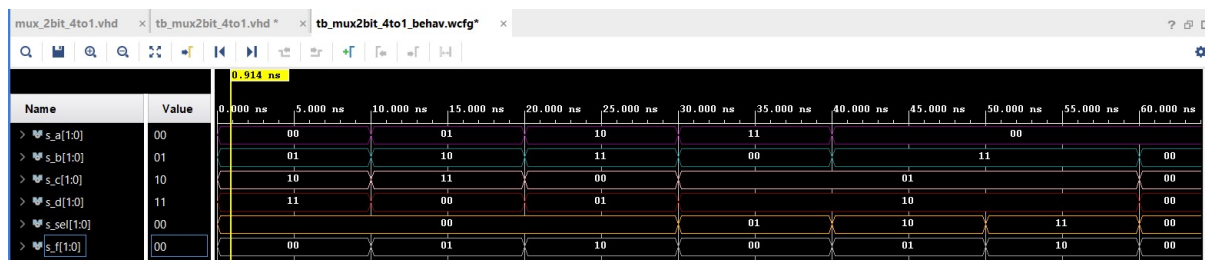
    s_d <= "10"; s_c <= "01"; s_b <= "11"; s_a <= "00" ;
    s_sel <= "10" ; wait for 10ns;

    s_d <= "10"; s_c <= "01"; s_b <= "11"; s_a <= "00" ;
    s_sel <= "11" ; wait for 10ns;

    report "Stimulus process finished" severity note;
    wait;
end process p_stimulus;

```

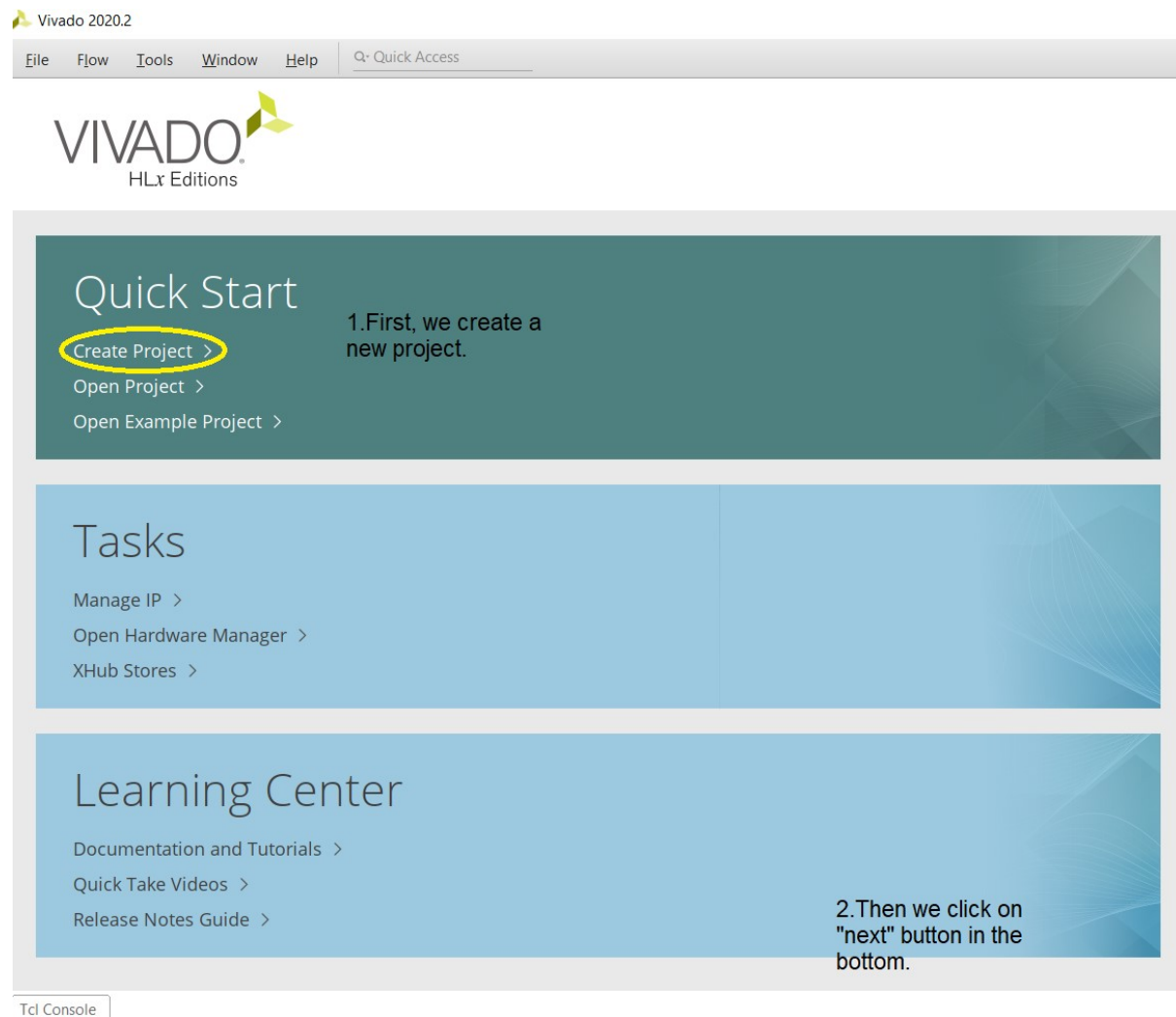
Screenshot with simulated time waveforms



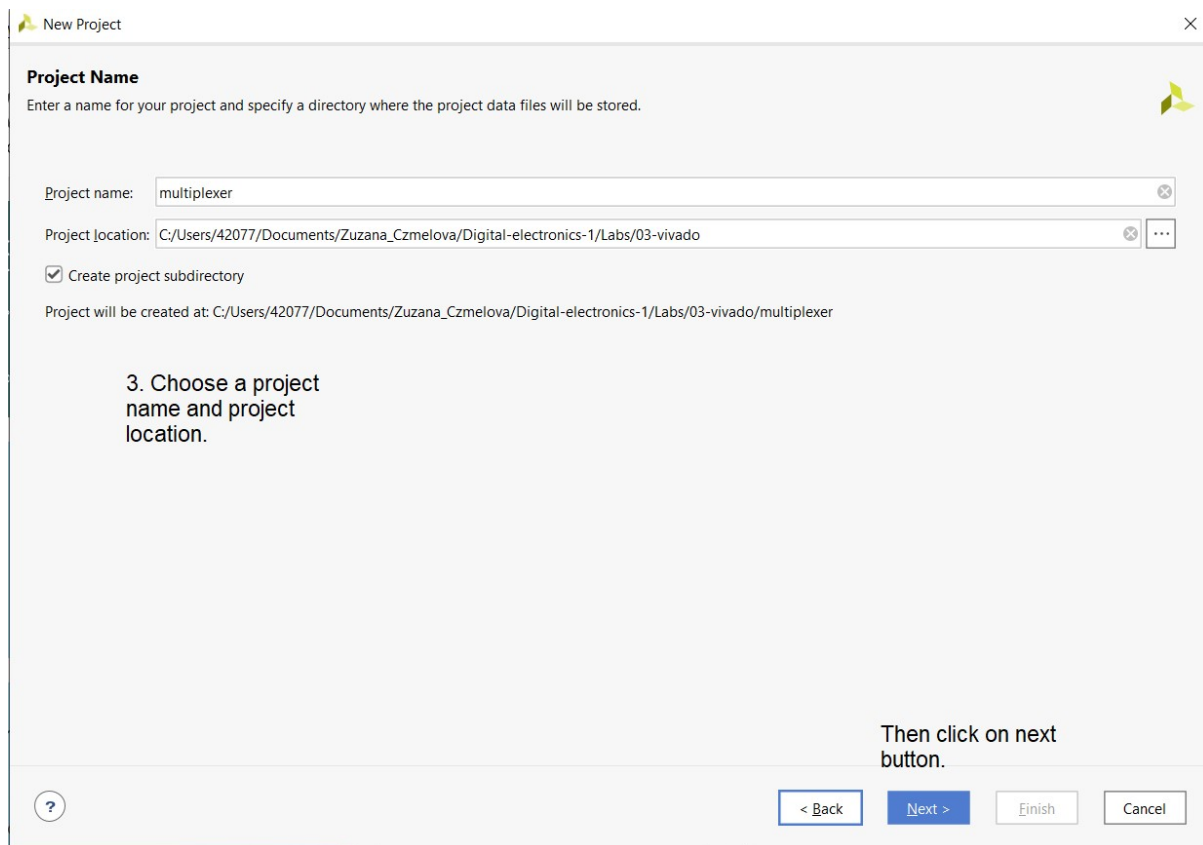
Part 3 - A Vivado tutorial

A) Creating a project

1.Create a project



2.Project name



New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

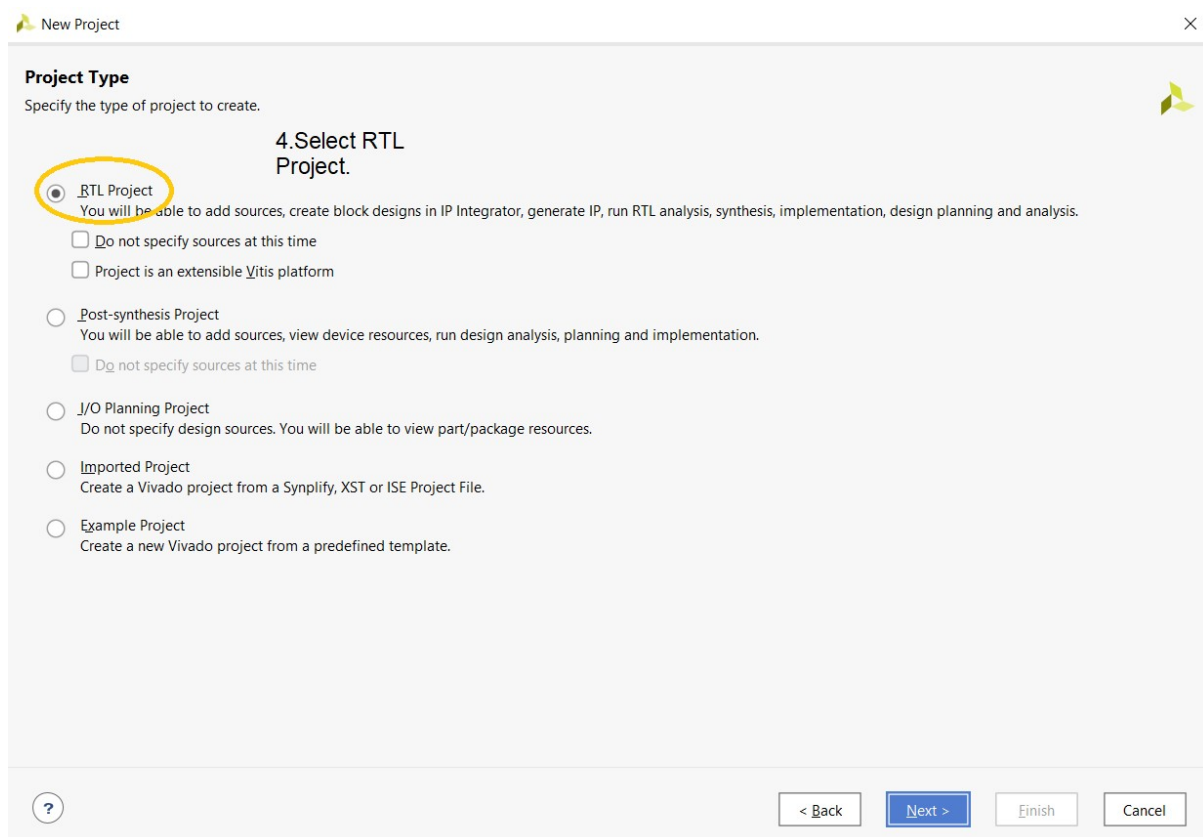
☒ Create project subdirectory

Project will be created at: C:/Users/42077/Documents/Zuzana_Czmelova/Digital-electronics-1/Labs/03-vivado/multiplexer

3. Choose a project name and project location.

Then click on next button.

2. Project type



New Project

Project Type
Specify the type of project to create.

4. Select RTL Project.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ Project is an extensible Vitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.

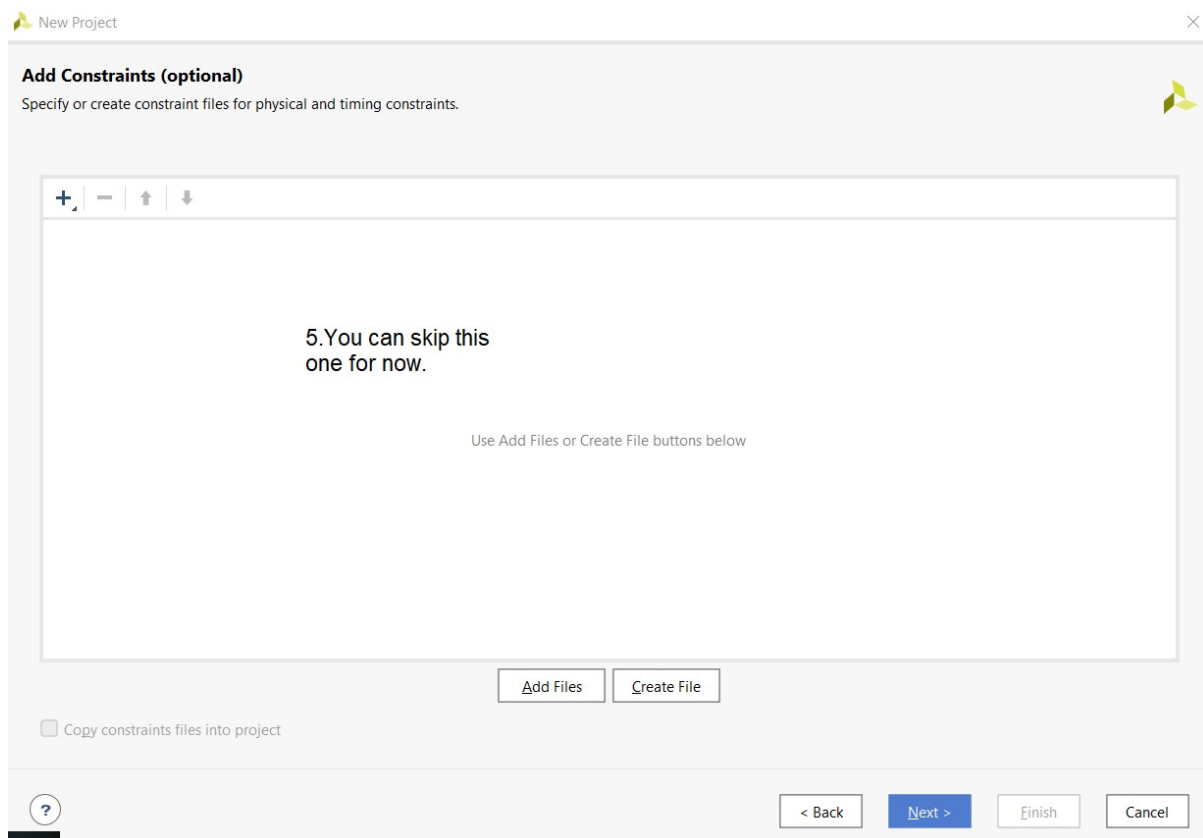
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

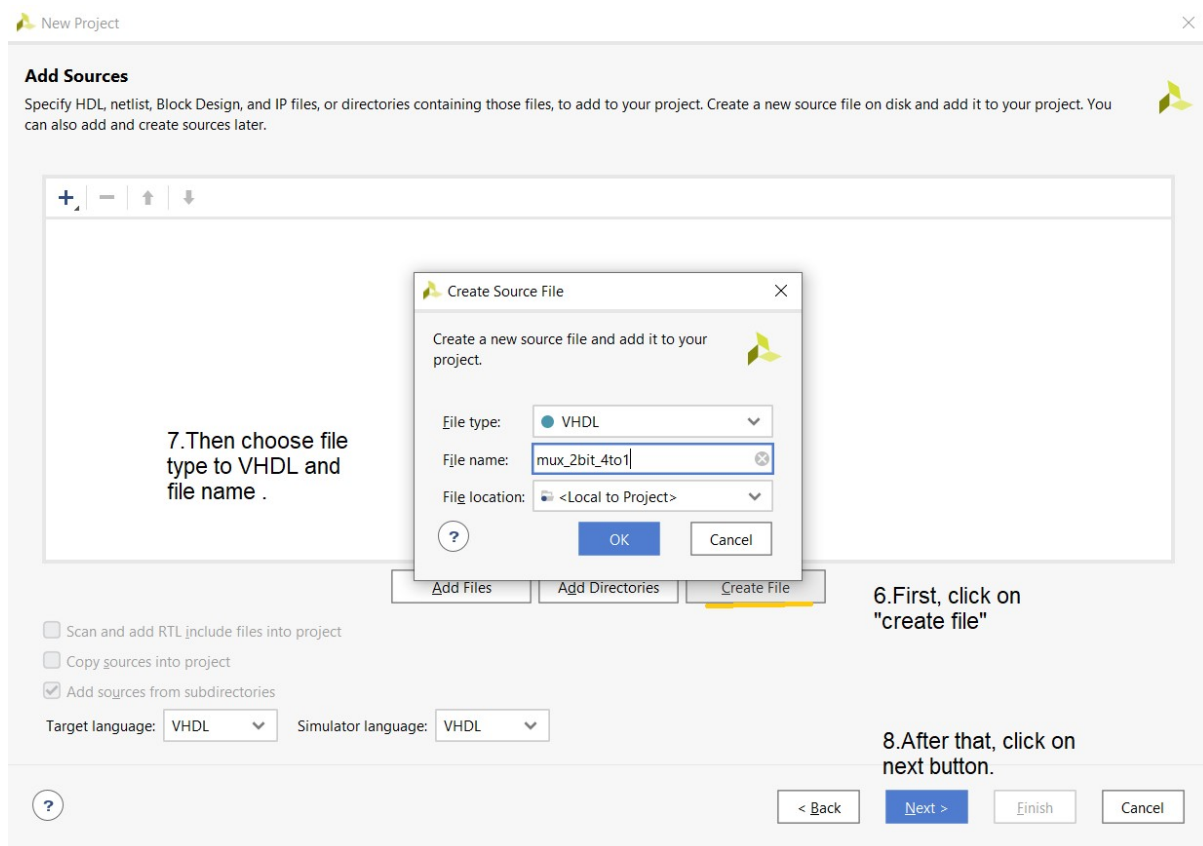
☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

3. Adding constraints (optional - in Part D)



4. Adding sources (in Part B too)



5. Default part

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts **Boards** 9. Choose boards.

[Reset All Filters](#)

Vendor: All Name: All Board Rev: Latest

Search: nexys (5 matches)

Display Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs	LUT Elem
Nexys A7-100T		digilentinc.com	1.0	xc7a100tcs324-1	324	D.0	210	63400
Nexys A7-50T		digilentinc.com	1.0	xc7a50tcs324-1L	324	D.0	210	32600
Nexys4		digilentinc.com	1.1	xc7a100tcs324-1	324	B.1	210	63400
Nexys4 DDR		digilentinc.com	1.1	xc7a100tcs324-1	324	C.1	210	63400
Nexys Video		digilentinc.com	1.1	xc7a200tsbg484-1	484	A.0	285	134600

10. Search for "Nexys A7-50T" and then click on "Install/Update boards."

11. Click next.

< Back Next > Finish Cancel

6. New project summary

New Project

VIVADO
HLx Editions

New Project Summary

- A new RTL project named 'multiplexer_' will be created.
- No source files or directories will be added. Use Add Sources to add them later.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:
 Default Board: Nexys A7-50T
 Default Part: xc7a50tcs324-1L
 Product: Artix-7
 Family: Artix-7
 Package: csg324
 Speed Grade: -1L

XILINX

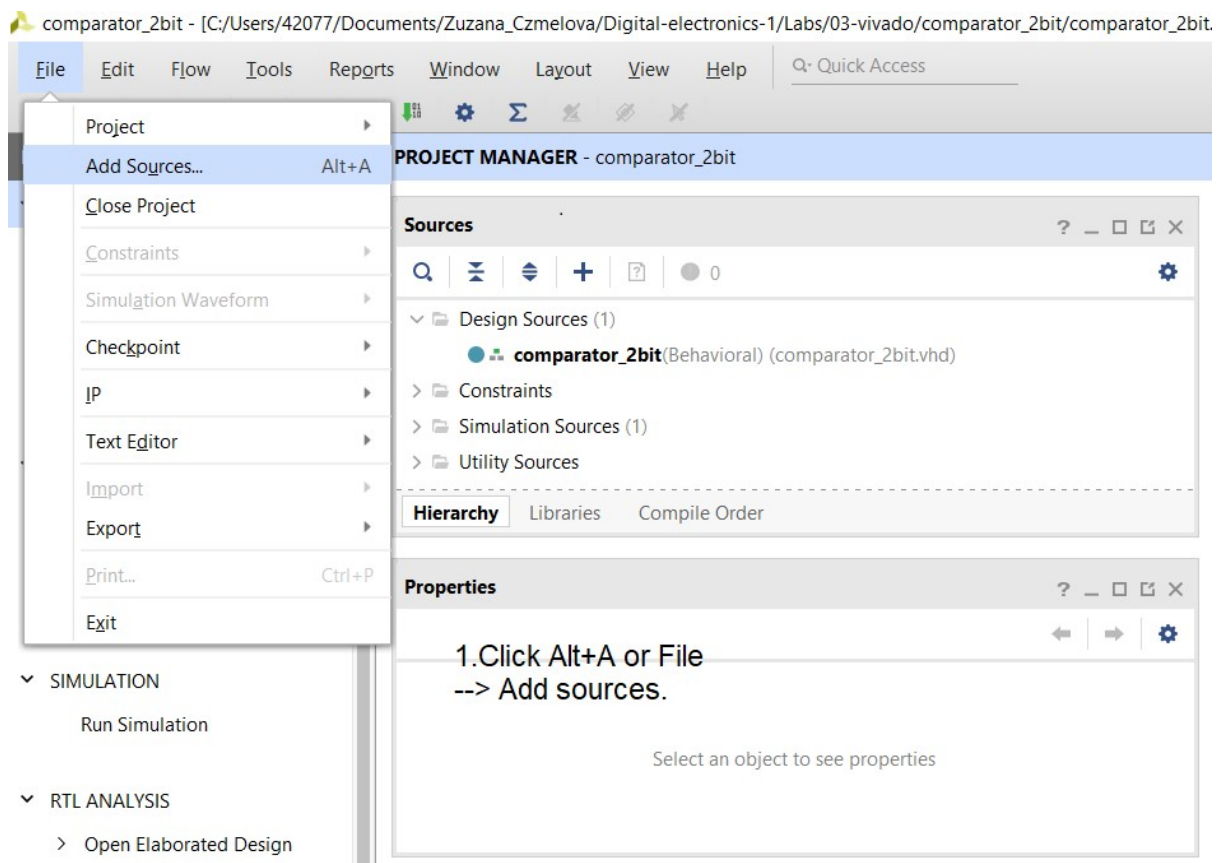
To create the project, click Finish

12. Check this summary and then click on finish button.

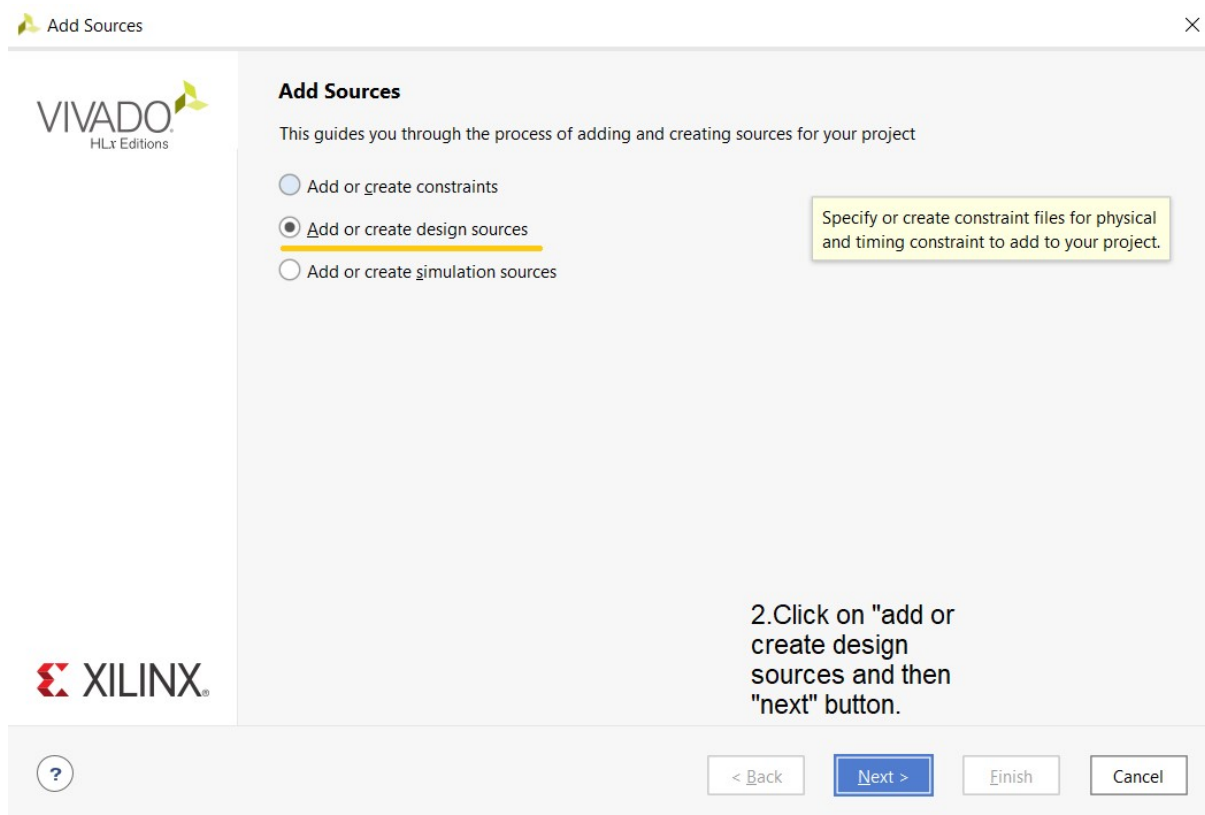
< Back Next > Finish Cancel

B) Adding source file

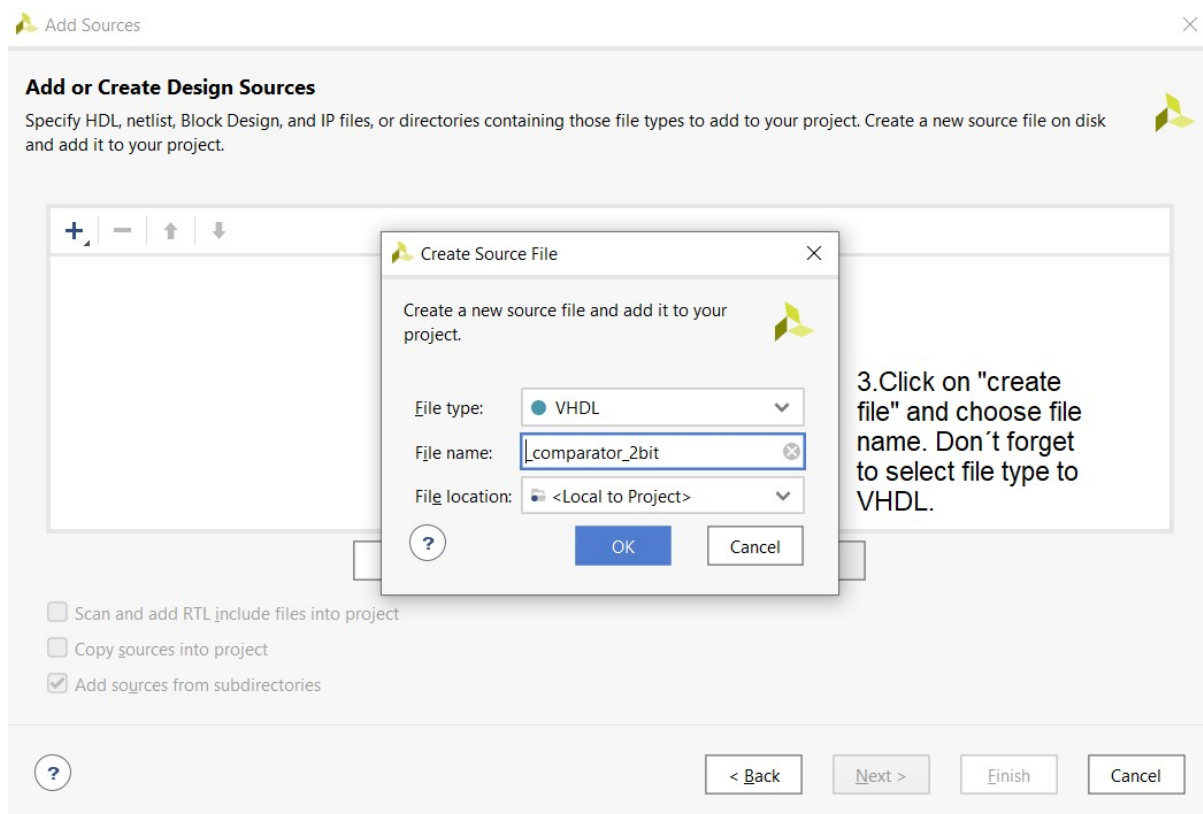
1. Add sources



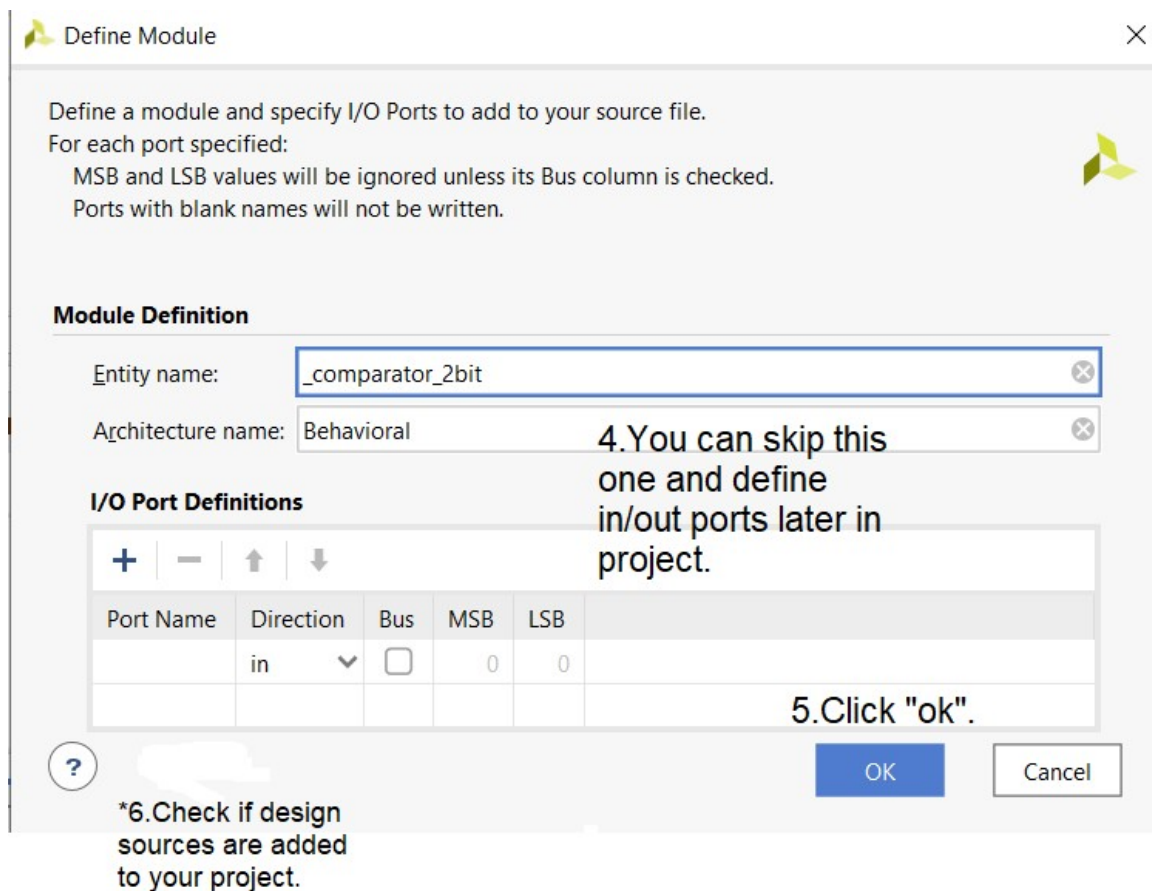
2. Choose design sources



3. Add or create design sources



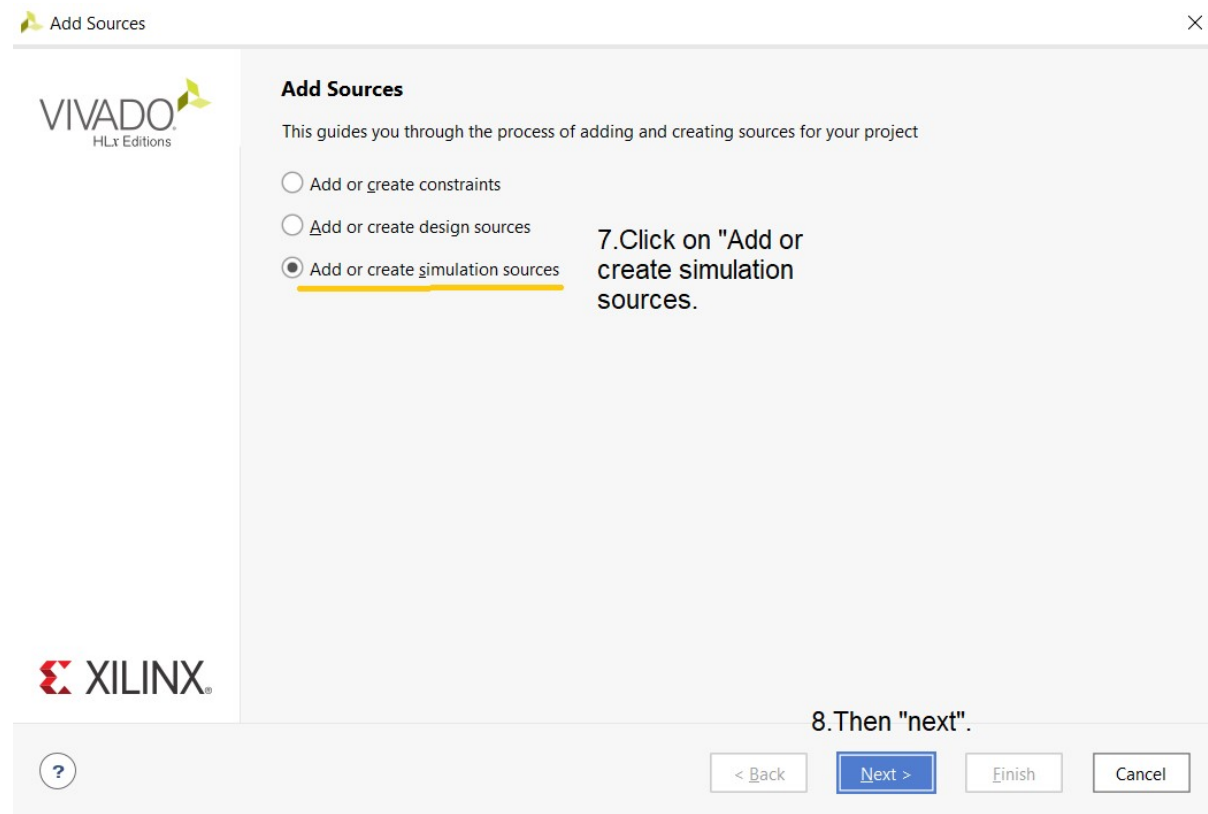
4. Define module



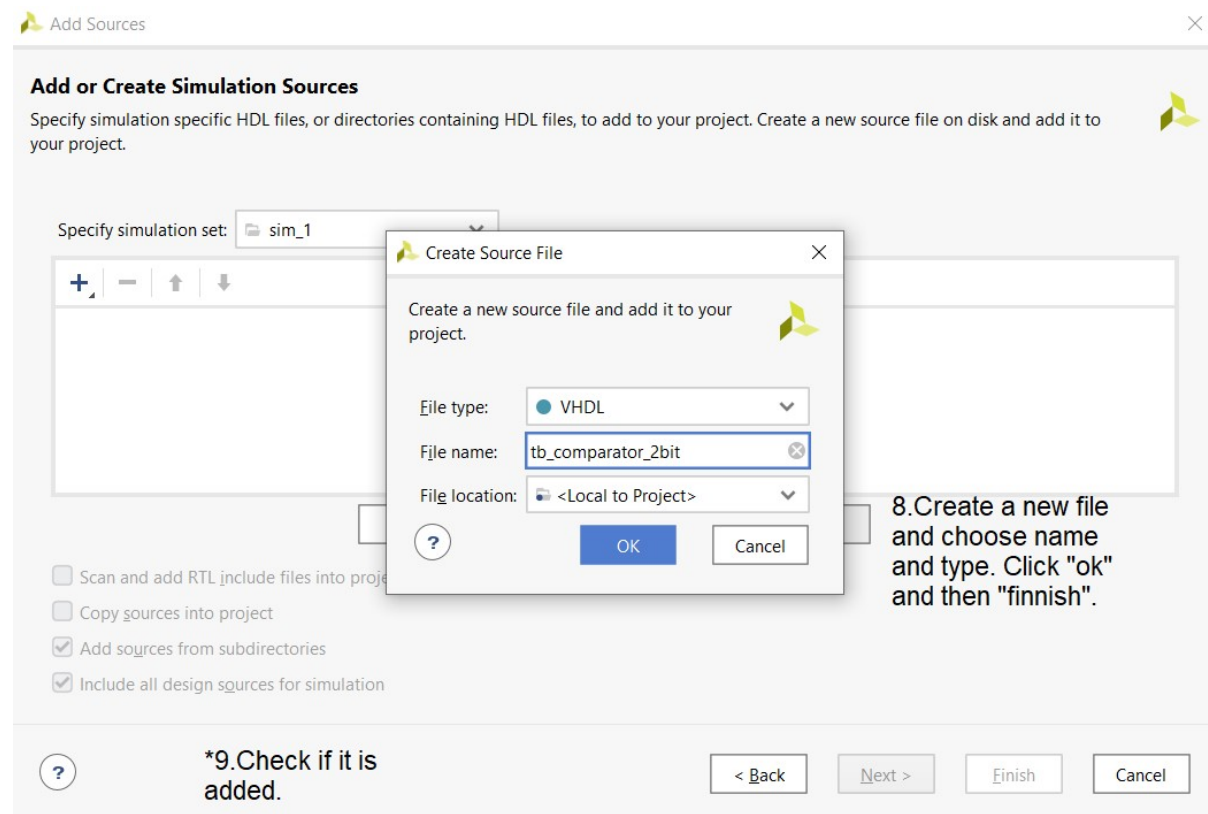
C) Adding testbench file

firstly, you click ALT+A for adding sources like in previous part (=adding source file)

1. Choose simulation sources

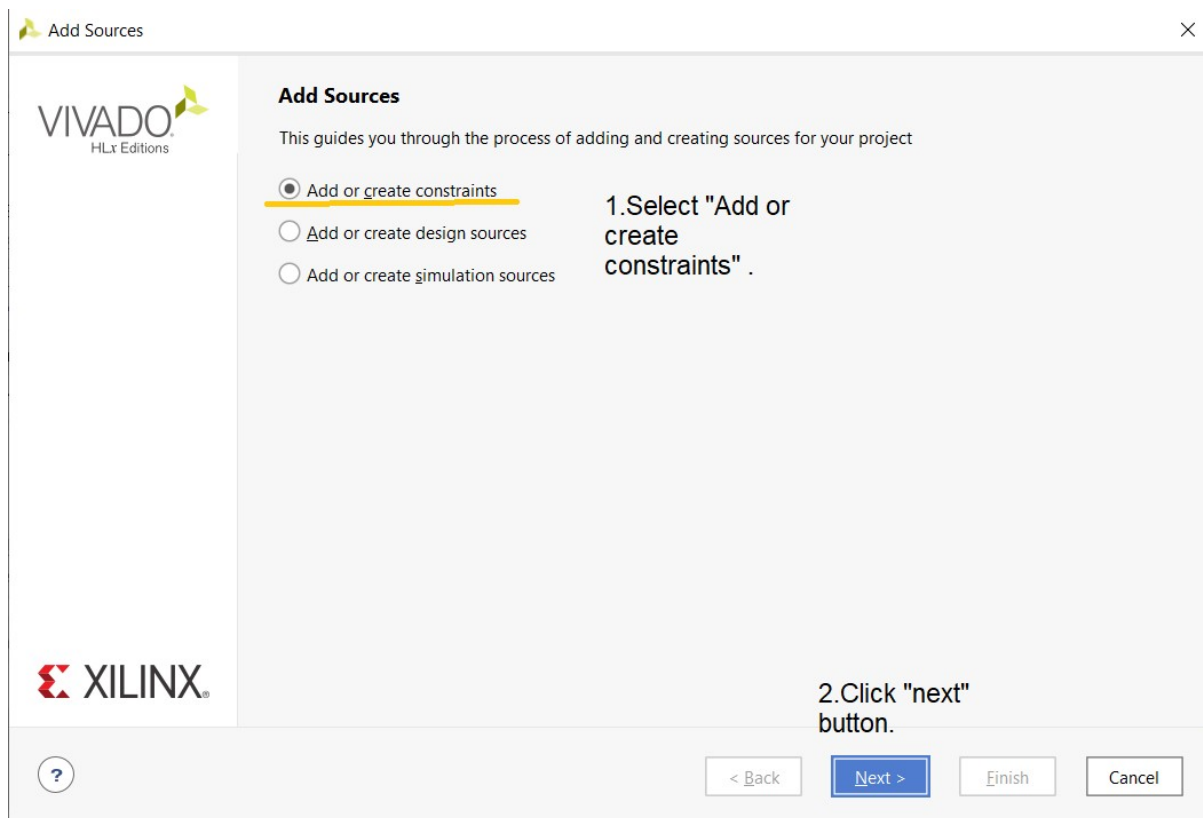


2. Add or create simulation sources

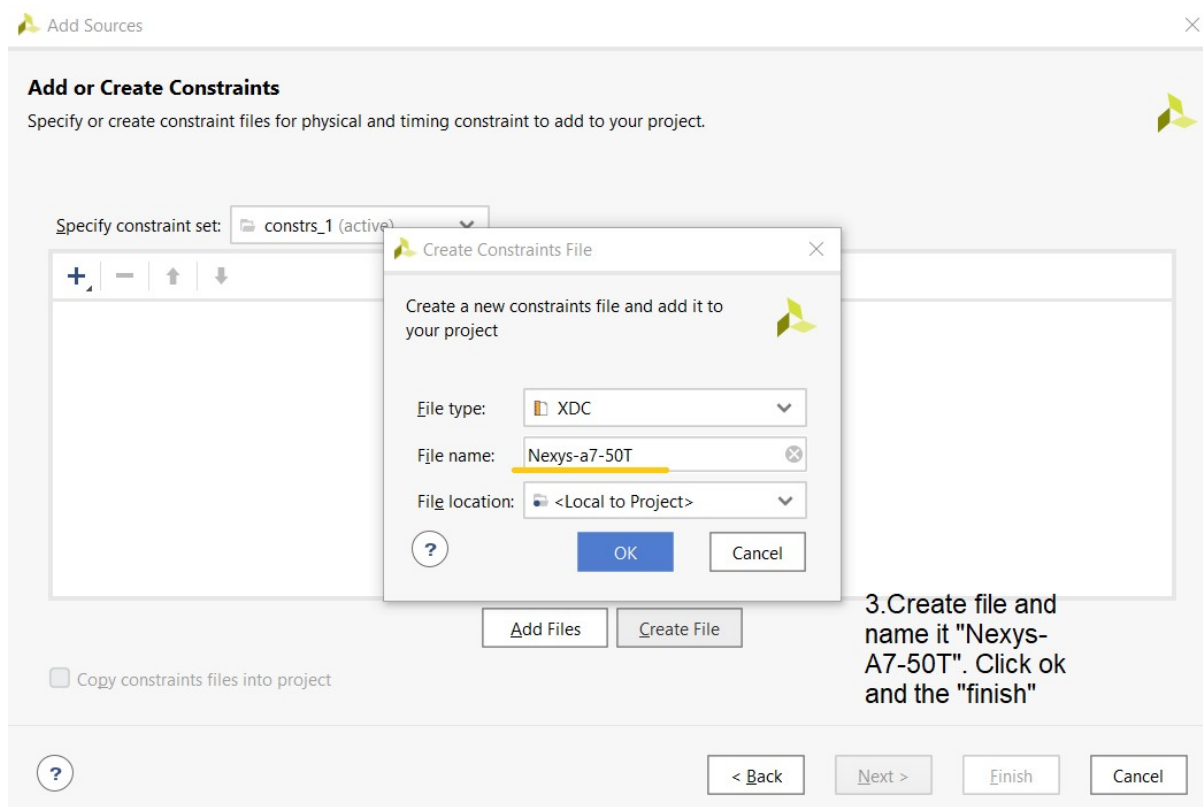


D) Adding XDC constraints file

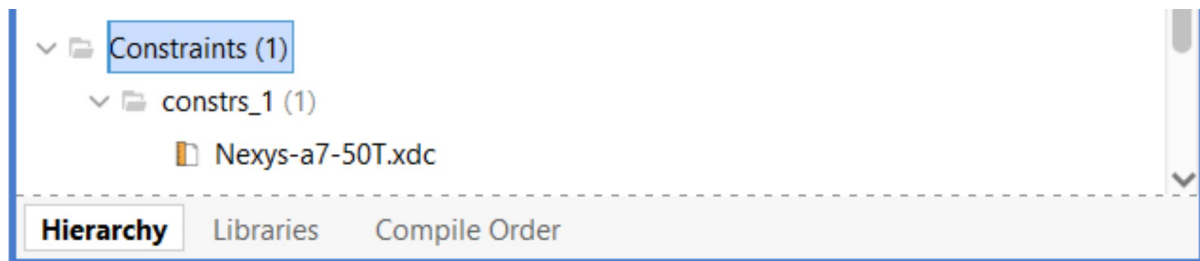
1. Choose "add or create constraints"



2. Naming constraints file



3. Checking if it is added



D) Running a simulation

