ECE649 Final Project Report

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Team Member Contributions

Both: We both decided on what different extra credit challenges we wanted to do based on how much knowledge we had of design beforehand.

Tannyr: Program Memory module, Decode module, temp, and report.

Zane: Registers module, ALU module, test code, and temp.

Introduction

For this project, we were tasked to build a CPU that supports a subset of RISC-V instructions. For this project we used Logisim-Evolution to handle the design work, and Ripes to write test code to port over to Logisim. The base requirement tasks for this project are as follows: 32-bit instruction set architecture (ISA), at least 8 registers, an Arithmetic Logic Unit (ALU), instruction support for RISC-V instructions (ADD, SUB, ADDI, LW, SW, BEQ), LCD output, and testing.

We were also given the opportunity to do advanced tasks for our CPU. These advanced tasks in most cases for us were just a basic expansion of the basic tasks and we felt they could be implemented without much difficulty. The advanced tasks we decided to implement were: support for 32 registers for addi/add/sub/lw/sw, support for R-Type instructions (and, or, xor), 3 stage pipeline support, and data hazard enhancement support. We felt like between the basic tasks and these advanced tasks, there will be enough challenge to be fun for our group but not too complicated that it felt unrealistic for us to complete the project.

CPU Hardware

Intro to section.

*Describing Hardware Layout*

Temp

*Logisim Schematics*

Temp

CPU Software

Intro to Section

*Intent Behind Code*

Temp

*LCD Task*

Temp

Conclusion

Intro to section.