ECE 65 – Components and Circuits Lab

Lab 1 Report – Circuit Simulations

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Abstract

The purpose of this lab was to apply and build upon concepts learned in ECE 35 while gaining a deeper understanding of operational amplifiers (op-amps). Several experiments were conducted, including circuit analysis of a voltage divider, graphing and simulating circuits using PSpice, and exploring the behavior of inverting terminals in op-amps. The results are closely aligned with theoretical equations, enhancing our comprehension of circuit components such as op-amps and their practical applications in real-world settings.

Experimental Procedures and Results

Problem 1: Voltage Divider (Bias Point, DC Sweep, Parametric sweep, plotting)

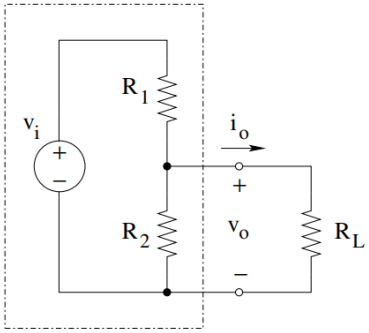


Figure 1: Circuit of Voltage Amplifier

1. Calculate the Thevenin equivalent circuit of the voltage divider (the ”box”). Use the Thevenin equivalent circuit to find vo and io in terms of vT , RT and RL. Prove that for RL >> RT , vo = vT.

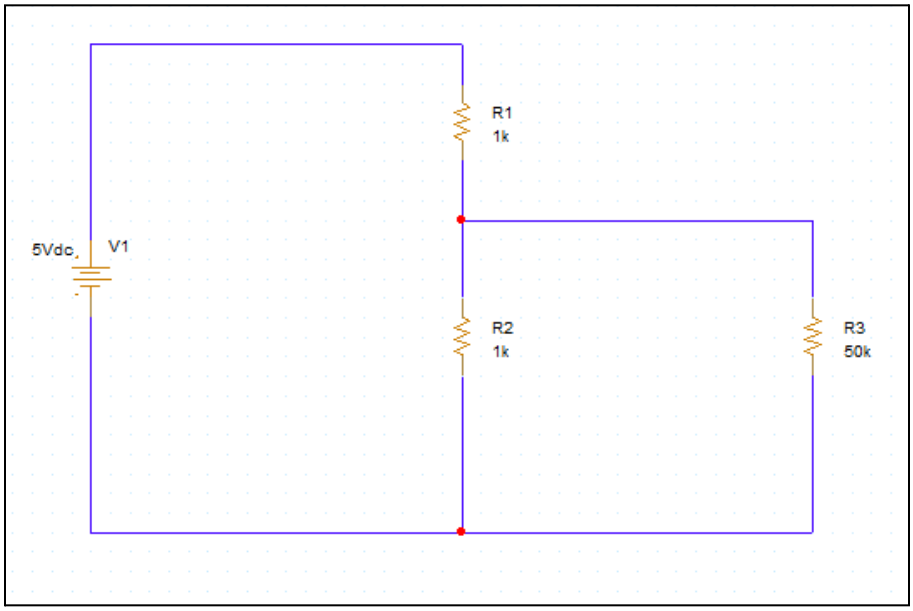


Figure 1A: Circuit Schematic of Voltage Divider Created in PSpice

In Figure 1B, we calculated the Thevenin equivalent circuit of the voltage divider (the "box") by first calculating the Thevenin resistance. To calculate the Thevenin resistance, all the independent sources are shut off; In this circuit, there is only one DC voltage source that will be shut off. As a result, the branch that the voltage source was placed in will become shorted. Therefore that branch will have 0V. Remaining the "box" is R1 and R2 in series. Therefore Rth is equal to R1+R2.

$$R_{Th} = R_1 + R_2$$

Whereas to calculate the Thevenin voltage of the Thevenin equivalent circuit, since if we turn off all independent sources, and draw the full circuit attached with the resistor RL, it can be assumed based on a KVL, that the voltage from RL, Vo, must be equal to the Thevenin voltage circuit box because both voltages must cancel out in order for KVL to be satisfied. Therefore, by calculating Vo using a voltage divider, which is:

$$V_o = V_i\left(\frac{R_2}{R_1+R_2}\right)$$

We can set Vth as equal to Vo, so: $V_{Th} = V_o = V_i\left(\frac{R_2}{R_1+R_2}\right)$. V_o can also be expressed as $V_o = R_L * i_o$ using Ohm's law.

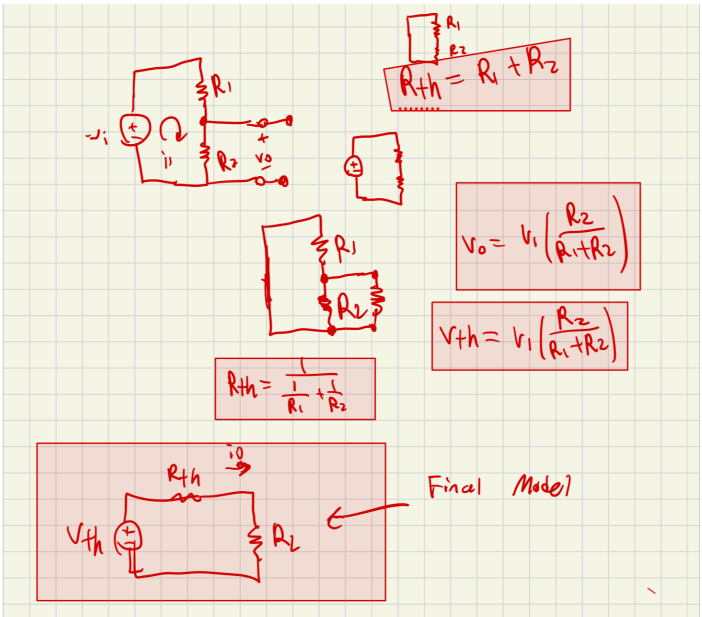


Figure 1B: Sketch of the values of Vth, Rth, and the new Thevnin Equivalent Circuit

As to why $V_o \approx V_{Th}$ when $R_L >> R_{Th}$, figure 1C in short describes the calculations made by substituting the values of Rth and io to show that Vo and Vth arrive to the same expression of $V_i(\frac{R_2}{R_1+R_2})$ when $R_L >> R_{Th}$.

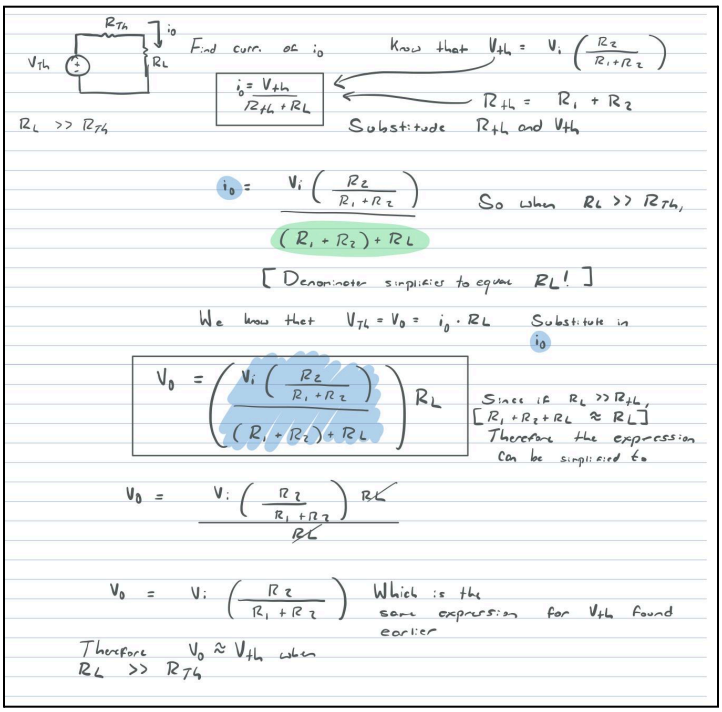


Figure 1C: Calculation as to why $V_o \approx V_{Th}$ when $R_L >> R_{Th}$

2. Use a circuit simulator to simulate the above circuit with R1 = 1 kΩ, R2 = 1 kΩ, RL = 50 kΩ, and vi = 5 V. Use ”Bias Point Details” option to find the value of vo and io.

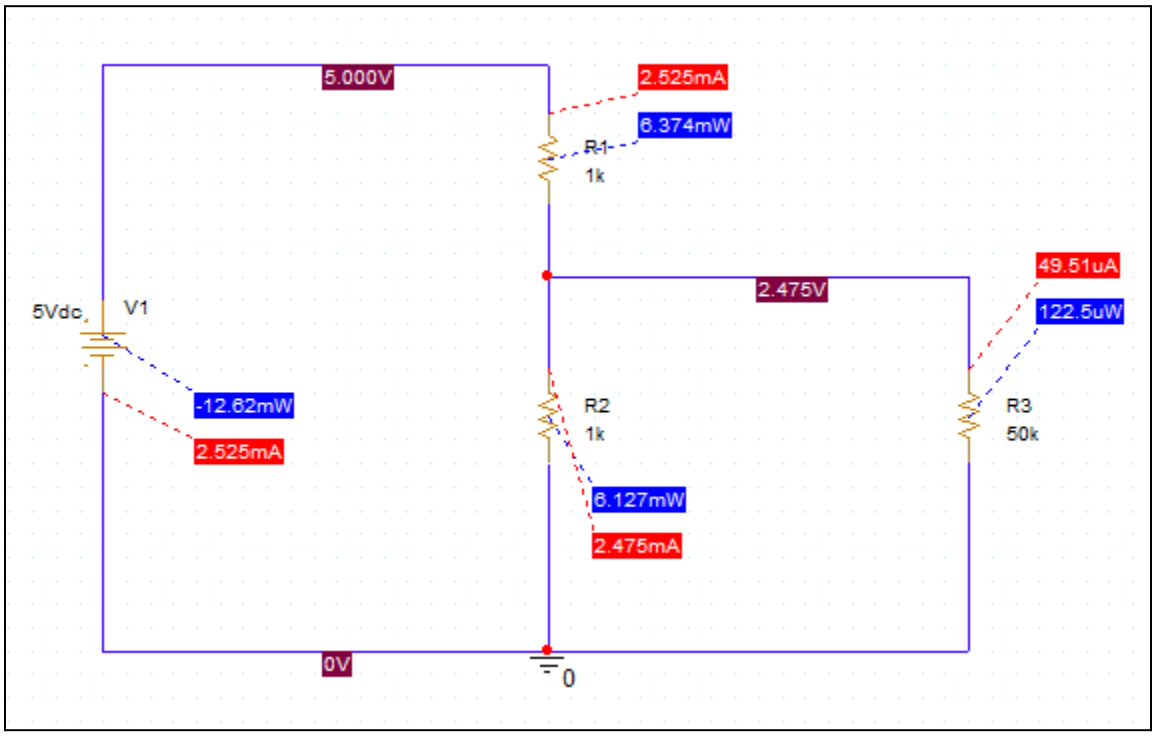


Figure 1D: Circuit Schematic of Voltage Divider Created in PSpice After Running A Bias Point Simulation

4.2 Bias Point (DC Calculations)
1) Analysis Type: Bias Point
2) Options: General Settings
   a. For Lab #6, you will also need to select Temperature (Sweep) to run the simulation at different temperatures.
3) Output File Options: None
4) Press OK and then simulate your circuit.
5) To display DC bias voltages and currents on your circuit after you run the simulation, go to PSpice => Bias Points, and check Enable, Enable Bias Current Display, and/or Enable Bias Voltage Display. You should now see values on your circuit representing current and/or voltage.

Figure 1E: Set of Instructions to Create a Bias Point (DC Calculation), Notes for ORCAD PSpice

We created this circuit diagram in PSpice, using elements such as DC voltage source, resistors, ground, and wires. Once all the circuit schematic was completed, to simulate a bias point, we

referred to the UC San Diego Notes for ORCAD PSpice, and followed these steps as instructed in figure 1E.

From the circuit schematic, we observed that vo is equal to 2.475V and that io is equal to 49.51uA.

3. Simulate the above circuit with R1 = 1 kΩ, R2 = 1 kΩ, and RL = 50 kΩ. Use DC SWEEP to generate a plot of vo as a function of vi for vi ranging from 0 to +10 V. Does it match the expression from part 1?

Figure 1F: Plot of Vo as a Function of Vi for Vi Ranging from 0 to 10V

4.3 DC Sweep on Input Source V_i
1) Analysis type: DC Sweep
2) Options: Primary Sweep
3) Sweep Variable: Voltage Source
4) Type in the name of the source you are sweeping.
5) Sweep Type: Linear (this is so you can sweep through a range of values)
6) Fill in the Start, End, and Increment Values. Type in 0.1V for the increment value to get a nice smooth plot.
7) Press OK and simulate. The simulation window should now include a place for you to plot your data. See Section 5 on how to make plots.

Figure 1G: Set of Instructions to Create a DC Sweep on Input Source Vi, Notes for ORCAD PSpice

To create this plot, we manipulated the simulation to run using the DC SWEEP to generate a plot. To set up DC SWEEP, we referred to the UC San Diego Notes for ORCAD PSpice, and followed these steps as instructed in figure 1G. Once we ran the simulation, we altered the X-axis to represent V_i ranging from 0 to +10V, and then traced V_o to generate the plot of V_o as a

function of V_i for V_i. Our results showed a linear line growing by 0.5V every following voltage increase of V_o by 1V.

This plot of Vo does match our expression from part 1 of $V_o = V_i(\frac{R_2}{R_1+R_2})(\frac{R_L}{R_L})$ as it will increase and if we plug in the resistor values given and plug in Vin as 2V into the expression $V_o = V_i(\frac{R_2}{R_1+R_2})(\frac{R_L}{R_L})$ we get that Vo is 1v, which matches with what we see on the plot.

$$V_o = (2)(\frac{1k\Omega}{1k\Omega+1k\Omega})(\frac{50\ k\Omega}{50\ k\Omega}) = 2\frac{1}{2}(1) = 1V$$

4. Simulate the above circuit with R1 = 1 kΩ and R2 = 1 kΩ, and vi = 5 V. Use parametric SWEEP to generate a plot of vo/vi as a function of RL for RL ranging from 0 to 50 kΩ (choose the increment in RL such that you have a meaningful plot, i.e., the curve looks nice and smooth). Does it match your expectations (consider cases of RL → 0, RL → ∞, and RL = RT)?

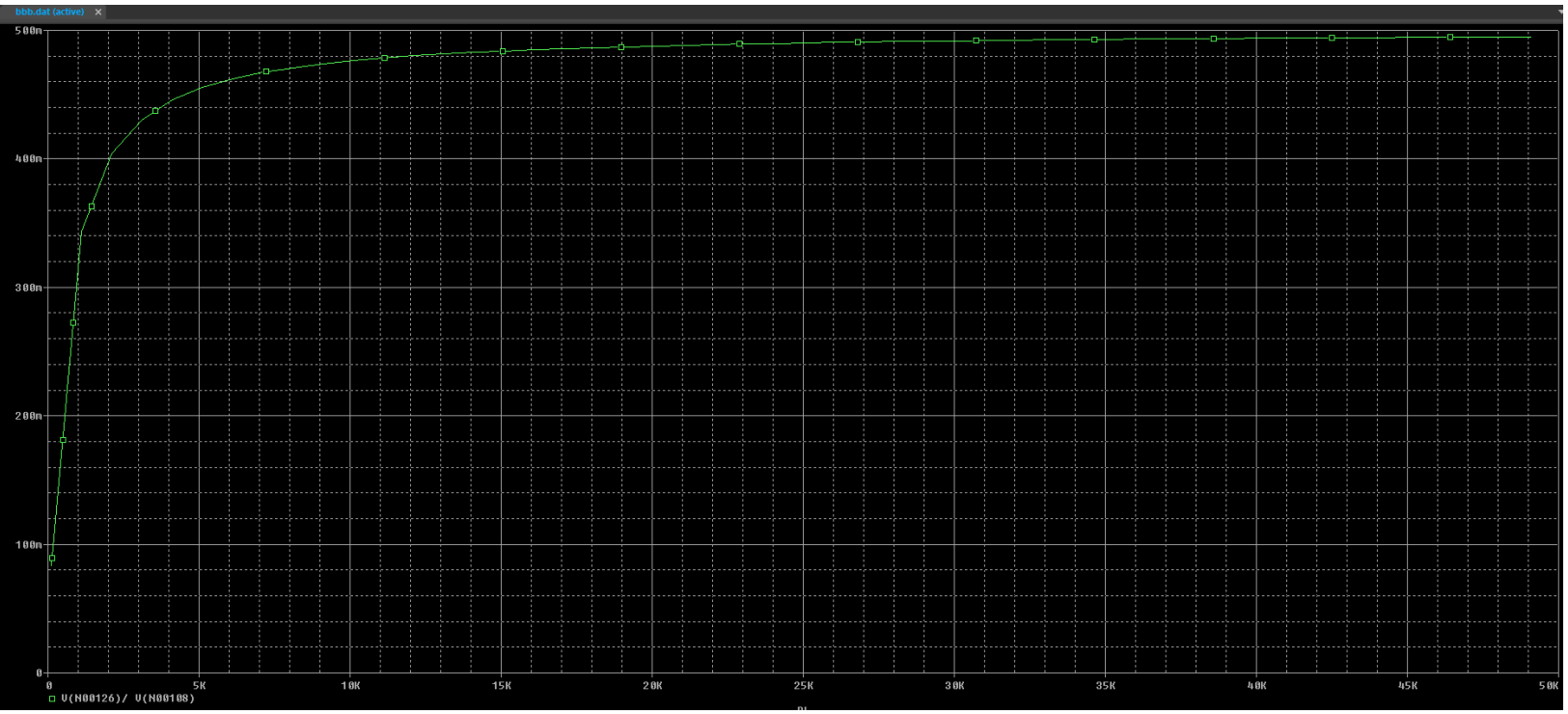


Figure 1H: Plot of Vo/Vi as a function of RL for Rl ranging from 0 to 50 kΩ

4.4 Parametric Sweep for Resistance
You will need to make the following changes to your circuit first:
1) Change the **value** of the part (not the name!) to {RL} (use curly braces, name is arbitrary)
2) Go to Place => Part
3) Add the part PARAM/SPECIAL to your schematic
4) Double click on the PARAM part
5) Click "New Row..."
6) Set the name to RL (same name as in “a” but with no curly braces)
7) Set the value to something, *e.g.,* 1k (this is the value that is used in calculating DC bias values, choose somewhere in the range of your sweep) and then press OK.
8) Select the RL column (do not double click!) so that it is highlighted and then click Display…
9) Select "Name and Value" and press OK.
10) Go back to the schematic window.
11) An example schematic from Lab 1 is shown below:

Figure 1I: Set of Instructions to Create a Parametric Sweep for Resistance, Notes for ORCAD PSpice

To create this plot, we manipulated the simulation to run using the Parametric SWEEP to generate a plot. To set up Parametric SWEEP, we referred to the UC San Diego Notes for ORCAD PSpice, and followed these steps as instructed in figure 1I.

The graph shown above matches with initial expectations that over time, as vo/vi increases and Rl increases, the voltage overall will come to a saturation point.

As RL increases, the ratio Vo/Vi gradually rises, eventually reaching a maximum value and stabilizing at a steady-state. This behavior is consistent with the circuit's expected response as RL approaches infinity because with a higher resistance, it’s harder for current to flow through the circuit, and eventually the circuit will become an open circuit if RL has a value of infinity.

5.Without changing the simulation settings in the previous part, plot io (current in RL) versus vo. Does it match your expectations? (consider cases of RL → 0, RL → ∞, and RL = RT)?

Figure 1J: Plot of io versus vo

It did match our expectations because as RL increases to infinity, the voltage of vo will approach zero since an increased resistance has to be inversely proportional to current based on Ohm's law. In the case in which RL equals 0 or near 0, the current will be near its peak since there is minimal resistance. Then in the case in which RL=RT, the current will reach a value between the minimum and maximum value of the current. These three cases help demonstrate that there is a linear relationship between io versus vo.

Problem 2: RC Circuit (VPULSE function, time-domain analysis, plotting)

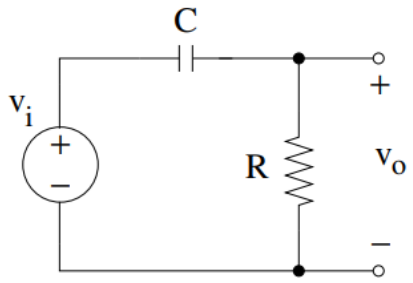


Figure 2: Circuit of RC Circuit

1.Plot vo and vi as a function of time for two periods for C = 100 nF, 1 µF, and 10 µF.

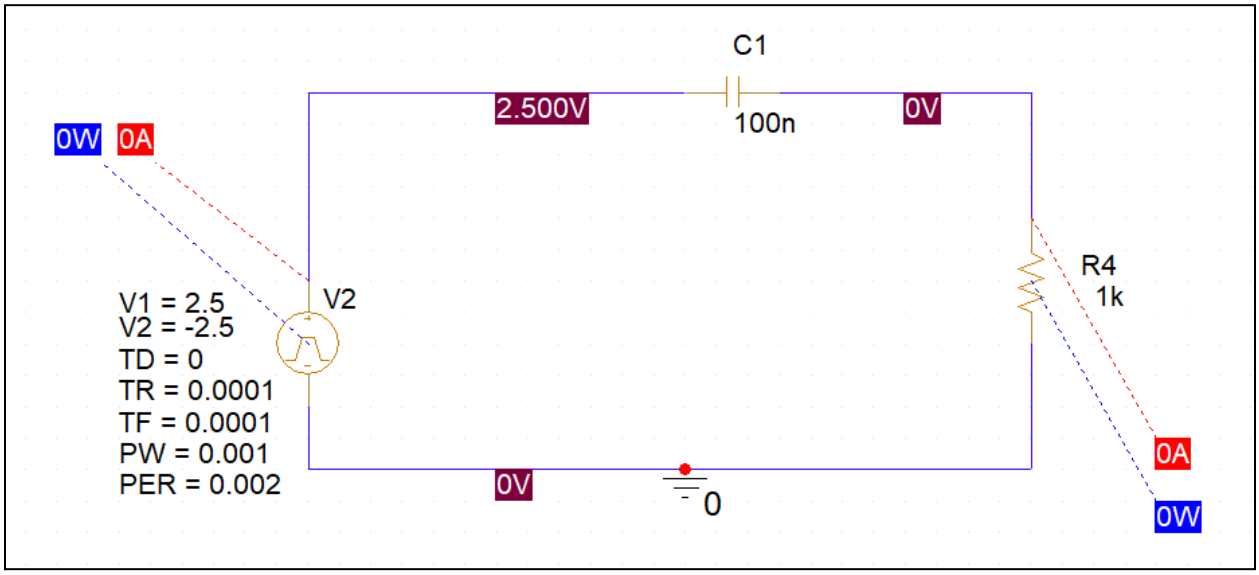


Figure 2B: Circuit Schematic of RC Circuit in PSpiceAfter Running Simulation

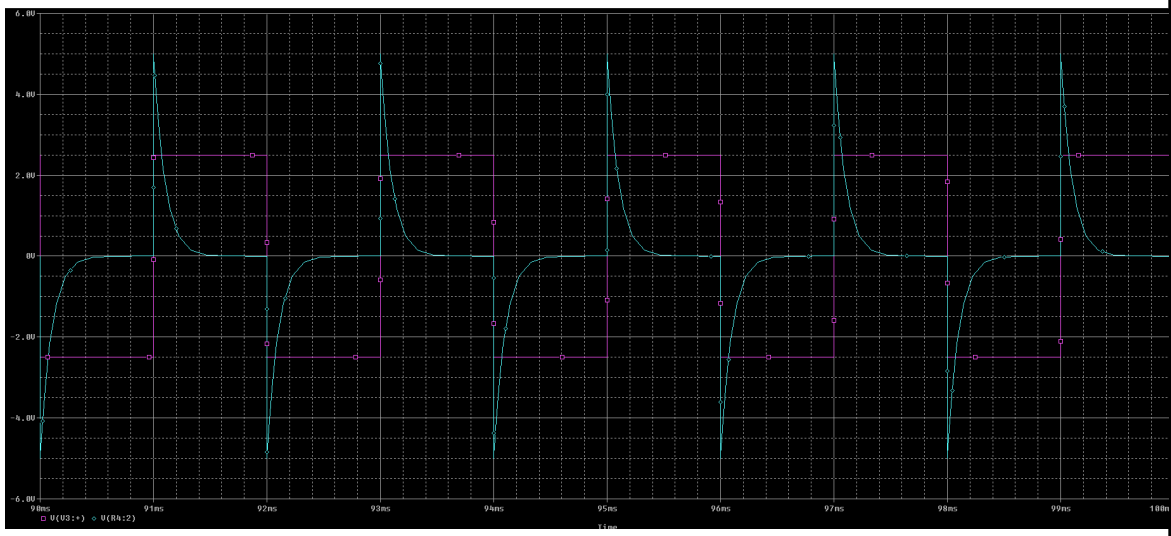
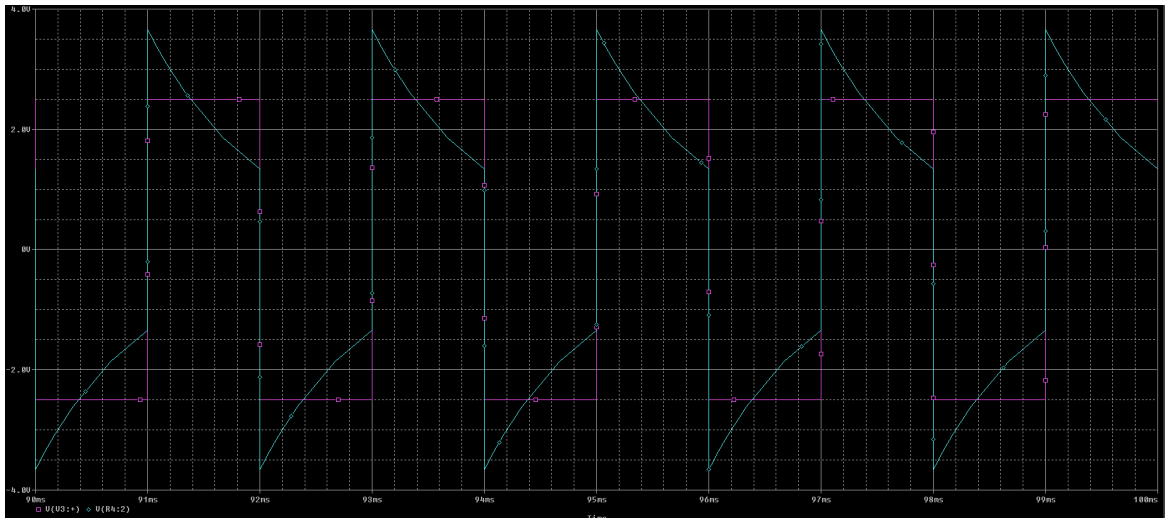
a. **Square Wave** is the VPLUSE function in the limit of TR = TF = 0 and PW = 0.5 * PER (PER is the period of the wave). This limit case, however, causes numerical difficulties in calculations. In any case, we can never make such a square function in practice. In reality, square waves have very small TR and TF. Typically, we use a symmetric function, i.e., we set TR = TF and PW = 0.5 * PER - 2 * TR. Thus, for a given frequency we can set up the square function if we choose TR. If we choose TR too large, the function does not look like a square wave. If we choose TR too small, the program will take a long time to simulate the circuit and for TR smaller than a certain value, the simulation will not converge numerically. A good choice for TR is to set it to be 1% of the PER (a period): TR = TF = 0.01 * PER, PW = 0.48 * PER. This usually results in a nice signal without a huge amount of computational need. Note that TR does not have to be exactly 1% of PER. You can choose nice round numbers for TR, TF, and PW.

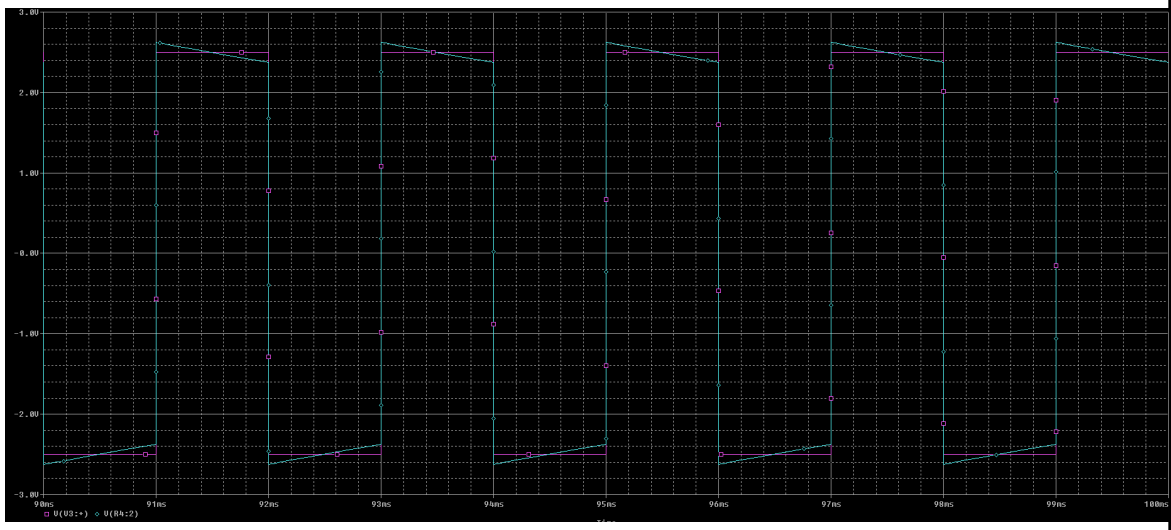
Figure 2C: Set of Instructions to Set Up VPULSE function, Notes for ORCAD PSpice

To plot Vo and Vi as a function of time for two periods for different values of C, we first recreated the circuit from Figure 2 in PSpice using the elements such as wires, resistors, a capacitor, and a VPULSE voltage source.

For the settings and values of the VPULSE voltage source, we followed the instructions for setting up the square wave from the “Notes for ORCAD Spice"; First we determined that the period of the wave is equal to 0.002 because $T = \frac{1}{f}$ and the given frequency is 500 Hz, therefore $T = \frac{1}{500} = 0.002\ s$. The PW, pulse width, is equal to 0.001; This value was calculated by taking the period value times 0.48, $0.002 * 0.48 = 0.00096$. We rounded this number up to 0.001 as a result.

Then to plot the graphs, we altered the capacitance in each case or the voltage peak to peak amplitude in each case and ran a time domain analysis simulation with 2ms as our “Run To Time” option.

5V Peak to Peak Amplitude V_i	
To the right, is the plot of V_o and V_i as a function of time for two periods for *C=100nF.* The period of the function was determined to be 0.002 s or 2 ms because $T = \frac{1}{500\ Hz} = 0.002\ s$	
1uF	

10uF	 3.0V 2.0V 1.0V -0.0V -1.0V -2.0V -3.0V 90ms 91ms 92ms 93ms 94ms 95ms 96ms 97ms 98ms 99ms 100ms V(V3:+) V(R4:2)

2. Repeat part 1 for vi having a peak to peak amplitude of 10 V, and zero DC bias

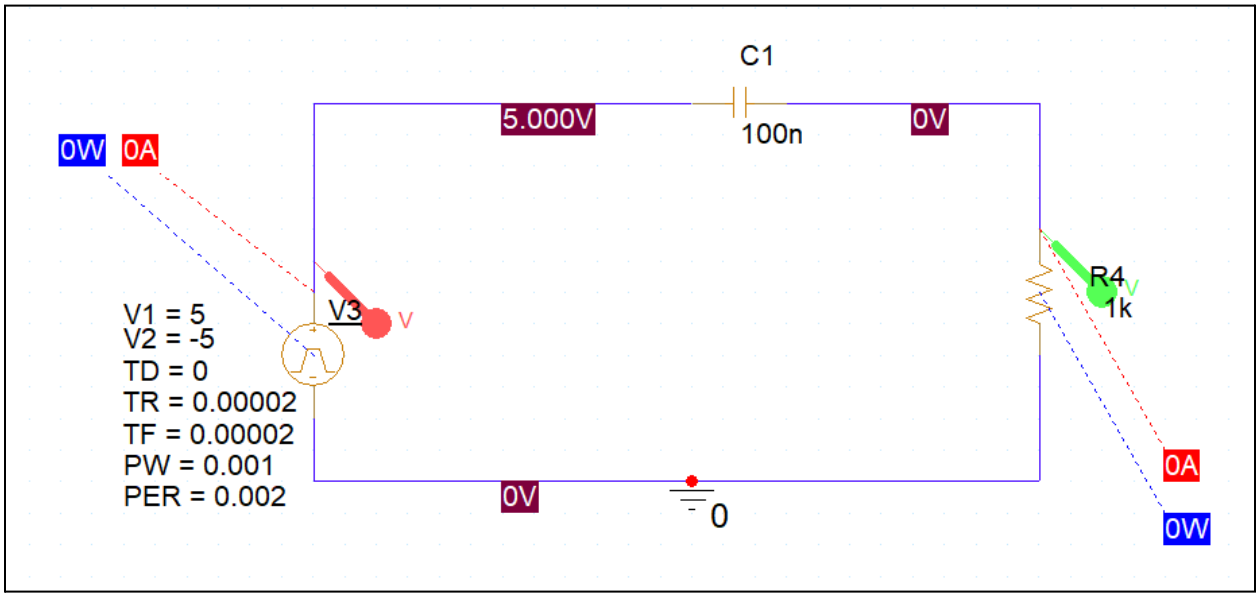
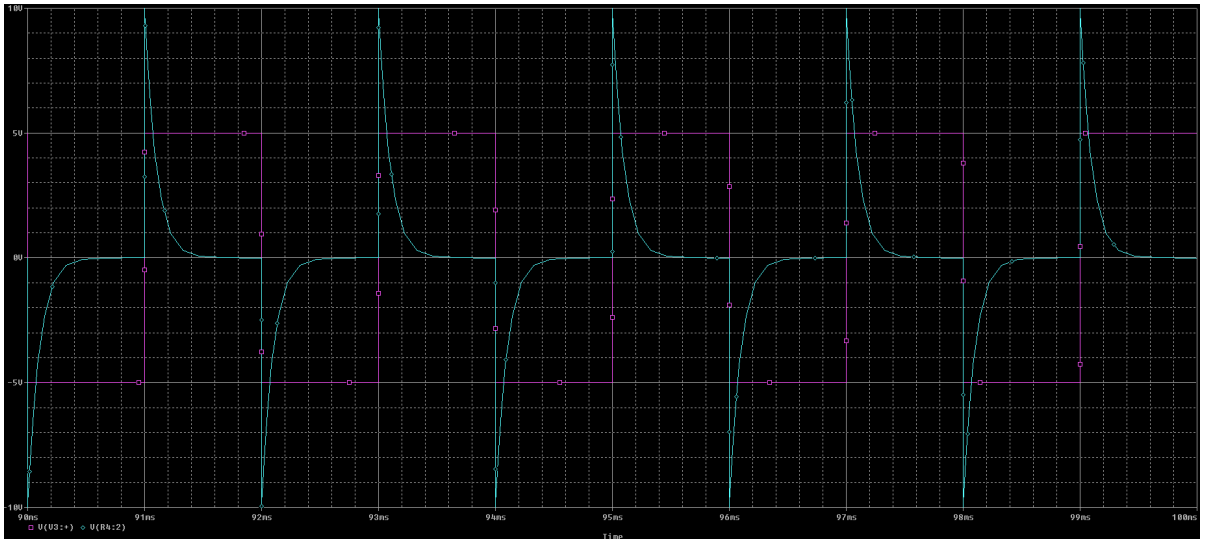
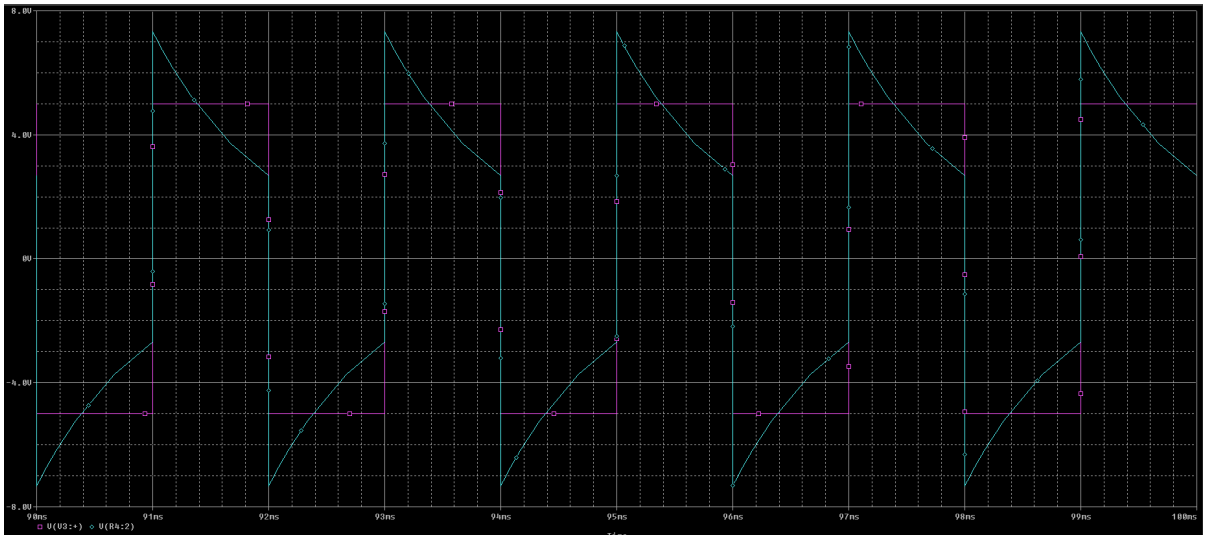
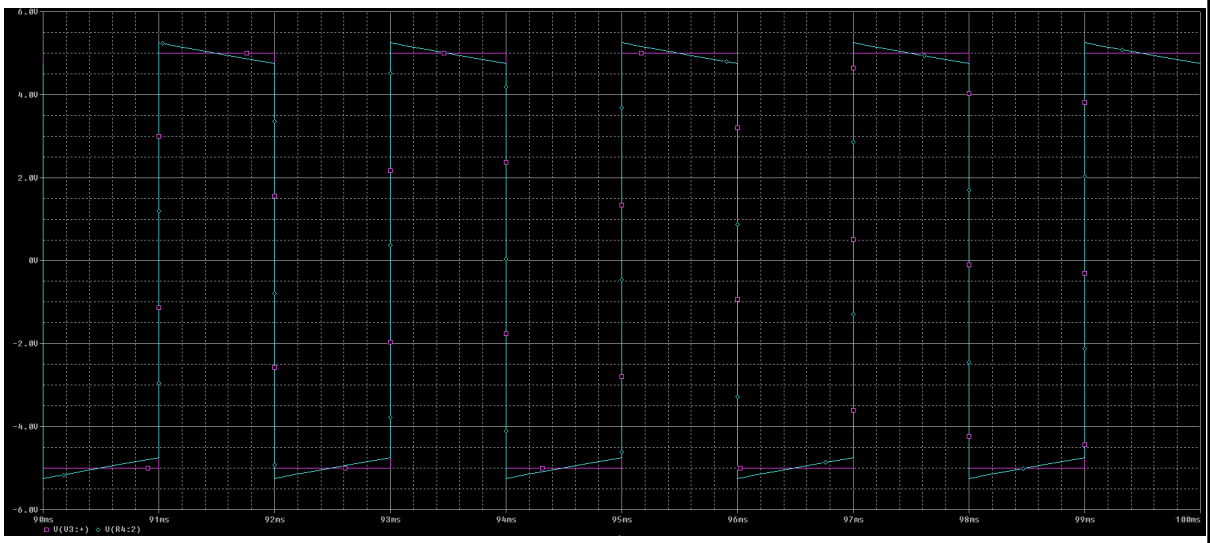


Figure 2D: Circuit Schematic of RC Circuit with a Peak to Peak Amplitude of 10V

In the figures below, the light blue represents the Vo, whereas Vi is represented by the purple square waves. For the procedure, we followed the same procedure as we did in part 2 question 1.

10V Peak to Peak Amplitude V_i	
100nF	
1uF	

10uF	 6.0V 4.0V 2.0V 0V -2.0V -4.0V -6.0V 90ms 91ms 92ms 93ms 94ms 95ms 96ms 97ms 98ms 99ms 100ms V(U3:+) V(R4:2)

3. Compute the time constant, τ = RC, of the three circuits (i.e., 3 different values of capacitor) and compare them to the half-period of the input voltage. What do you conclude from the above two simulations?

When C = 100nF, the time constant in comparison to the half-period of the input voltage is smaller than the value of the half-period of the input voltage. Given that period is equal to $T = \frac{1}{500} = 0.002\ Hz$ as we calculated earlier:

$$\tau = (1k\Omega)(100nF) = 0.0001 = 0.1\ ms$$

$$\text{Half-period} = \frac{T}{2} = \frac{0.002}{2} = 1\ ms$$

When C = 1μF, the time constant in comparison to the half-period of the input voltage is equal to the value of the half-period of the input voltage.

$$\tau = (1k\Omega)(1\mu F) = 0.001 = 1\ ms$$

$$\text{Half-period} = \frac{T}{2} = 1\ ms$$

When C = 10μF, the time constant in comparison to the half-period of the input voltage is roughly equal to the value of the half-period of the input voltage.

$$\tau = (1k\Omega)(10\mu F) = 0.01 = 10\ ms$$

$$\text{Half-period} = \frac{T}{2} = 1\ ms$$

From the above two simulations, we can conclude that if the time constant is smaller than the half-period (100nF case). The capacitor voltage will charge quickly to max and then discharge to

0 at a fasten rate. If the time constant is the same as the half period (1uf case). The capacitor voltage will be charged but not to max and decreased at a slow rate. Lastly, if the time constant is bigger than the half period (10uf case). Then the capacitor voltage will stay close to 0.

Problem 3: Op-amp as a Voltage Amplifier (Sine function, time-domain analysis, plotting)

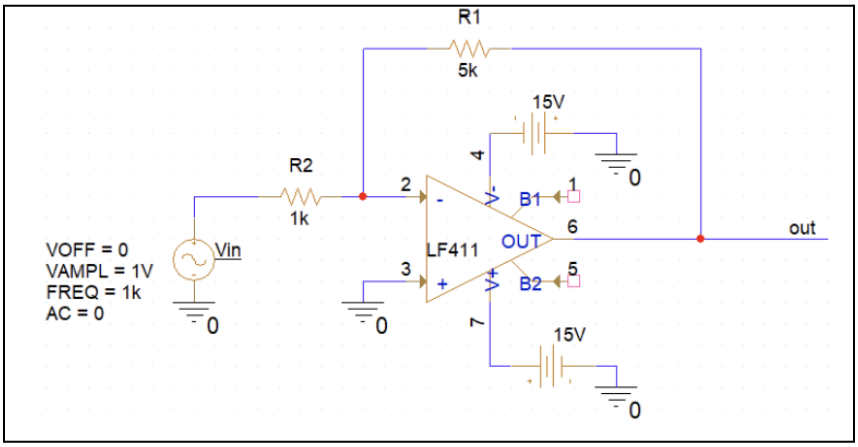


Figure 3: Circuit of Voltage Amplifier

1. Plot vo and vin as a function of time for two periods (both traces on the same plot.) Is there a linear relationship between vo and vi?

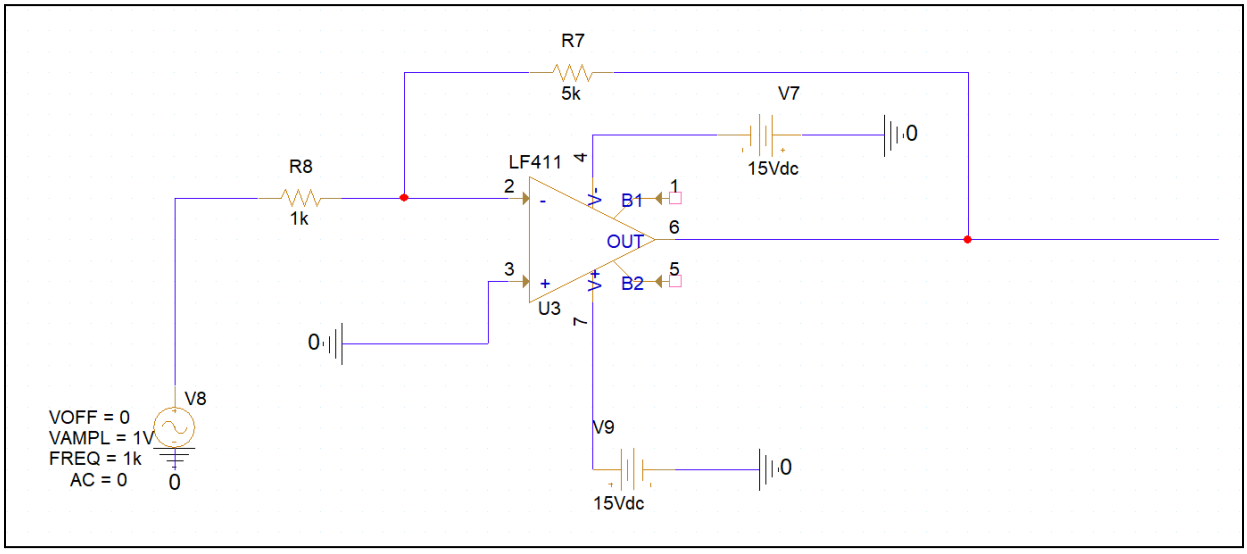


Figure 3A:Circuit Schematic of a Voltage Amplifier

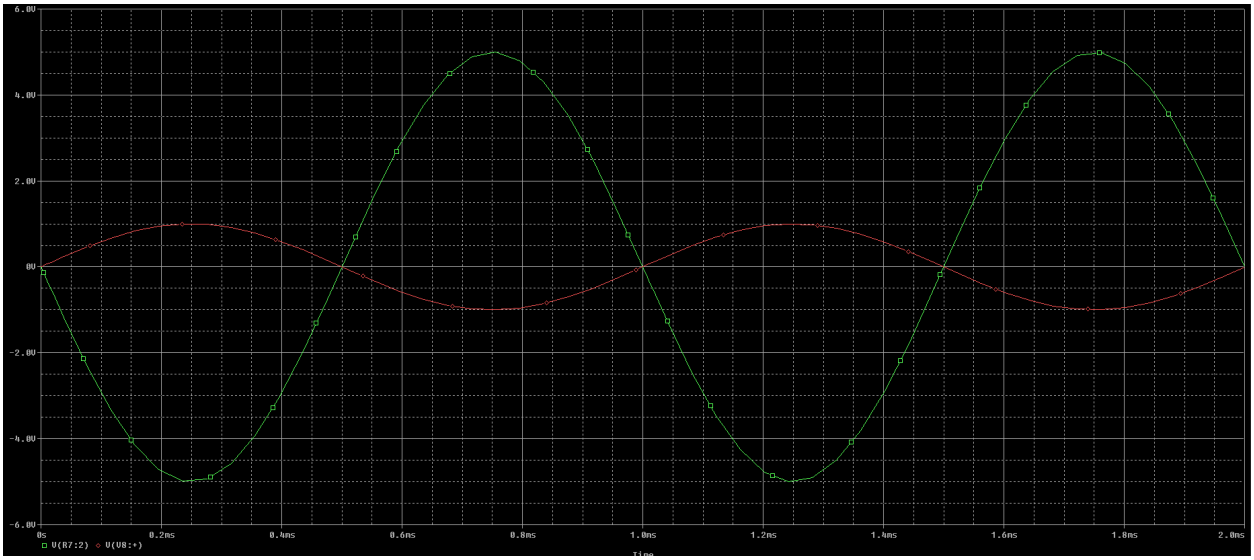


Figure 3B: The Plot of Vo and Vin as a Function of Time for Two Periods

To plot V_o and V_{in} of the circuit for two periods, we first created the circuit on PSpice, using elements such as: wires, resistors, ground, DC voltage sources, an operational amplifier (LF411), and a sinusoidal input source. Once the circuit was set up, we created an environment using the time-domain feature that recorded the voltage of V_o and V_{in} for two periods. Then by using the voltage probes, we attached them to where the values of V_o and V_{in} are recorded. Our results are as shown in Figure 3B. The plot generated two sinusoidal functions

Overall we found that there is a linear relationship between V_o and V_{in}. When vin is at the positive peak, vo will be at the negative peak and vice versa. This plot reflects how a negative feedback op amp functions.

2. Plot the output current of the op-amp as a function of time for two periods.

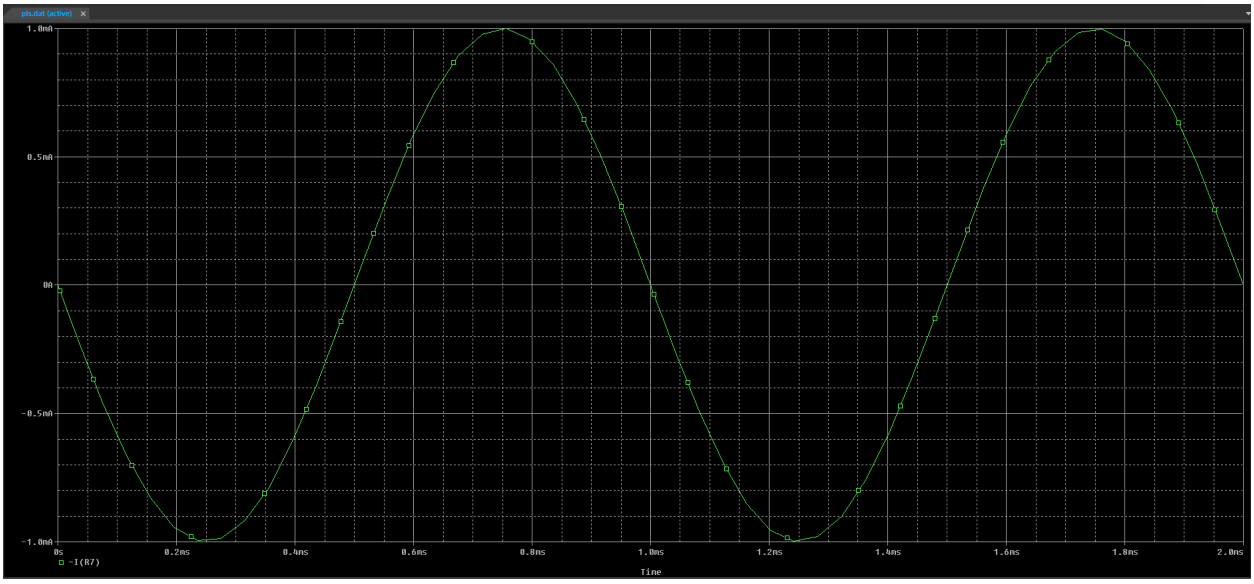


Figure 3C: The Plot of the Output Current of the Op-Amp as a Function and Vin as a Function of Time for Two Periods

To create the plot of the output current of the op-amp as a function of time for two periods, we first calculated the time for two periods, which resulted in being 2ms. Then using a time domain analysis with a run to time from 0s to 2ms, we ran the simulation and traced the plot with the output current of the op-amp.

3. Plot of the node voltage at the input inverting terminal (V-). How does the amplitude of this node voltage compared to the amplitude of Vin and the node voltage at the input non-inverting terminal?

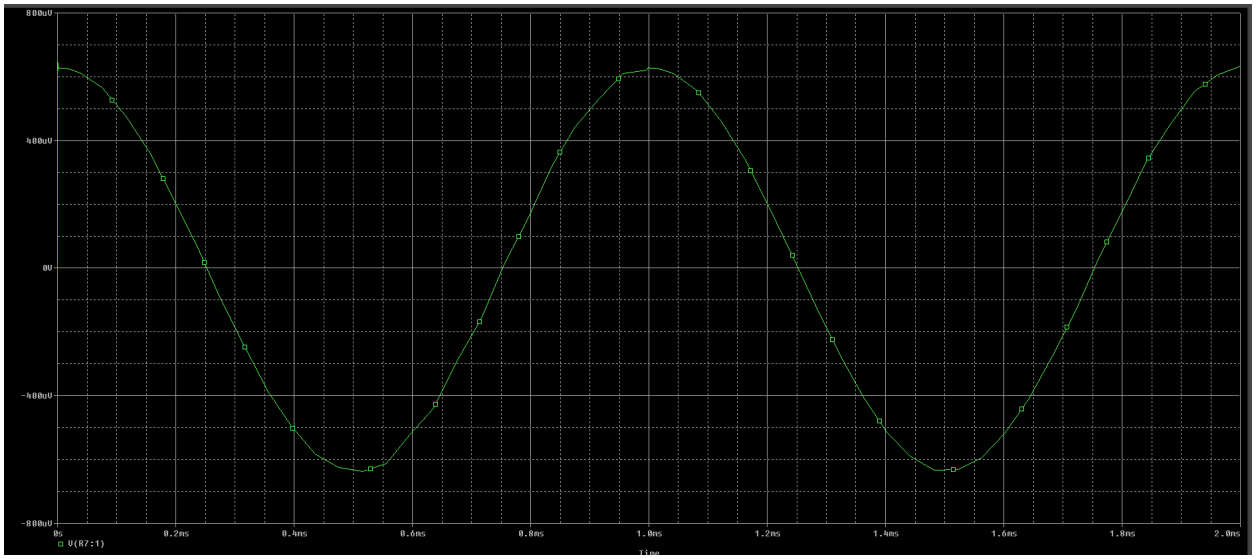


Figure 3D: The Plot of the Node Voltage at the Input Inverting Terminal (V-) for Two Periods

To create the plot of the output current of the op-amp as a function of time for two periods, we first calculated the time for two periods, which resulted in being 2ms. Then using a time domain analysis with a run to time from 0s to 2ms, we ran the simulation and traced the plot with the node voltage at the input inverting terminal (V-).

The amplitude of this node voltage is comparable to the voltage at the non-inverting terminal, as both are very close to 0. However, when compared to the amplitude of Vin, the node voltage is significantly smaller, highlighting the contrast between the two.

Conclusion

In this lab, we analyzed three distinct circuits, each with unique characteristics.

In the first experiment, we examined a voltage divider circuit with a load resistor. By determining the Thevenin voltage (Vth) and resistance (Rth), we constructed a Thevenin model and attached it to the load resistor. We concluded that when the load resistor is larger than the Thevenin resistor, the voltage drop across the load resistor significantly exceeds that across the Thevenin resistor. Using KVL, we observed that the voltage across the load resistor was closely aligned with Vth. Simulations in PSpice, incorporating different "sweeps," demonstrated that the voltage drop across the load resistor was linearly proportional to the load resistance. As the load resistance decreased, the voltage drop similarly decreased.

In the second experiment, we analyzed an RC circuit's response to different time constants by using three capacitors with varying capacitance values. Our observations revealed that when the time constant was less than half the period, the capacitor charged and discharged rapidly, moving from maximum voltage to zero efficiently. When the time constant was approximately equal to half the period, the capacitor struggled to reach maximum voltage and exhibited slower decay. For time constants exceeding half the period, the capacitor barely charged, resulting in small and stable voltage levels.

In the final experiment, we explored the voltage amplification capabilities of operational amplifiers. Using a sinusoidal input source and an LF411 op-amp, we constructed a negative feedback voltage amplifier. The feedback circuit fed the output back into the inverting terminal, creating an amplified yet inverted output. Simulations revealed that the node voltage at the inverting terminal (V^-) remained near zero, consistent with the grounded non-inverting terminal

(V^+). The output voltage displayed an inverted sinusoidal waveform, showcasing the expected behavior of the op-amp.