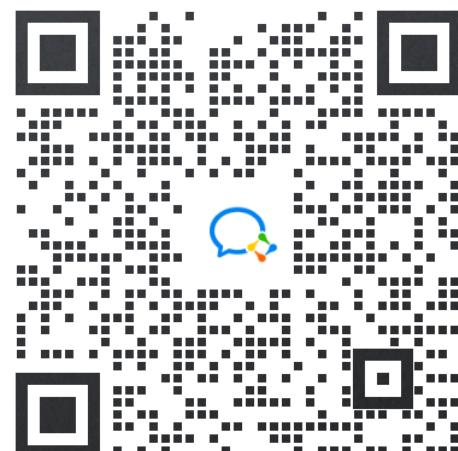


iEDA: An Open-Source Intelligent Physical Implementation Toolkit and Library

ISEDA 2023

May 09, 2023

WeChat Group:



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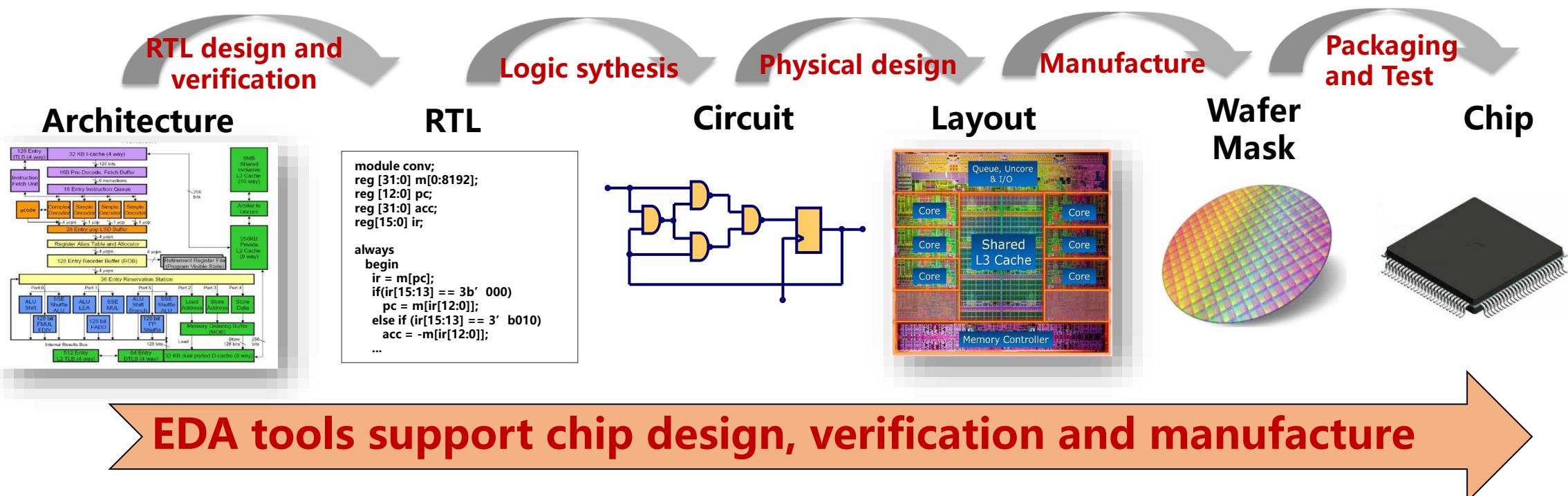
QQ Group : 793409748



- 01 **Introduction**
- 02 **iEDA Today**
- 03 **iEDA Future**

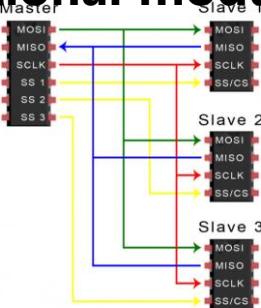
Chip Design Flow

- **Function:** Generate module-level and system-level chip code and verify functionality validity.
- **Circuit:** Convert RTL code into a netlist through logic design and technology mapping.
- **Layout:** Physicalize the netlist into a layout (GDSII) by using physical design tools.
- **Manufacture:** Form a chip by etching and packaging the designed layout.

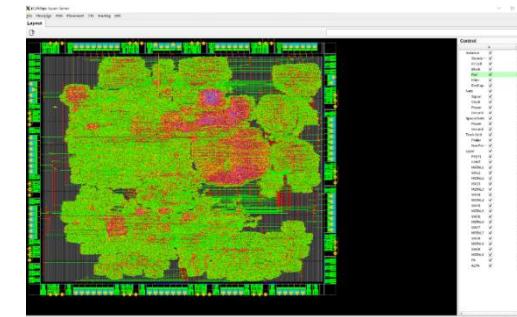


Chip Design Elements

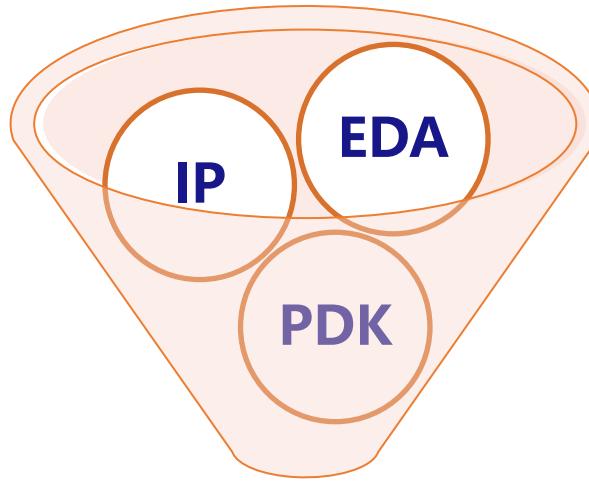
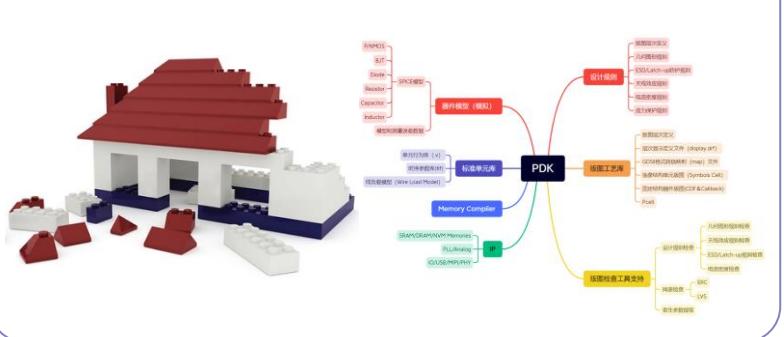
**IP: Intellectual Property
Functional module**



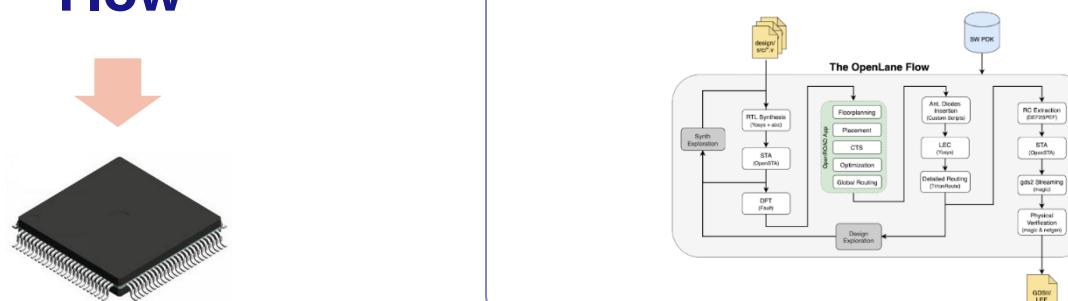
**EDA: Electronic design
automation software (tool)**



**PDK: Process design
kits from foundry**



**Flow: Chip design flow
config and script**



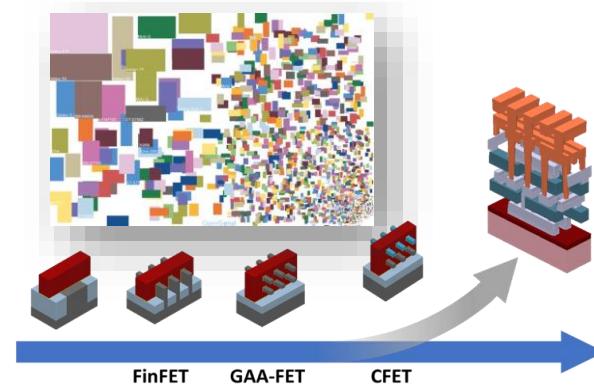
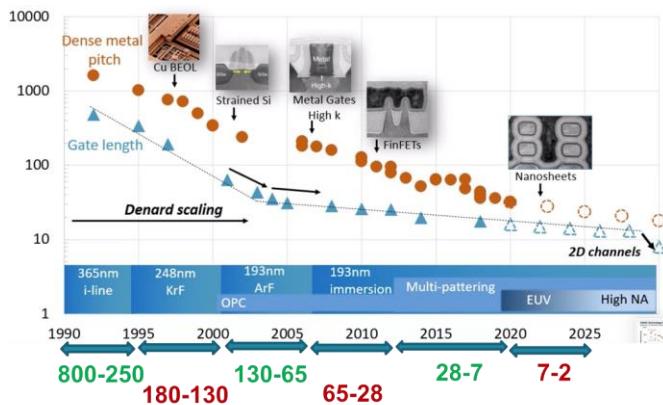
Challenges and Chances

• Challenges

- Moore's Law is almost reaching its limit.
- Due to the "black box" of EDA closedness, the gap between academic and industrial is becoming greater.
- EDA design is tending towards a systematic approach, making innovation more difficult.
- The EDA chain is long and involves multi-disciplines, and design requirements and rules are evolving all the time.

• Chances

- New technologies such as AI and computability bring new opportunities.
- Building open-source, common infrastructure for innovation in EDA is necessary.



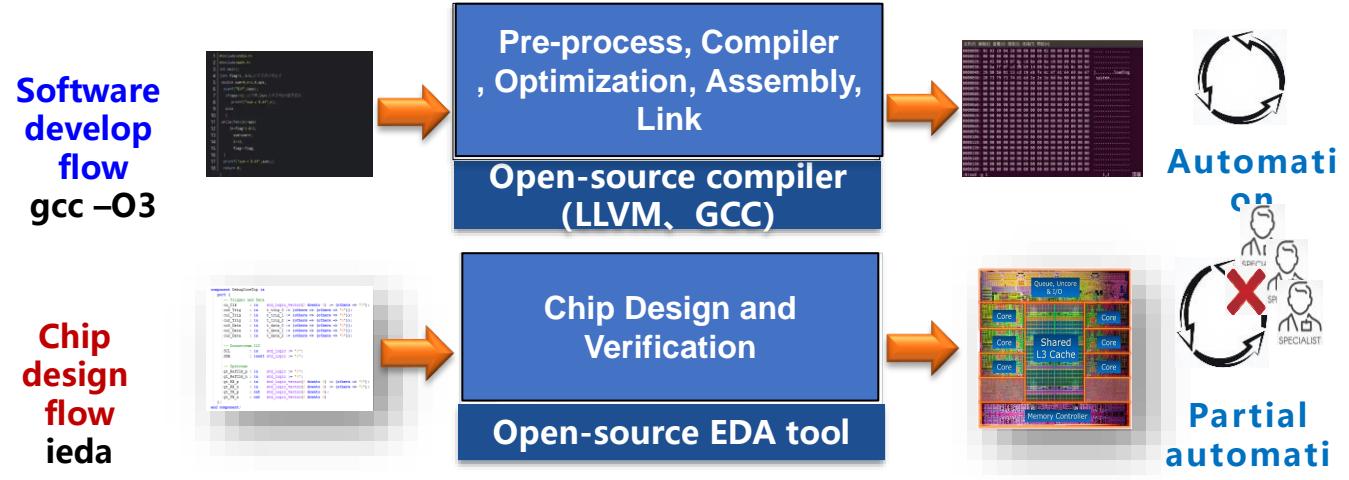
Open-source and Intelligence

● Open-source

- It lowers barriers to entry EDA
- More people in EDA
- Prosperity and Quality

● Intelligence

- Induction and deduction are two way to explore truth for people
- Previous EDA design methodologies mainly are based on **deduction**
- **Induction** and **deduction** should work together, it would be better
 - EDA is an engineering science
 - Some key idea and parameter are **inducted** from rich experience
 - AI is good at engineering **induction**



	Model	Data	Package	Computility
Classical AI	GPT4 Transformer		TensorFlow PyTorch	
AI for EDA	?	?	?	

A Promising Precedent

- **OpenROAD: No Humans, 24 Hours**
- **Efabless-OpenLane: RTL2GDS Digital Flow**

OpenROAD: No Humans, 24 Hours

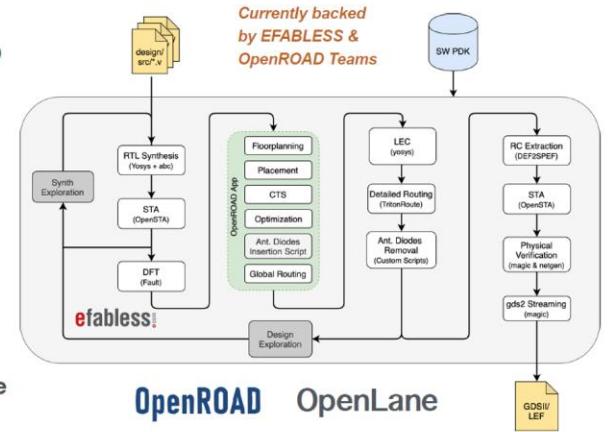
- **FOCUS:** Ease of use and runtime
- **Directly attack the crises of design and innovation**
 - **Schedule barrier:** **RTL-to-GDS** in 24 hours
 - **Expertise barrier:** No-human-in-loop, tapeout GDS
 - **Cost barrier:** Open source (and, runs in 24 hours)
- **Unleash system innovation and design innovation**
- **Enable tool customization to system, application needs**

Efabless: OpenLane

DIGITAL COMPILER-LIKE RTL2GDS

OpenLane is a no-human in the loop RTL to GDS compiler built around OpenROAD that works like a **GNU software compiler with trade-offs in area and performance.**

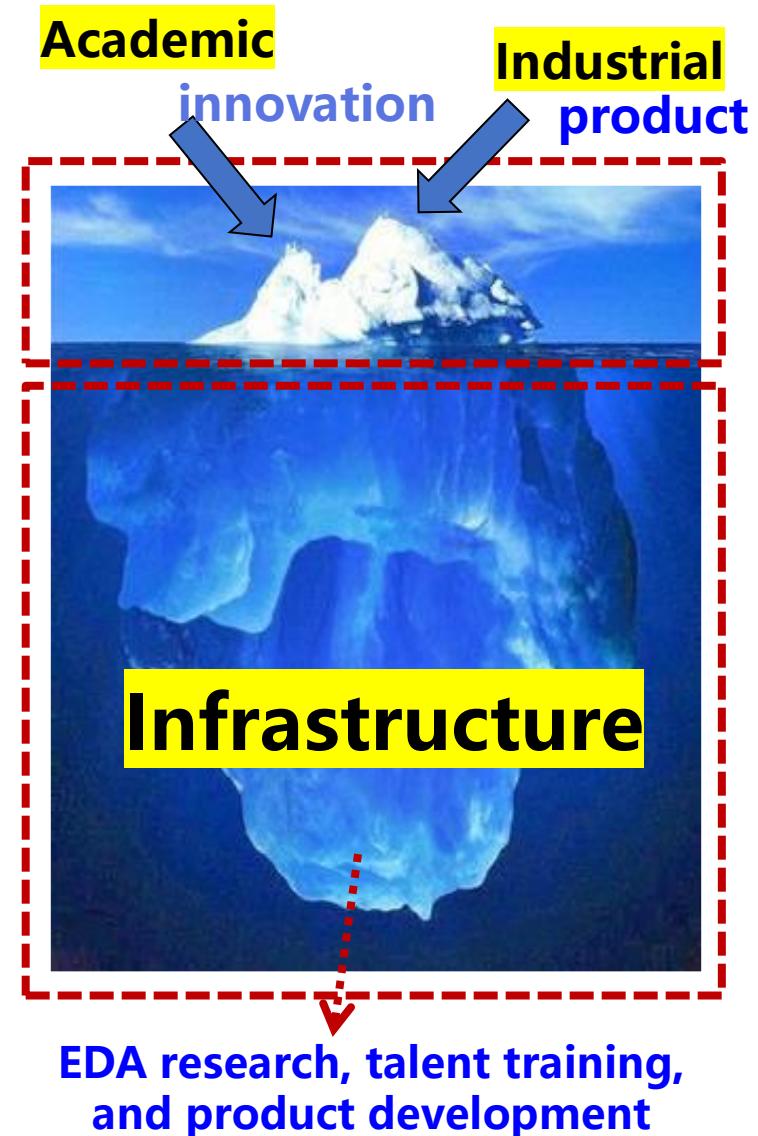
It opens the door for software developers to generate hardware representation without the need for details. That's at least a **1000X** more potential designers!



Supports SKY130, GF130, XFAB180
12nm support is under development by OpenROAD team

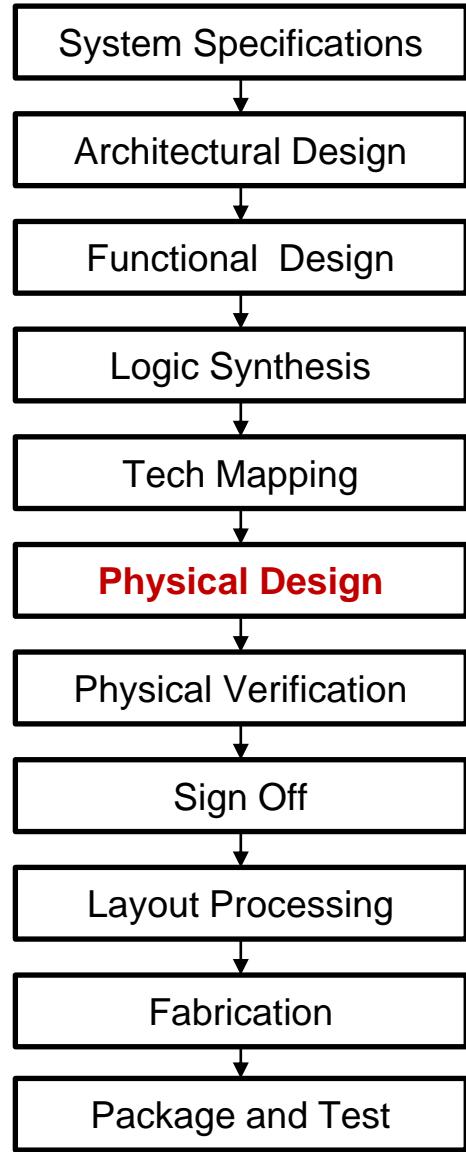
The Goal of iEDA

- **EDA Infrastructure**
 - Supports EDA research, talent training, and product prototype
 - Includes platform software, data, framework, toolkit, model, script.
- **Explore new and efficient EDA R&D methodology**
 - Open-source, Intelligence, Cloud-native, Co-design of chip and EDA
- **Achieve High quality and performance EDA tool**
 - Can be used to design practical chip

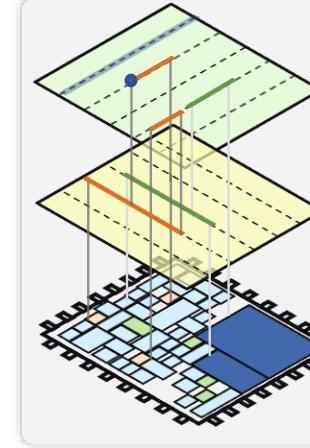
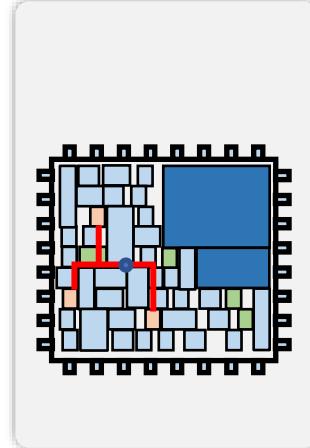
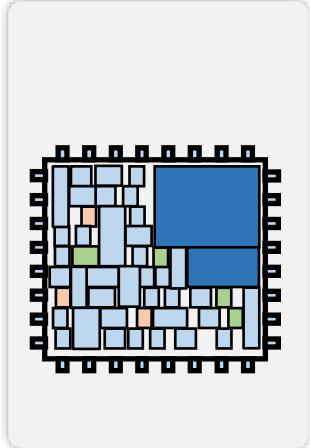
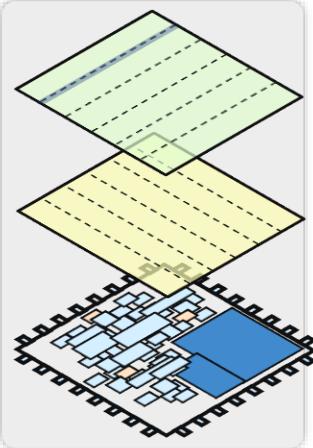


- 01 Introduction
- 02 iEDA Today
- 03 iEDA Future

Physical Design



Evaluation and Analysis (timing, power, congestion, DRC, wirelength)

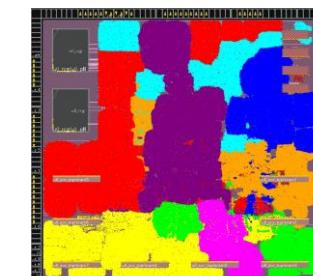
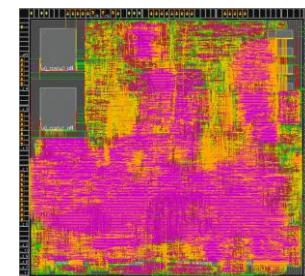
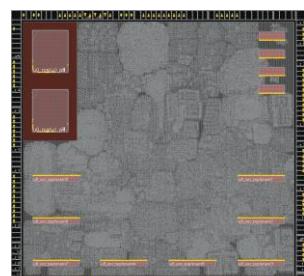
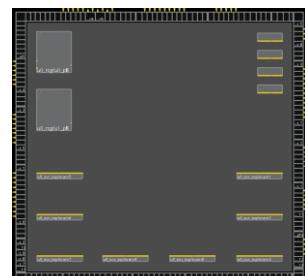


Floorplan: init Die and Core, place IO cell/pad, Macro and physical cell, plan PDN

Placement: place std cell, optimize timing, congestion, wirelength

CTS: design clock network, optimize skew, power, latency, route clock net

Routing: connect signal net, optimize drc, timing, power, reliability manufacturability



Floorplan

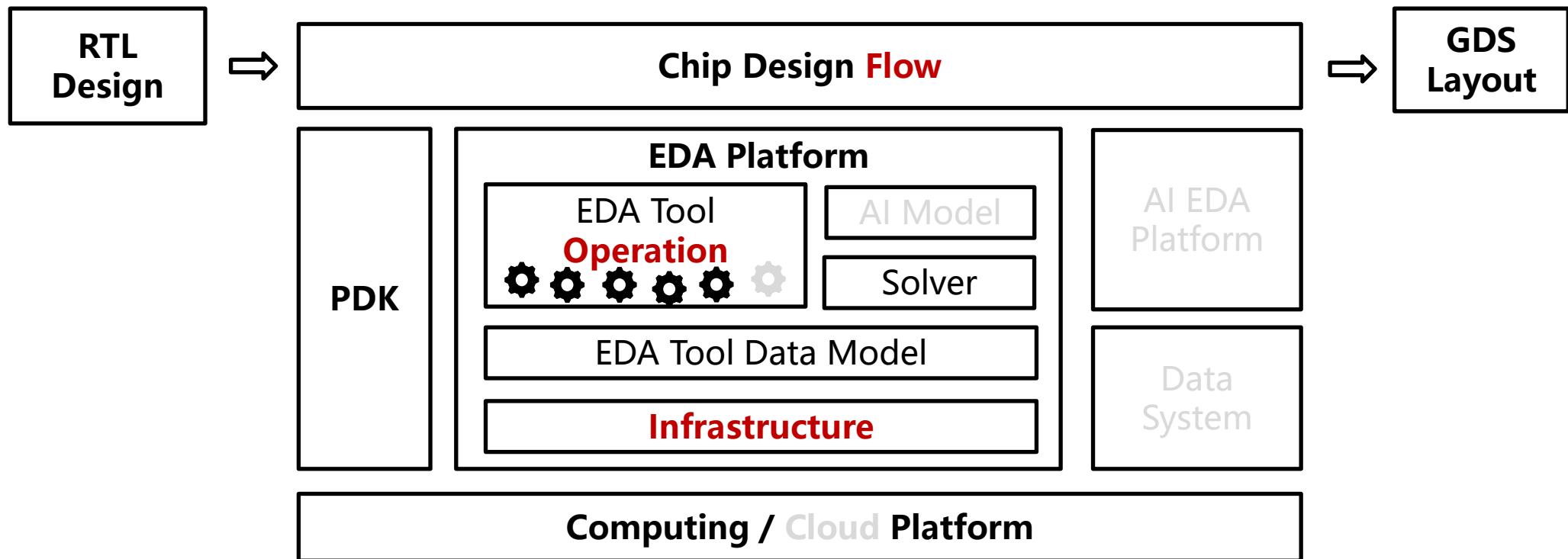
Placement

Routing

Layout

iEDA

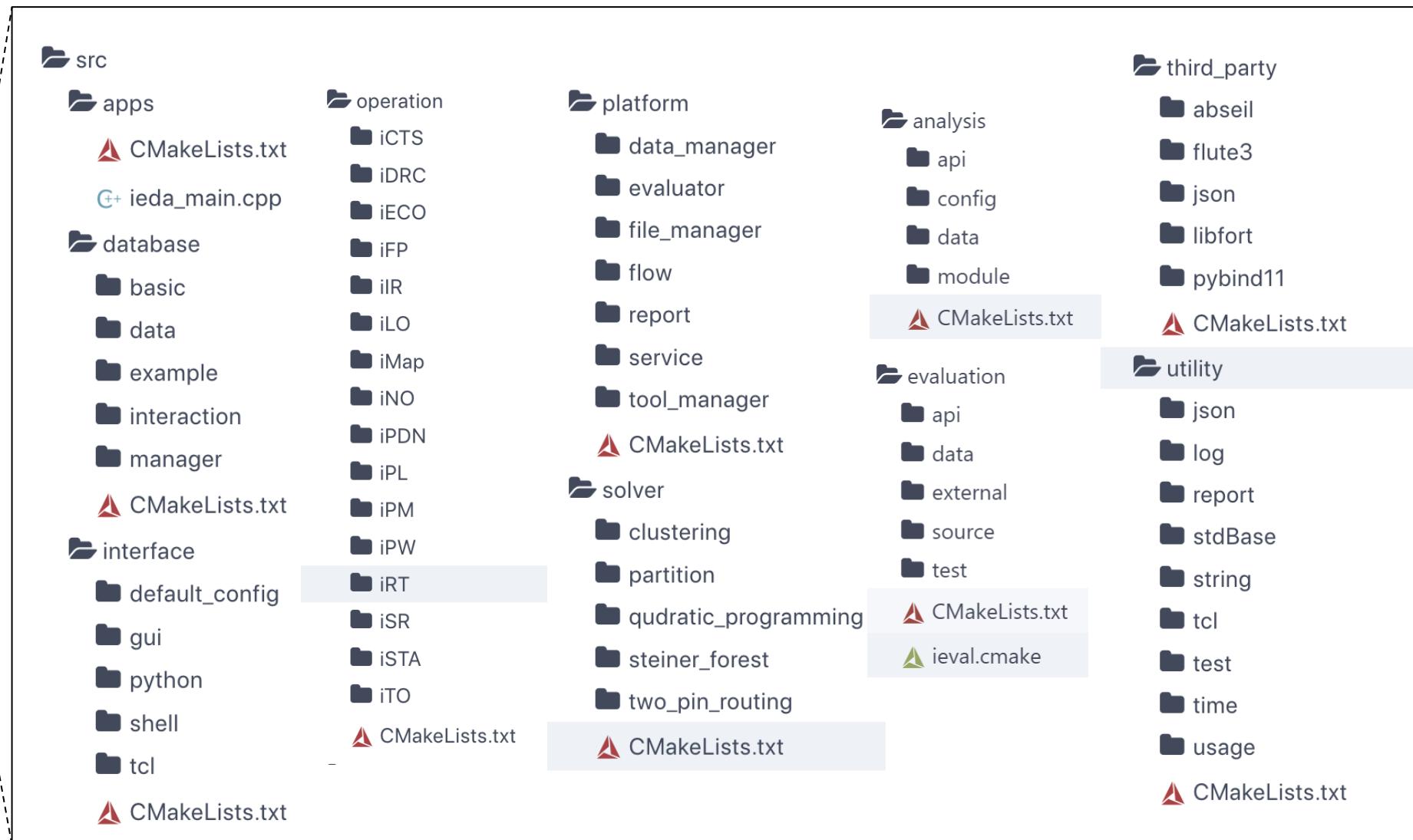
- **System integration:** include the main elements for chip design
- **Loose coupling:** data & operation, tool & tool, tool & solver, EDA&AI, EDA&chip
- **Pluggable and compatibility:** Heterogeneous modules are compatible with each other and homogeneous modules can be replaced with each other



iEDA-Frame: File Structure

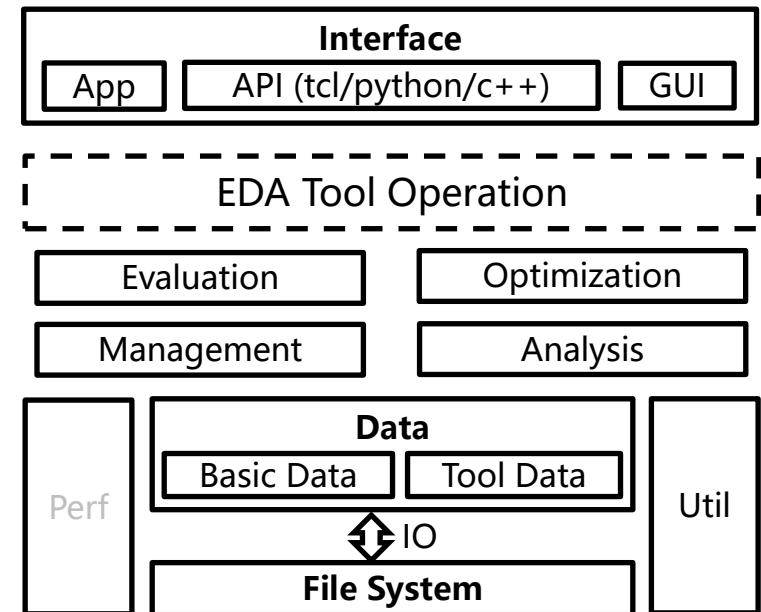
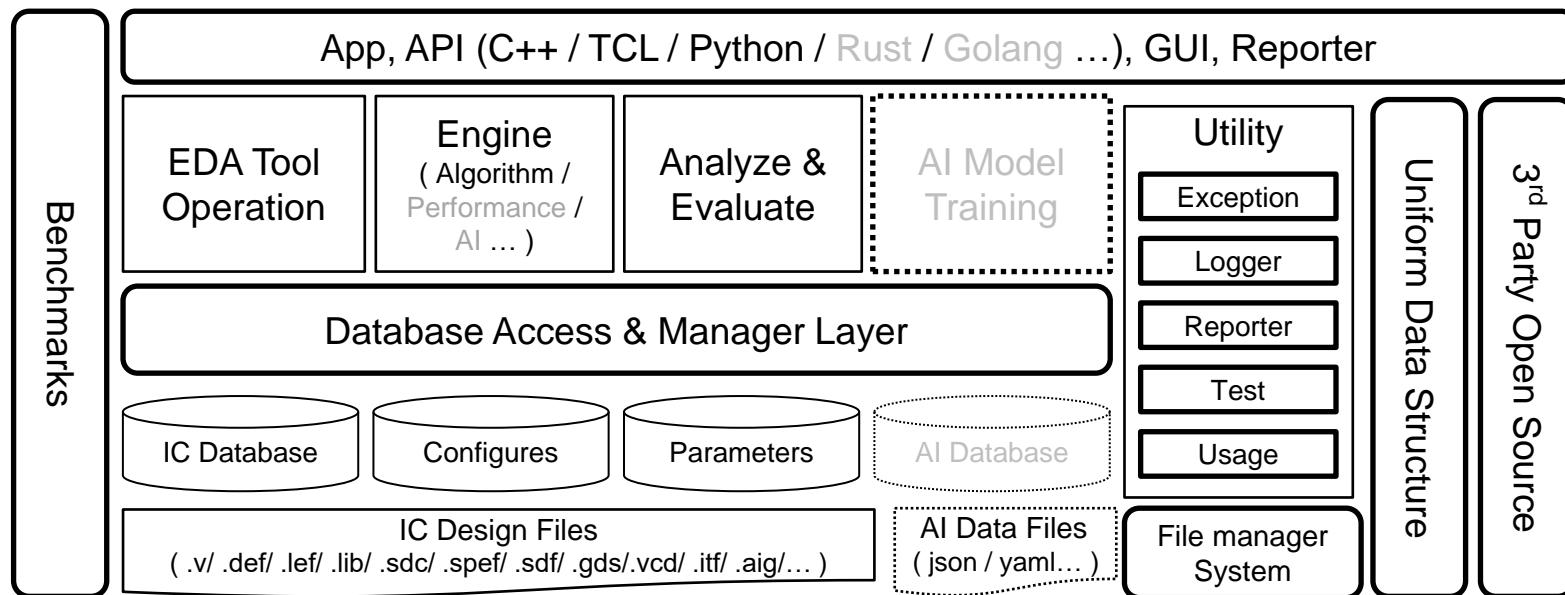
- iEDA structure

```
.gitee  
cmake  
docs  
scripts  
src  
.clang-format  
.clang-tidy  
.gitignore  
CMakeLists.txt  
LICENSE  
README.md  
README.zh-cn.md  
build.sh
```



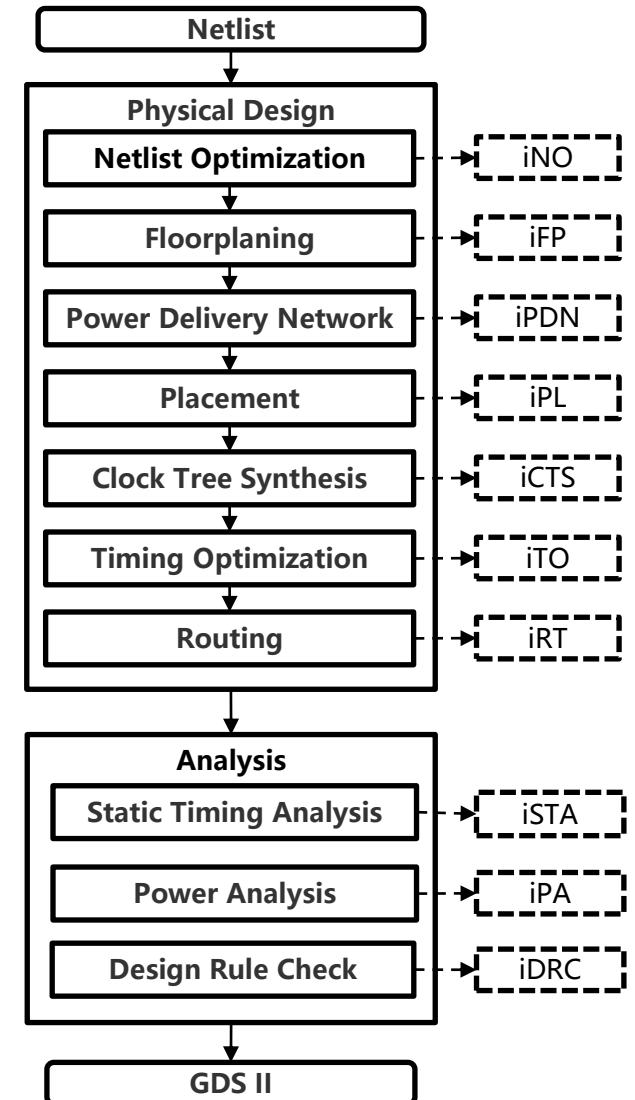
iEDA-Infrastructure

- **File system** (with file parser, manager),
- **Database** (with builder, data structure, basic data, tool data, data service, data api),
- **Platform** (with management, evaluation, analysis, optimization),
- **Interface** (with api (C++, python, tcl), GUI, reporter),
- **Utility and some perf tools**

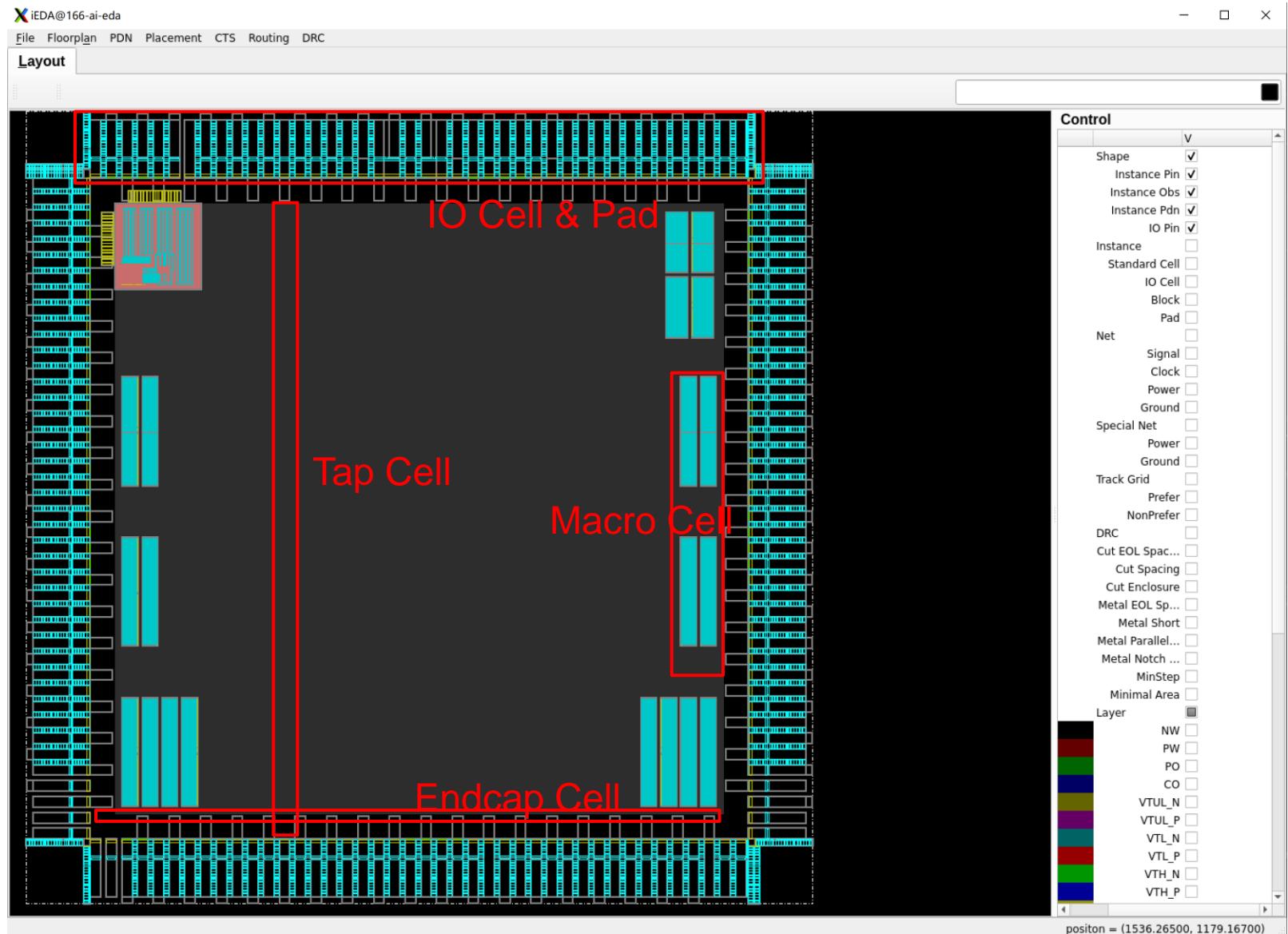
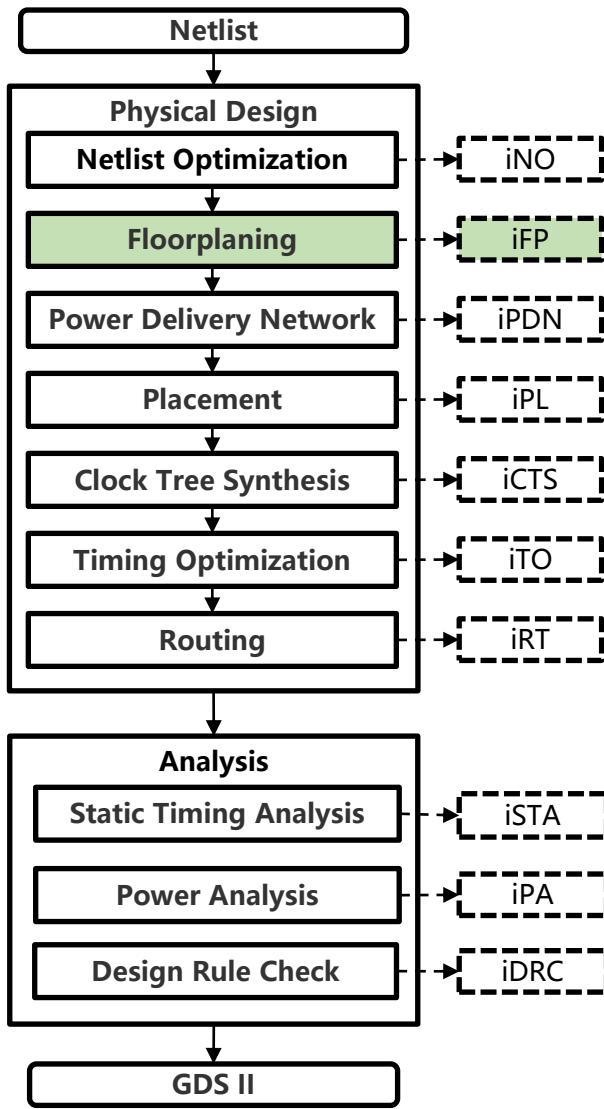


iEDA-Operation (Tool)

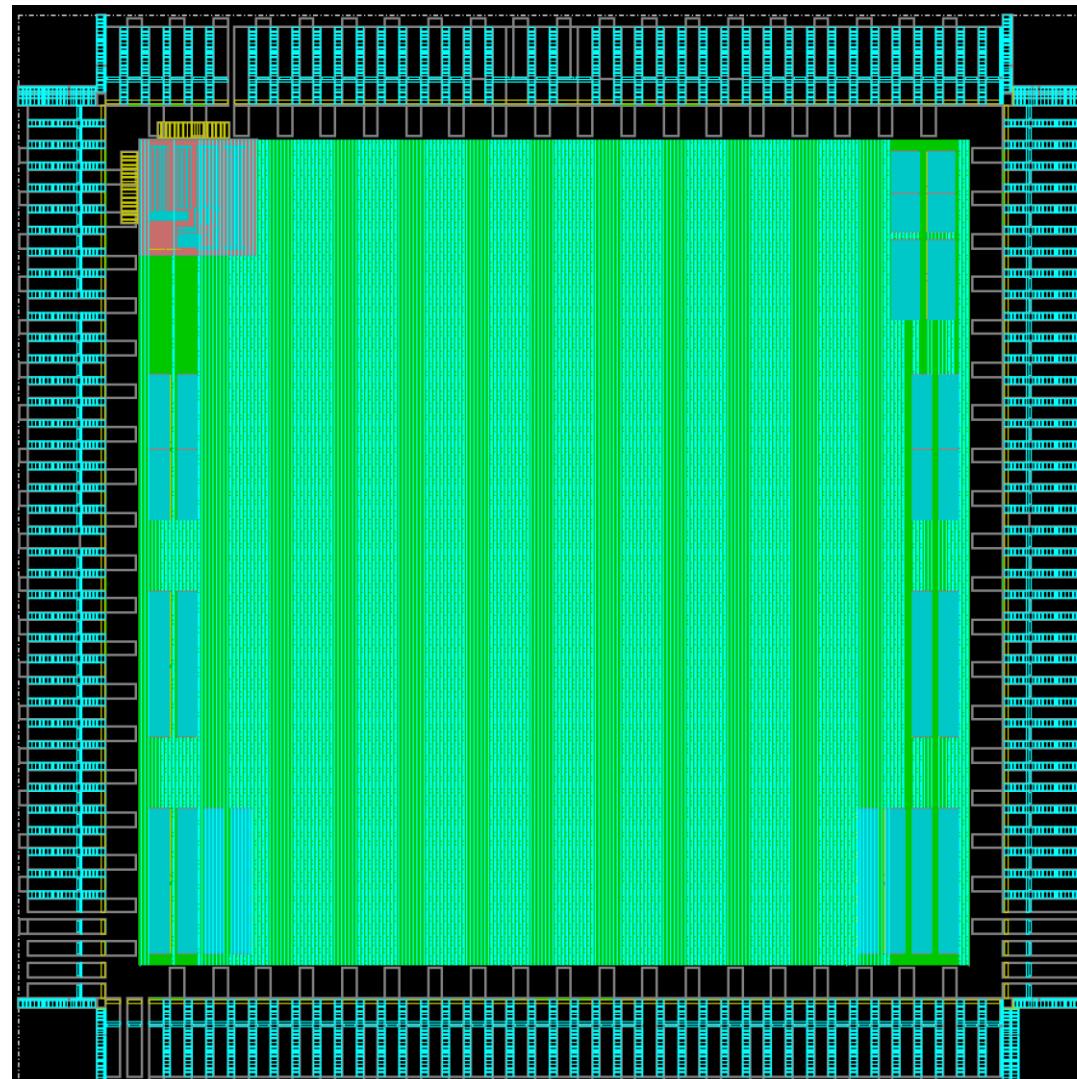
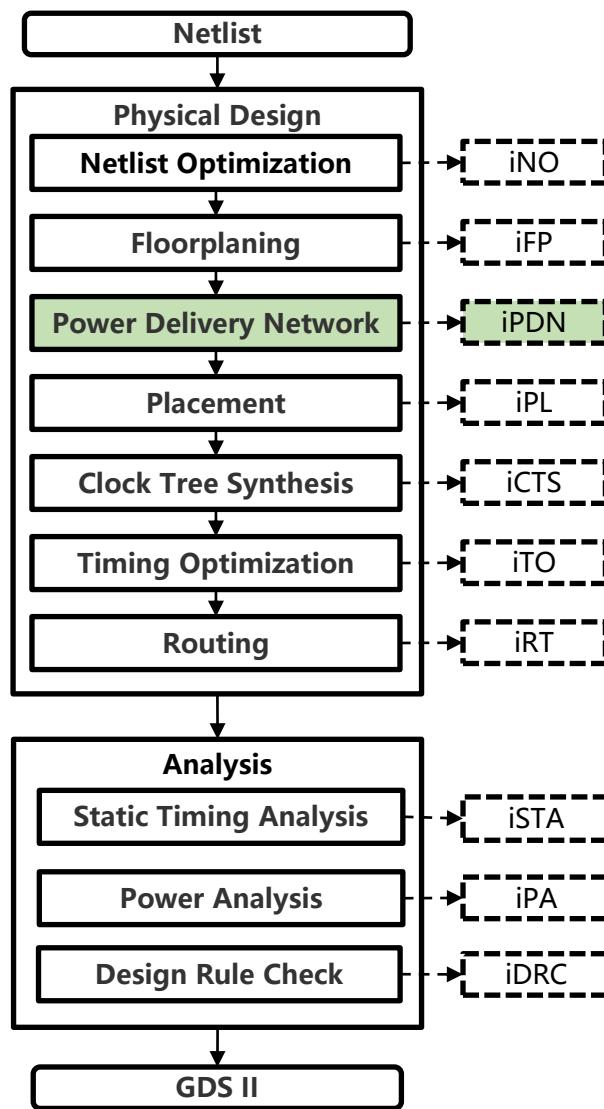
- **Netlist-GDS II**
 - 11 tools, the same structure, separation development
- **Decomposition**
 - Disassemble tool into >100 steps, divide steps into >500 software requirements or algorithm problems
 - Key problem -> abstraction -> description -> problem white book
- **Integration**
 - Requirement/problem -> approach/solution -> summary design and detailed design
 - Architecture design -> functional design -> data design -> software development -> unit test -> integration test -> validation
- **Introduction**
 - >0.3M lines code (exclude 3rd party, exclude history code)



iEDA-Operation: iFP

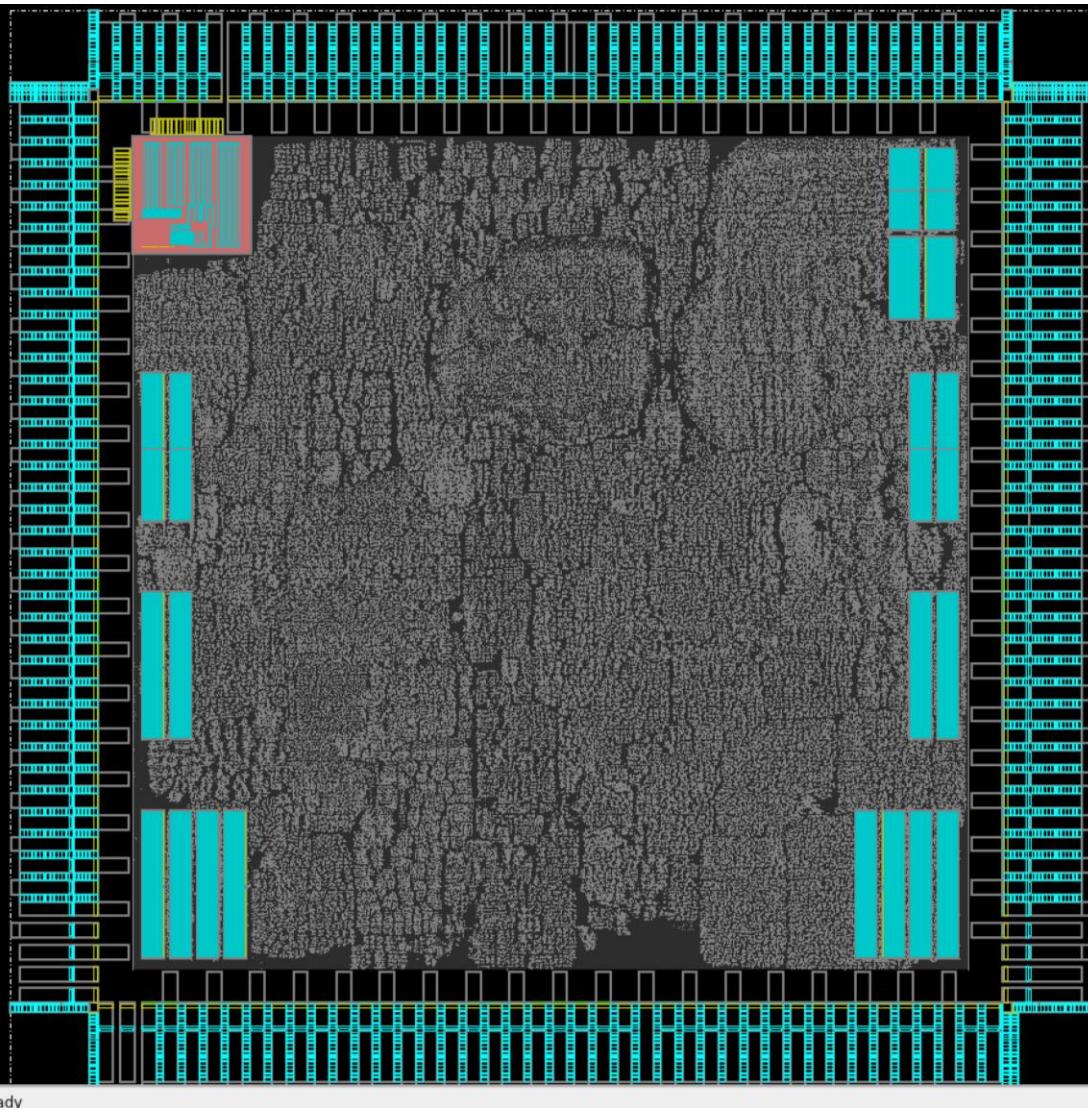
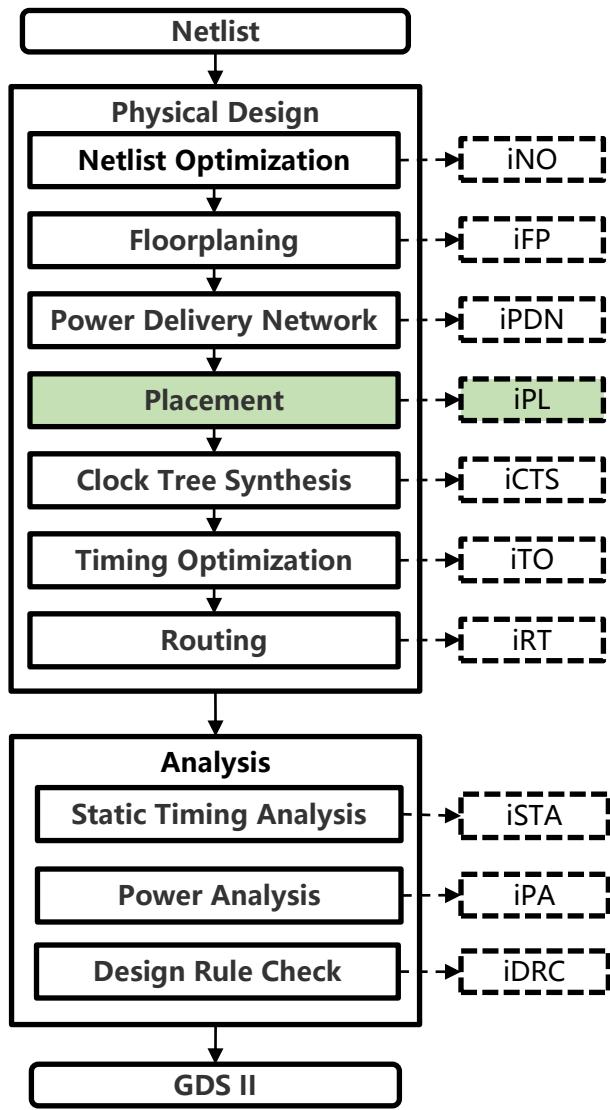


iEDA-Operation: iPDN



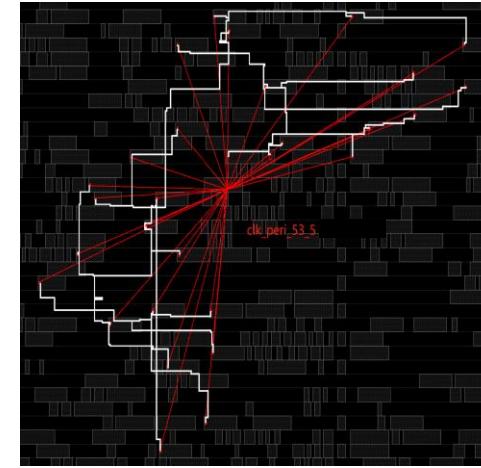
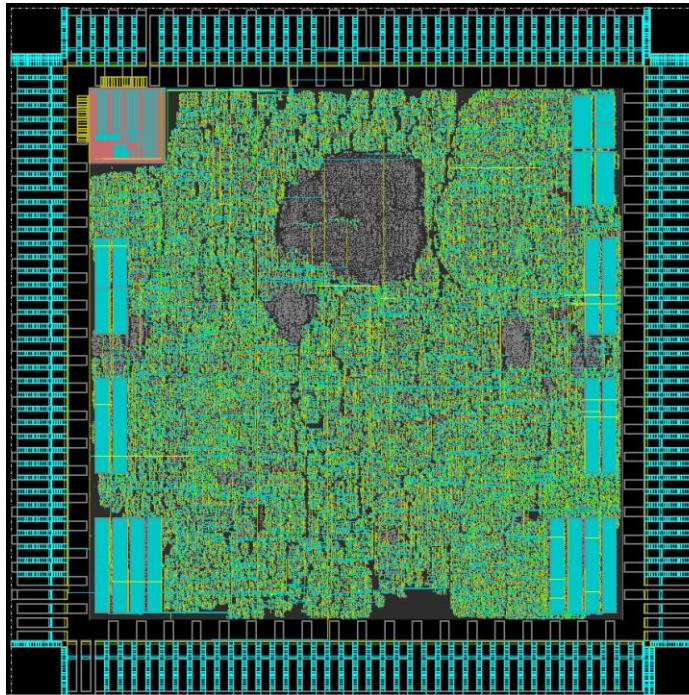
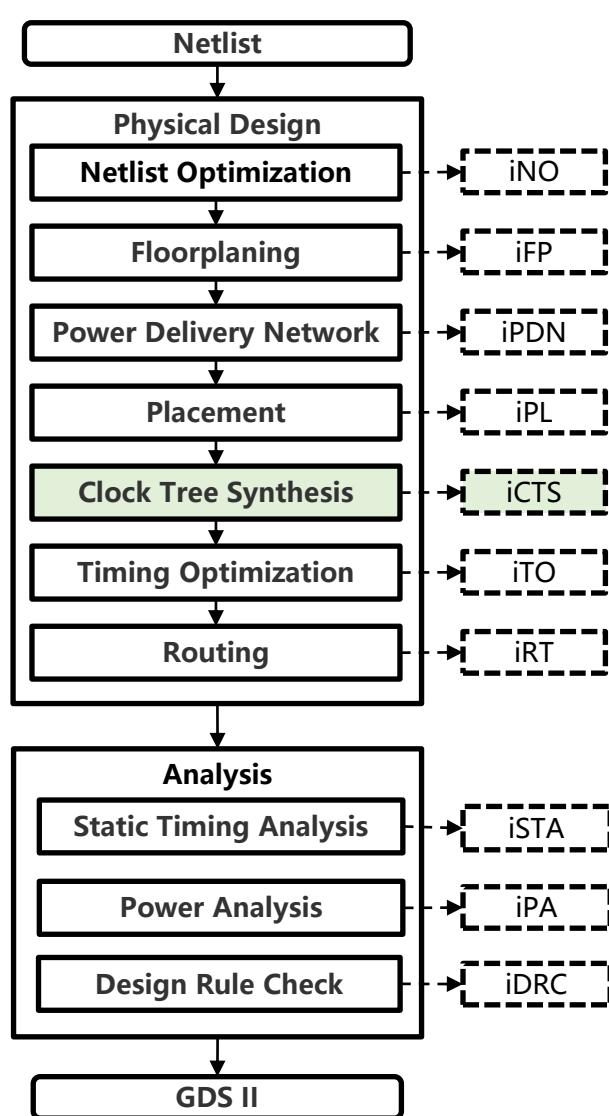
- Evaluate power requirement
- Plan power delivery network
- Connect power stripe and ring by power via

iEDA-Operation: iPL

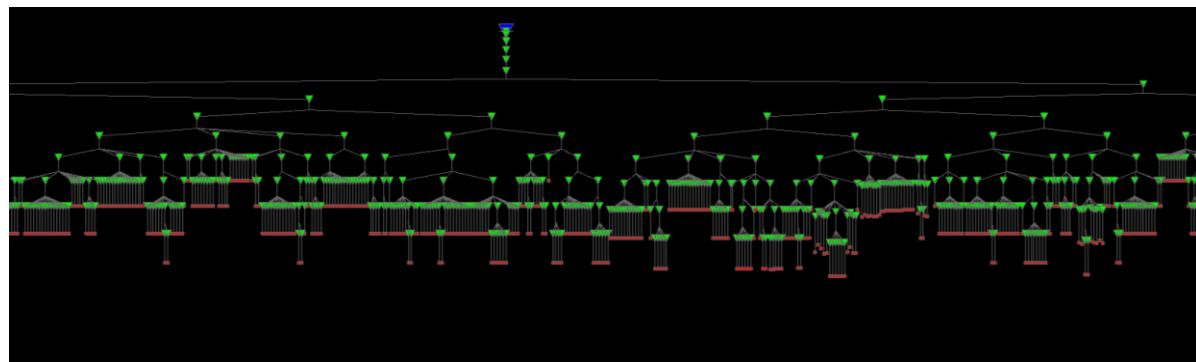


- Place std cell into proper location,
 - satisfy layer poly, well, contact, and metal 1 design rule,
 - optimize wirelength, timing, congestion
- Place macro cell location automatically
- Incremental placement
- Timing-driven placement (coming soon)
- Congestion-driven placement (coming soon)

iEDA-Operation: iCTS

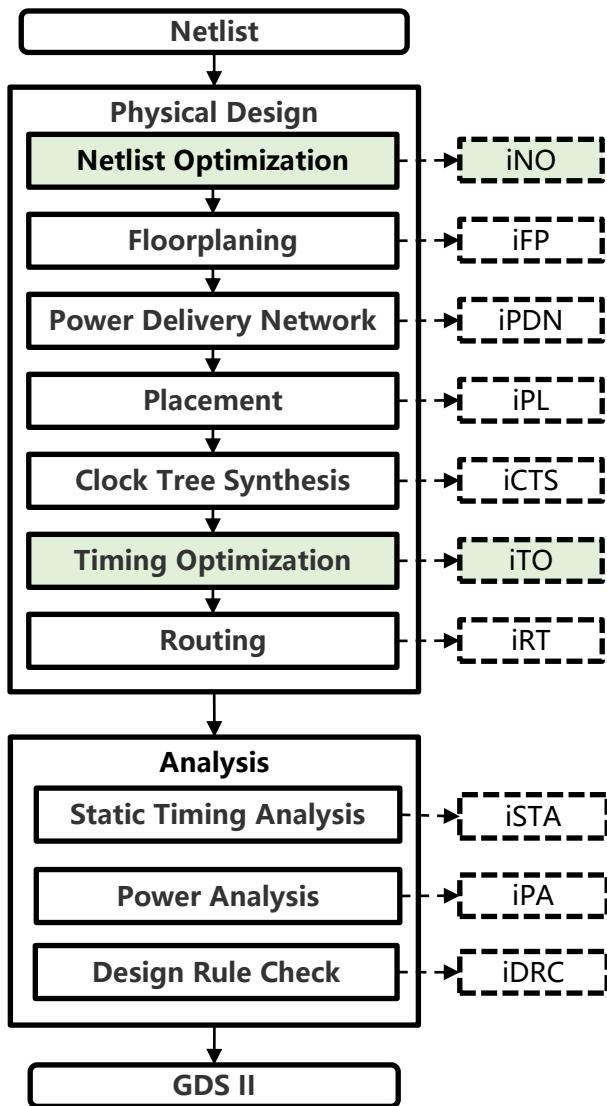


	Latency	Skew	
(DFQD1BWP40P140LVT)	0.444		rp++
	0.625	0.181	rp++
(DFQD1BWP40P140LVT)	0.444		rp++
	0.624	0.180	rp++
(DFQD1BWP40P140LVT)	0.444		rp++
	0.624	0.180	rp++



- Fix clock net fanout
- Elmore net delay evaluation
- Slew and cap learning for clock buffer
- Fix clock net timing design rule violation
- Route clock net by calling iRT tool

iEDA-Operation: iTO

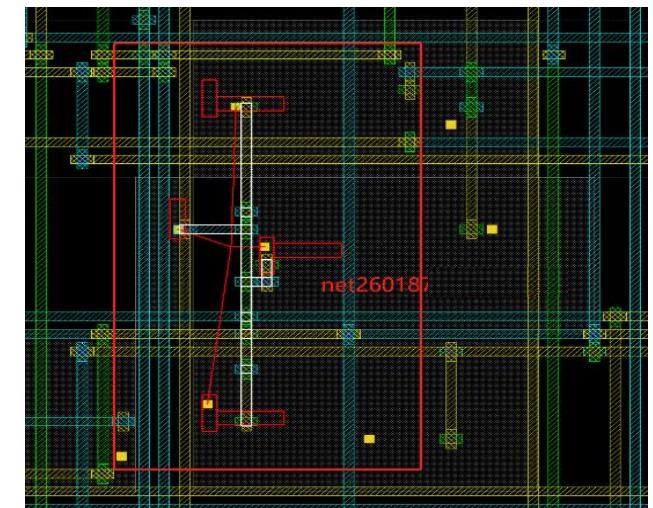
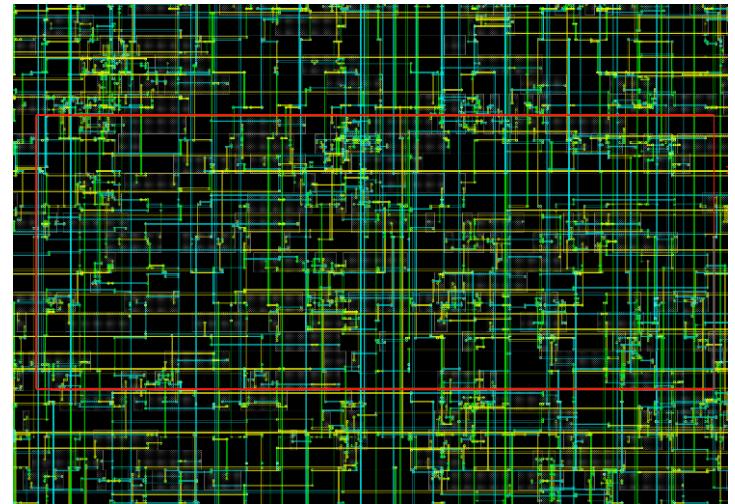
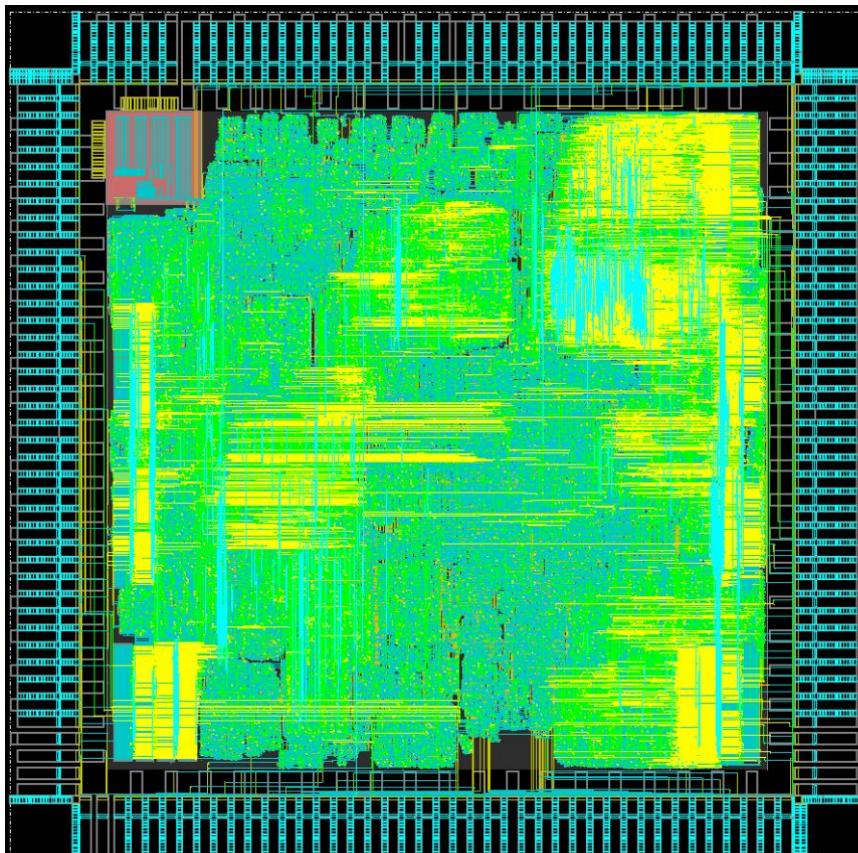
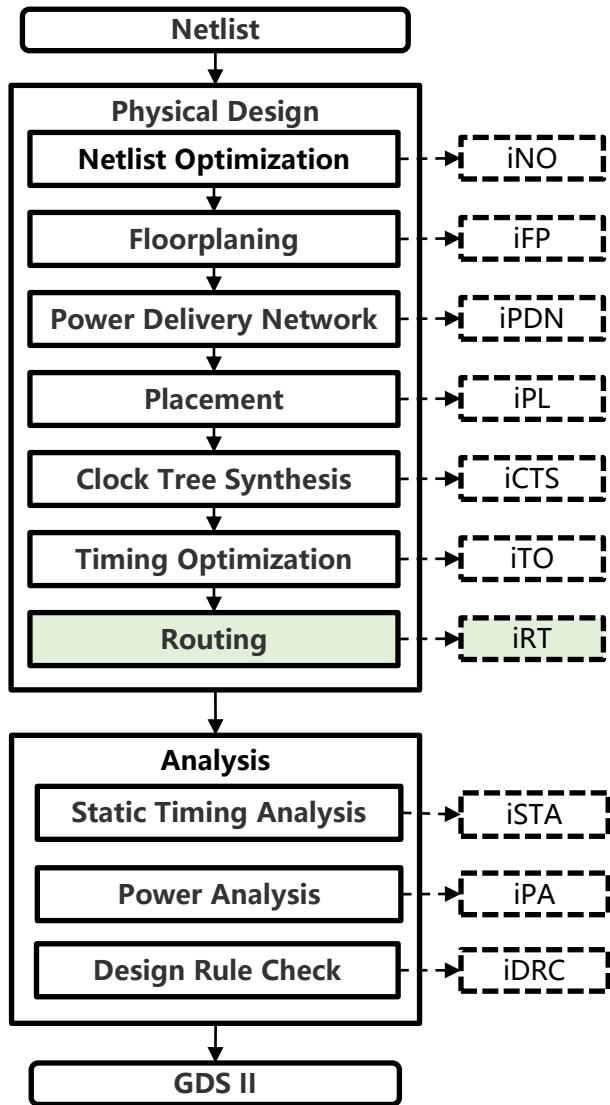


Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Derate	Incr	Path
u1_clk:X_C (PDXOEDG_V_G)	1	0.002	0.000	0.000	0.000	1.000	0.000	0.000r
sys_clk_100m (clock net)						1.000	0.000	0.000r
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		0.885	0.012	0.012r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.005	0.000	0.007				
sys_clk_100m_buf (clock net)	2	0.001	0.000	0.007	0.000	1.000	0.000	0.012r
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.008	0.000	0.021		0.885	0.034	0.046r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.004	0.000	0.021	0.000	1.000	0.000	0.046r
u0_rcg/mux_core_clk (clock net)	5	0.004	0.000	0.008		0.885	0.019	0.066r
u0_rcg/u1_lvt_ckmux2hdv4_balance_0_buf:I (CKBD24BWP35P140)		0.008	0.000	0.015		1.039	0.021	0.486r
u0_rcg/u1_lvt_ckmux2hdv4_balance_0_buf:Z (CKBD24BWP35P140)		0.001	0.000	0.000	NA	1.000	0.000	0.486r
u0_rcg/mux_core_clk_0 (clock net)	17	0.008	0.000	0.015		0	0	
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.001	0.000	0.000		0.486	0.486	
clock CLK_U1_clk_XC (rise edge)						0.486	0.486	
clock network delay (propagated)						0.486	0.486	
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)						0.000	0.486	
library hold time						-0.073	0.413	
clock reconvergence pessimism								
data require time							0.413	
data arrival time							0.458	
slack (MET)							0.045	

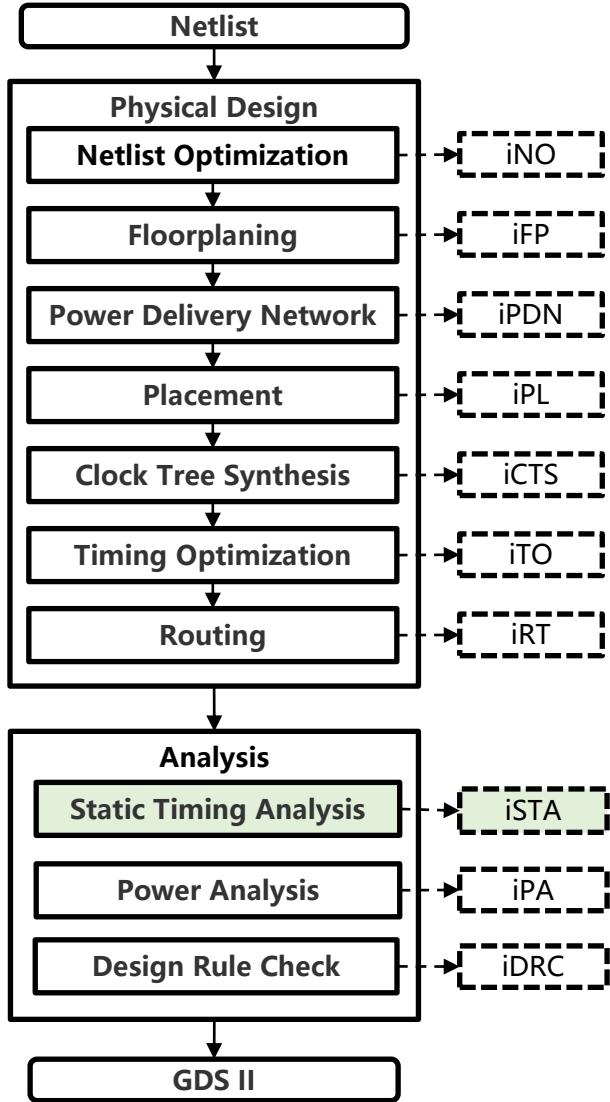


- Fix timing design rule violation
 - Max cap
 - Max slew
 - Max wirelength
 - Max fanout
- Fix hold time
- Fix setup time
- Cell sizing
- Buffer Insertion
- Load Insertion
- Buffer/load location

iEDA-Operation: iRT



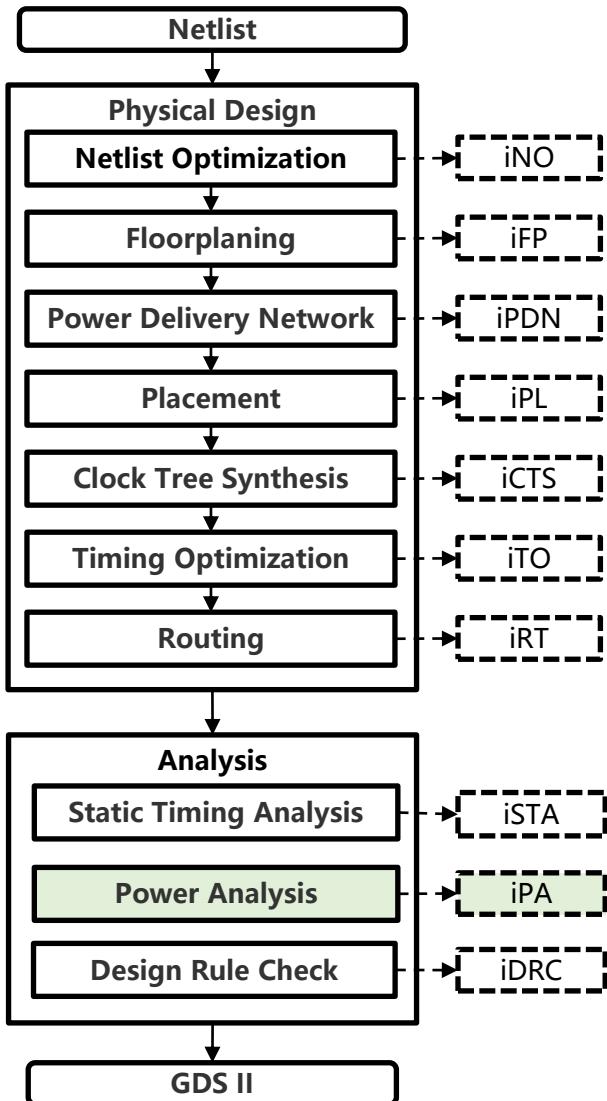
iEDA-Operation: iSTA



Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Derate	Incr	Path
u1_clk_XC (PDXOEDG V_G)	1	0.002	0.000	0.000	1.000	0.000	0.000r	
u1_clk_10nm_buf (clock net)	1	0.002	0.000	0.006	0.000	1.000	0.000	0.000r
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)	1	0.002	0.000	0.006	0.000	0.885	0.011	0.011r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)	1	0.002	0.000	0.006	0.000	0.000	0.000	0.000r
sys_clk_10nm_buf (clock net)	2	0.001	0.000	0.006	0.000	1.000	0.000	0.011r
u0_rcp/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)	1	0.002	0.000	0.018	0.000	0.885	0.032	0.043r
u0_rcp/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)	1	0.002	0.000	0.018	0.000	0.000	0.000	0.000r
u0_rcp/mux_core_clk (clock net)	5	0.001	0.000	0.018	0.000	1.000	0.000	0.043r
u0_rcp/mux_core_clk_0_buf:I (CKBD4BWP35P140)	1	0.001	0.000	0.018	0.000	0.885	0.021	0.064r
u0_rcp/mux_core_clk_0_buf:Z (CKBD4BWP35P140)	1	0.008	0.000	0.015	0.000	0.000	0.000	0.000r
u0_rcp/mux_core_clk_0 (clock net)	17	0.000	0.000	0.015	0.000	1.000	0.000	0.064r
u0_rcp/mux_core_clk/div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)	1	0.001	0.000	0.015	0.000	1.000	0.000	0.064r
clock CLK_u1_clk_XC (rise edge)	1	0.001	0.000	0.009	0.000	0.820	0.045	0.169r
clock network delay (propagated)	1	0.001	0.000	0.009	0.000	0.000	0.000	0.000r
u0_rcp/mux_core_clk/div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)	1	0.001	0.000	0.009	0.000	1.000	0.000	0.109r
u0_rcp/mux_core_clk/div3/gt_en1_reg:Q (DFSNQD1BWP40P140LVT)	1	0.001	0.000	0.009	0.000	1.000	0.000	0.000r
u0_rcp/mux_core_clk/div3/gt_en1_reg:U_G1:E (CKLNQD4BWP40P140LVT)	1	0.001	0.000	0.009	0.000	1.000	0.000	0.000r
u1_clk_XC (PDXOEDG V_G)	1	0.002	0.000	0.000	0.000	1.000	0.000	0.000r
sys_clk_10nm_buf (clock net)	1	0.002	0.000	0.000	0.000	1.000	0.000	0.000r
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)	1	0.002	0.000	0.006	0.000	1.000	0.000	0.013r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)	1	0.002	0.000	0.006	0.000	1.039	0.013	0.013r
sys_clk_10nm_buf (clock net)	2	0.001	0.000	0.006	0.000	1.000	0.000	0.013r
u0_rcp/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)	1	0.001	0.000	0.006	0.000	1.039	0.038	0.051r
u0_rcp/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)	1	0.006	0.000	0.018	0.000	1.000	0.000	0.051r
u0_rcp/mux_core_clk (clock net)	5	0.001	0.000	0.018	0.000	1.000	0.000	0.051r
u0_rcp/mux_core_clk_0_buf:I (CKBD4BWP35P140)	1	0.008	0.000	0.015	0.000	1.039	0.025	0.076r
u0_rcp/mux_core_clk_0_buf:Z (CKBD4BWP35P140)	1	0.008	0.000	0.015	0.000	NA	0.000	0.076r
u0_rcp/mux_core_clk_0 (clock net)	17	0.001	0.000	0.000	0.000	1.000	0.000	0.076r
u0_rcp/mux_core_clk/div3/U_G1:CP (CKLNQD4BWP40P140LVT)	1	0.001	0.000	0.000	0.000	0.000	0.000	0.076r
clock CLK_u1_clk_XC (rise edge)	1	0.001	0.000	0.000	0.000	0.076	0.076	0.076r
clock network delay (propagated)	1	0.001	0.000	0.000	0.000	0.000	0.000	0.076r
u0_rcp/mux_core_clk/div3/U_G1:CP (CKLNQD4BWP40P140LVT)	1	0.001	0.000	0.000	0.000	-0.011	0.064	0.045r
library hold time								
clock reconvergence pessimism								
data require time								
data arrival time								
slack (MET)								

- Evaluate timing before / during / after the physical design process
- Cell delay
 - NLDM model
 - CCS model
 - ML interpolation
- Net delay
 - Elmore / ECM / D2M / DCM
 - High-order model (arnoldi)
 - AI
- CPPR/Noise/AOCV
- Report/API
- ...

iEDA-Operation: iPW



```

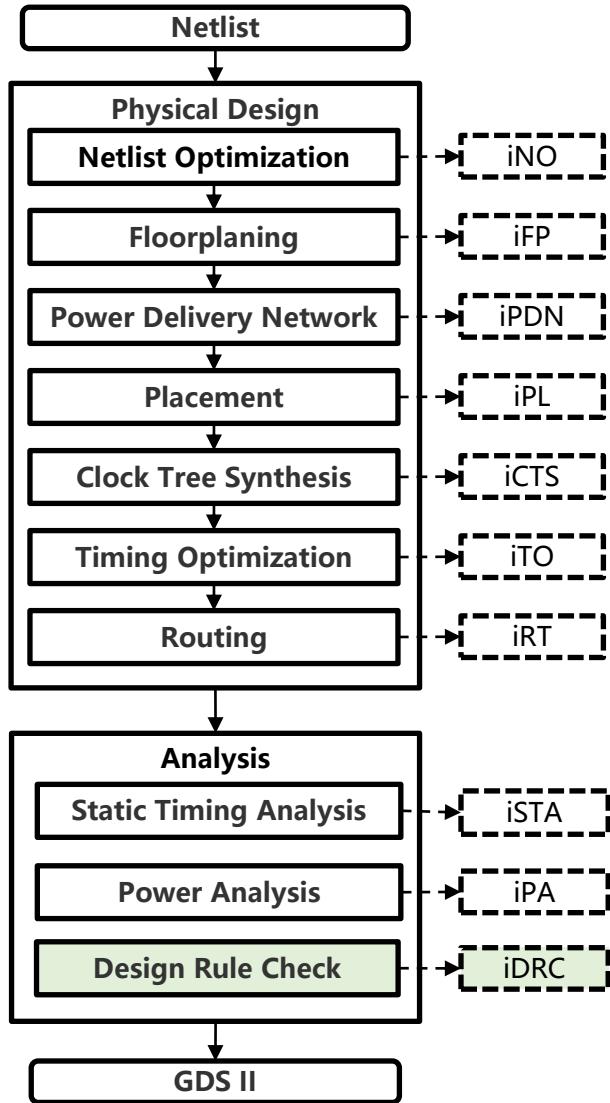
Generate the report at 2023-05-06T09:54:06
Report : Averaged Power
+-----+-----+-----+-----+-----+
| Power Group | Internal Power | Switch Power | Leakage Power | Total Power | (%) |
+-----+-----+-----+-----+-----+
| combinational | 1.064e-07 | 5.063e-09 | 3.079e-08 | 1.422e-07 | (27.595%) |
| sequential | 2.862e-07 | 7.337e-09 | 7.963e-08 | 3.732e-07 | (72.405%) |
+-----+-----+-----+-----+-----+
Net Switch Power == 1.240e-08 (2.406%)
Cell Internal Power == 3.926e-07 (76.173%)
Cell Leakage Power == 1.104e-07 (21.422%)
Total Power == 5.154e-07

I0506 09:50:50.732399 3182449 PwrPropagateConst.cc:166] propagate const start
I0506 09:50:50.732499 3182449 PwrPropagateConst.cc:270] propagate const end
I0506 09:50:50.732555 3182449 PwrPropagateConst.cc:272] propagate const memory usage 0MB
I0506 09:50:50.732573 3182449 PwrPropagateConst.cc:274] propagate const time elapsed 0.000176s
I0506 09:50:50.732645 3182449 PwrPropagateToggleSP.cc:186] propagate toggle sp start
I0506 09:50:50.736701 3182449 PwrPropagateToggleSP.cc:288] propagate toggle sp end
I0506 09:50:50.737669 3182449 PwrPropagateToggleSP.cc:291] propagate toggle sp memory usage 0MB
I0506 09:50:50.737720 3182449 PwrPropagateToggleSP.cc:293] propagate toggle sp time elapsed 0.005075s
I0506 09:50:50.737866 3182449 PwrPropagateClock.cc:53] propagate clock start
I0506 09:50:50.737897 3182449 PwrPropagateClock.cc:64] propagate clock end
I0506 09:50:50.737979 3182449 PwrPropagateClock.cc:66] propagate clock memory usage 0MB
I0506 09:50:50.738003 3182449 PwrPropagateClock.cc:68] propagate clock time elapsed 0.000138s
I0506 09:50:50.738090 3182449 PwrCalcLeakagePower.cc:54] calc leakage power start
I0506 09:50:50.739434 3182449 PwrCalcLeakagePower.cc:78] calc leakage power result 0.000110417mw
I0506 09:50:50.739460 3182449 PwrCalcLeakagePower.cc:81] calc leakage power end
I0506 09:50:50.739544 3182449 PwrCalcLeakagePower.cc:83] calc leakage power memory usage 0MB
I0506 09:50:50.739562 3182449 PwrCalcLeakagePower.cc:85] calc leakage power time elapsed 0.001471s
I0506 09:50:50.739634 3182449 PwrCalcInternalPower.cc:468] calc internal power start
I0506 09:50:50.740906 3182449 PwrCalcInternalPower.cc:500] calc internal power result 0.000392628mW
I0506 09:50:50.740923 3182449 PwrCalcInternalPower.cc:502] calc internal power end
I0506 09:50:50.740972 3182449 PwrCalcInternalPower.cc:504] calc internal power memory usage 0MB
I0506 09:50:50.740983 3182449 PwrCalcInternalPower.cc:506] calc internal power time elapsed 0.001351s
I0506 09:50:50.741034 3182449 PwrCalcSwitchPower.cc:25] calc switch power start
I0506 09:50:50.741125 3182449 PwrCalcSwitchPower.cc:77] calc switch power result 1.24003e-05mw
I0506 09:50:50.741138 3182449 PwrCalcSwitchPower.cc:79] calc switch power end
I0506 09:50:50.741183 3182449 PwrCalcSwitchPower.cc:81] calc switch power memory usage 0MB
I0506 09:50:50.741194 3182449 PwrCalcSwitchPower.cc:83] calc switch power time elapsed 0.00016s
I0506 09:50:50.741662 3182449 Power.cc:406]

+-----+-----+-----+-----+-----+
| Power Group | Internal Power | Switch Power | Leakage Power | Total Power | (%) |
+-----+-----+-----+-----+-----+
| combinational | 1.064e-07 | 5.063e-09 | 3.079e-08 | 1.422e-07 | (27.595%) |
| sequential | 2.862e-07 | 7.337e-09 | 7.963e-08 | 3.732e-07 | (72.405%) |
+-----+-----+-----+-----+-----+
  
```

- Evaluate power before / during / after the physical design process
- Average model
- Timing window (coming soon)
- VCD parser
- Report/API
- ...

iEDA-Operation: iDRC

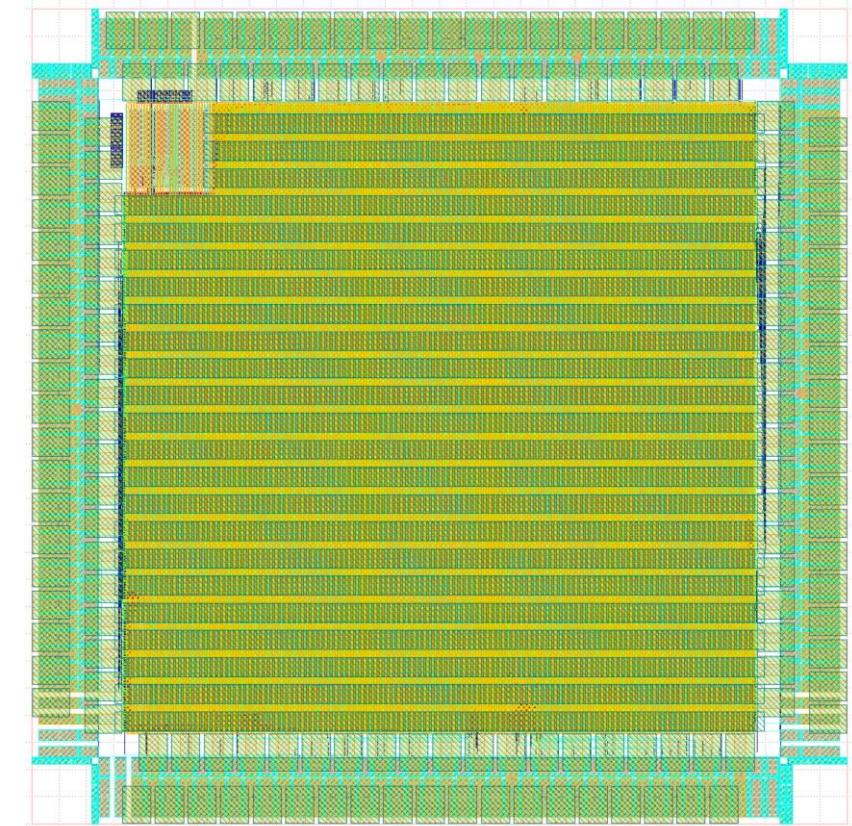
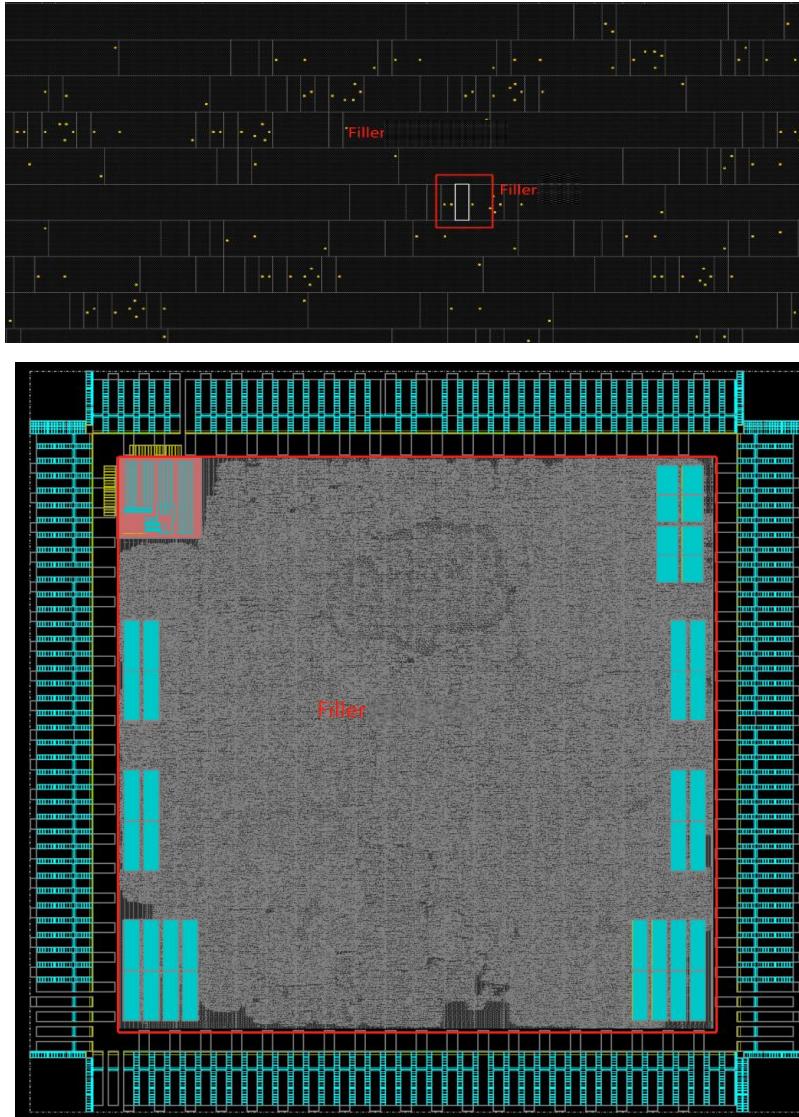
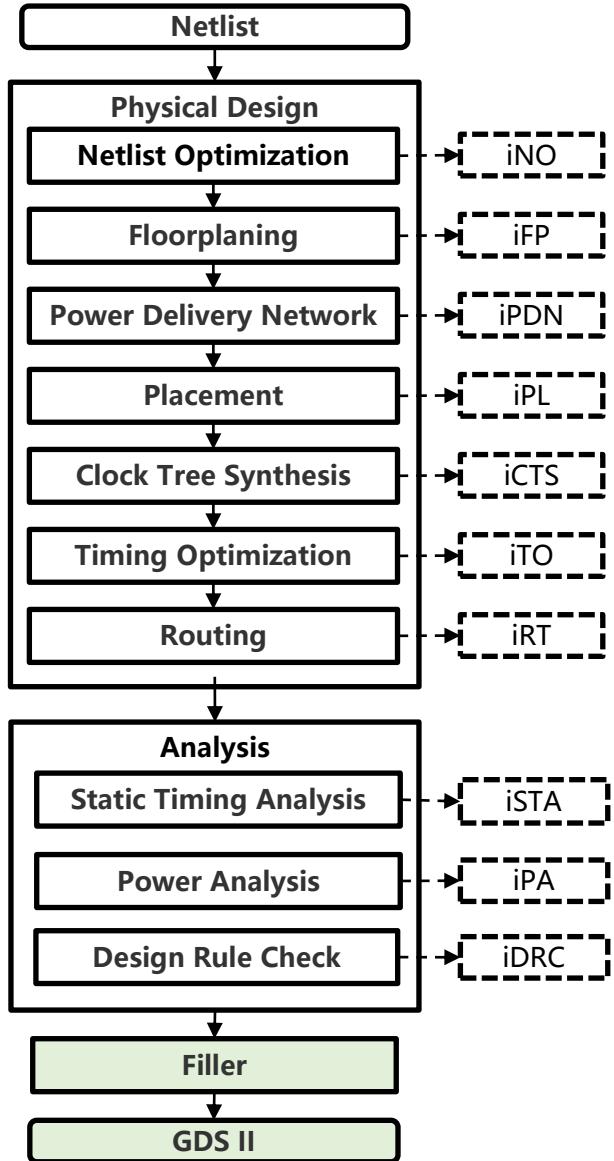


Drc Summary	
DRC Type	Number
Cut Different Layer Spacing	2228892
Cut EOL Spacing	3719612
Cut Enclosure	184490
Cut EnclosureEdge	0
Cut Spacing	3120490
Metal Corner Filling Spacing	0
Metal EOL Spacing	3912985
Metal JogToJog Spacing	0
Metal Notch Spacing	31464
Metal Parallel Run Length Spacing	2144327
Metal Short	5685276
MinHole	0
MinStep	1225544
Minimal Area	6782308

Connectivity Summary	
Connectivity Check	Number
Disconnected nets [pin number >= 2]	105 / 377248
Disconnected nets [pin number < 2]	23607 / 377248

- Check design rule during routing and after routing
- Support $\geq 28\text{nm}$ process node geometric rule checking of mainstream foundry
- ...

iEDA-Operation: Filler and GDS



iEDA-Evaluation

- **Evaluating metrics by some different calculation methods**
 - Timing, power, area, wirelength, congestion, skew, res, cap, slew, fanout, utilization, density, cells, nets, drc (metal, cut, connection), ...

Summary

Module	Value				
DIE Area (um^2)	28628.640000 = 169.200000 * 161.200000				
DIE Usage	0.93%				
CORE Area (um^2)	11872.505600 = 149.280000 * 144.000000				
CORE Usage	0.308462				
Number - Site	2				
Number - Layer	14				
Number - Track	12				
Number - Layer	13				
Number - Routing Layer	6				
Number - Cut Layer	5				
Number - Cell Master	41				
Number - Via Rule	54				
Number - IO Pin	58				
Number - Instances	97				
Number - Blockage	0				
Number - Filler	0				
Number - Net	69				
Number - Special Net	2				
Summary - Instance					
+ Type	Number Num				
All Instances	974	1			
Netlist	656	0			
Physical	318	0			
Timing	6	0			
Core	974	1			
Core - logic	656	0			
Pad	0	0			
Block	0	0			
Endcap	0	0			
Cover	0	0			
Ring	0	0			
Summary - Net					
+ Net Type	Number Num				
All Nets	692	1			
Signal	674	0			
Clock	18	0			
Power & Ground	0	0			
Summary - Layer					
+ Layer	Net - Wire Length				
pwell	0				
pwell	0				
lil	0				
mcon	0				
mcn	0				
via	0				
met2	0				
via2	0				
met3	0				
via3	0				
met4	0				
via4	0				
met5	0				
via5	0				
Summary - Pin Distribution					
+ Pin Number	Net Number Net Ratio Instance Number Instance Ratio				
0	0	0.000000	0	0.000000	
1	0	0.000000	0	0.000000	

DRC Summary

DRC Type	Number
Cut Different Layer Spacing	2228892
Cut EOL Spacing	1
Cut Enclosure	1
Cut EnclosureEdge	1
Cut Spacing	1
Metal Corner Fillin	1
Metal EOL Spacing	1
Metal JogToJog Spac	1
Metal Notch Spacing	1
Metal Parallel Run	1
Metal Short	1
MinHole	1
MinStep	1
Minimal Area	1

Wirelength

Time	Date
2023-04-12T19:03:23	V23.03-OS-01
iEDA	iDB - iEDA Database
Stage	Runtime
Memmory	0.000000 s
Design Name	0.000000 MB
DEF&LEF Version	gcd
DBU	5.8
DBU	1000

Wire Length Report

Wire-length Model	Total Length	Avera
HPWL	11774379	17443
Bound2Bound	13181660	19528
Flute	12888507	19094

Overflow Edge num after earlyGlobal

Total overflow is : 34442

Generate the report at 2023-04-24T16:58:44

Endpoint	Clock Group	Delay Type	TNS
dpath/a/reg_141_d	core_clock	max	-54.997
dpath/z/reg_138_d	core_clock	max	-54.997
dpath/a/reg_133_d	core_clock	min	0.000
dpath/a/reg_142_d	core_clock	min	0.000
dpath/a/reg_146_d	core_clock	min	0.000
dpath/a/reg_136_d	core_clock	min	0.000
clock	delay	type	TNS
core_clock	max		-54.997
core_clock	max		-54.997
core_clock	max		-54.997
core_clock	min		0.000
core_clock	min		0.000
core_clock	min		0.000
Point			
clk (port)			
clk (clock net)			
dpath/b/reg_133_d:CLK (sky130_fd_sc_hd)			
clock core_clock (rise edge)			
dpath/a/reg_146_d:CLK (sky130_fd_sc_hd)			
clock network delay (ideal)			
dpath/a/reg_146_d:CLK (sky130_fd_sc_hd)			
library hold time			
clock reconvergence pessimism			
data require time			
data arrival time			
slack (MET)			

Skew

Clock Pin	Latency	Skew
u0_soc_top/u0_nic400_bus/u_cd_core/u_ib_nic400_axi4_sdram_ib_s/u_aw_fifo_wr/u_cdc_launch_wr_ptr_gry/out_async_reg_0 :CP (DFCNQD1BWP40P140LVT)	0.617	rp+
u0_soc_top/u0_nic400_bus/u_cd_hs_peri/u_ib_nic400_axi4_sdram_ib_m/u_aw_fifo_rd/u_sync_wr_ptr_gry/u_cdc_capt_sync_ptr_0/d_sync1_reg_0 :CP (DFCNQD1BWP40P140LVT)	0.439	-0.168
u0_soc_top/u0_nic400_bus/u_cd_core/u_ib_nic400_axi4_sdram_ib_s/u_aw_fifo_rd/u_sync_wr_ptr_gry/u_cdc_capt_sync_ptr_0/d_sync1_reg_0 :CP (DFCNQD1BWP40P140LVT)	0.617	rp+
u0_soc_top/u0_nic400_bus/u_cd_hs_peri/u_ib_nic400_axi4_sdram_ib_m/u_aw_fifo_rd/u_sync_wr_ptr_gry/u_cdc_launch_wr_ptr_gry/u_cdc_capt_sync_ptr_0/d_sync1_reg_0 :CP (DFCNQD1BWP40P140LVT)	0.439	-0.168
u0_soc_top/u0_nic400_bus/u_cd_core/u_ib_nic400_axi4_sdram_ib_s/u_aw_fifo_rd/u_sync_wr_ptr_gry/u_cdc_launch_wr_ptr_gry/u_cdc_capt_sync_ptr_0/d_sync1_reg_0 :CP (DFCNQD1BWP40P140LVT)	0.439	-0.168

Congestion Report

Grid Bin Size	Bins	Spills	Total	Count
584 * 573	256 by 256			65536

Slew

Net / InstPin	MaxTranTime	TranX	TranY	TranSlack	CellPort	Remark	Percentage
osc_25m_out_pad	5.000r/5.000f	242.114r/9.550f	-237.114r/-4.550f	PDXOEDG_V_G/XOUT	R		50
u0_clk:XOUT	5.000r/5.000f	242.114r/9.550f	-237.114r/-4.550f	PDXOEDG_V_G/XOUT	R		02
osc_100m_out_pad	5.000r/5.000f	242.114r/9.550f	-237.114r/-4.550f	PDXOEDG_V_G/XOUT	R		07
u1_clk:XOUT	5.000r/5.000f	242.114r/9.550f	-237.114r/-4.550f	PDXOEDG_V_G/XOUT	R		06
fanout_net_1	0.437r/0.437f	0.358r/0.380f	0.080r/0.057f	BUFFDBWP30P140LVT/Z			00
fanout_buf_1:z	0.437r/0.437f	0.358r/0.380f	0.080r/0.057f	BUFFDBWP30P140LVT/Z			00

Timing

Group	Delay Type	Path Delay	Path Required	Comments
clock	max	2.147f	1.132	
clock	max	2.147f	1.132	
clock	max	2.147f	1.132	
clock	min	0.411r	0.008	
clock	min	0.411r	0.008	
clock	min	0.411r	0.008	

Cap

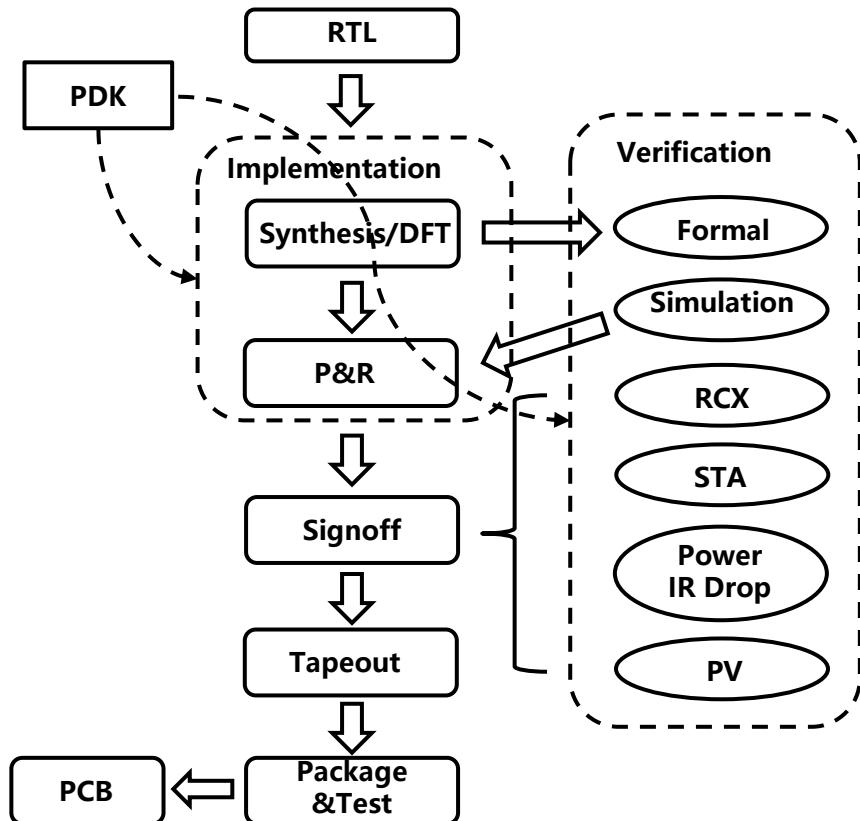
Net / InstPin	MaxCap	Cap	Capslack	CellPort	Remark
u0_soc_top/u0_spi_flash/u0_spi_top/shift/n787	0.058r/0.058f	0.050r/0.050f	0.009r/0.009f	INR2D1BWP40P140LVT/ZN	
u0_soc_top/u0_spi_flash/u0_spi_top/shift/U358:ZN	0.037r/0.037f	0.010r/0.009f	0.027r/0.028f	ND3D1BWP40P140LVT/ZN	
u0_soc_top/u0_spi_flash/u0_spi_top/shift/n337	0.037r/0.037f	0.010r/0.009f	0.027r/0.028f	ND3D1BWP40P140LVT/ZN	
u0_soc_top/u0_spi_flash/u0_spi_top/shift/U457:ZN	0.037r/0.037f	0.010r/0.009f	0.027r/0.028f	ND3D1BWP40P140LVT/ZN	
u0_soc_top/u0_spi_flash/u0_spi_top/shift/n439	0.037r/0.037f	0.010r/0.009f	0.027r/0.028f	ND3D1BWP40P140LVT/ZN	
u0_soc_top/u0_spi_flash/u0_spi_top/shift/U570:ZN	0.037r/0.037f	0.010r/0.009f	0.027r/0.028f	ND3D1BWP40P140LVT/ZN	

Power

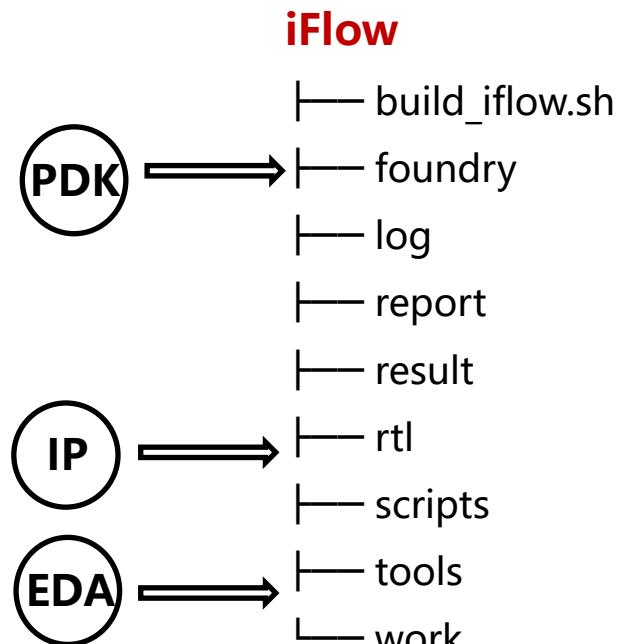
Report : Averaged Power				
Power Group	Internal Power	Switch Power	Leakage Power	Total Power (%)
combinational	1.064e-07	5.063e-09	3.079e-08	1.422e-07 (27.595%)
sequential	2.862e-07	7.337e-09	7.963e-08	3.732e-07 (72.405%)
Net Switch Power	== 1.240e-08 (2.406%)			
Cell Internal Power	== 3.926e-07 (76.173%)			
Cell Leakage Power	== 1.104e-07 (21.422%)			
Total Power	== 5.154e-07			

iEDA-Flow and Evaluating

- **iFlow:** a chip design flow, integrating some different EDA tools for completing flow
- **iEDA-script:** an iEDA specialized execution script, for testing, evaluating, parsing data



Chip design flow



iEDA-script

```
scripts
  docker
  ispd18
  sky130
    common
    iEDA_config
      cts_default_config.json
      db_default_config.json
      drc_default_config.json
      flow_config.json
      fp_default_config.json
      no_default_config_fixfanout.json
      pl_default_config.json
      rt_default_config.json
      to_default_config_drv.json
      to_default_config_hold.json
      to_default_config_setup.json
    sdc
    .gitignore
    README.md
    run_iEDA.py
    run_iEDA.sh
    .gitignore
  lef
  lib
```

The screenshot shows the contents of the iEDA-script directory, which includes sub-directories for docker, ispd18, sky130, sdc, and various configuration files like cts_default_config.json and run_iEDA.py.

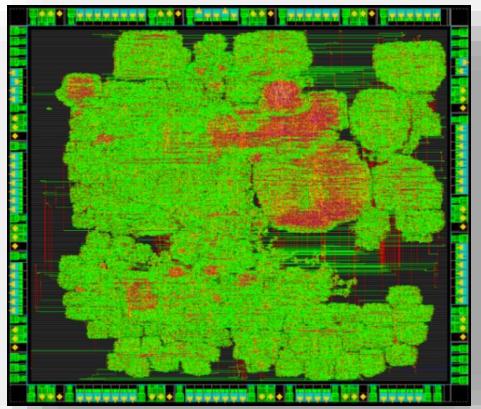
iEDA-Flow and Evaluating

Flow		PDK	时钟_MHz	placement		routing			sta		
				GP_original HPWL (um)	DP HPWL(PL_eval)	drouote run time (s)	total wire length	total vias	setup_slack (max)	hold_slack (min)	suggest freq(MHz)
openroad	APU	sky130	50	108025.8	304807.6	900	348193	42309	14.28	0.44	174.8251748
	BM64	sky130	50	950721.2	1151209.6	660	1298431	118906	14.22	0.42	173.0103806
	PPU	sky130	50	799473.6	1325241.3	14220	1666739	173502	15.46	0.38	220.2643172
	aes	sky130	50	1736825.9	2234547.8	1920	2695657	280870	14.7	0.22	188.6792453
	aes_core	sky130	50	1915862.8	2353877.1	2040	2809505	271884	14.73	0.4	189.7533207
	blabla	sky130	50	2162081.7	2401241.7	1320	2651252	226526	9.84	0.38	98.42519685
	caravel_upw	sky130	50	35240.4	60479.9	180	66621	7595	17.82	0.4	458.7155963
	gcd	sky130	50	10958.5	23153.9	60	25345	3798	16.73	0.44	305.8103976
	picorv32a	sky130	50	955226.7	1458821.9	2040	1659581	177160	8.78	0.38	89.12655971
	s44	sky130	50	3153.7	6408.8	1020	7149	1220	19.25	0.42	1333.333333
iEDA	salsa20	sky130	50	2014421.6	2231403.5	1140	255535	262945	9.93	0.41	99.30486594
	APU	sky130	50	101311.635	108052.855	59.15	153766.992	39682	15.81	0.364	238.638
	BM64	sky130	50	724102.907	734325.379	167.71	814055.014	183714	15.73	0.386	234.199
	PPU	sky130	50	798854.543	814966.702	236.65	1133497.302	141243	16.185	0.354	262.124
	aes	sky130	50	1787923.281	1804659.776	456.84	2447231.105	284325	15.856	0.261	241.341
	aes_core	sky130	50	1869162.753	1880282.585	417.38	2360070.252	261450	15.934	0.366	245.913
	blabla	sky130	50	1915513.912	1935383.056	305.18	2004497.857	192730	12.203	0.341	128.25
	caravel_upw	sky130	50	34144.56	35161.52	1.17	50311073	15885	18.313	0.353	592.825
	gcd	sky130	50	11282.203	11774.379	0.78	16126254	9534	17.735	0.403	441.47
	picorv32a	sky130	50	928885.74	951888.682	236.62	1093014.143	163736	13.825	0.341	161.933
Ratio	s44	sky130	50	3008.324	3292.983	0.27	4641801	2764	19.421	0.388	1727.05
	salsa20	sky130	50	1895922.266	1938562.099	429.95	2331960.542	267963	12.629	0.384	135.676
	APU	sky130	50	1.066272398	2.820912043	15.21	2.264419662	1.0662013	0.903225806	1.208791209	0.732595709
	BM64	sky130	50	1.312964208	1.56771049	3.94	1.59501628	0.647234288	0.904005086	1.088082902	0.738732363
	PPU	sky130	50	1.000774931	1.626129383	60.09	1.470439318	1.22839362	0.955205437	1.073446328	0.840305799
	aes	sky130	50	0.97142082	1.23821001	4.20	1.101513051	0.987848413	0.927093845	0.842911877	0.781795241
	aes_core	sky130	50	1.024984473	1.251874117	4.89	1.190432784	1.039908204	0.924438308	1.092896175	0.771627855
	blabla	sky130	50	1.128721481	1.240706171	4.33	1.322651451	1.175354122	0.806359092	1.114369501	0.767447929
	caravel_upw	sky130	50	1.032094132	1.720059315	154.50	0.001324182	0.478124016	0.973079233	1.133144476	0.773779102
	gcd	sky130	50	0.971308529	1.966464643	77.09	0.001571661	0.398363751	0.943332394	1.091811414	0.692709352
Ratio	picorv32a	sky130	50	1.028357589	1.532555148	8.62	1.518352723	1.081985635	0.635081374	1.114369501	0.55039158
	s44	sky130	50	1.048324582	1.946198933	3,784.06	0.001540135	0.441389291	0.991195098	1.082474227	0.772029376
	salsa20	sky130	50	1.062502211	1.15106114	2.65	0.10957947	0.981273534	0.786285533	1.067708333	0.731926545
	Average			1.058884123	1.641989218	374.51	0.961530974	0.866006925	0.88630011	1.082727813	0.741212805

iEDA-Tapeout

- **1st Tapeout**
 - 2022-02-02, 110nm node, 0.7M gates, Freq: 25MHz, Core Density: 30%
- **2nd Tapeout**
 - 2022-08-12, 110nm node, 1.5M gates, Freq: 25MHz, Core Density: 35%
- **3rd Tapeout**
 - 2023-01-04, 28nm node, 1.5M gates, Freq: 200MHz, Core Density: 40%

2022-02-02, 1st Tapeout

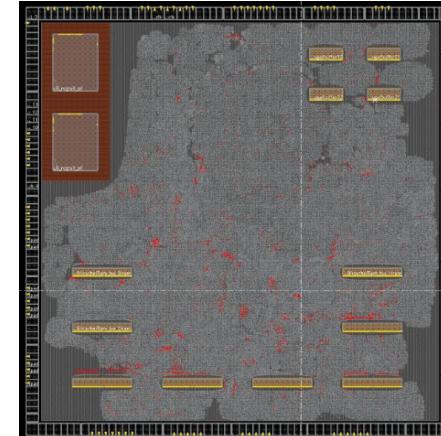


110nm node, 0.7M gates, 25MHz
(5-level pipeline, IP:Chiplink, UART, SPI)

Macro, Multi-clock,
Scale increasing,
Auto-design



2022-08-12, 2nd Tapeout

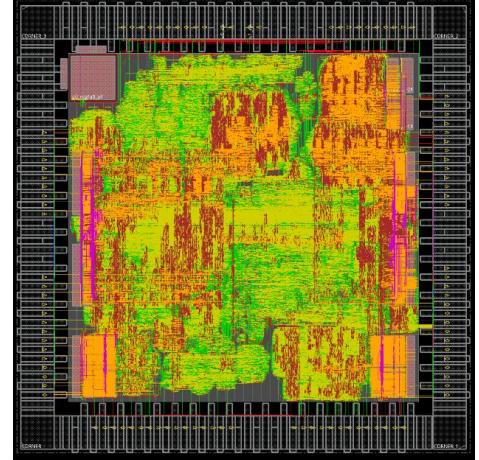


110nm node, 1.5M gates
(11-level pipeline with cache, IP:
UART, VGA, PS/2, SPI, SDRAM,
Two PLL on SoC, Support Linux)

110nm → 28nm

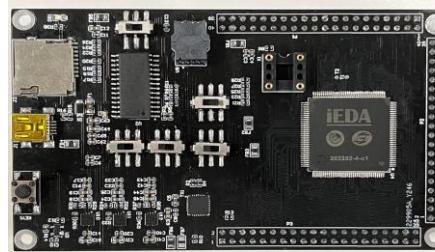
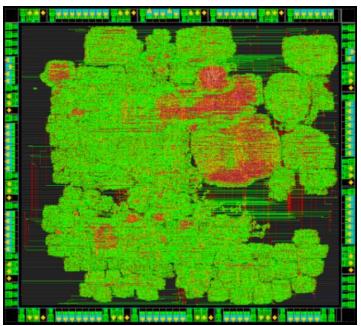


2023-01-04, 3rd Tapeout



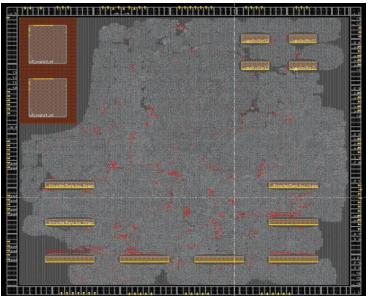
28nm node, 1.5M gates
(11-level pipeline with cache, IP:
UART, VGA, PS/2, SPI, SDRAM,
Two PLL on SoC, Support Linux)

iEDA-Tapeout

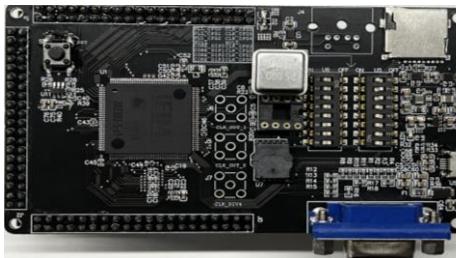
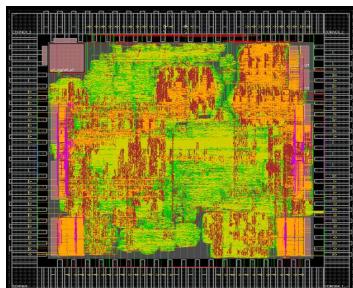


```
*Verdi* : Create FSDB file 'asic_top.fsdb'.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
[0.0 ns ns] ==INFO== Hold condition disabled: commun
[0.0 ns ns] ==INFO== Protocol selected is extended
[0.0 ns ns] ==INFO== z_ Load memory content from fil
[0.0 ns ns] ==INFO== VCore has been
[0.0 ns ns] ==INFO== Single Trans
[1.0 ns ns] ==INFO== Load flash di
[150.0 ns ns] ==INFO== Power up: d
[150.0 ns ns] ==INFO== Protocol se
[150.0 ns ps] ==INFO== Single Tran
heap: [0x8000d470 - 0x8640d470]
\\ /
- RT - Thread Operating System
/ | \
/   \ 4.0 build Sep 11 2022
2006 - 2021 Copyright by rt-thread
Hello RISC-V!
```

2022-02-02, 1st Tapeout



2022-08-12, 2nd Tapeout



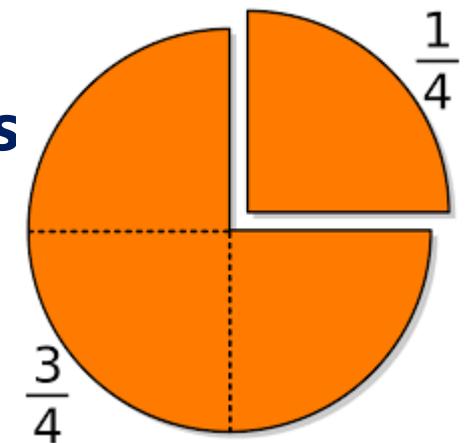
2023-01-04, 3rd Tapeout

- 01 **Introduction**
- 02 **iEDA Today**
- 03 **iEDA Future**

Some Notices

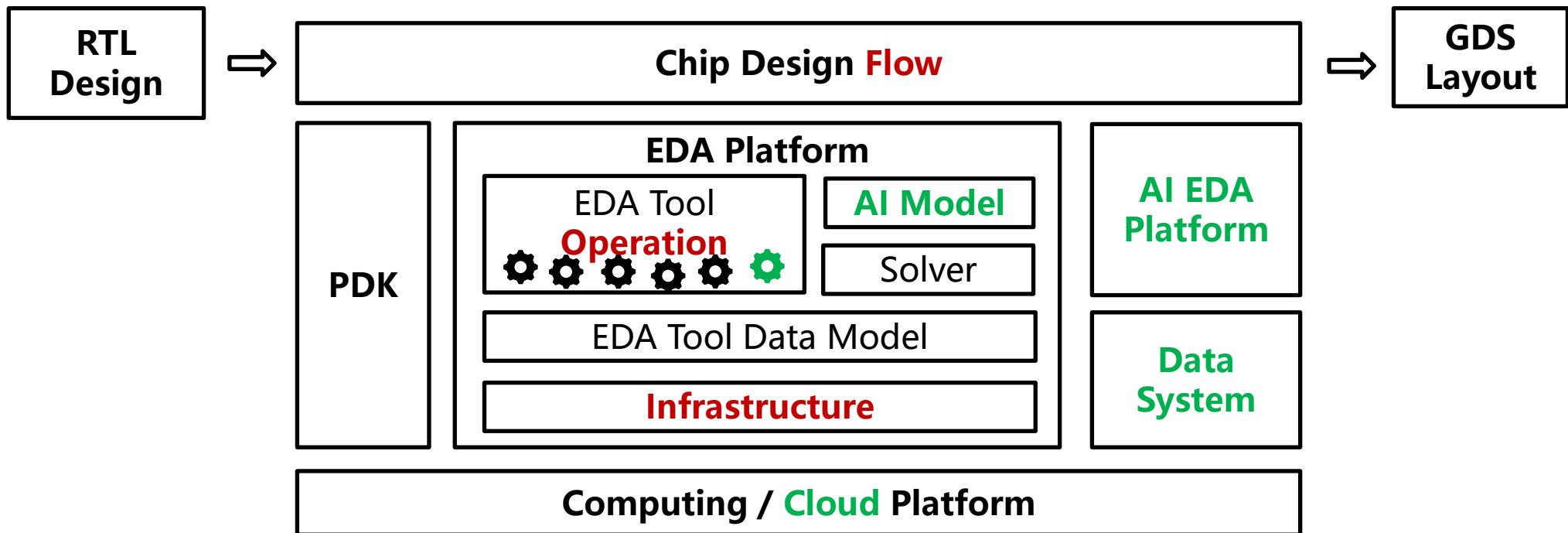
- **Open-source code link:**
 - **Gitee:** <https://gitee.com/oscc-project/iEDA>
 - **GitHub:** <https://github.com/OSCC-Project/iEDA>
- **Testing:** 3 months of testing
- **Release:** Official version will be released after 3 months
- **Tutorial:** At least a tutorial each month
- **Quarterly version**
 - Since 2023-09-01, version will be iterated every quarter

3 months



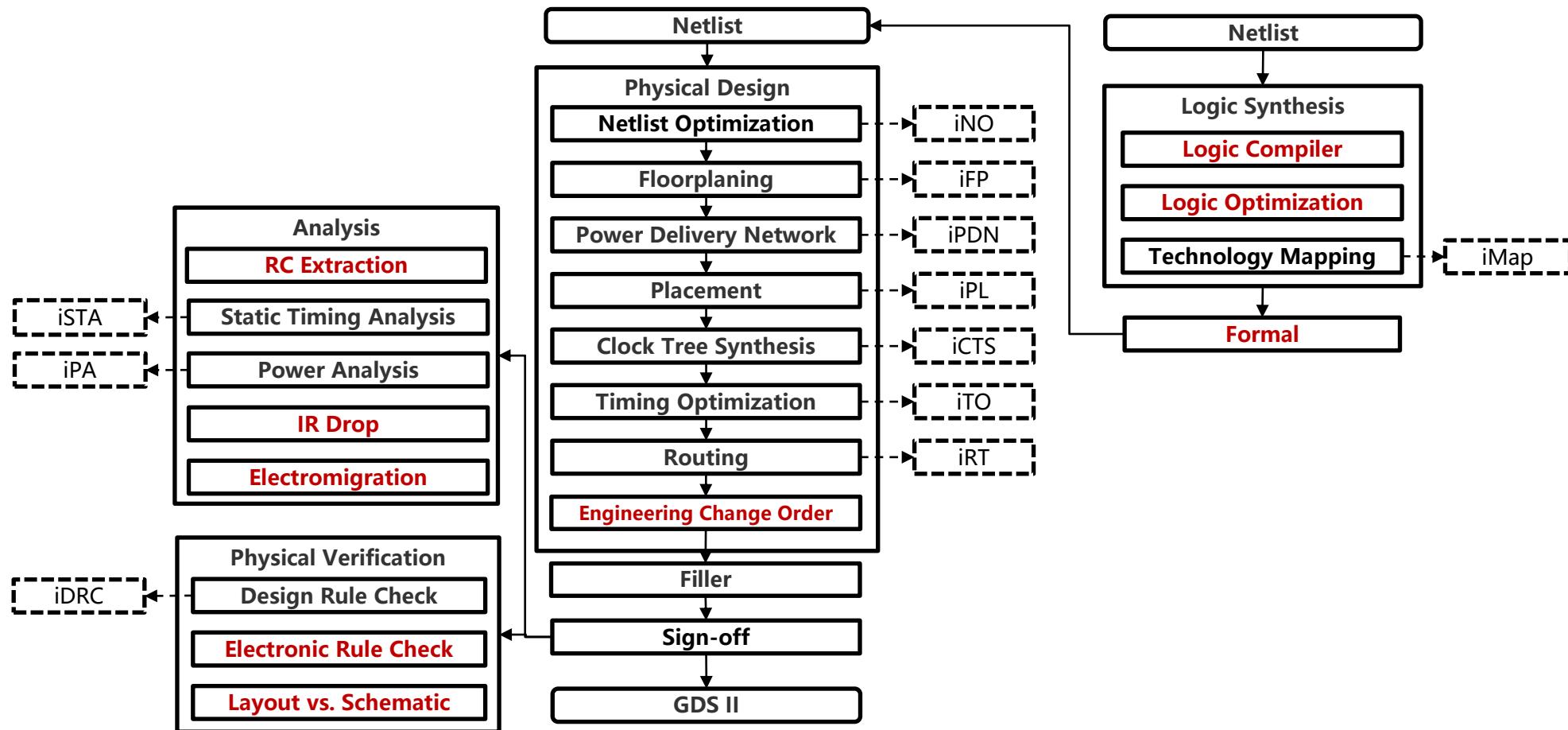
iEDA

- Enhance the **infrastructure** to support more design requirement
- Complete the EDA **tool chain** from **RTL-GDS II**
- Improve the **quality and performance** of all EDA tool operations
- Construct **AI for EDA platform** and introduce trained **AI model** to the EDA platform
- Build **data system** with enough **chip** design and labeling process **data**
- Achieve the adaptability of the EDA platform for **cloud-native**



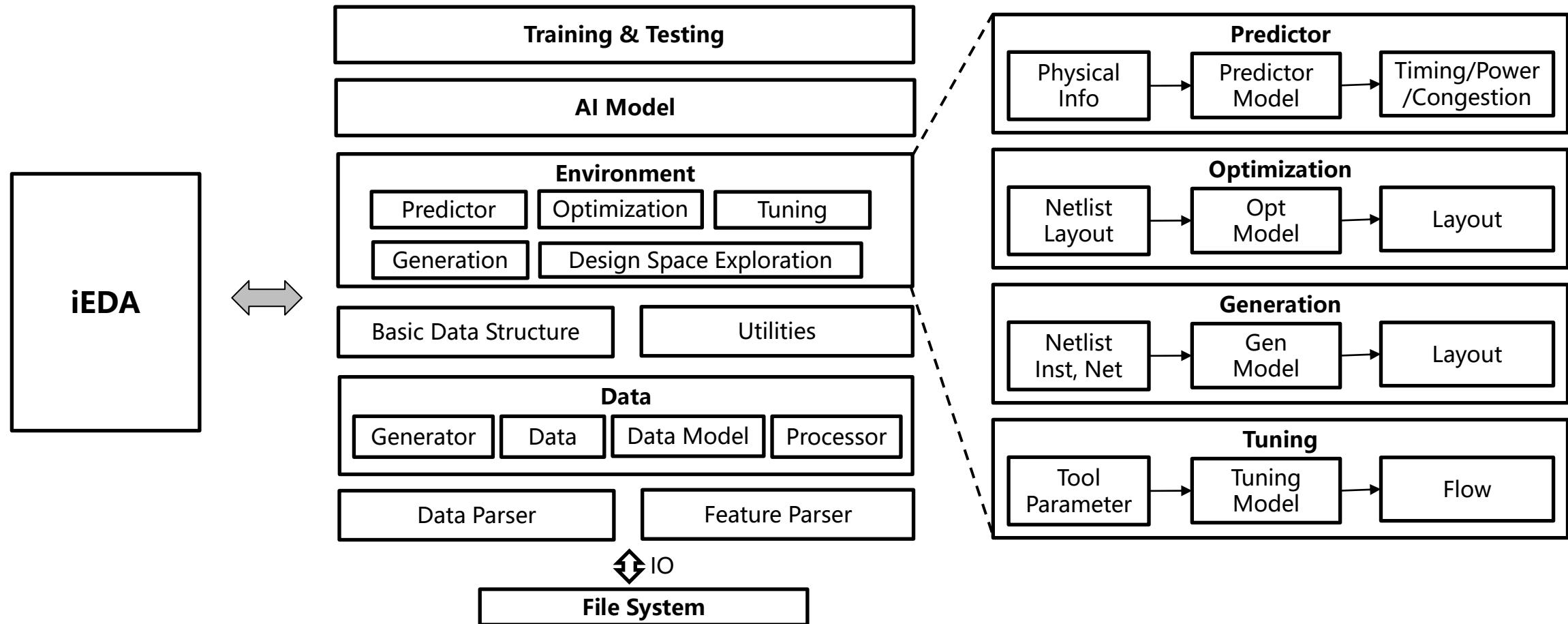
iEDA-Tool

- We continuously develop more EDA tools (include **Logic Synthesis, Physical Design and Sign-off**), to achieve RTL-GDS II closure
- Improve the quality of iEDA tools operation near the commercial tools.



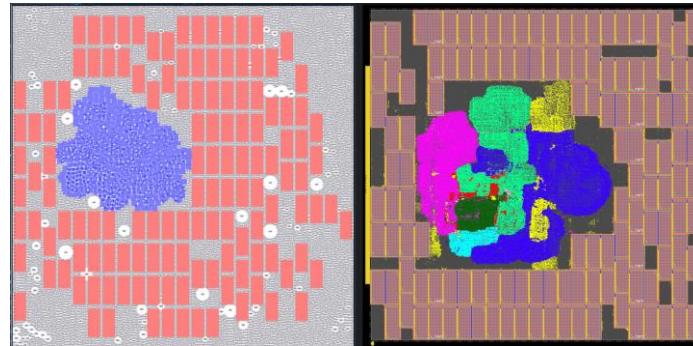
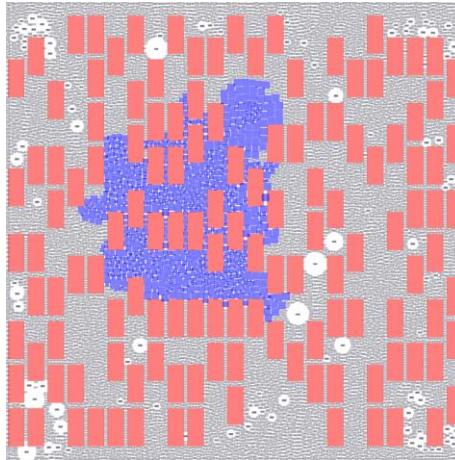
iEDA-AiEDA: Framework and Toolkit

- Construct a AI + EDA framework and package
- Research AI for EDA instead of AI in EDA



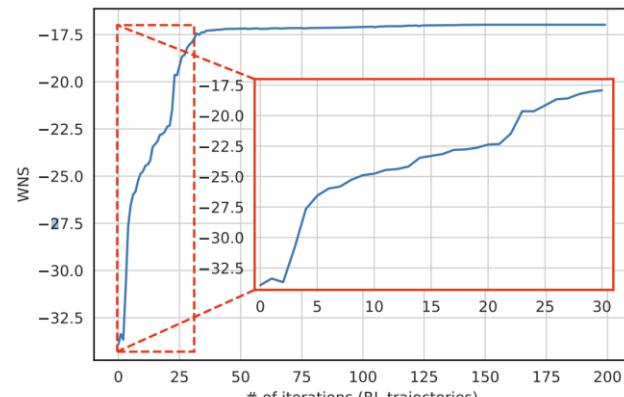
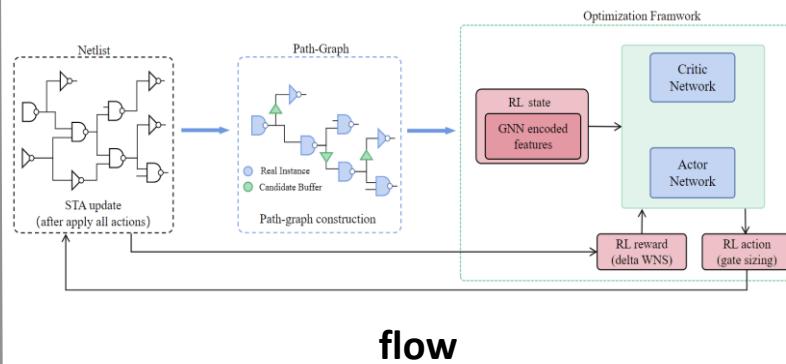
iEDA-Solver and AI Model

AI floorplan
(AiFP)



Wirelength: **AiFP < engineer**

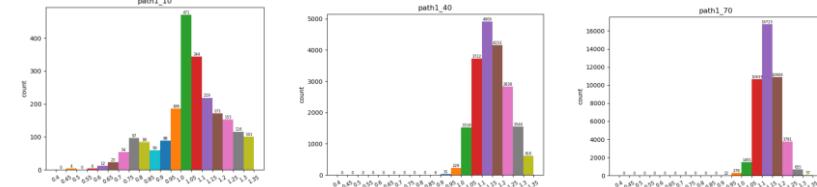
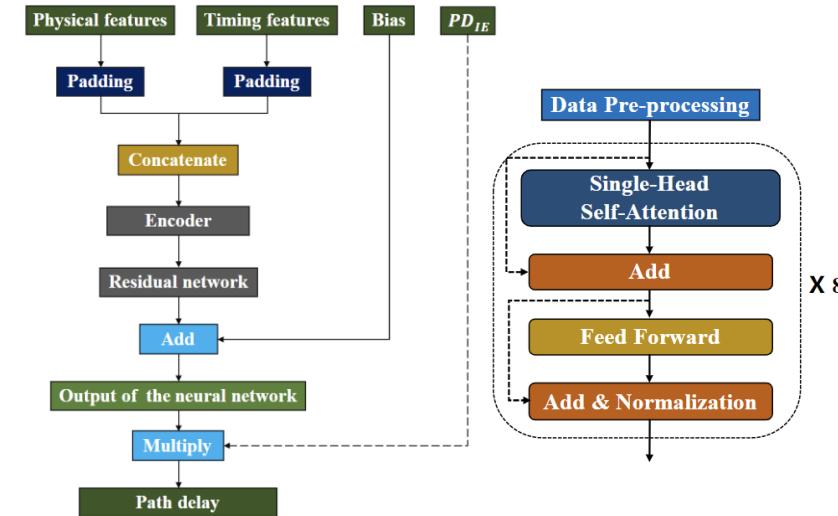
AI timing optimization
(AiTO)



iteration

Based on innovus, improve **4%**

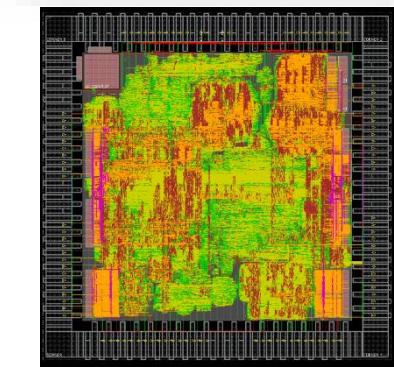
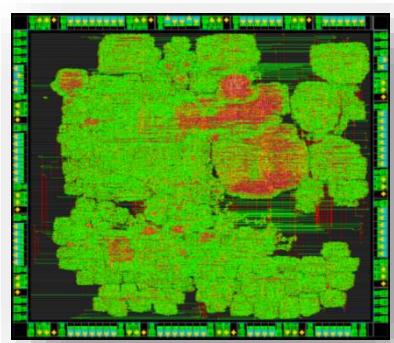
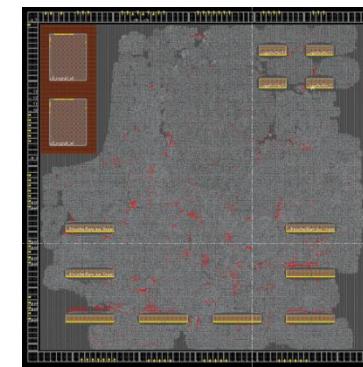
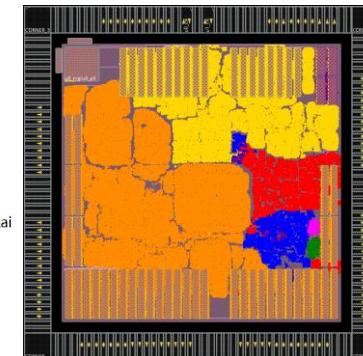
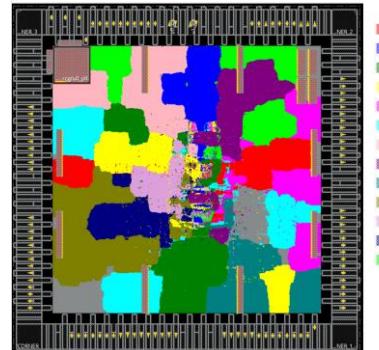
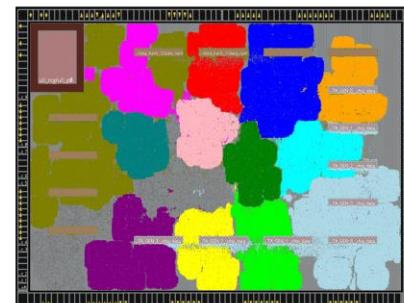
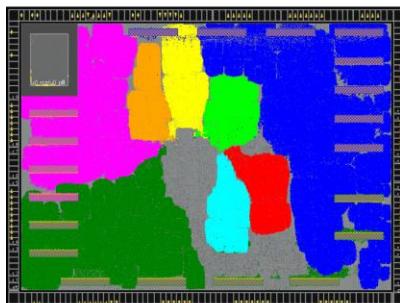
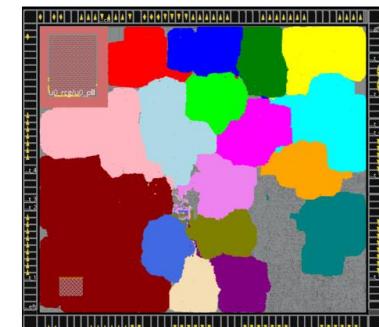
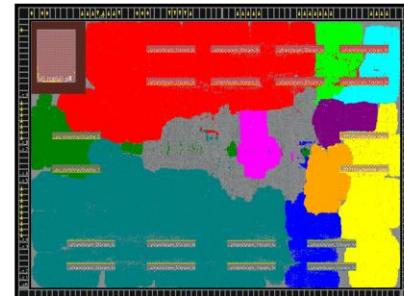
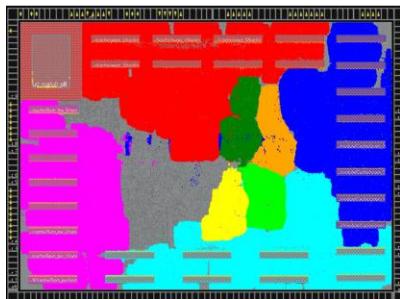
AI timing analysis
(AiSTA)



Error with commercial tool <3%

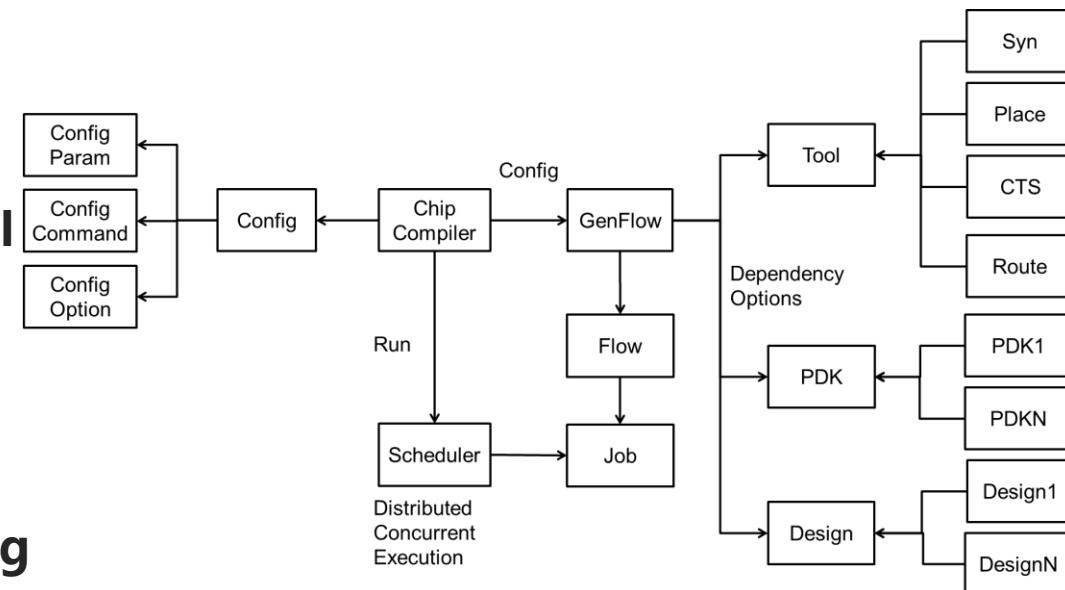
iEDA-Data System: Chip Design Data

- Design or generate chip design in RTL format
- Construct open-source chip design dataset for validating and training or testing EDA tool, algorithm and AI model



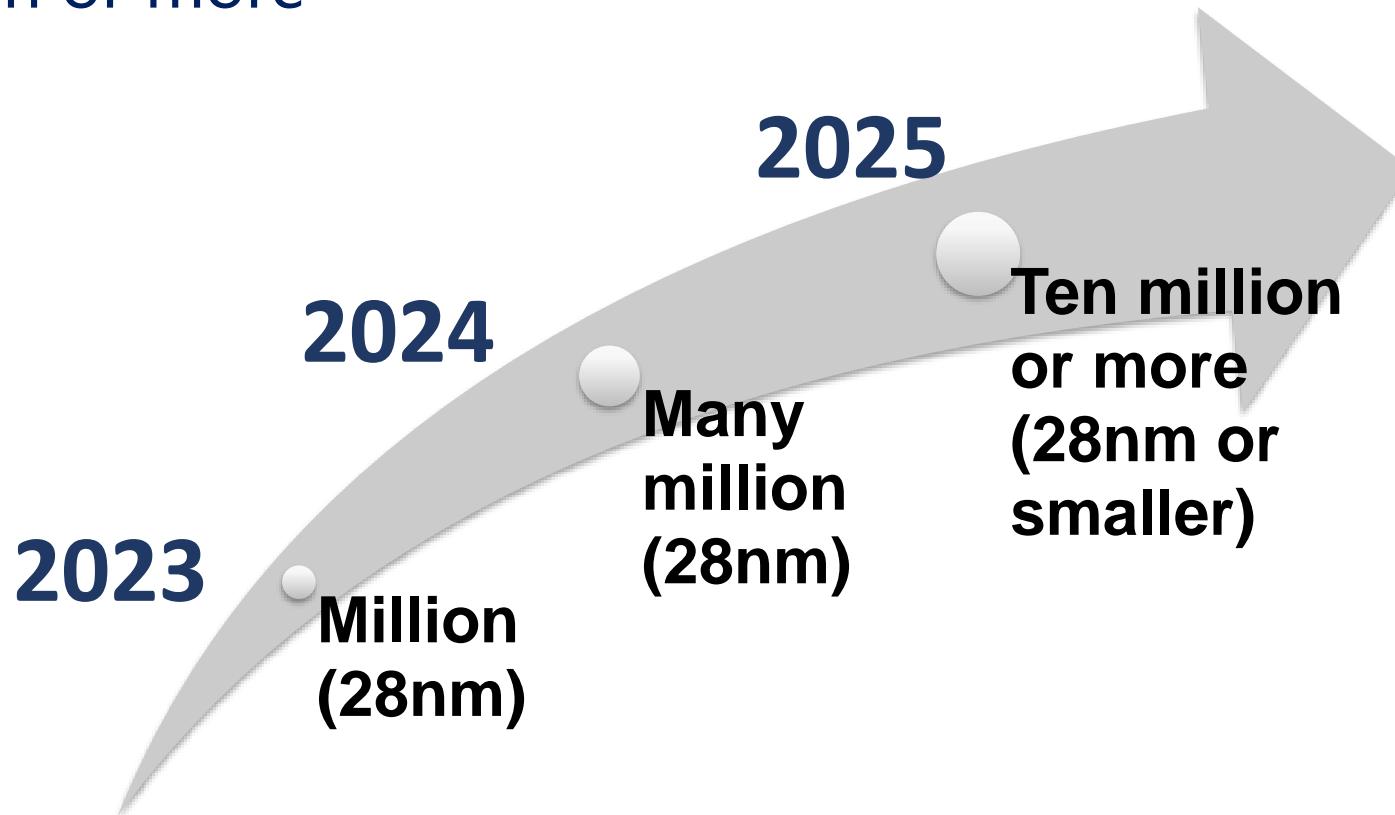
iEDA-Data System: Labeled Data

- Construct EDA dataset with enough labeled data from RTL-netlist-def-GDS II
 - Include architecture, logic, aig, circuit, netlist, nets, layout (metal1, >metal 2, cut) and so on.
- Chip compiler
 - Use to automatically design chip from RTL-GDS II and report by traveling different key parameter
- Feature parser tool
 - Parse feature and label from process report or log
- Data Storage
 - File format (Json, csv, yaml, h5, ...), database (mongoDB, MySQL, ...)



iEDA-Chip Design

- In the next 3 years, we will continuously support chip design by using open-source EDA tool
- At 28nm and below process node, we enlarge the design scale up to ten million or more



Conclusion

- **iEDA Features**

- Support industrial and academic,
- Common EDA infrastructure,
- Open-source development,
- Introduce new technologies, AIEDA,
- Co-design between chip and EDA,
- Support EDA talent training,
- Support chip design,
- Standard software development,
- Emphasize process data analysis,
- Cloud-native.

- **iEDA Contents**

- EDA base platform,
- EDA infrastructure,
- EDA operations (tools)
 - (iNO/ iFP/iPDN/ iPL/iCTS/iTO/iRT/iSTA/iPW /iDRC),
 - (iLS/iMap/iECO/iFL/iRCX/iLR/iERC/iLVS)
- Chip design flow,
- AIEDA framework,
- EDA AI models,
- EDA label data system,
- Web development.

About iEDA

- About “i” in **iEDA**
 - Meaning 1: **Infrastructure**
 - Meaning 2: **Intelligent**
- The goal of the **iEDA project**
 - **EDA Infrastructure**
 - **High quality and performance EDA tool**
- **Open-source is not a goal but a way**

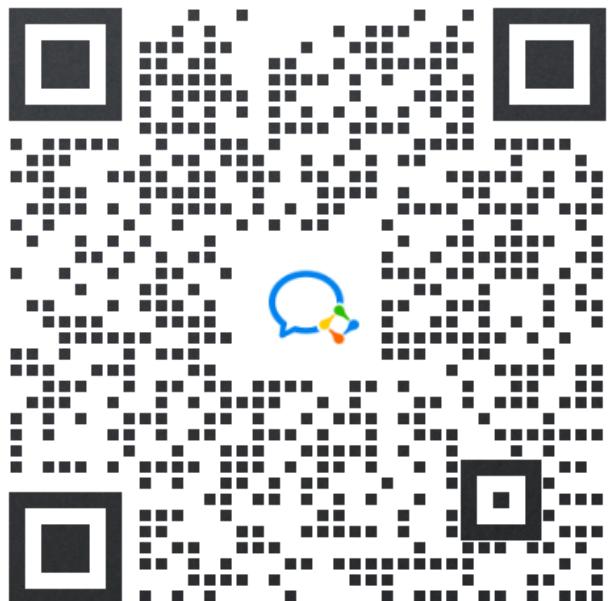


Acknowledgment



We've had a lot more support than that, and we look forward to seeking more users and developers

WeChat Group:



QQ Group : 793409748

Thanks
Welcome to join us