Design and Simulation of a CMOS Inverter using eSim

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Supply Voltage: 3.3 V

Abstract

This report presents a test submission for the eSim Marathon: a basic CMOS inverter implemented and simulated using an ngspice-compatible netlist. The inverter is intended to validate the submission process and demonstrate transient switching behaviour at a 3.3 V supply. The design uses one PMOS and one NMOS transistor with a resistive load to observe rail-to-rail transitions.

Objective

1. Provide a working inverter netlist compatible with ngspice and eSim. 2. Demonstrate expected input-output switching for a pulse input. 3. Prepare a submission package compatible with the eSim Marathon test requirements.

Circuit Description

The CMOS inverter consists of a PMOS (M1) connected between the output node and Vdd, and an NMOS (M2) between the output node and ground. Both gates are driven by the same input node 'in'. A resistive load of 10 kΩ is connected from output to ground for observation. The netlist included uses simple Level-1 MOS models as placeholders; for foundry-accurate results, include the SG13G PDK models in the schematic (.include).

Simulation Setup

Simulation commands provided in the netlist: • .tran 0.1u 5u uic — transient analysis (time step 0.1 µs, total 5 µs) • .op — operating point • .ac dec 100 1 1G — AC sweep (for small-signal analysis) Input source: PULSE(0 3.3 0 1n 1n 1u 2u) — a pulse from 0 to 3.3 V with rise/fall times of 1 ns and period 2 µs.

Expected Results and Analysis

Transient analysis should show Vout toggling between 0 V and 3.3 V when Vin is pulsed. The inverter transfer characteristic (VTC) can be derived by performing a DC sweep of Vin from 0 to 3.3 V and plotting V(out) vs V(in). Key observations to report: • Logic-level correctness (rail-to-rail output) • Propagation delay (measure time difference between Vin crossing threshold and output transition) • Rise/fall times and any overshoot (depends on device models and load capacitance)

How to reproduce

1. Open a terminal in the provided folder and run: ngspice CMOS_Inverter.cir 2. To view transient waveforms in interactive ngspice: plot v(out) v(in) 3. To perform DC transfer: replace .tran with .dc Vin 0 3.3 0.01 and plot v(out) 4. In eSim/Eeschema, create a schematic using PMOS/NMOS symbols, wire nodes as in the schematic descriptor, and include this netlist or copy model definitions into the schematic's SPICE directives.

Files included

• CMOS_Inverter.cir — SPICE netlist • CMOS_Inverter.kicad_sch — KiCad schematic file (best-effort) • CMOS_Inverter.sch.txt — human-readable descriptor • README.txt — instructions • submission_report_detailed.pdf — this report

Future Scope

• Replace placeholder MOS models with SG13G PDK transistor models for foundry-accurate simulations. • Add load capacitance and measure dynamic power and switching metrics. • Expand into a ring oscillator or inverter chain to measure propagation and power at different loads.

References

1. Razavi, B. (2001). Design of Analog CMOS Integrated Circuits. 2. eSim documentation and ngspice user manual.