EE 533: Network Processor Design and Programming

Instructor: Young Cho, Ph.D.

Zhongqi Zhao: 7864803206

Github link:

https://github.com/ZzqXAUT/EE533.git

Questions

Verilog & Schematic

The generated Verilog code is functionally reasonable and synthesizable, but it is clearly an auto-generated schematic netlist, which makes it verbose, hard to read, and difficult to maintain. It correctly represents the intended hardware, but it is not suitable for manual modification or long-term reuse.

In general, writing Verilog is easier than drawing schematics because it is more concise, scalable, and easier to debug, simulate, and maintain. Complex logic can be expressed clearly in a small amount of code, which is not practical with schematics.

Schematics are mainly useful for learning, visualization, or very small and simple designs, while Verilog is preferred for larger, more complex, or reusable designs.

a) Explain the pattern matching algorithm in the report

The pattern matching algorithm works by comparing incoming data with a stored pattern. The data is divided into smaller parts, and each part is checked at the same time. Some bits can be ignored using a mask, so the match does not have to be exact. If the required parts match, the circuit reports a pattern match.

b-i) What is the purpose of AMASK[6:0]?

AMASK[6:0] is used to control which bits are compared and which bits are ignored. A masked bit is treated as “don’t care,” which allows flexible matching instead of strict bit-by-bit comparison.

b-ii)What exactly does busmerge.v do?

The busmerge.v module combines two input buses into one wider bus. It simply concatenates the inputs so that they can be processed together by other modules.

b-iii)What do the comp8 modules do in this schematic?

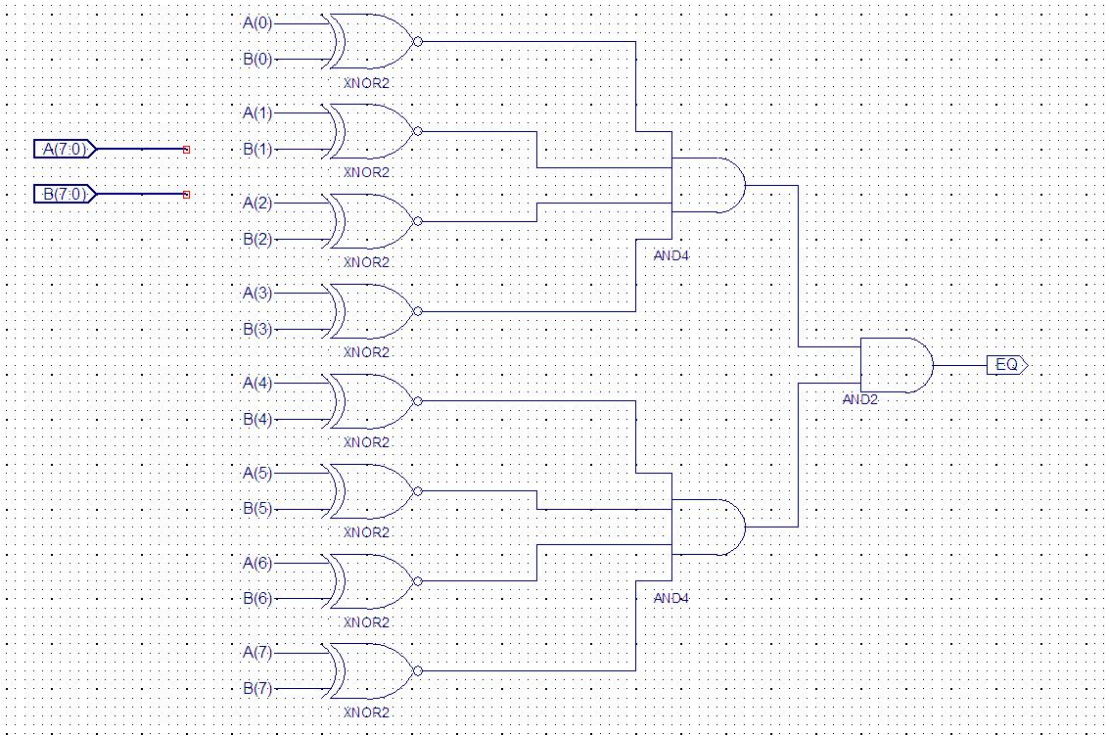
The comp8 module compares two 8-bit values and outputs a signal when they are equal. It is used to check whether parts of the data match the expected values.

b-iv) What is the purpose of dual9Bmem in dropfifo.sch?

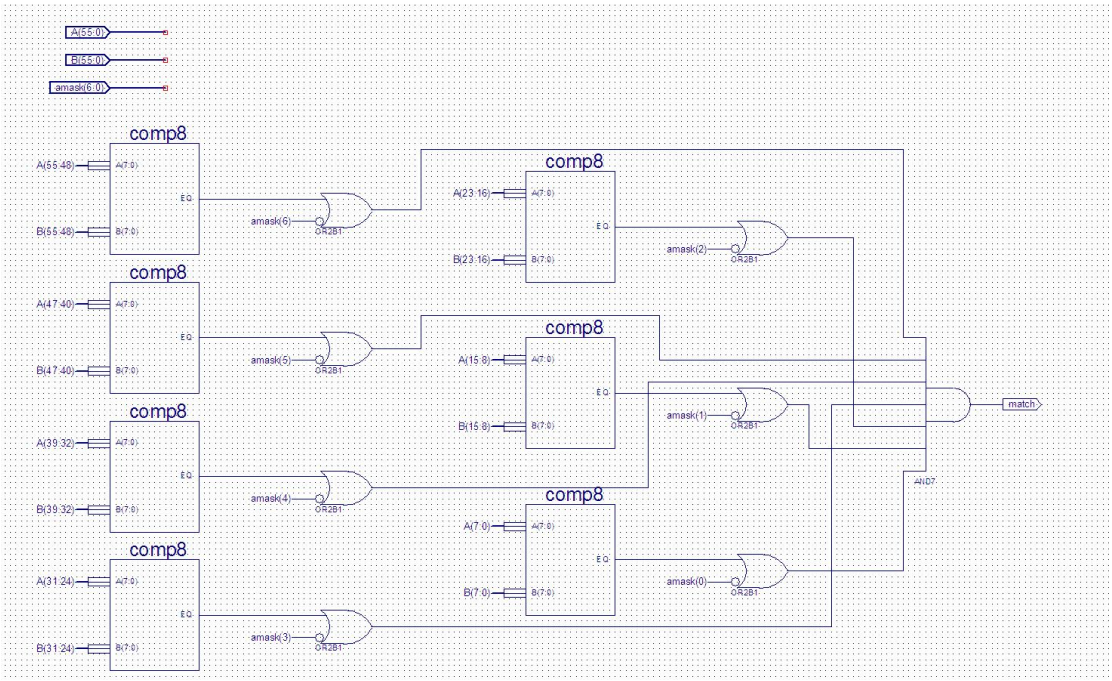
In dropfifo.sch, the dual9Bmem module is a dual-port memory used as a FIFO buffer. It stores 72-bit data words and allows reading and writing at the same time, which helps manage data flow through the circuit.

Schematics

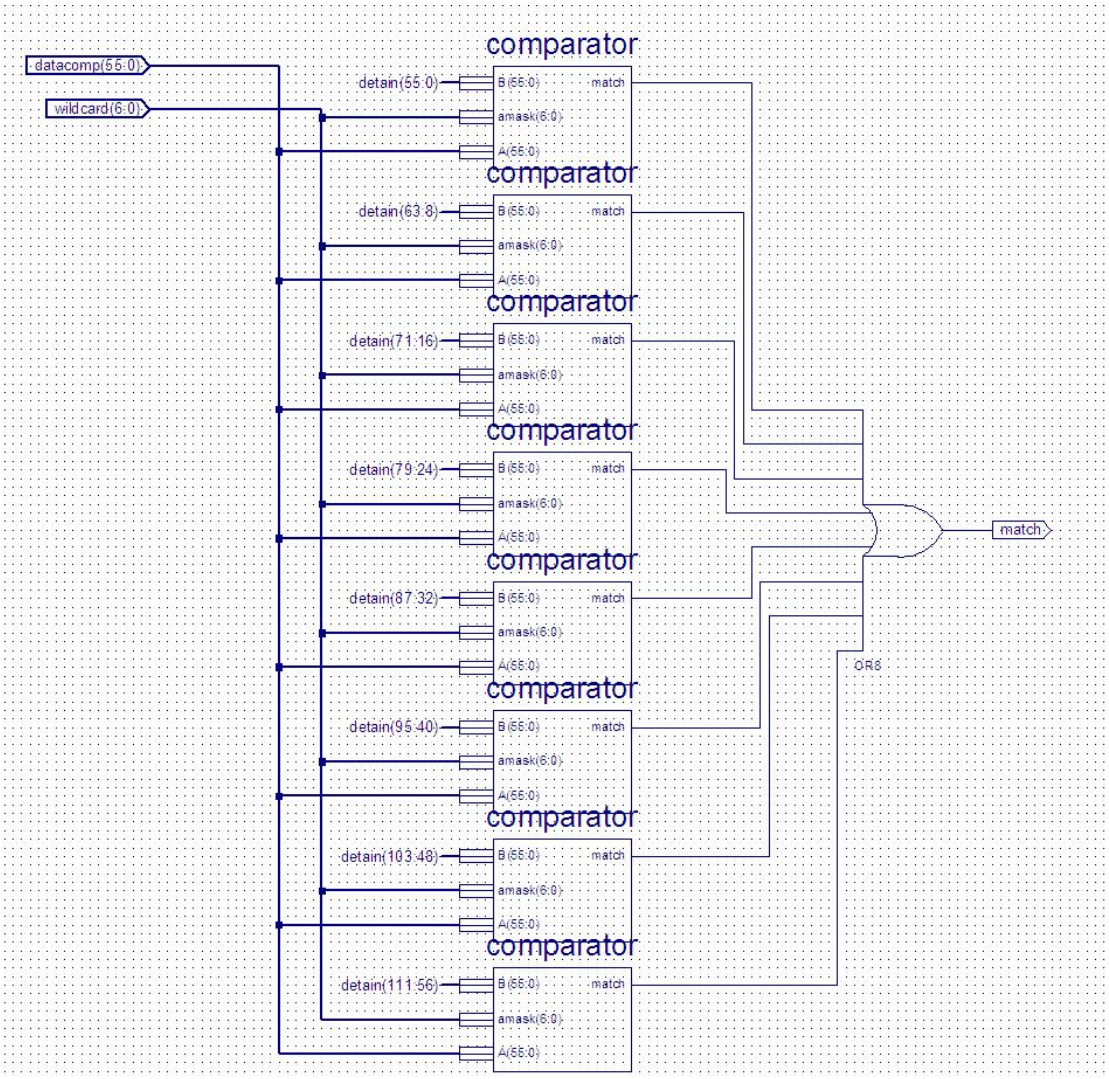
comp8



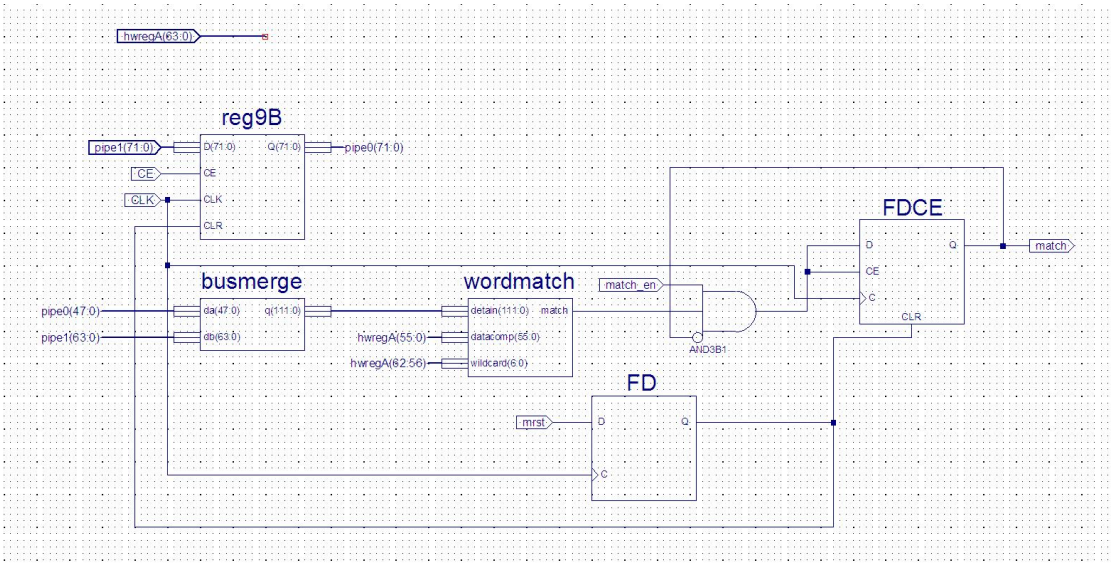
comparator



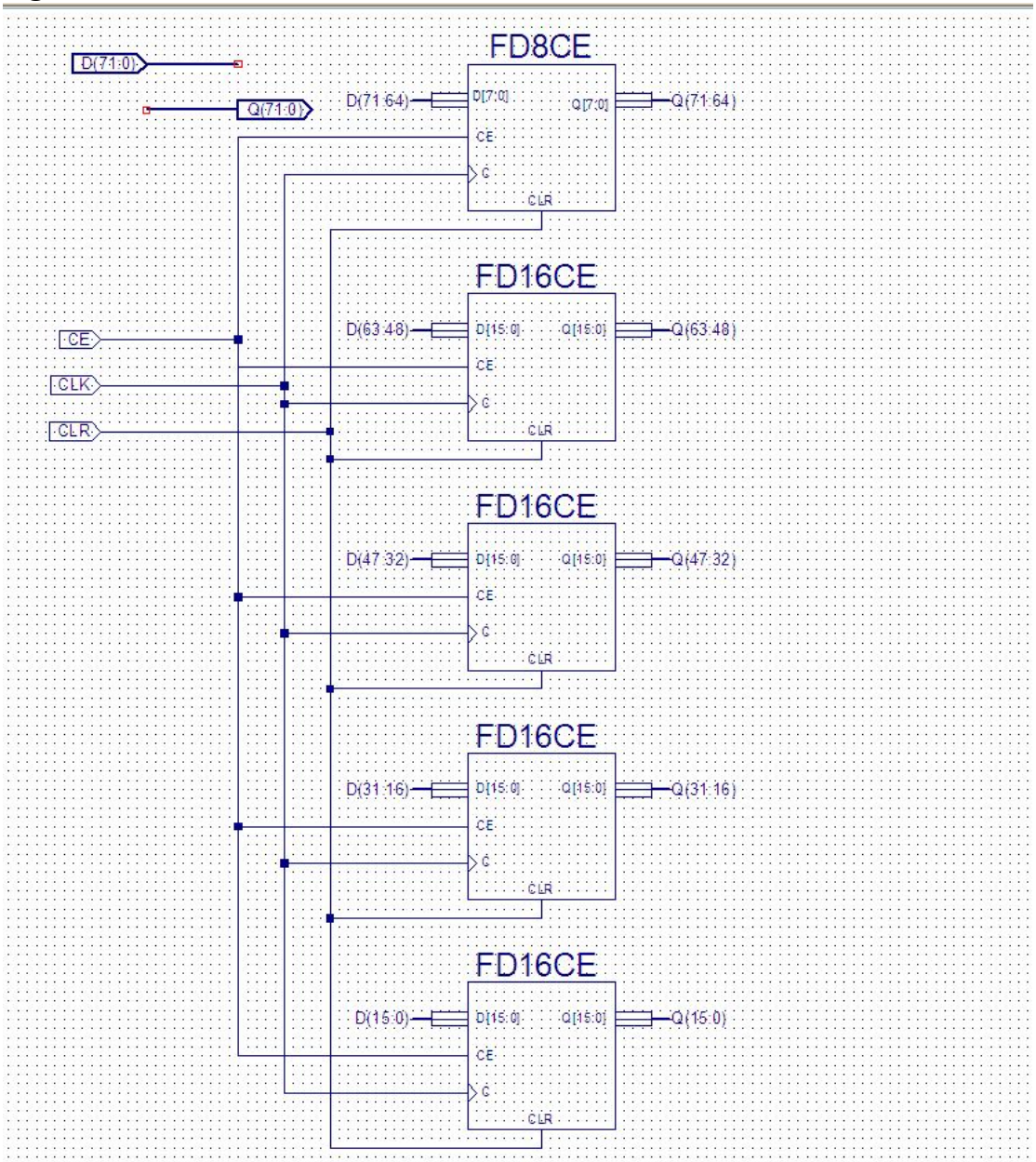
wordmatch



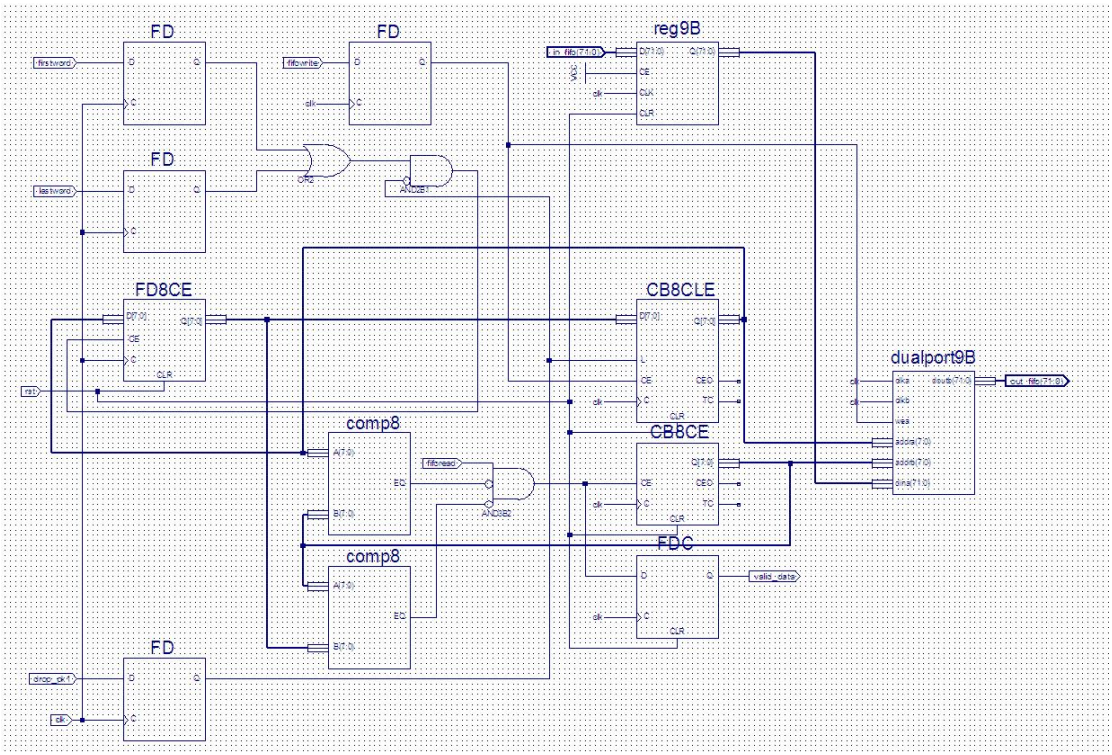
detect7B

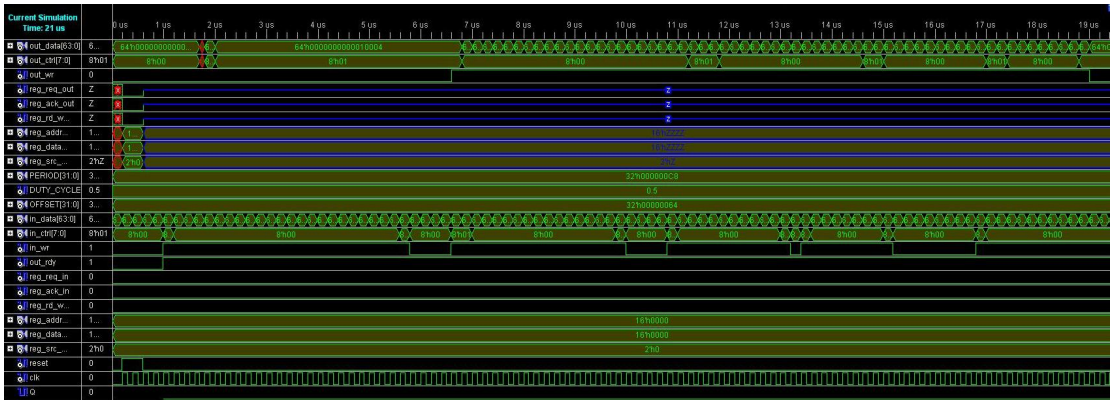


reg9B


D(71:0)
Q(71:0)
FD8CE
D(71:64)
D[7:0]
Q[7:0]
Q(71:64)
CE
C
CLR
FD16CE
D(63:48)
D[15:0]
Q[15:0]
Q(63:48)
CE
CLK
CLR
FD16CE
D(47:32)
Q(47:32)
FD16CE
D(31:16)
Q(31:16)
FD16CE
D(15:0)
Q(15:0)

dropfifo


FD
FD
reg9B
FD
FD8CE
CB8CLE
dualport9B
comp8
CB8CE
comp8
FDC
FD


Current Simulation Time: 21 us
out_data[63:0]
out_ctrl[7:0]
out_wr
reg_req_out
reg_ack_out
reg_rd_w...
reg_addr...
reg_data...
reg_src_...
PERIOD[31:0]
DUTY_CYCLE
OFFSET[31:0]
in_data[63:0]
in_ctrl[7:0]
in_wr
out_rdy
reg_req_in
reg_ack_in
reg_rd_w...
reg_addr...
reg_data...
reg_src_...
reset
clk
IO