



EE 533: Network Processor Design and Programming

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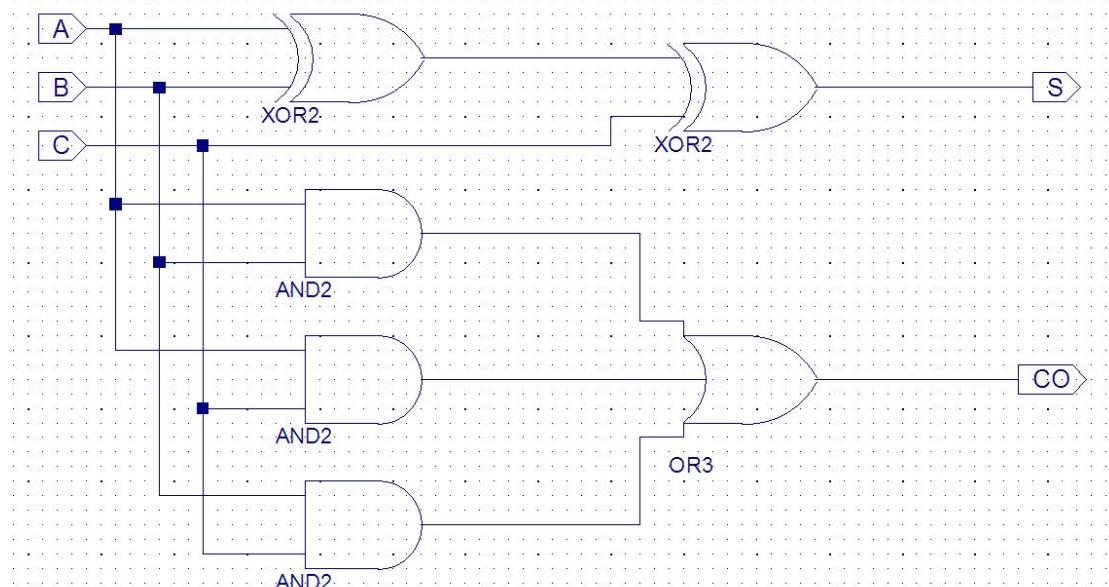
Github link:

<https://github.com/ZzqXAUT/EE533.git>

Schematic

1-bit Full Adder

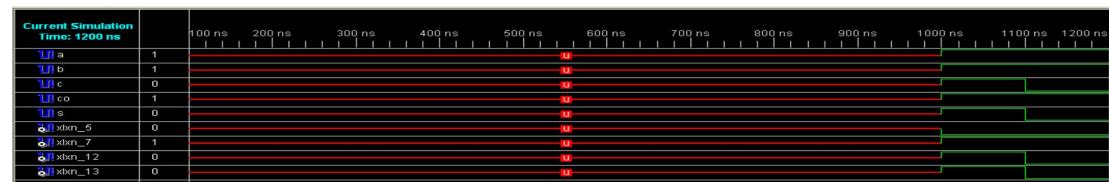
Schematic:



Test data:

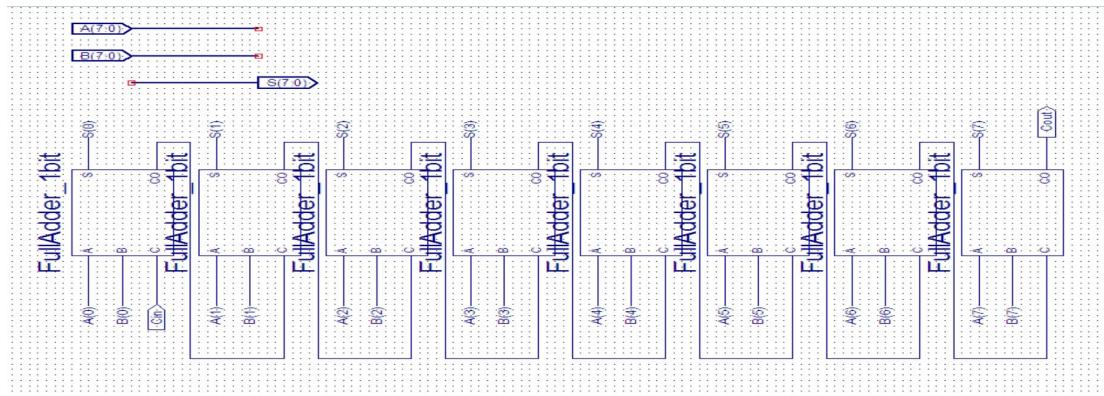
```
This is a Full version of ISE Simulator (ISim).
Simulator is doing circuit initialization process.
Finished circuit initialization process.
> % put a 1
> % put b 1
> % put c 1
> % run
> % put c 0
> % run
%
```

Functional waveforms:



8-bit Full Adder without D Flip Flop

Schematic:



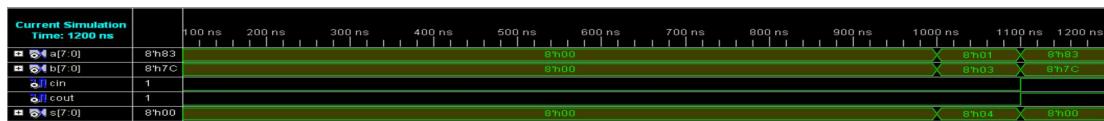
Test data:

```

Simulator is doing circuit initialization process.
Finished circuit initialization process.

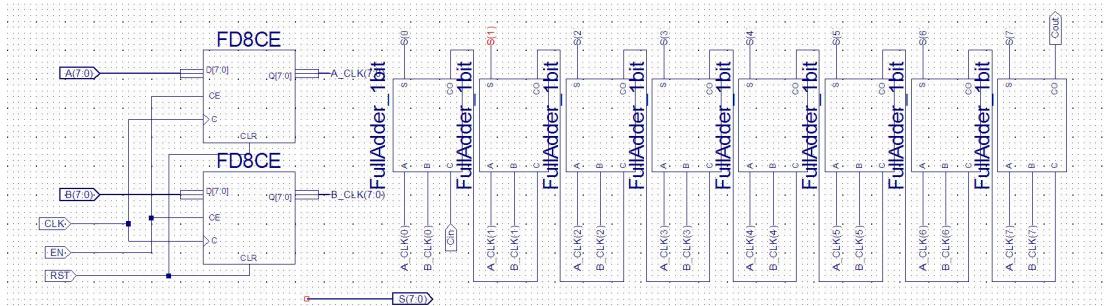
▶% put A 00000001
▶% put B 00000011
▶% put cin 0
▶% run
▶% put A 10000001
▶% put B 01111100
▶% put cin 1
▶% run
    
```

Functional waveforms:

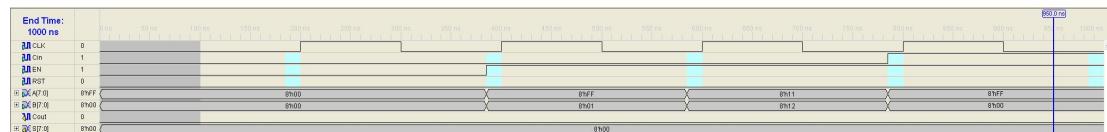


8-bit Full Adder with D Flip Flop

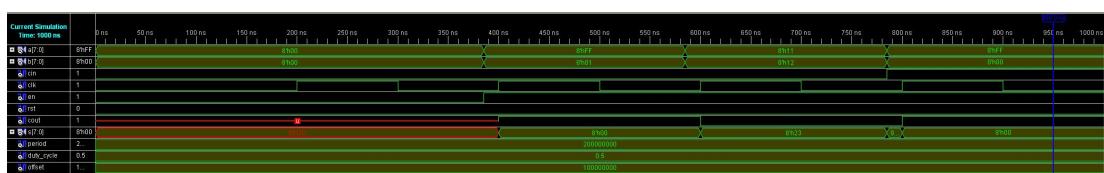
Schematic:



Test data:

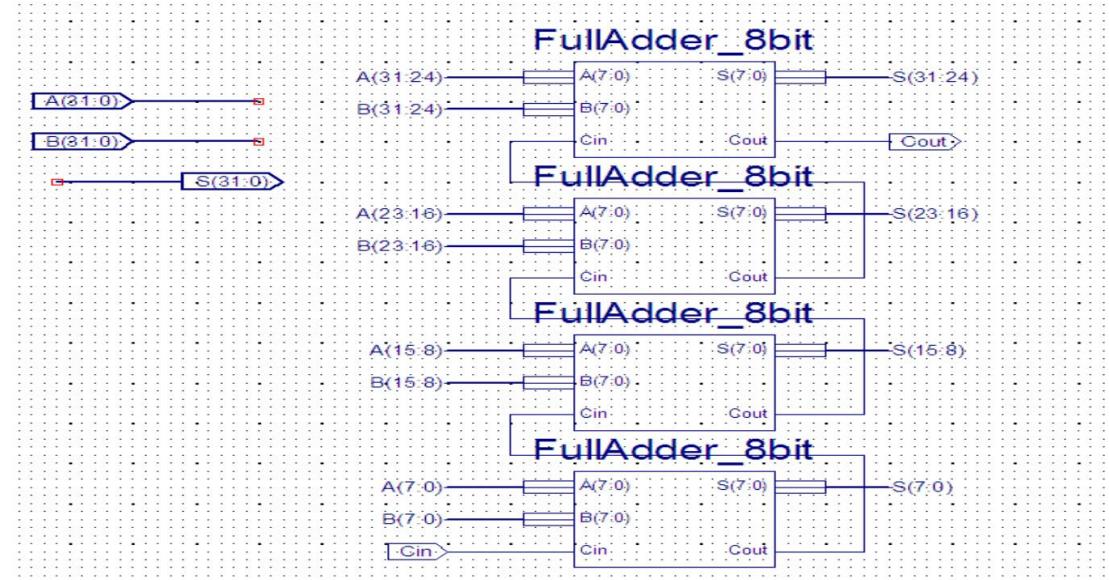


Functional waveforms:

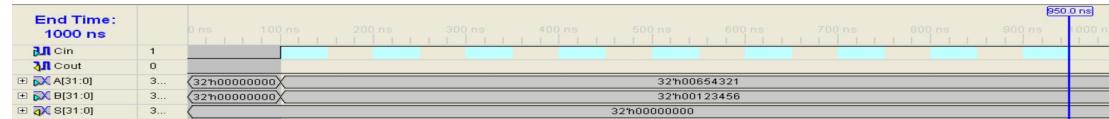


32-bit Full Adder without D Flip Flop

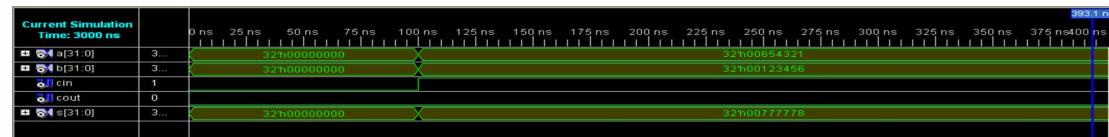
Schematic:



Test data:



Functional waveforms:

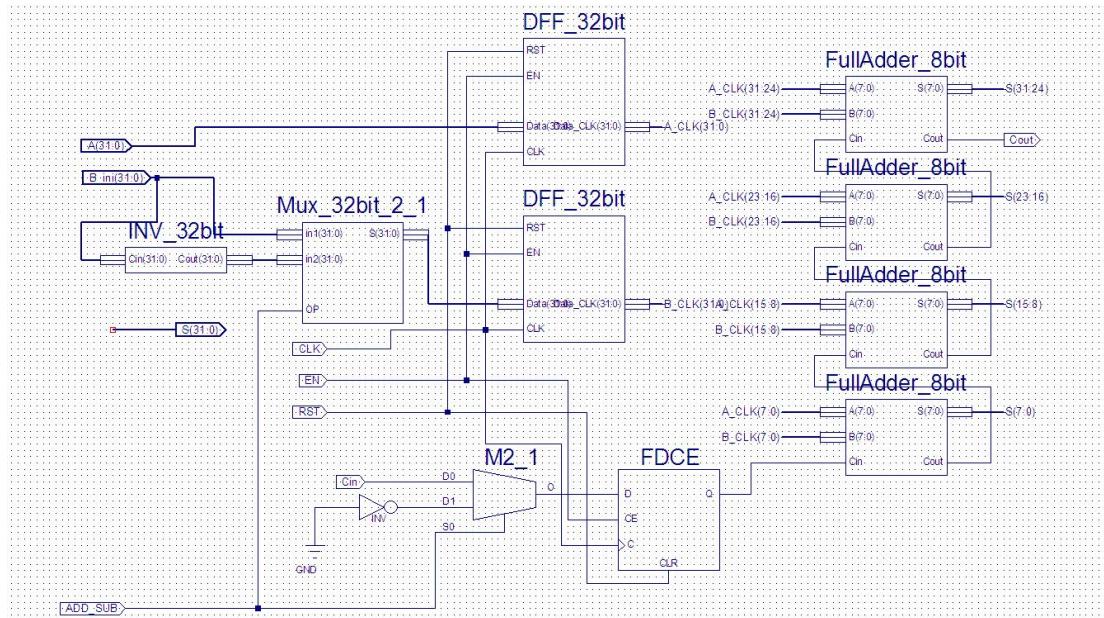


32-bit Full Adder with D Flip Flop

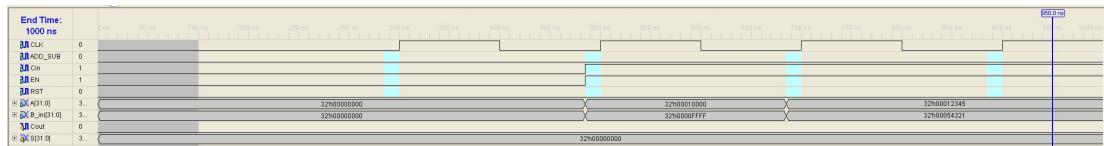
This module implements a 32-bit ripple-carry adder by cascading four 8-bit full adder blocks. The 32-bit inputs $A[31:0]$ and $B[31:0]$ are divided into four 8-bit segments. Each **FullAdder_8bit** computes the sum of its corresponding 8-bit slice. The carry-out (**Cout**) of each lower 8-bit adder is connected to the carry-in (**Cin**) of the next higher adder. The four 8-bit sum outputs are concatenated to form the final 32-bit sum $S[31:0]$. The carry-out of the most significant adder is the overall **Cout** of the 32-bit addition.

In short, the module performs 32-bit binary addition using a ripple-carry structure built from 8-bit adders.

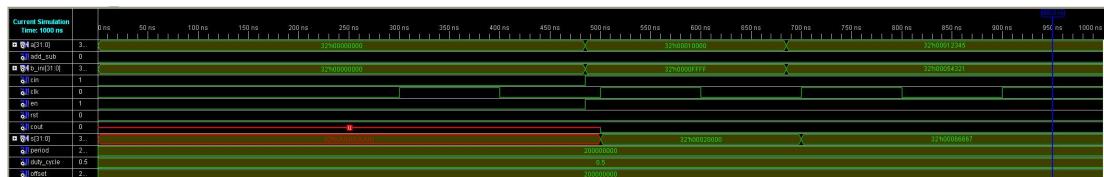
Schematic:



Test data:

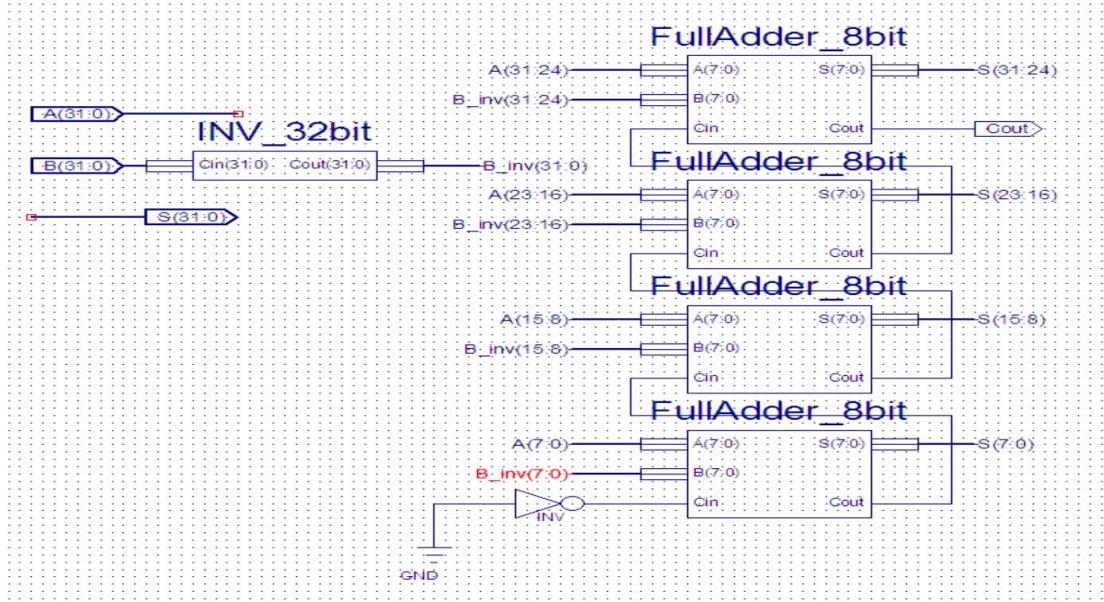


Functional waveforms:

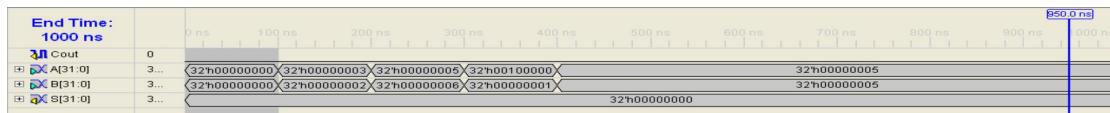


32-bit Subtractor

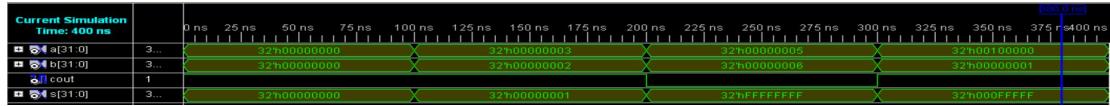
Schematic:



Test data:

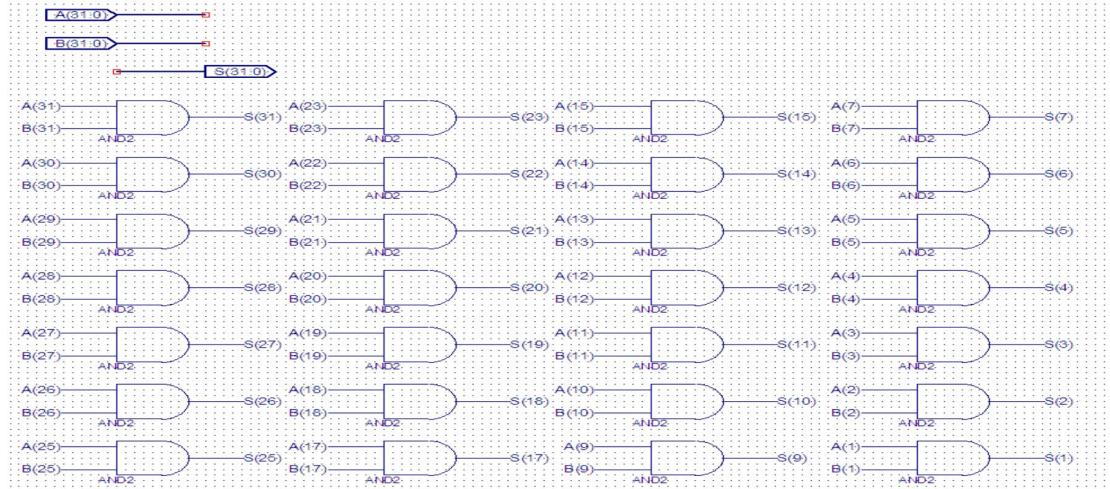


Functional waveforms:



32-bit And Gate

Schematic:



Test data:

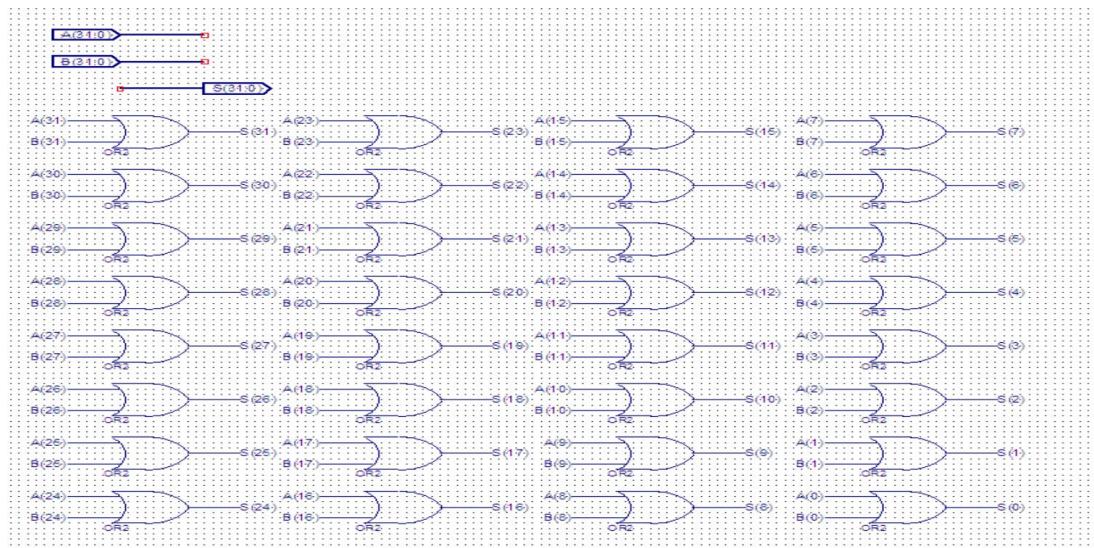


Functional waveforms:



32-bit Or Gate

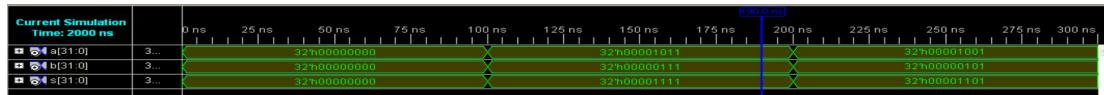
Schematic:



Test data:

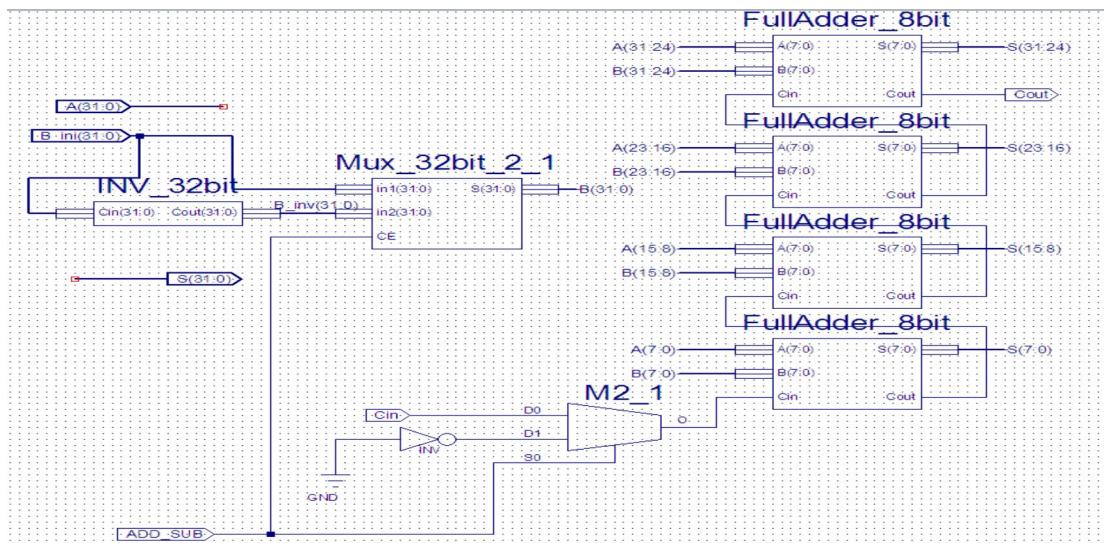


Functional waveforms:

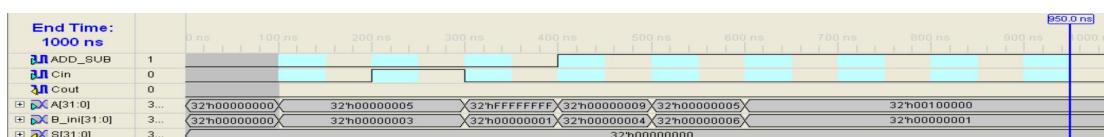


32-bit Add and Sub

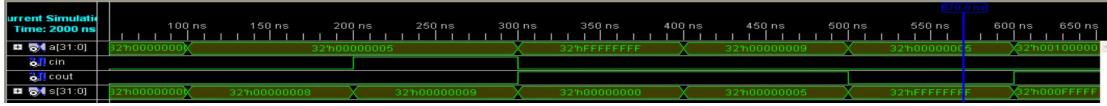
Schematic:



Test data:

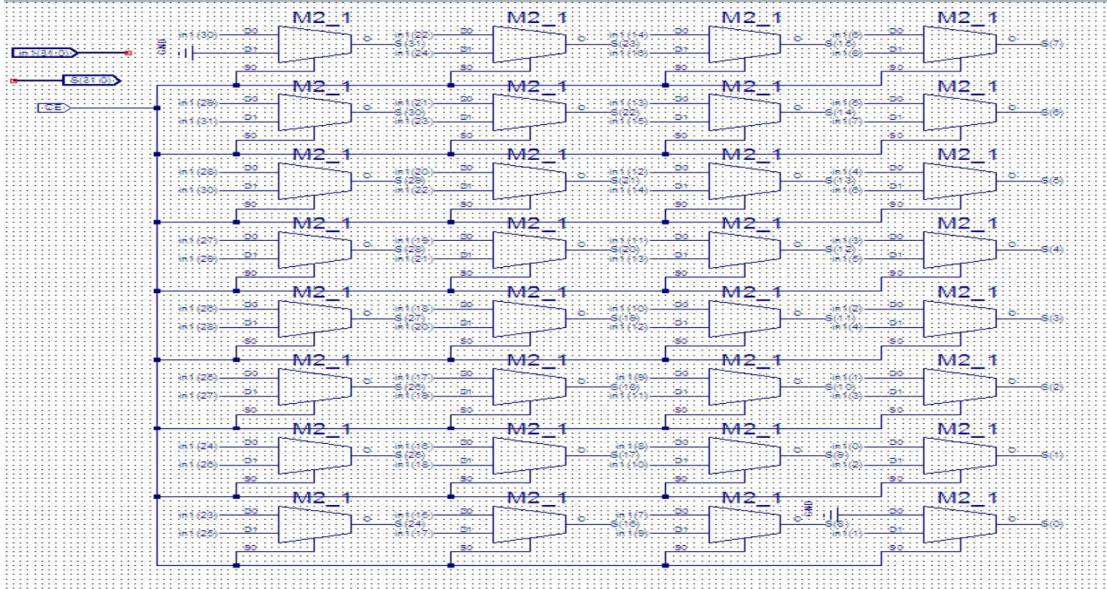


Functional waveforms:

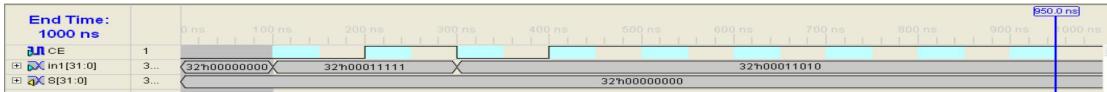


32-bit Shift

Schematic:



Test data:



Functional waveforms:

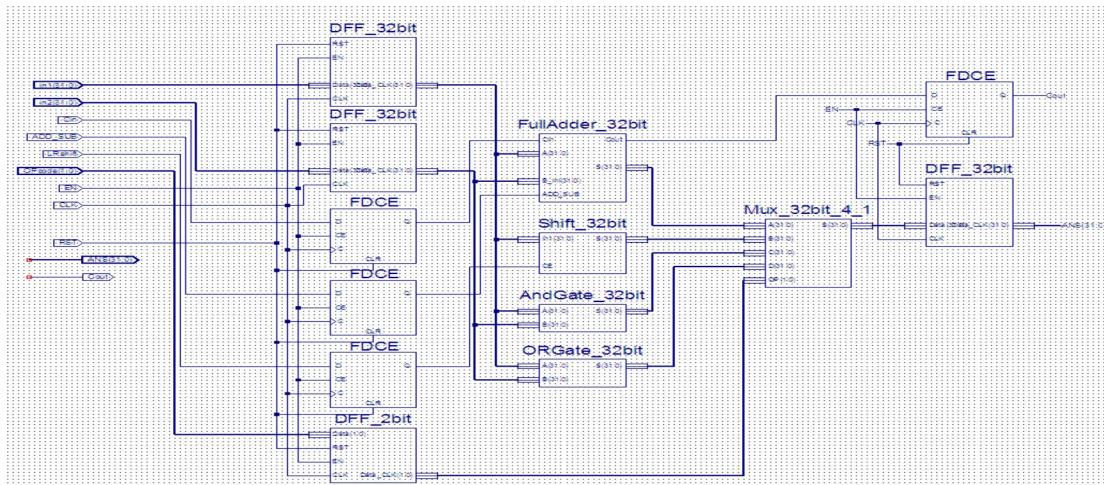


32-bit ALU with D Flip Flop

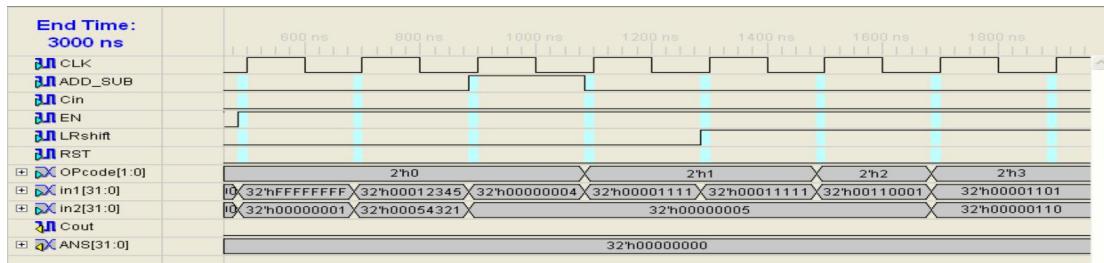
Module Function Description:

This module implements a 32-bit Arithmetic Logic Unit (ALU). Two 32-bit input operands are first registered using flip-flops to ensure stable and synchronous operation. Based on the control signals, the ALU performs different operations, including 32-bit addition or subtraction, logical left or right shifts, bitwise AND, and bitwise OR. The outputs of these functional units are connected to a 4-to-1 multiplexer, which selects the final result according to the opcode. The selected result is then stored in an output register and provided as a 32-bit output.

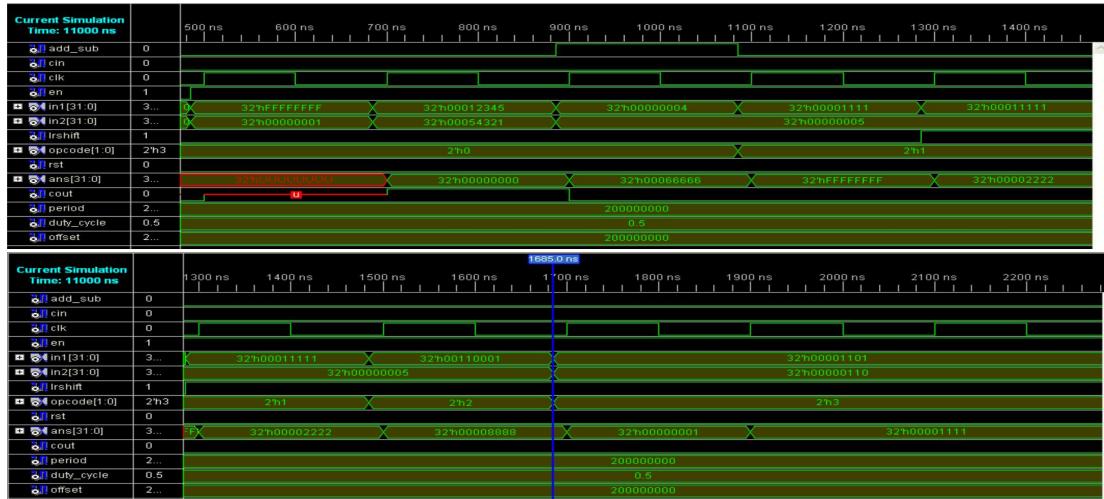
Schematic:



Test data:



Functional waveforms:



32-bit ALU Utilization

EE533-lab2 Project Status (01/24/2026 - 17:30:02)					
Project File:	EE533-lab2.ise	Current State:	Placed and Routed		
Module Name:	ALU_32bit	• Errors:	No Errors		
Target Device:	xc3s700a-4fg484	• Warnings:	No Warnings		
Product Version:	ISE 10.1 - Foundation Simulator	• Routing Results:	All Signals Completely Routed		
Design Goal:	Balanced	• Timing Constraints:	All Constraints Met		
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	0 [Timing Report]		

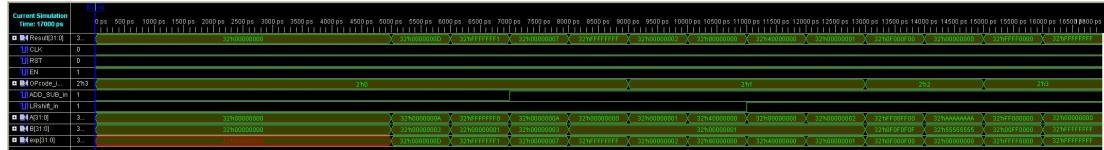
EE533-lab2 Partition Summary			
No partition information was found.			

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	102	11,776	1%
Number of 4 input LUTs	190	11,776	1%
Logic Distribution			
Number of occupied Slices	131	5,888	2%
Number of Slices containing only related logic	131	131	100%
Number of Slices containing unrelated logic	0	131	0%
Total Number of 4 input LUTs	190	11,776	1%
Number of bonded IOBs	105	372	28%
Number of BUFGMUXs	1	24	4%

Performance Summary			
Final Timing Score:	0	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Verilog

Functional waveforms:



Test Result:

```

Simulator is doing circuit initialization process.
Finished circuit initialization process.
? PASS | OP=00 A=0000000a B=00000003 | Result=0000000d
? PASS | OP=00 A=fffffff0 B=00000001 | Result=ffffffff1
? PASS | OP=00 A=0000000a B=00000003 | Result=00000007
? PASS | OP=00 A=00000000 B=00000001 | Result=fffffffff
? PASS | OP=01 A=00000001 B=00000001 | Result=00000002
? PASS | OP=01 A=40000000 B=00000001 | Result=80000000
? PASS | OP=01 A=80000000 B=00000001 | Result=40000000
? PASS | OP=01 A=00000002 B=00000001 | Result=00000001
? PASS | OP=10 A=ffffff00 B=0ff0f0f0f | Result=0f000f00
? PASS | OP=10 A=aaaaaaaa B=55555555 | Result=00000000
? PASS | OP=11 A=00000000 B=0ffff0000 | Result=ffff0000
? PASS | OP=11 A=00000000 B=f0fffff | Result=f0fffff
?? All tests finished.
Stopped at time : 17.000 ns : File "C:/Documents and Settings/student/EE533-lab2/EE533verilog/tb_ALU.v" Line 159
Stopped at line=159 file name=C:/Documents and Settings/student/EE533-lab2/EE533verilog/tb_ALU.v
:

```

Verilog Utilization:

EE533verilog Project Status					
Project File:	EE533verilog.ise	Current State:	Placed and Routed		
Module Name:	ALU02	• Errors:	No Errors		
Target Device:	xc3s700a-4fg484	• Warnings:	5Warnings		
Product Version:	ISE 10.1 - Foundation Simulator	• Routing Results:	All Signals Completely Routed		
Design Goal:	Balanced	• Timing Constraints:	All Constraints Met		
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	0 [Timing Report]		

EE533verilog Partition Summary			
No partition information was found.			

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	126	11,776	1%
Logic Distribution			
Number of occupied Slices	63	5,888	1%
Number of Slices containing only related logic	63	63	100%
Number of Slices containing unrelated logic	0	63	0%
Total Number of 4 input LUTs	126	11,776	1%
Number of bonded IOBs	100	372	26%

Performance Summary			
Final Timing Score:	0	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Gate Count Comparison with Schematic Designs

Compared with schematic-based implementations, Verilog-based designs typically use the same or fewer logic gates. This is because synthesis tools can automatically optimize the circuit by eliminating redundant logic and efficiently mapping the design onto the FPGA's lookup tables (LUTs). In contrast, schematic designs depend largely on manual construction, which limits optimization potential and often results in unnecessary or duplicated logic. As a result, Verilog implementations are generally more compact and make more efficient use of hardware resources.