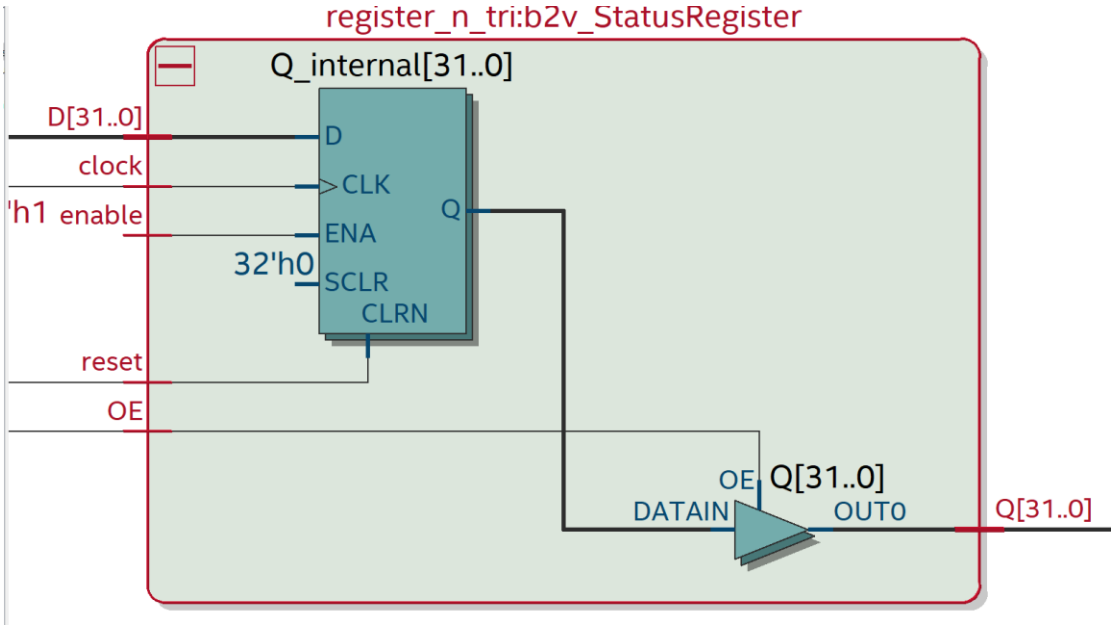
UART Status Register

The design of the Status Register features a 32-bit register, Q_internal, and uses an always @(*) block triggered by the rising edges of Reset and Clock. Upon the rising edge of Reset, Q_internal is reset to 0. Otherwise, If the enable signal is 1, Q_internal is set to the value D. Concurrently, the output Q is set to the value of Q_internal when OE is 1; otherwise, Q is assigned a high-impedance value of 32 z's.

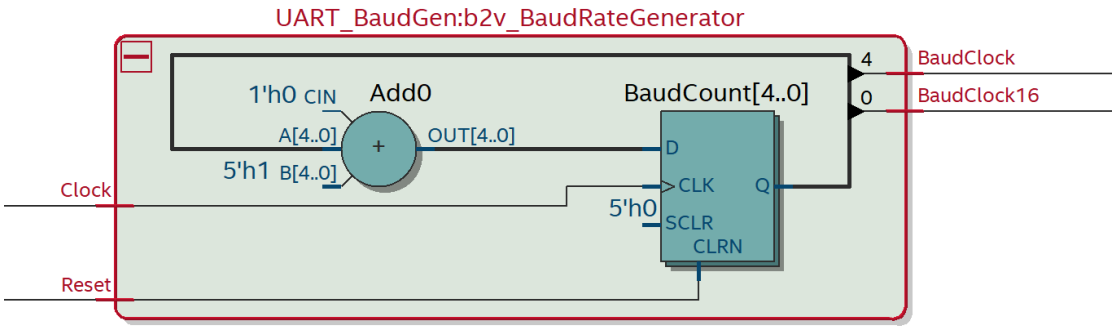
Synthesized Schematic:



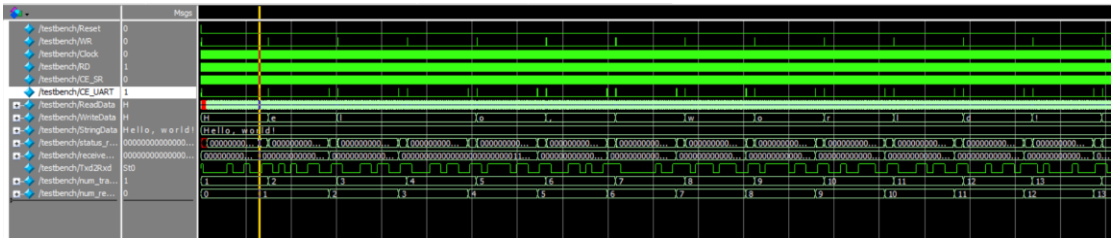
UART Baud Clock Generator

The design of the Baud Clock Generator includes a 5-bit register, BaudCount, and also employs an always @(*) block triggered by the rising edges of Reset and Clock. On the rising edge of Reset, BaudCount is reset to 0. If not, BaudCount is incremented by 1. Concurrently, the output BaudClock is set to the MSB of the register BaudCount, BaudCount[4], and the output BaudClock16 is set to the LSB of the register BaudCount, BaudCount[0].

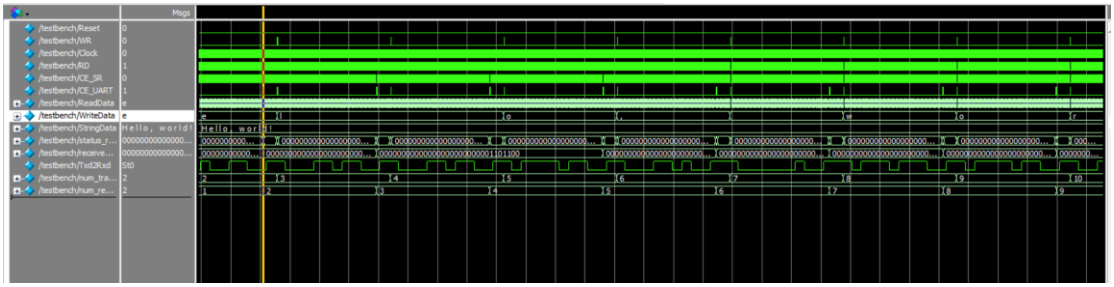
Synthesized Schematic:



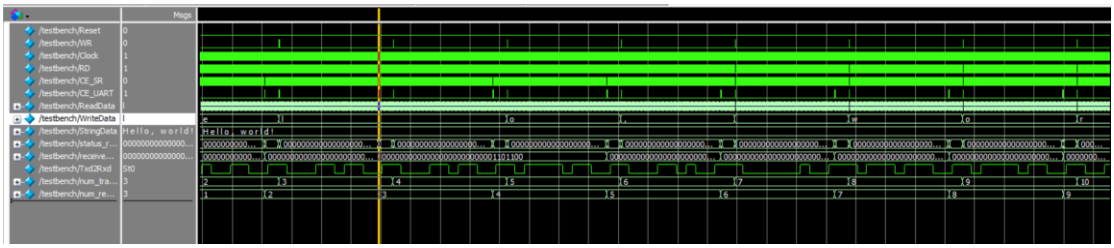
Testbench Result for H:



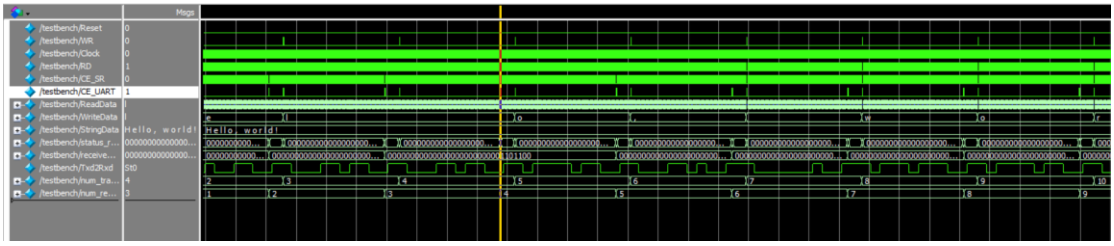
Testbench Result for e:



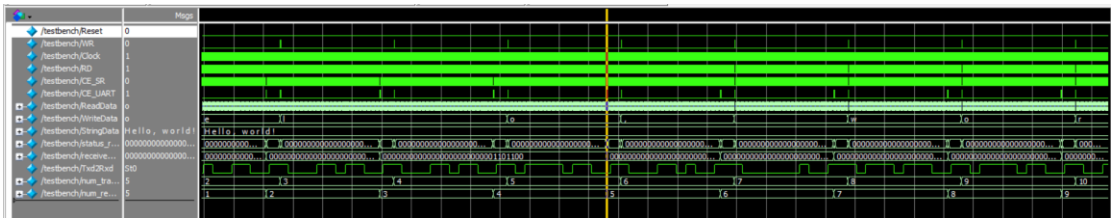
Testbench Result for l:



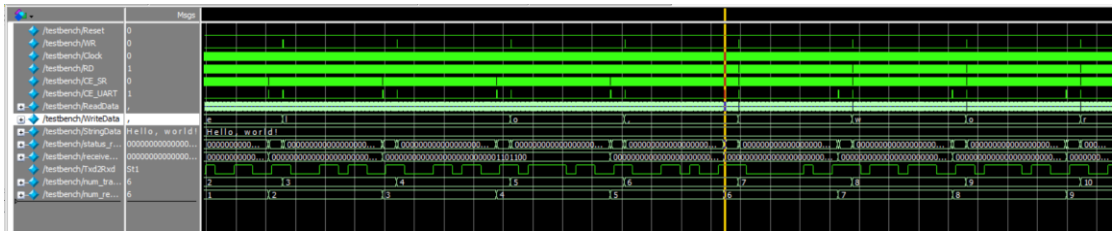
Testbench Result for l:



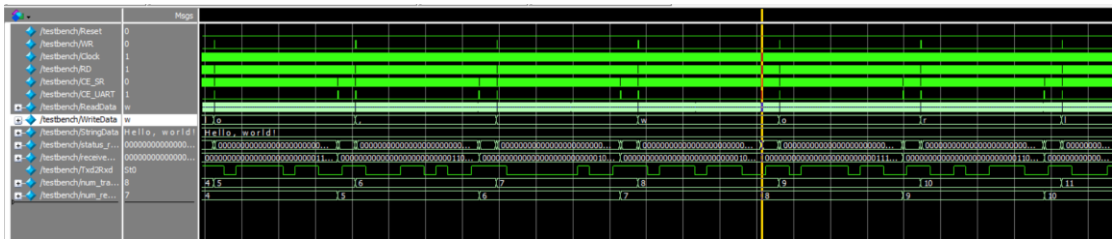
Testbench Result for o:



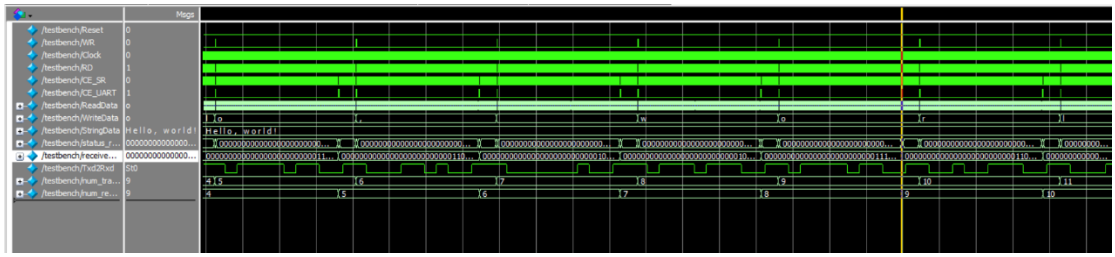
Testbench Result for ,:



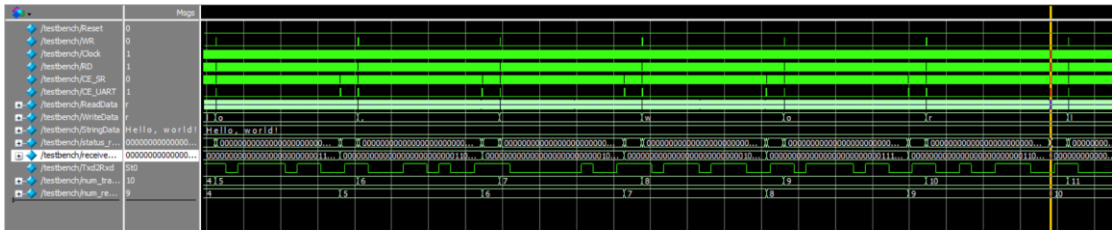
Testbench Result for w:



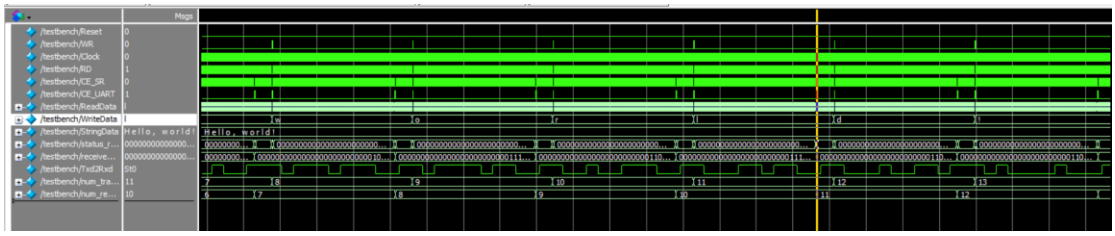
Testbench Result for o:



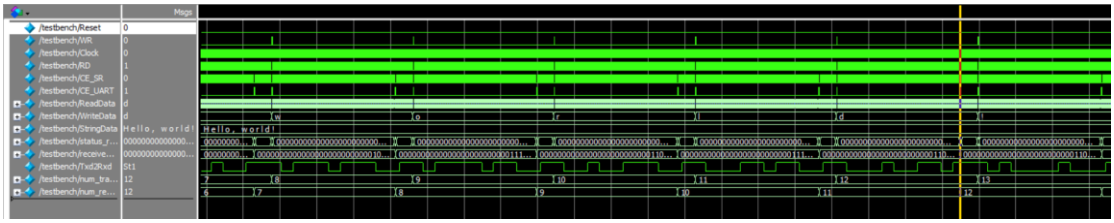
Testbench Result for r:



Testbench Result for l:



Testbench Result for d:



Testbench Result for !: