COMPUTER ORGANIZATION

COURSE CODE: 20CA3103 **L T P C**

3 0 0 3

Course Outcomes: At the end of the course, the student will be able to

CO1: Discuss basic structure and organization of computers

CO2: Apply fixed and floating point arithmetic algorithms.

CO3: Explain micro operations and input/output organization.

CO4: Explain pipeline and Parallel Processors.

CO5: Discuss about memory design and memory organizations.

UNIT-I **(10 Lectures)**

Functional blocks of a computer

CPU, memory, input-output subsystems, control unit.lnstruction set architecture of a CPU: registers, instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.

Learning outcomes: At the end of this unit, the student will be able to

1. understand the basic principles of Computer Systems. (L2)
2. summarize various addressing modes for a Processor. (L2)
3. describe Instruction Execution cycle. (L2)

UNIT-II **(10 Lectures)**

Data representation

Signed number representation, fixed and floating point representations, character representation. Computer arithmetic: integer addition and subtraction, ripple carry adder, carry look-ahead adder, multiplication — shift-and add, Booth multiplier, carry save multiplier, Division restoring and non-restoring techniques, Division Techniques, floating point arithmetic.

Learning outcomes: At the end of this unit, the student will be able to

l .understand various Data Representations. (L2)

2. summarize various Arithmetic Algorithms for fixed point Representation. (L2)
3. describe various Arithmetic Algorithms for floating Point Arithmetic. (L2)

UNIT-III **(10 Lectures)**

CPU control unit design

Hardwired and microprogrammed design approaches, Peripheral devices and their characteristics: Input-output subsystems, I/O device interface, I/O transfers: program controlled, interrupt driven and DMA, privileged and non-privileged instructions, software interrupts and exceptions. Programs and processes, Interrupt driven I/O, I/O device interfaces Serial Communication, asynchronous data transfer.

Learning outcomes: At the end of this unit, the student will be able to

1. describe knowledge on micro programming. (L2)
2. understand principles of I/O devices are accessed. (L2)
3. understand various data Transfers. (L2)

UNIT-IV (**10 Lectures)**

Pipelining: Basic concepts of pipelining, throughput and speedup, pipeline hazards.Parallel Processors: Introduction to parallel processors, Concurrent access to memory and cache coherency, Flynns Classification.

Learning outcomes: At the end of this unit, the student will be able to

l .understand concepts of pipelining. (L2)
2. discuss concepts of Parallel Processors. (L2)
3. understand concepts of Multiprocessors. (L2)

UNIT-V **(10 Lectures)**

Memory system design:

Semiconductor memory technologies, Memory organization: Memory interleaving, concept of hierarchical memory organization, cache memory, cache size vs. block size, mapping functions, replacement algorithms, write policies.

Learning outcomes: At the end of this unit, the student will be able to

1. understand memory system design(L2)
2. explain the concept of hierarchical memory organization(L2)
3. explain the concept of Cache Memory(L2)

TEXT BOOK:

1. M. Moris Mano, *"Computer Systems Architecture*", 3rd Edition, Pearson Education, 2007.

REFERENCE BOOKS:

l . John P. Hayes, *"Computer Architecture and Organization*", 3rd Edition, WCB/McGraw-Hill
2. William Stallings, *"Computer Organization and Architecture: Designing for Performance*", 10th Edition, Pearson Education, 2015.
3. Vincent P. Heuring and Harry F. Jordan, *"Computer System Design and Architecture*", 2nd Edition, Pearson Education.
4. David A. Patterson and John L. Hennessy, *"Computer Organization and Design: The Hardware/Software Interface*", 5th Edition, Elsevier.
5. Carl Hamacher, ZvonkoVranesic, SafwatZaky, NaraigManjikian, *"Computer Organization and Embedded Systems"*, 6th Edition, McGraw Hill Higher Education, 2012.