Spiderchip64

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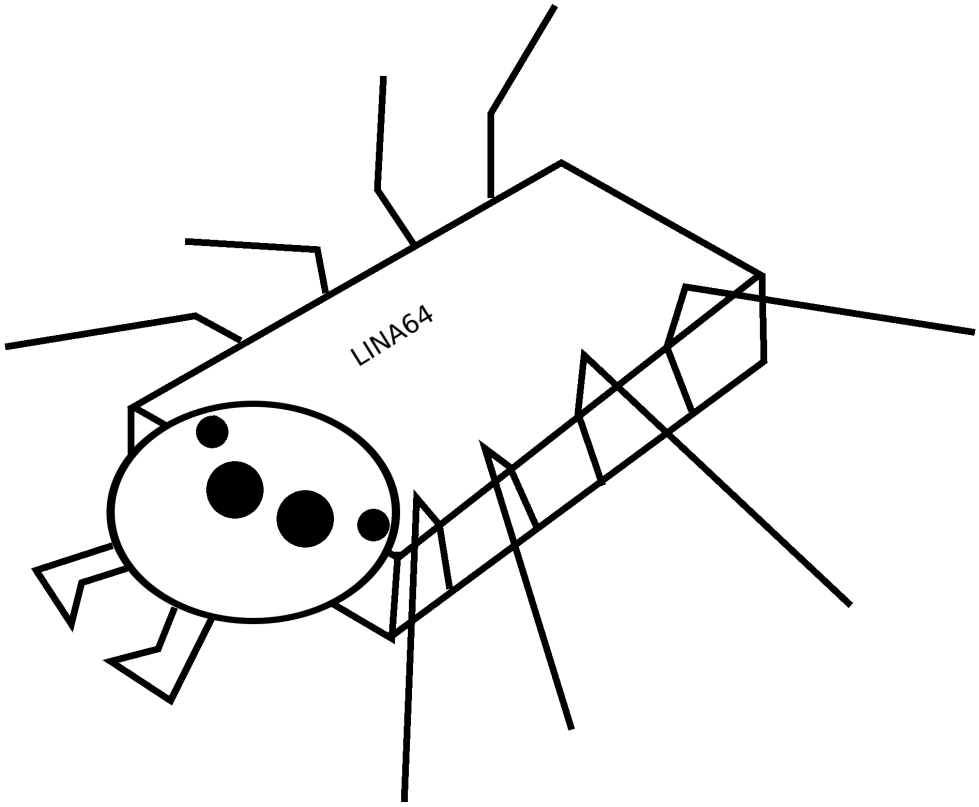

Spiderchip64 is a 64 bits little endian ISA. This ISA tries to apply the KISS principle and also tries to respect the Popek and Goldberg virtualization requirement. Also, this CPU will include atomic memory operation for a multi-core version. So Spiderchip64 is a RISC ISA. Spiderchip64 has a 64 bits-wide data bus, a 64 bits-wide address bus, two sets of 31 64 bits-wide registers for a total of 47 registers, plus a zero register. There is also a status register and a saved status register. One set of register is used by the user's program and the other set is reserved for fast interrupt handling or for the supervisor usage. The instruction word is 32 bit wide.

Summary

- RISC ISA
- applies the KISS principle
- respects the Popek and Goldberg virtualization requirement
- have atomic memory operations
- 64 bits or less address bus (more than you will ever need (16 EiB))
- 64 bits data bus
- 64 bits registers
- 32 bits instruction word
- 15 registers shared between the user and the supervisor
- 16 registers are user specific and 16 registers are supervisor specific
- 32 registers visible at the same time (including a zero register)
- one address space for everything (Von Neumann architecture with I/O mapped in memory)
- "user" and "supervisor" mode
- one instruction per clock cycle if the architecture is pipelined (excluding memory instructions especially if the memory is slow)
- SIMD instructions on 2 words, 4 half-words or 8 bytes
- free and open source

Notes :

- This ISA is intended to be implemented the first time on a FPGA development board (Arduino MKR Vidor 4000, with an Intel Cyclone 10)
- I am aware that Intel Quartus is not free software. I am searching a FOSS FPGA "compiler" and FOSS-friendly FPGA board

- This is just an ISA for the CPU part of a computer. So it doesn't have and doesn't specify a MMU, a FPU, a GPU, a cache, a PIC, or an I/O controller. However, some of these elements will be on the FPGA SoC.
- In the first version of this ISA, there won't be double instructions.

Glossary of the acronyms :

CPU : Central Processing Unit

FPGA : Field Programmable Gate Array

FPU : Floating Point Unit

FOSS : Free and Open Sourced Software

GPU : Graphical Processing Unit

I/O : Input / Output

ISA : Instruction Set Architecture

KISS : Keep It Simple Stupid

MIMD : Multiple Instruction Multiple Data

MMU : Memory Management Unit

PIC : Programmable Interrupt Controller

RISC : Reduced Instruction Set Computing

SoC : System On Chip