

Latch: Outputs Will Change Whenever the inputs Change

Flip flop: Outputs Will Change When there is a Clock pulse, and will therefore need a clock.

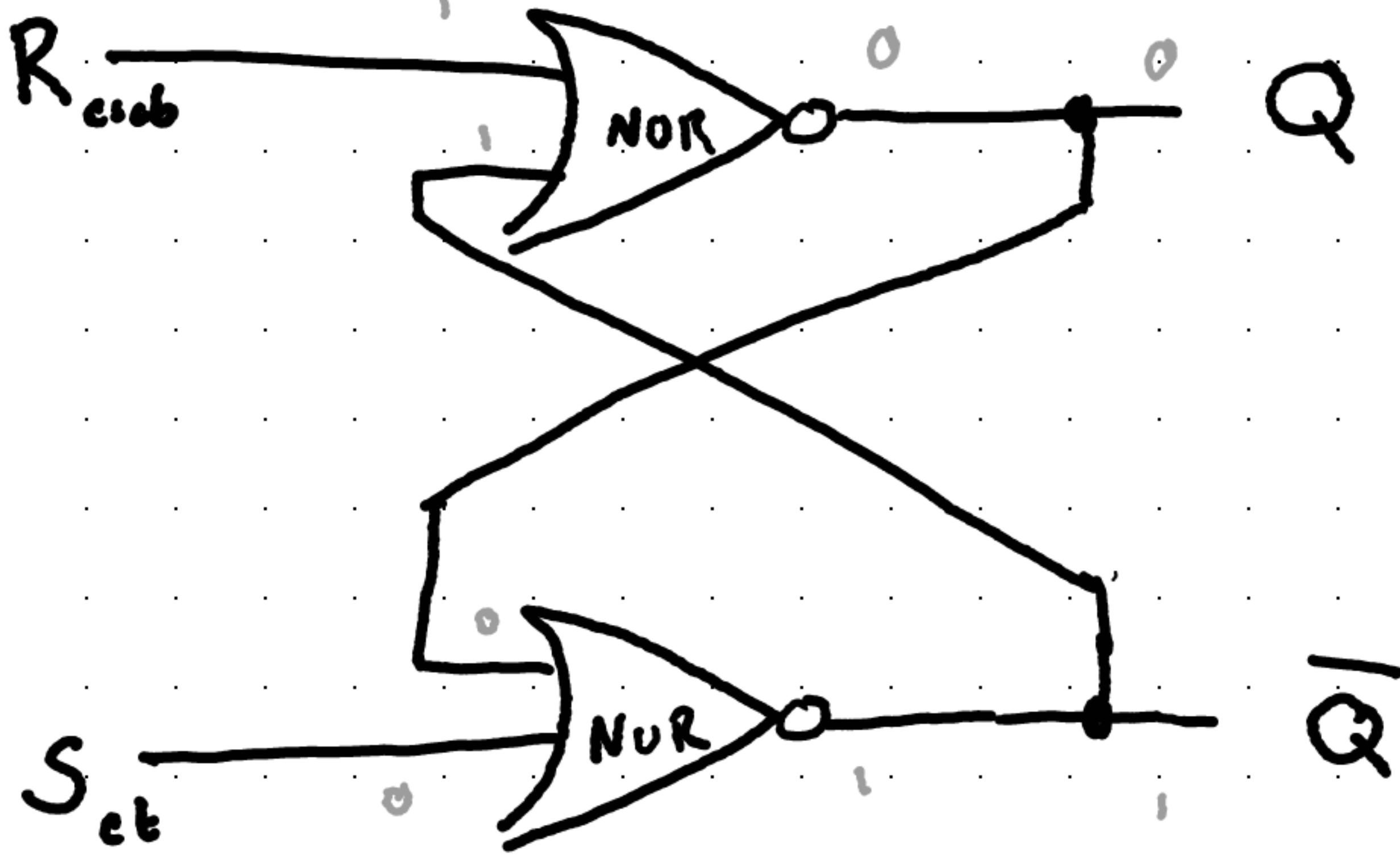
ASync Inputs:

All latches have the possibility of having Asynchronous inputs, which don't require a clock signal to update

Typically:

Clear: Clears Element to Zero

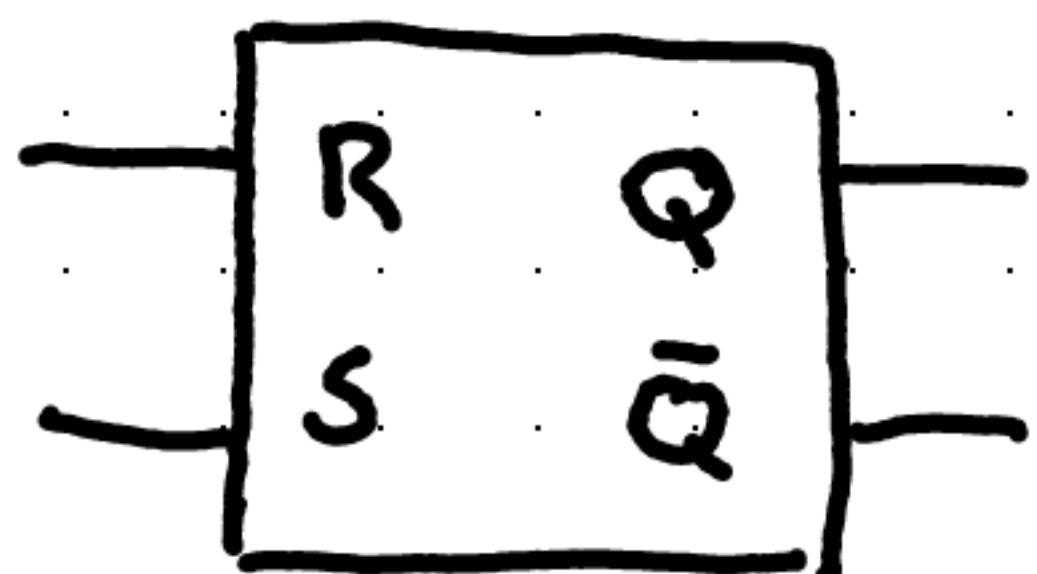
Set : Sets Q to One



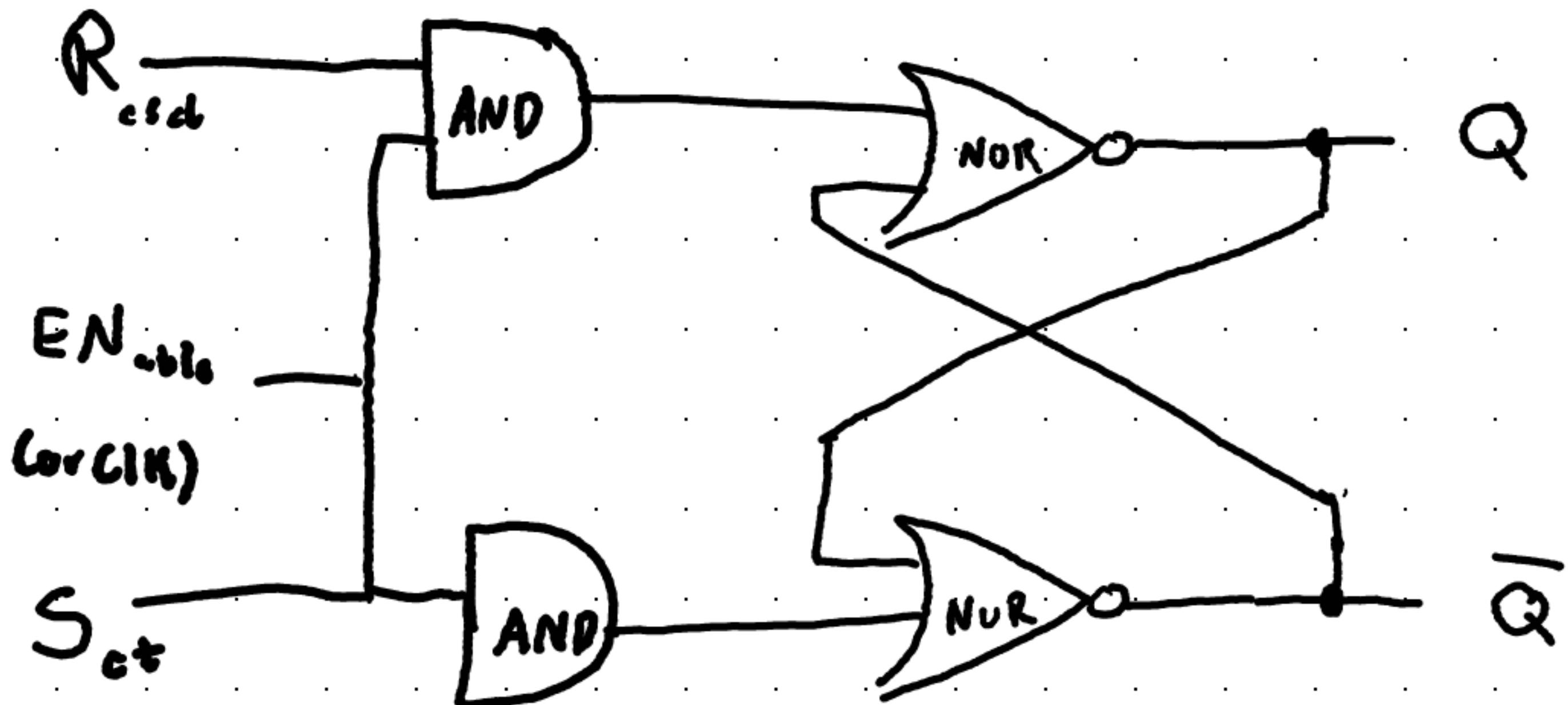
S-R Latch

Set in either \bar{Q} or Q.

Typically, one cares about Storing Q, not so much \bar{Q} .



Memory Element

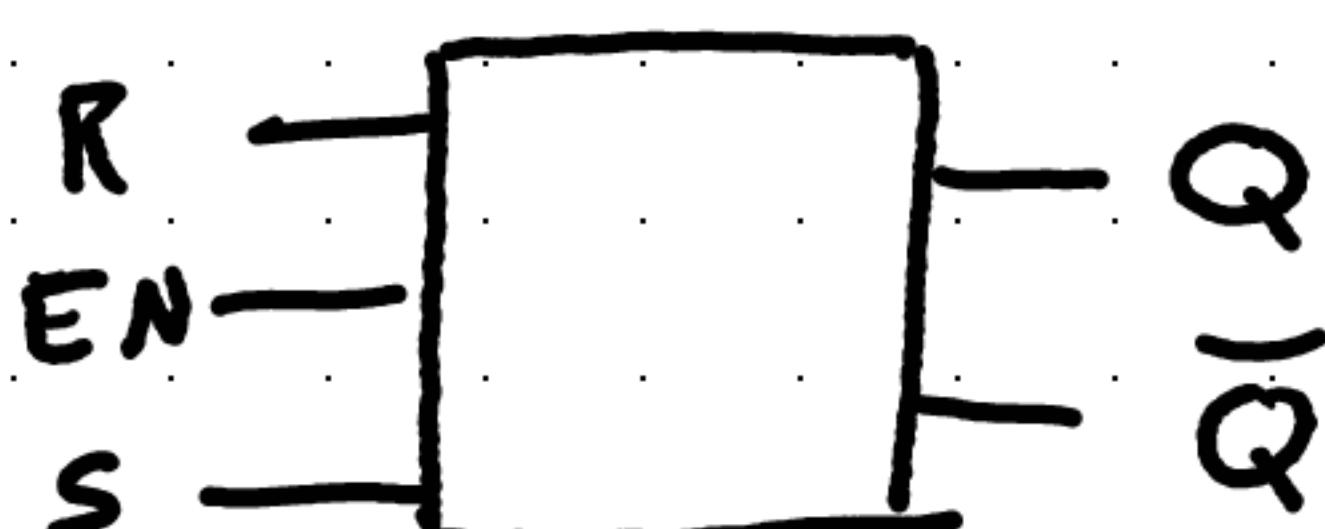


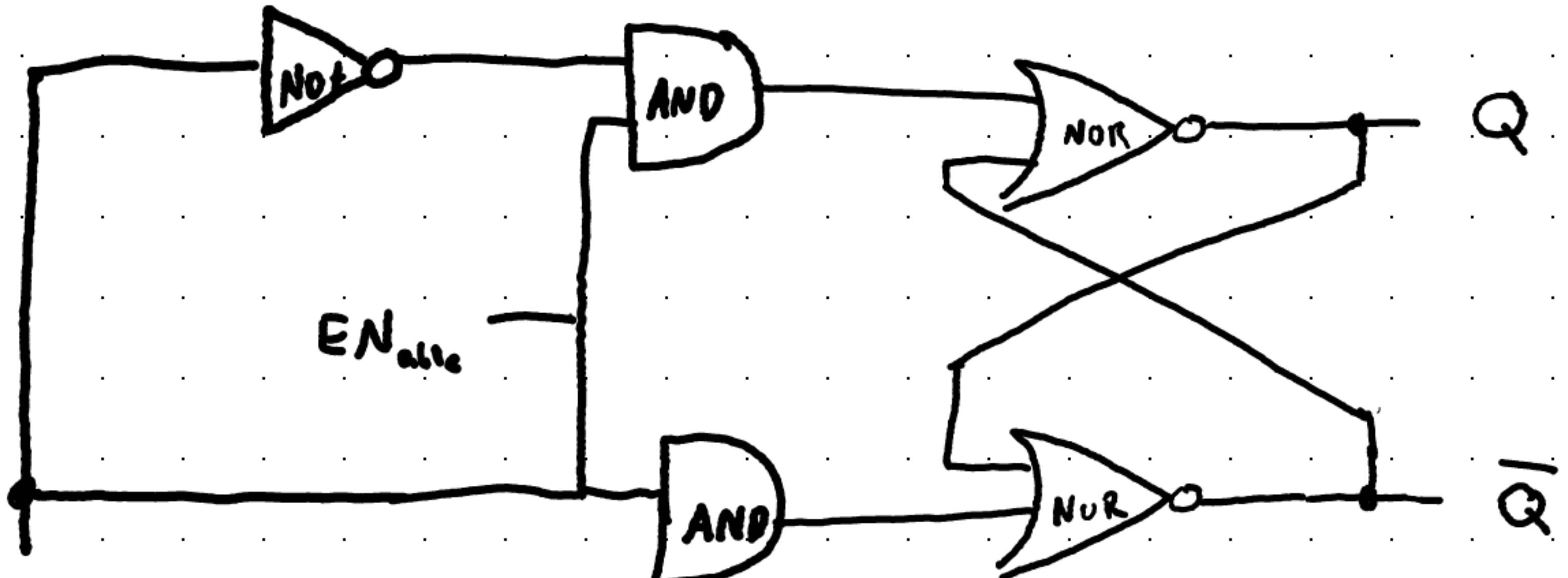
→ OR F-F with clock

S-R Latch with enable

Enable must be "pushed" or "high" to have any inputs register. All future enables require the same. We can store one bit with these latches.

- 1) The Set=0, Reset=0 condition must be avoided
- 2) If S or R change state while EN is high the correct latching action may not occur





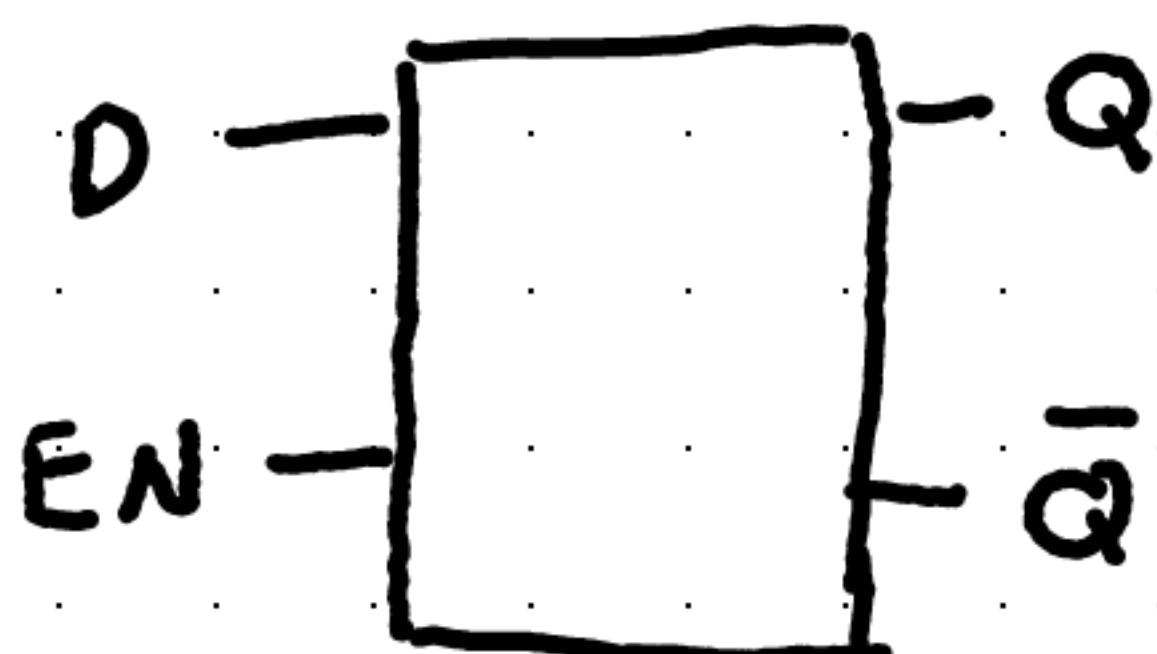
D_{in}

D Latch

Single input toggle latch with memory.

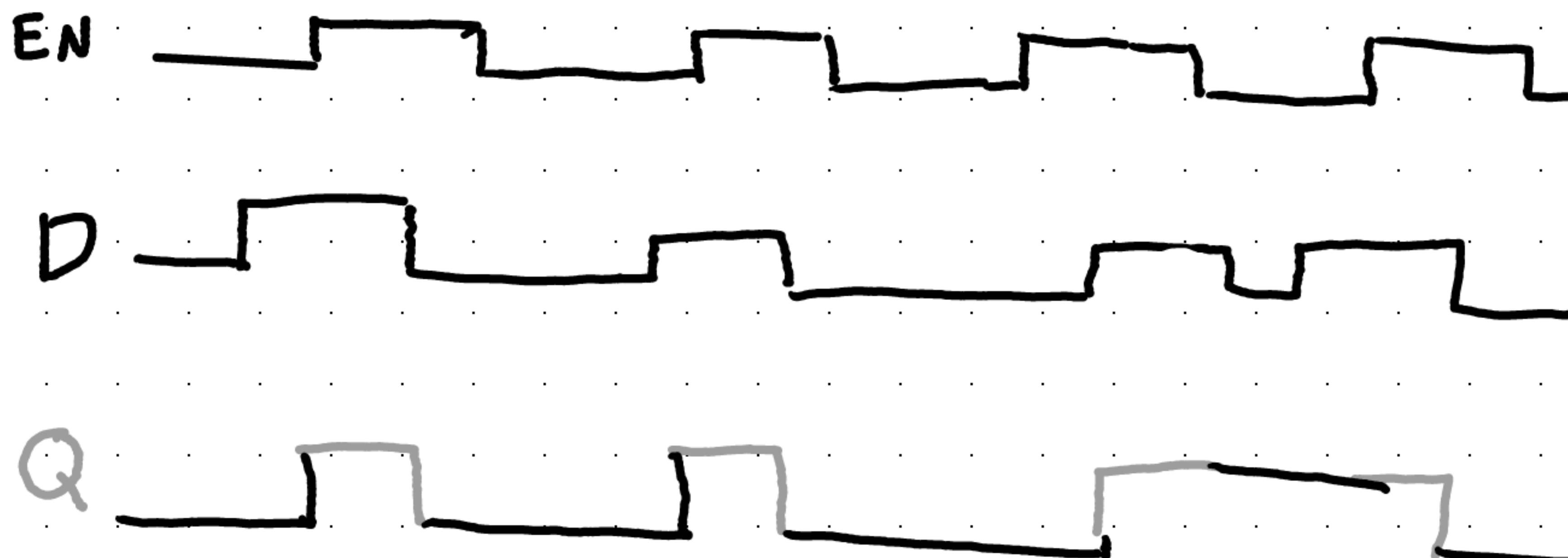
Extra Enable logic needed for the memory aspect of the latch

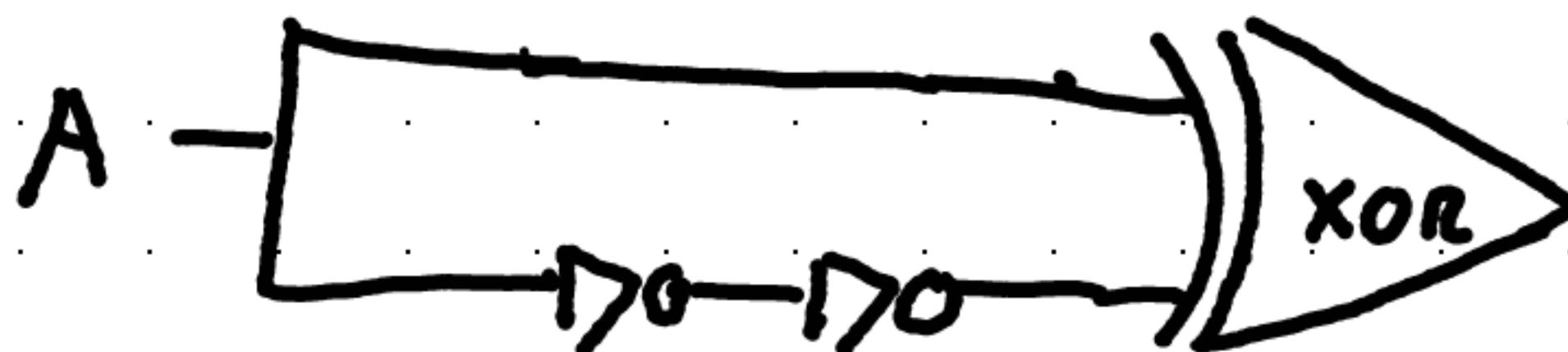
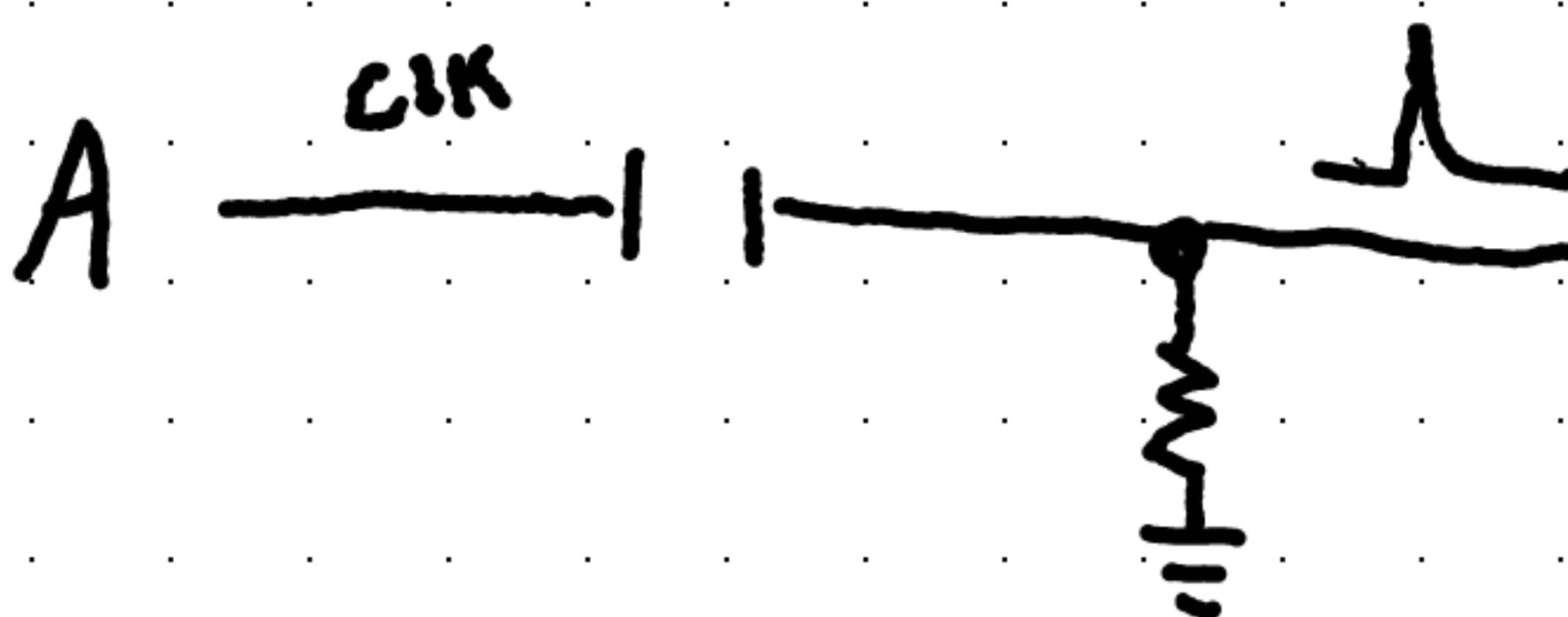
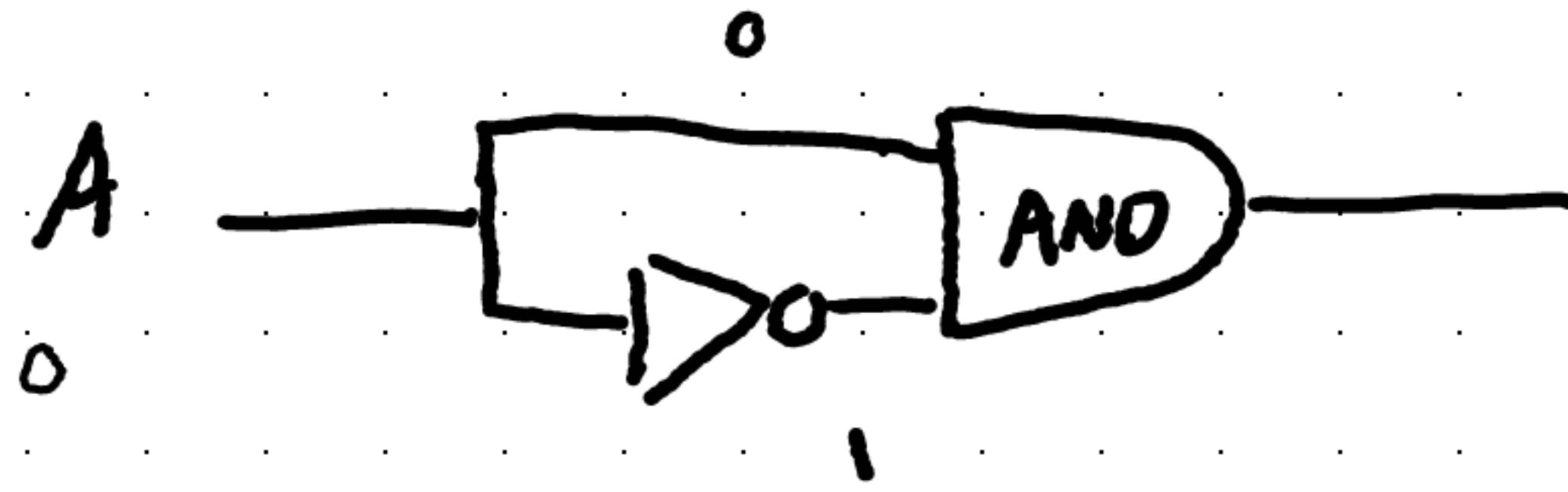
If enable is always held, by pushing D, it will just toggle Q. To "Set" Q, one must hold enable and push D, and then let go of enable before letting go of D. It won't be able to update back



"Style Bit of
Data Latch"

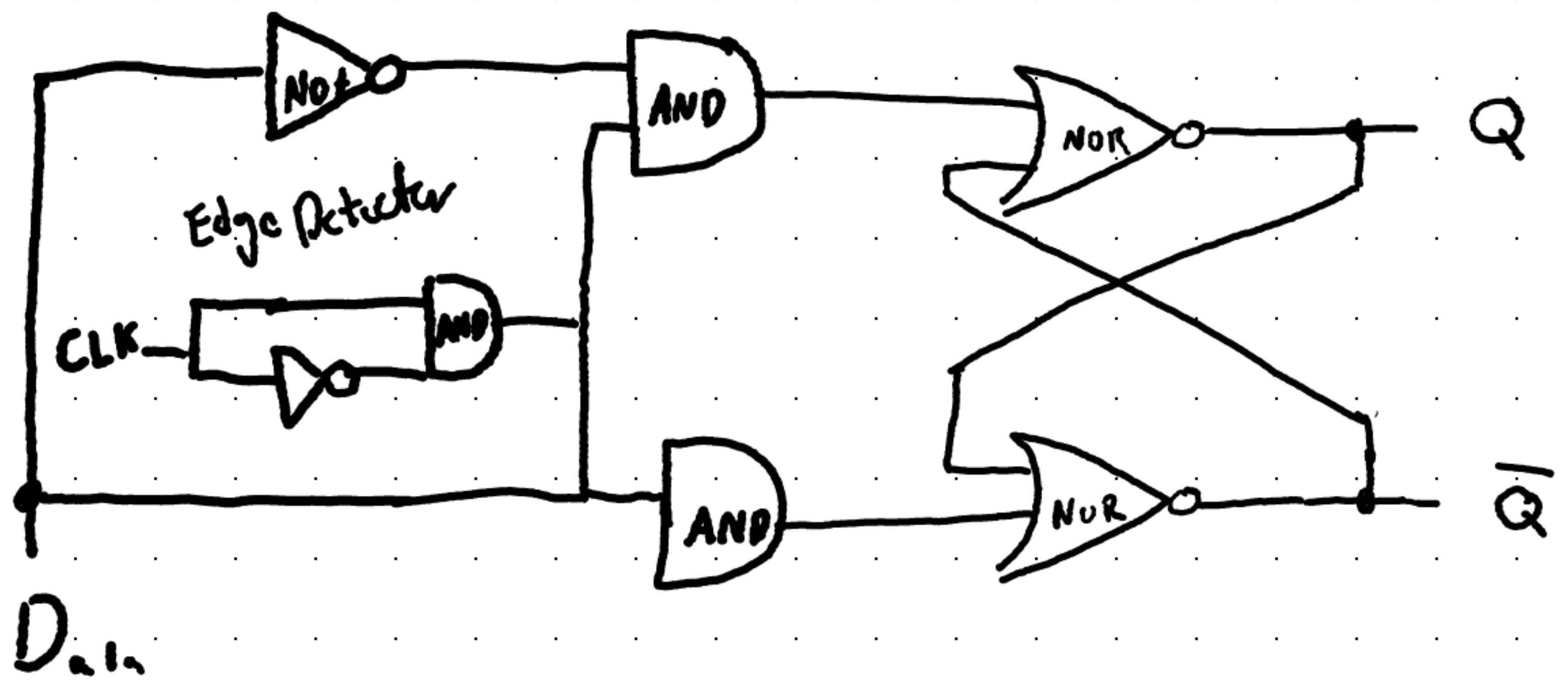
D Latch Simulation





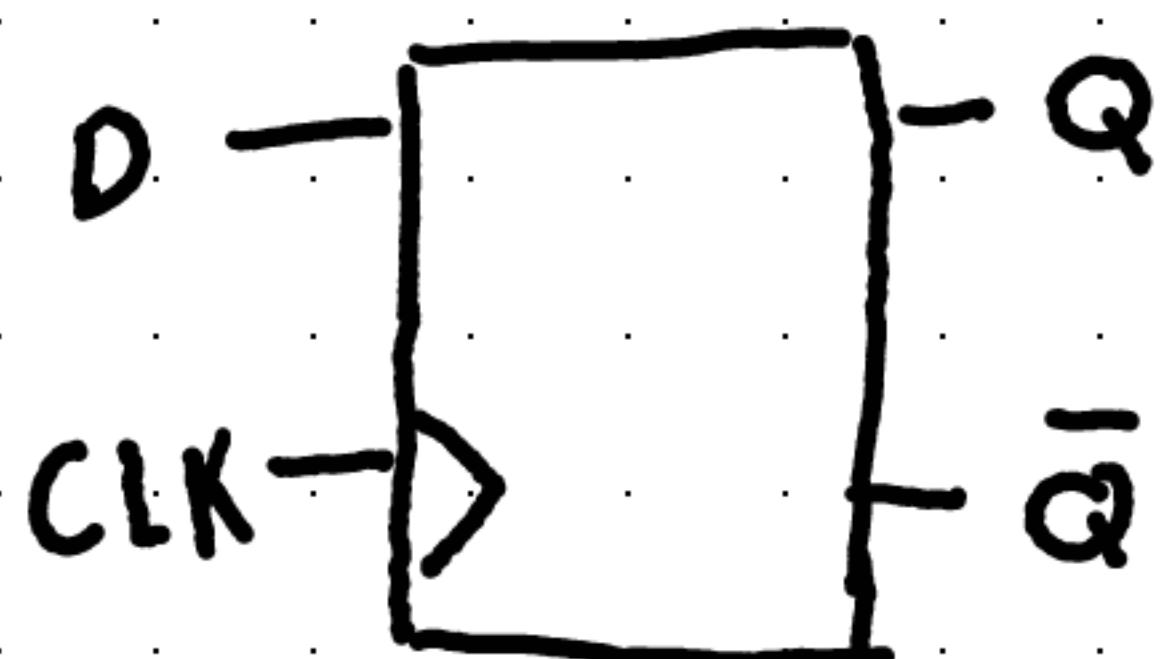
Edge-Dictator circuit

One may ask, when would this ever be on?
 In the instant that A switches on, both will
 be high due to the delay of the NOT gate

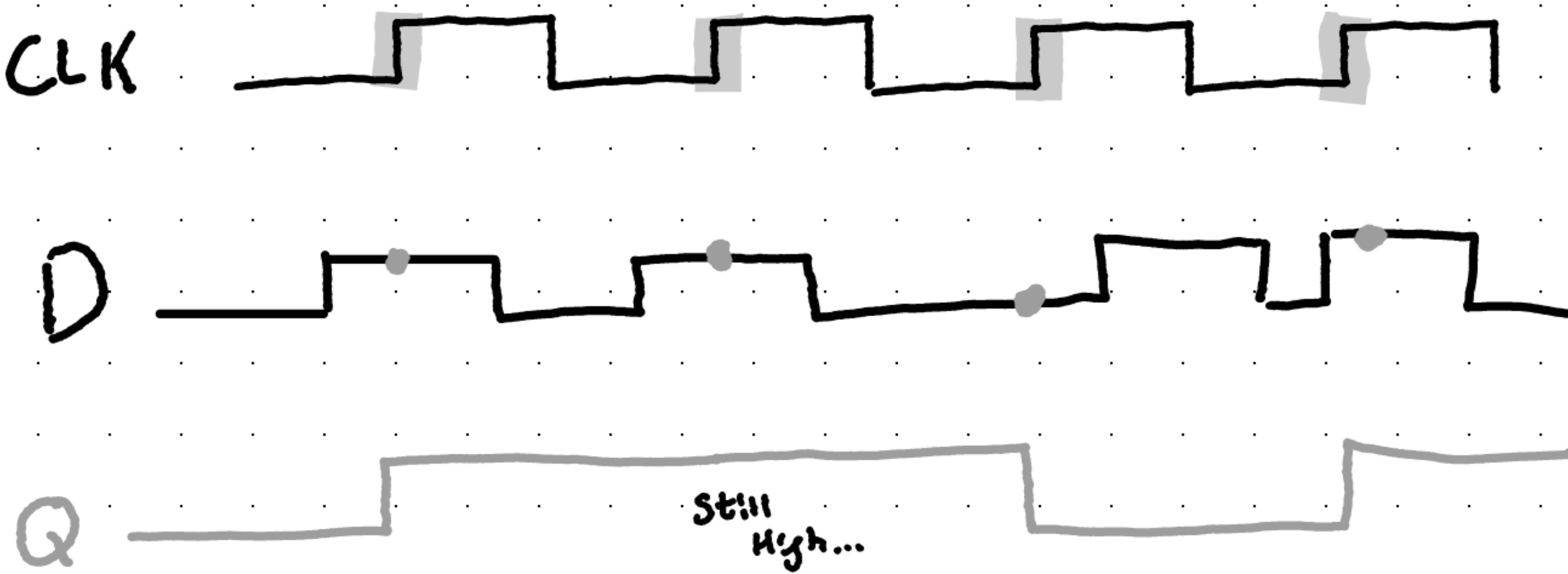


D Flip-Flop

The most common way of storing data!



D Flip-Flop Simulation



The rising edge is almost as U...



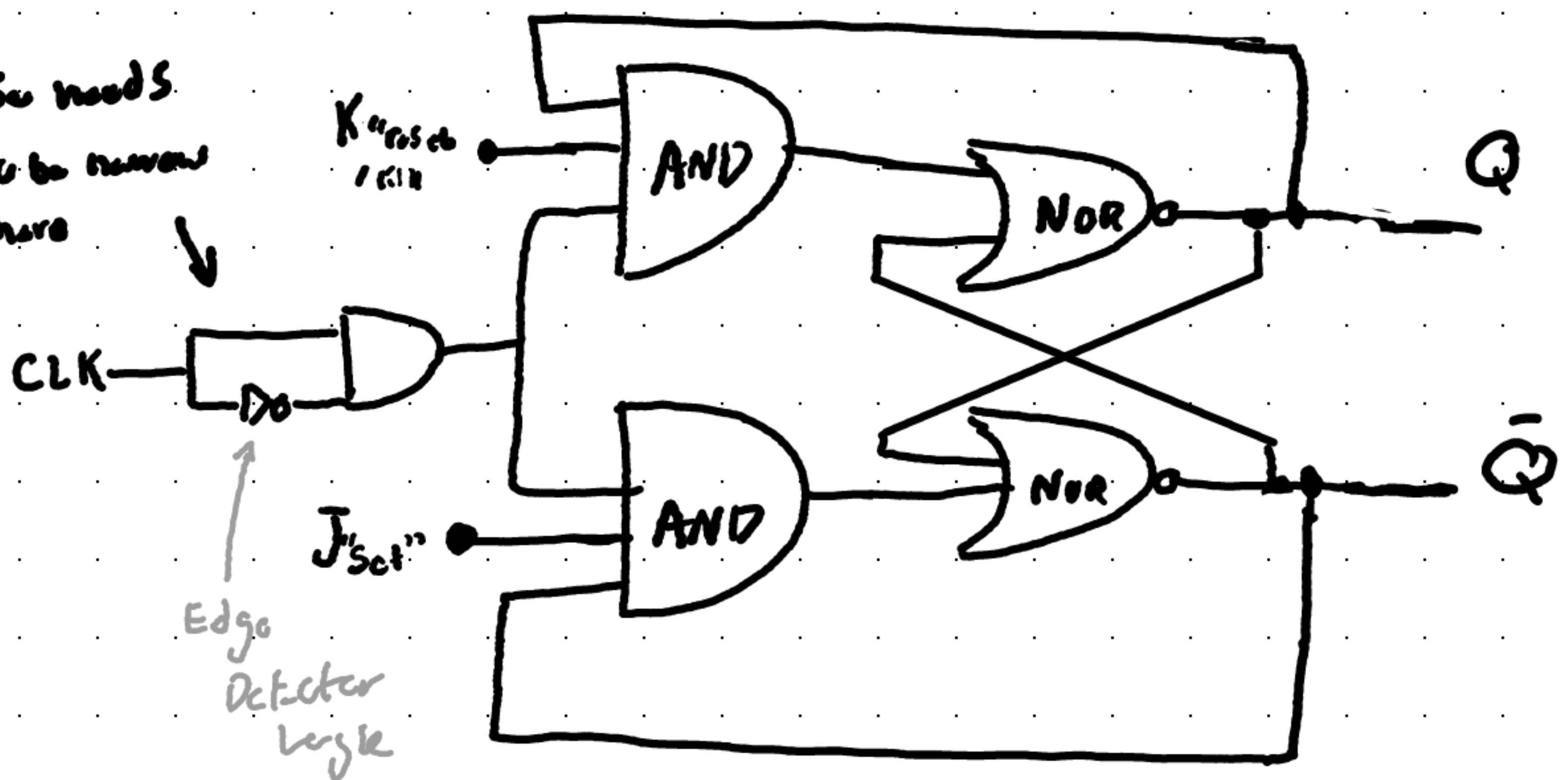
This is why we need an edge detector on the DFF

We care about the rising edge of the clock

This is far more common

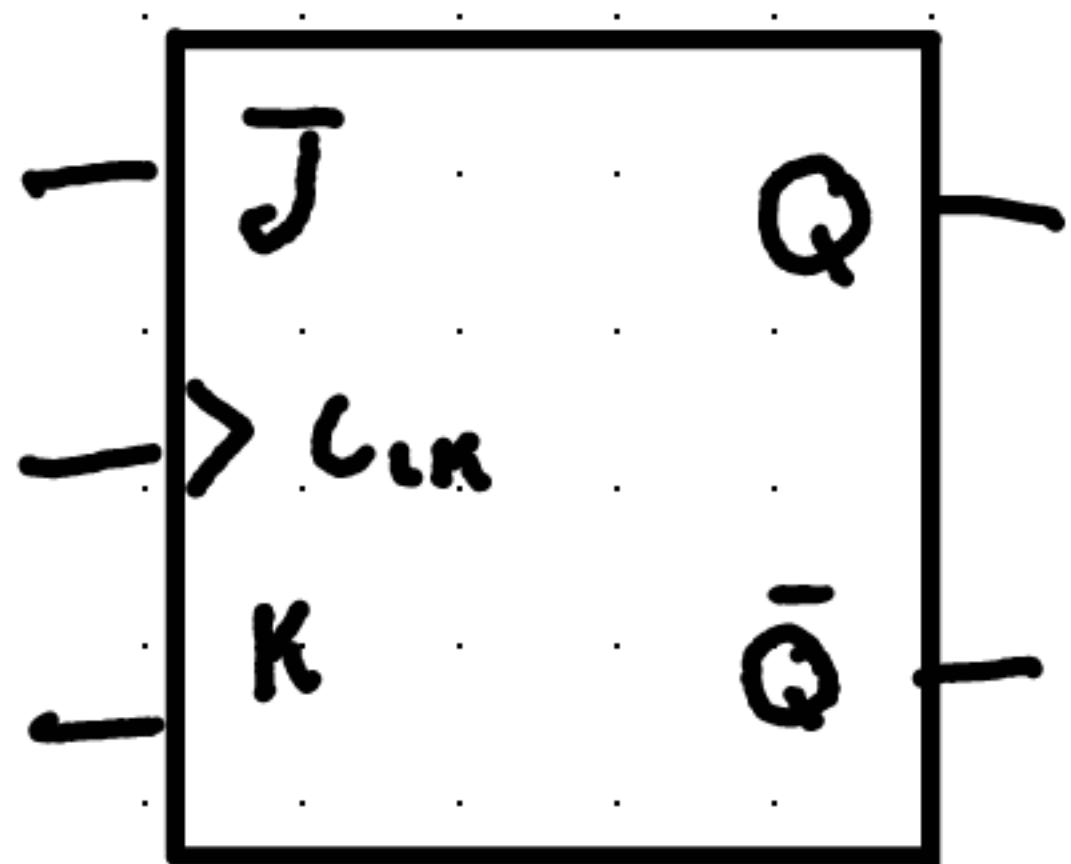
Pulse woods.

to be removed
here



J-K Flip Flop

- Named after inventor Jack Kilby
 - The JK Flip flop is the only universal flip-flop, and can be configured to act as an SR, D or T flip flop.
 - Designed to overcome flaws of S-R Flip-flop
No illegal states.



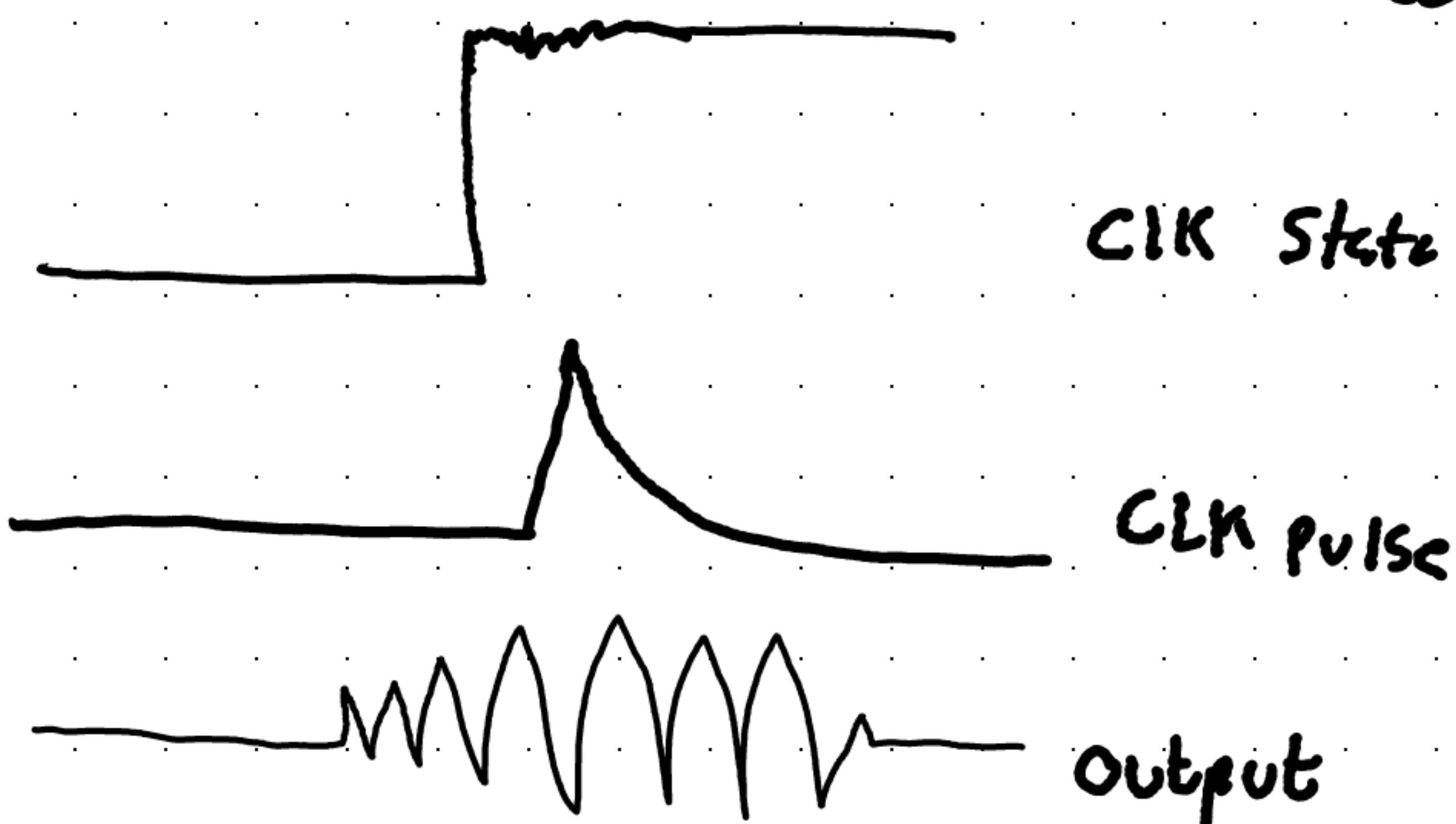
Truth Table for the JK Flip Flop

Toggle Action	Same as for the SR Latch	Clock	Input		Output		Description
		CIK	J	K	Q	\bar{Q}	
		X	0	0	1	0	Memory, No Change Last State
		X	0	0	0	1	
		↑	0	1	0	1	Reset Q \gg 0
		X	0	1	1	0	
		↑	1	0	1	0	Set Q \gg 1
		X	1	0	0	1	
		↑	1	1	0	1	Toggle
		↑	1	1	0	1	on and off

↑
ON Each
Clock

J-K Flip Flop Racking

With a fast Clock Signal, with J and K both being Oh... Weirdness can occur.



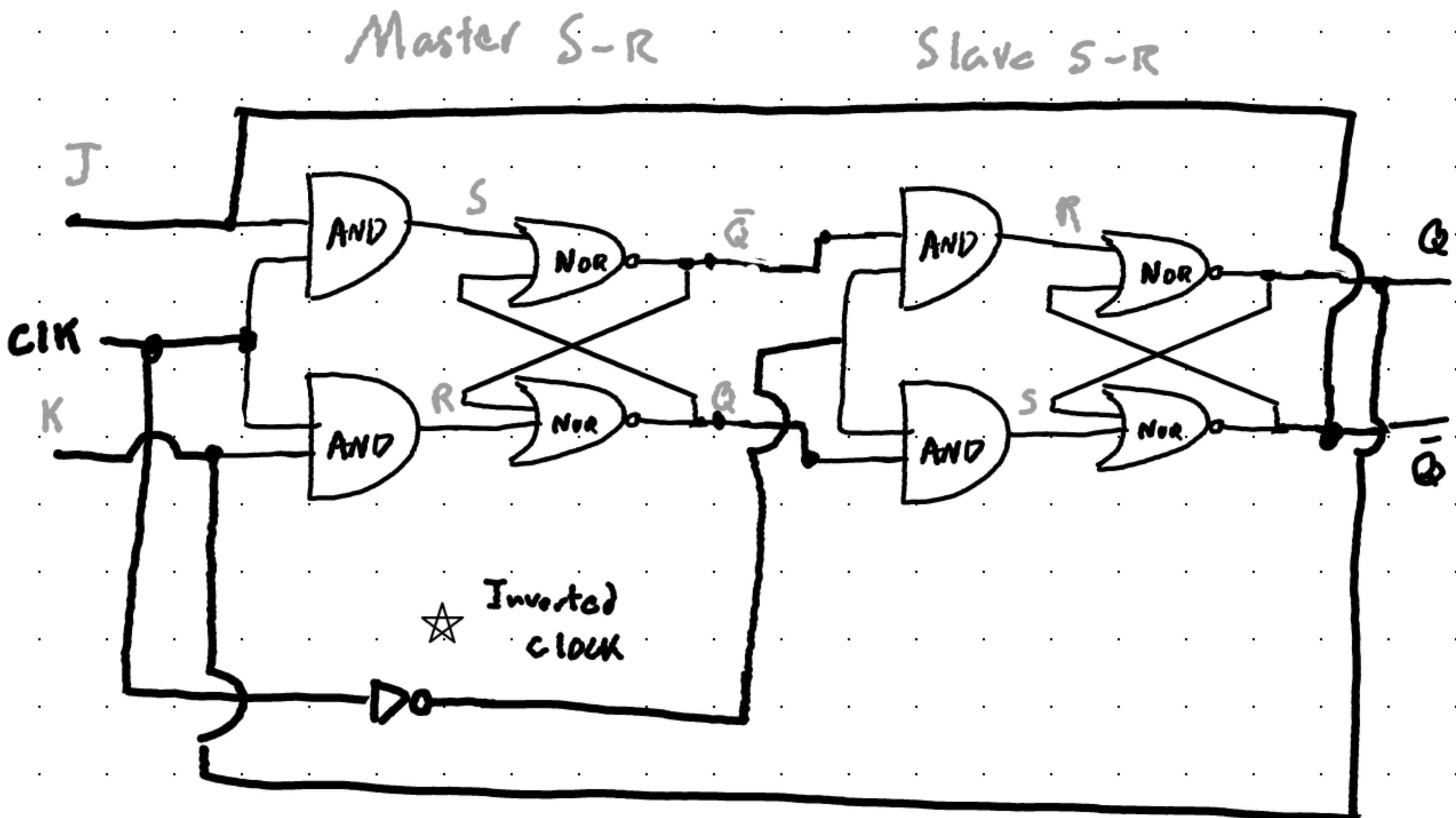
Really Zoomed In On Scope

The RC Clock detection circuit detects the edge, but freaks out as clock pulse isn't instantaneous, due to the RC Circuit's time constant.

This causes the output to toggle extremely fast between the J-K Flip Flop.

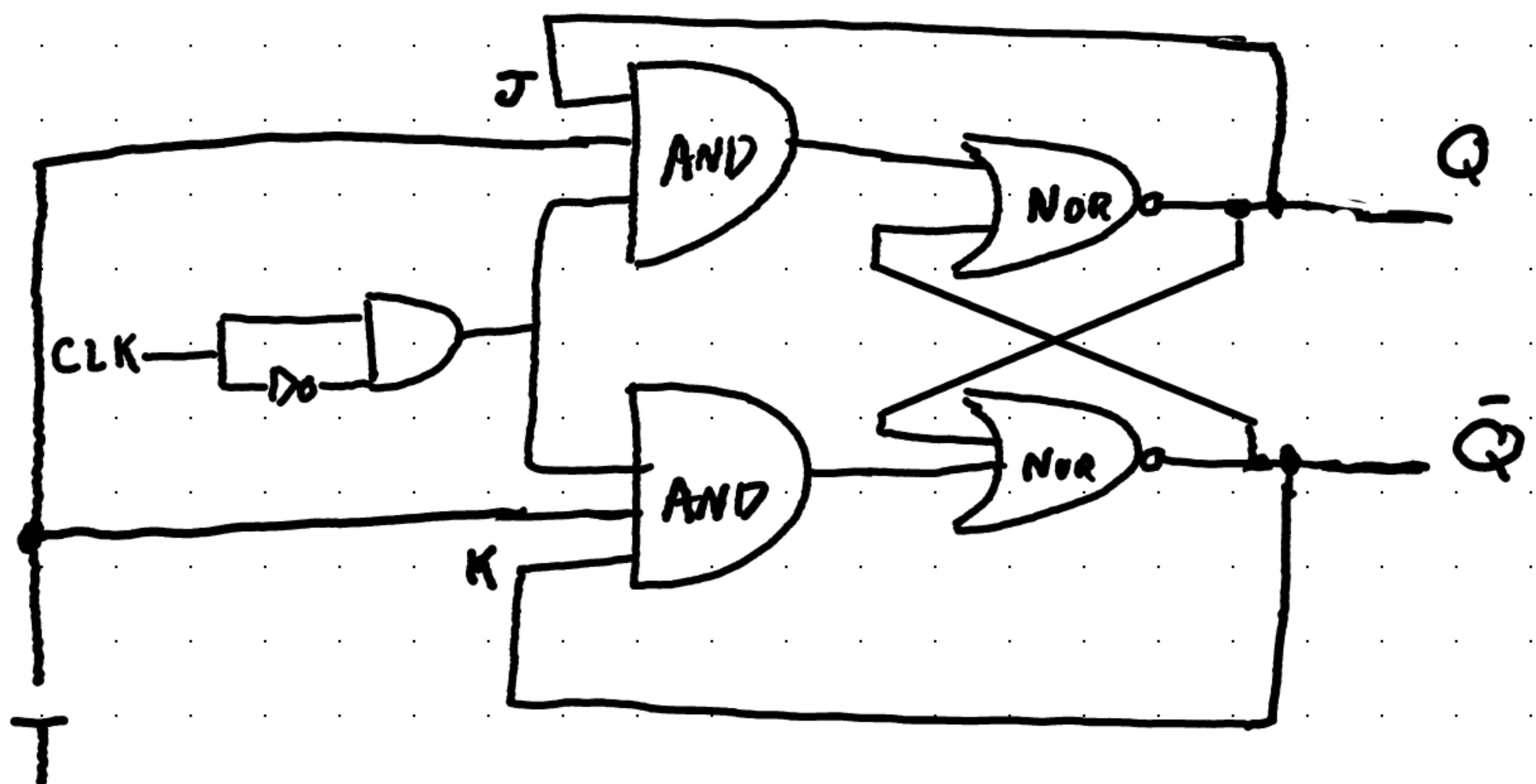
This phenomenon is known as racking.

To fix this, and to have a steady
toggle System, we employ another
kind of Circuit



Master-Slave J-K Flip Flop

- Here, One of the two flip flops will be active, whether the clock is low, or high.
- Toggle Works Much better here.



T Flip Flop

J-K's D flip flop!

Single Input Toggler

ExampleS:

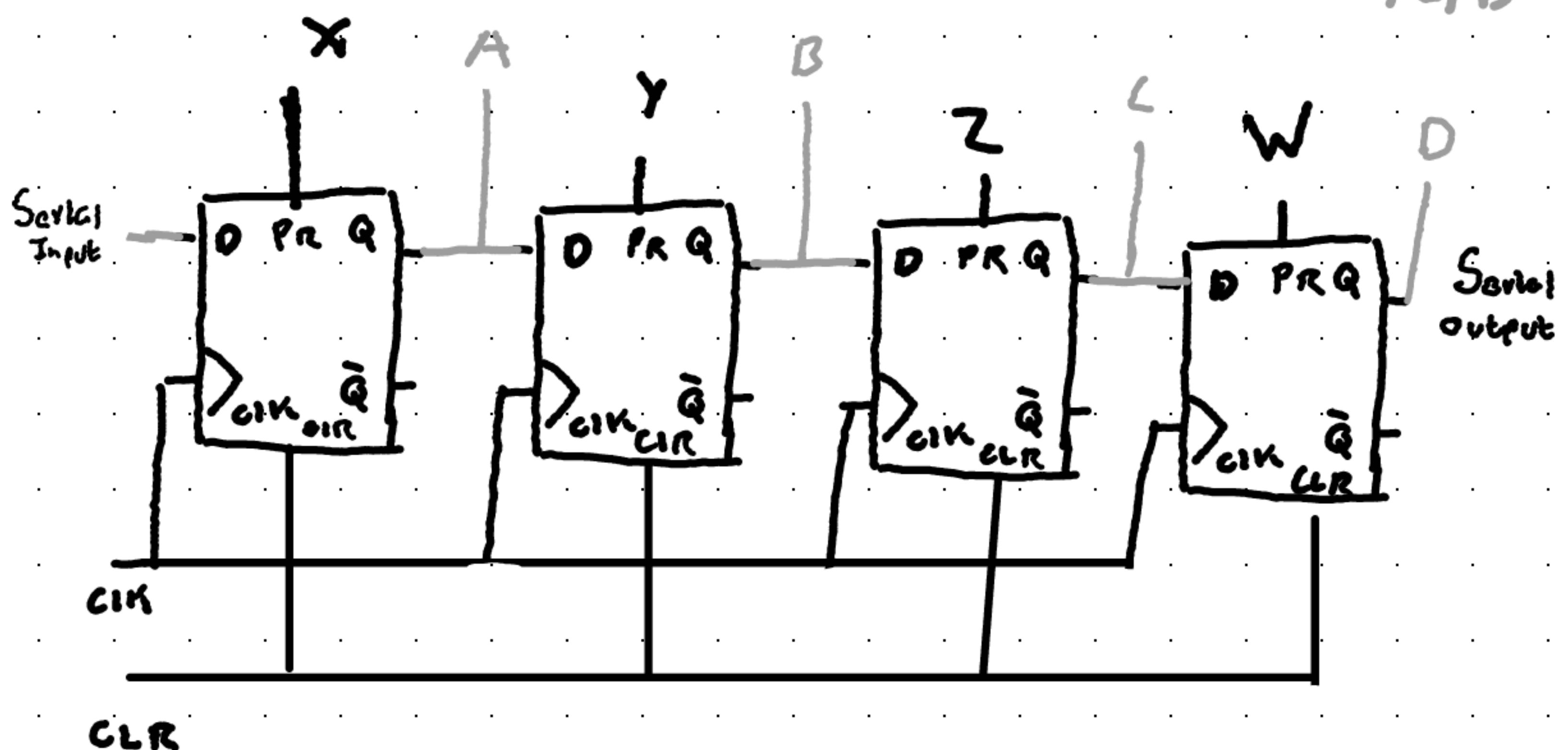
Draw the Circuit for a four-bit Shift register using D Flip-Flops that can perform parallel to Serial Conversion, as well as Serial to Parallel.

Identify:

- i) Two Serial Input terminals
- ii) Two Serial Output terminals
- iii) Two parallel input terminals
- iv) Two parallel output terminals

Parallel Input: X, Y, Z, W

Parallel Output: A, B, C, D



Shift registers

A Shift register is a Sequential logic circuit that stores data. Each flip flop adds a bit of storage. Updates on Clock pulse.

1. Serial In - Serial Out (SISO)

- Data is inputted one bit at a time
- Output is taken from the last flip flop after four clock cycles.

2. Serial In - Parallel out (SIPU)

- Data is loaded serially, but all four bits are available simultaneously at the outputs

3. Parallel in - Serial out (PiSO)

- Data is loaded in parallel (all four bits at once), but shifted out serially.

4. Parallel in - Parallel out (PiPO)

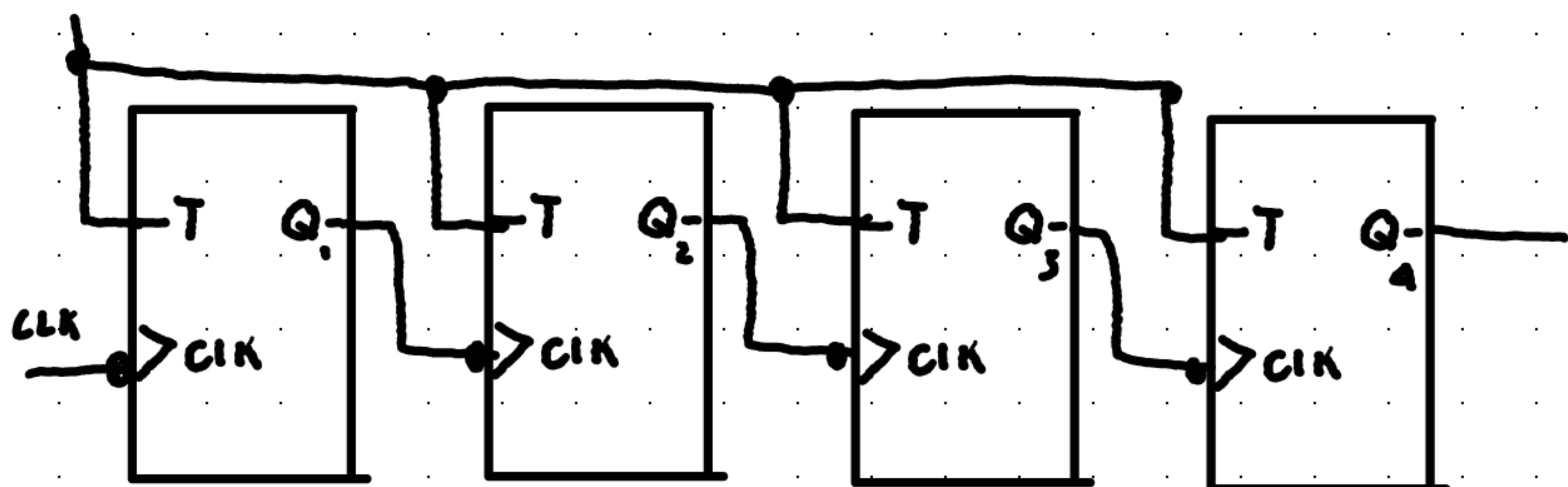
- Data is loaded in, and read in parallel.

Example:

Provide the State transition table for an asynchronous binary up-Counter that goes through the sequence (0000, 0001, 0010, ..., 1110, 1111, 0000, 0001)

- a) Draw the ripple binary up-Counter using T flip flops.

V_{cc}



$Q_1 \ Q_2 \ Q_3 \ Q_4$	$Q_1^+ \ Q_2^+ \ Q_3^+ \ Q_4^+$
0 0 0 0	0 0 0 1
0 0 0 1	0 0 1 0
0 0 1 0	0 0 1 1
0 0 1 1	0 1 0 0
0 1 0 0	0 1 0 1
0 1 0 1	0 1 1 0
0 1 1 0	0 1 1 1
0 1 1 1	1 0 0 0
1 0 0 0	1 0 0 1
1 0 0 1	1 0 1 0
1 0 1 0	1 0 1 1
1 0 1 1	1 1 0 0
1 1 0 0	1 1 0 1
1 1 0 1	1 1 1 0
1 1 1 0	0 0 0 0

Decade Counter:

using T flip flops

1) State Table

$Q_1 Q_2 Q_3 Q_4$	$Q_1' Q_2' Q_3' Q_4'$	$T_1 T_2 T_3 T_4$
0 0 0 0	0 0 0 1	0 0 0 0 1
0 0 0 1	0 0 1 0	0 0 0 1 1
0 0 1 0	0 0 1 1	1 0 0 1 1
0 0 1 1	0 1 0 0	1 0 0 0 1
0 1 0 0	0 1 0 1	2 0 0 0 1
0 1 0 1	0 1 1 0	3 0 1 1 1
0 1 1 0	0 1 1 1	4 0 0 0 1
0 1 1 1	1 0 0 0	5 0 0 1 1
1 0 0 0	1 0 0 1	6 0 0 0 1
1 0 0 1	0 0 0 0	7 1 1 1 1

T_4 is always 1

• Need to build K-maps for other three
using current Q states

$Q_3 Q_4$	00	01	11	10
$Q_1 Q_2$	00	01	10	11
00	0	0	0	0
01	0	1	1	1
11	x	x	x	x
10	0	1	1	0

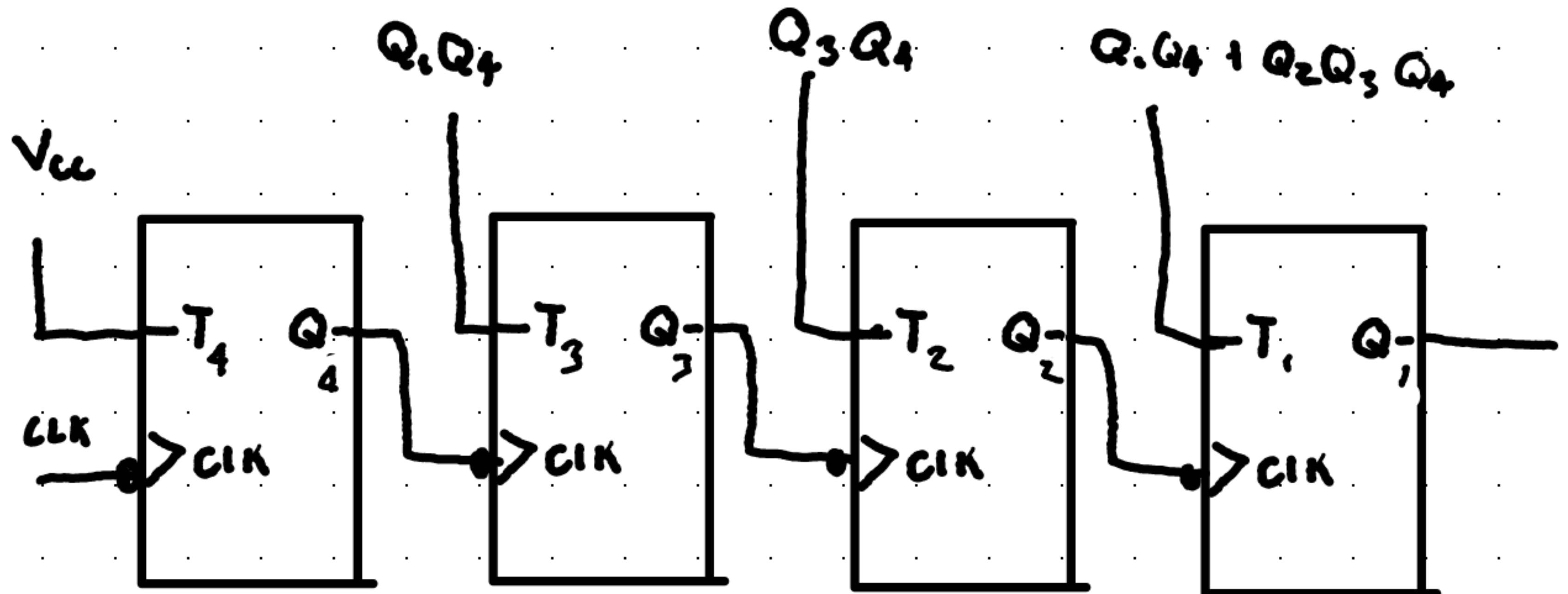
$Q_3 Q_4$	00	01	11	10
$Q_1 Q_2$	00	01	10	11
00	0	0	0	0
01	0	1	1	1
11	x	x	x	x
10	0	1	1	0

$Q_3 Q_4$	00	01	11	10
$Q_1 Q_2$	00	01	10	11
00	1	1	0	2
01	0	1	1	1
11	x	x	x	x
10	c	8	cq	x

$$T_1 = Q_1 Q_4 + Q_2 Q_3 Q_4$$

$$T_2 = Q_3 Q_4$$

$$T_3 = Q_1 Q_4$$



$$T_1 = Q_1 Q_4 + Q_2 Q_3 Q_4$$

$$T_2 = Q_3 Q_4$$

$$T_3 = Q_1 Q_4$$

$$T_4 = 1$$

1) Asynchronous operation Meaning in this context

- Each Flip Flop (except the first) is clocked by the output of the previous flip flop.
- The LSB Flip Flop toggles on every clock pulse. Q_1 toggles when Q_0 falls, etc.,

2) Each Flip Flop is a negative-edge-triggered T flip flop. (Toggles on clock falling edge)

→ Because of this, we add not gates on all of the clock inputs

<u>Feature</u>	<u>Decade Up Counter</u>	<u>Ripple (ASync) Up Counter</u>
Counting Sequence	0000 → 0001 → ... → 1001 → <u>0000</u> (0 to 9)	0000 → 0001 → ... → 1111 → <u>0000</u> (0 to 15)
Modulus	Mod-10 (Reset after 9)	Mod-16 (Reset after 15 or four bit)
Flip-Flop Usage	4 FF's, but logic resets at 10 (1010)	4 FF's, no fixed reset (natural binary count)
Synchronization	Can be Async or Synchronous	Always Async
Applications	Decade Systems, Digital Clocks, BCD Systems	General purpose Counting, timers, dividers.

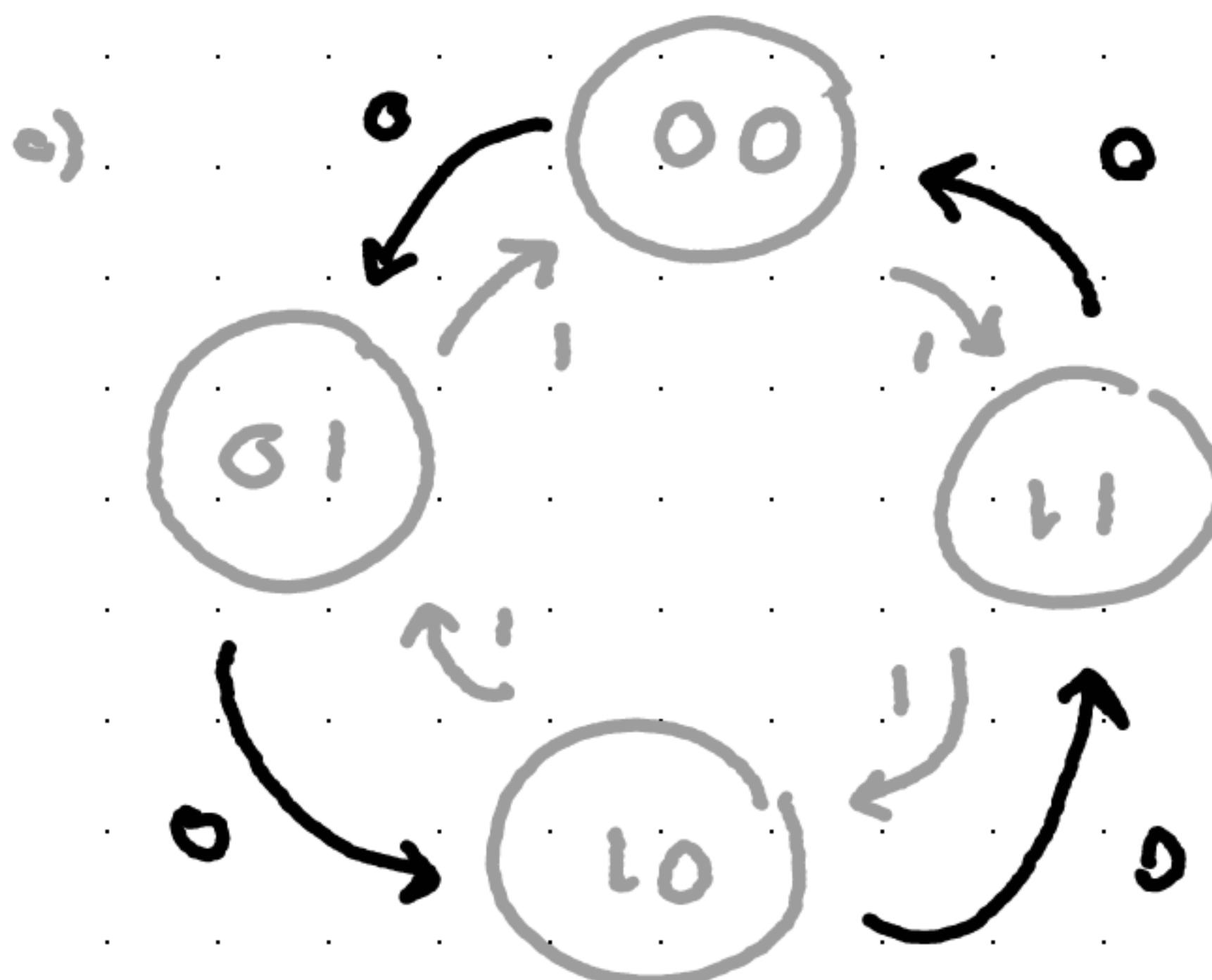
Decade = Human readable displays

Ripple = Binary operations.

Examples:

Use JK flip flops to design a Finite State Machine (FSM) that works as a 2-bit binary Synchronous Up-Counter when its input $X=0$ and as a 2-bit binary Synchronous down-Counter when its input $X=1$.

- draw the state transition diagram
- build the state transition table. Include values of flip flop inputs
- find minimized logic expressions for flip flop inputs
- draw the resulting logic circuit that implements this FSM

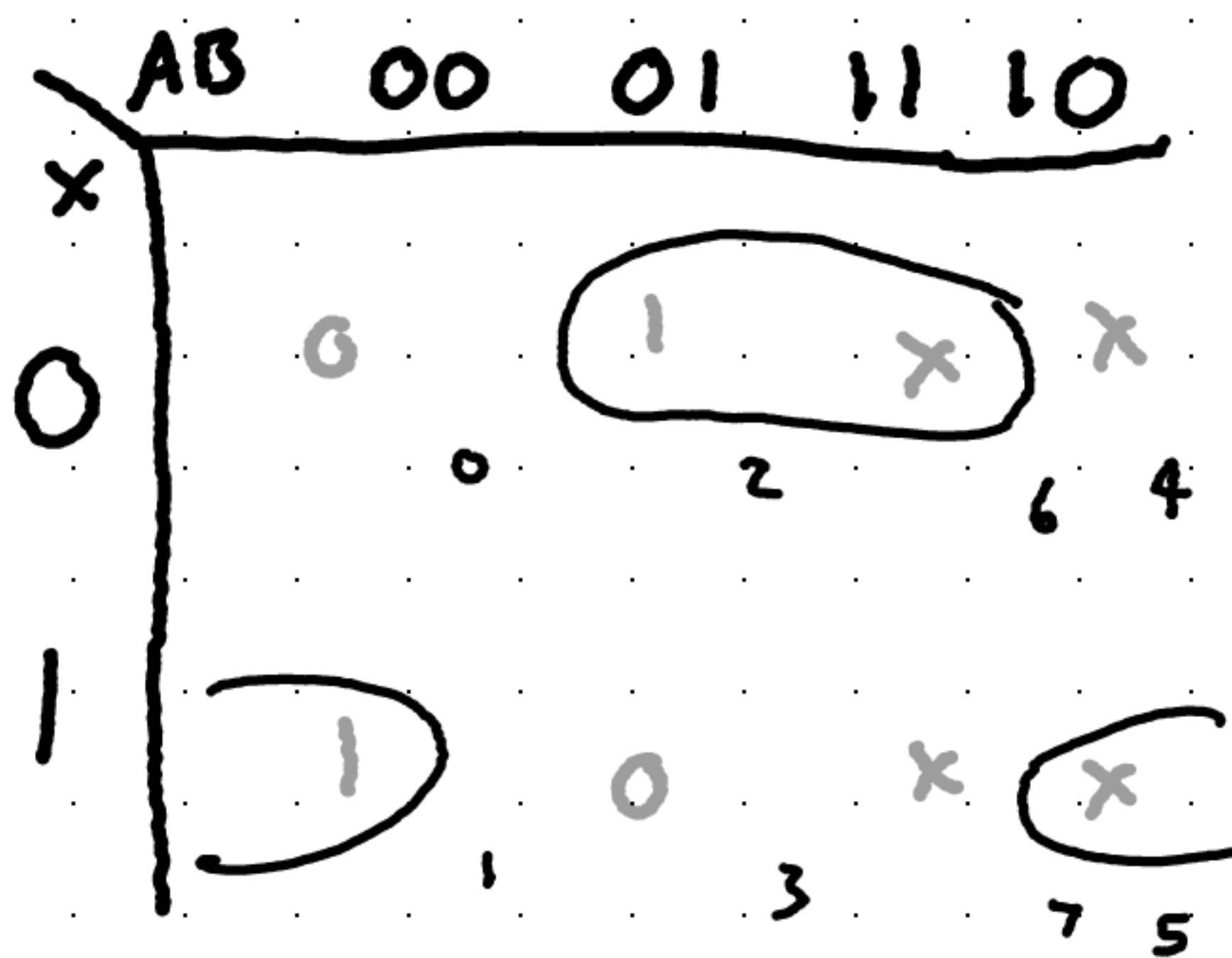


b)

 $O = \text{up}$ $I = \text{down}$

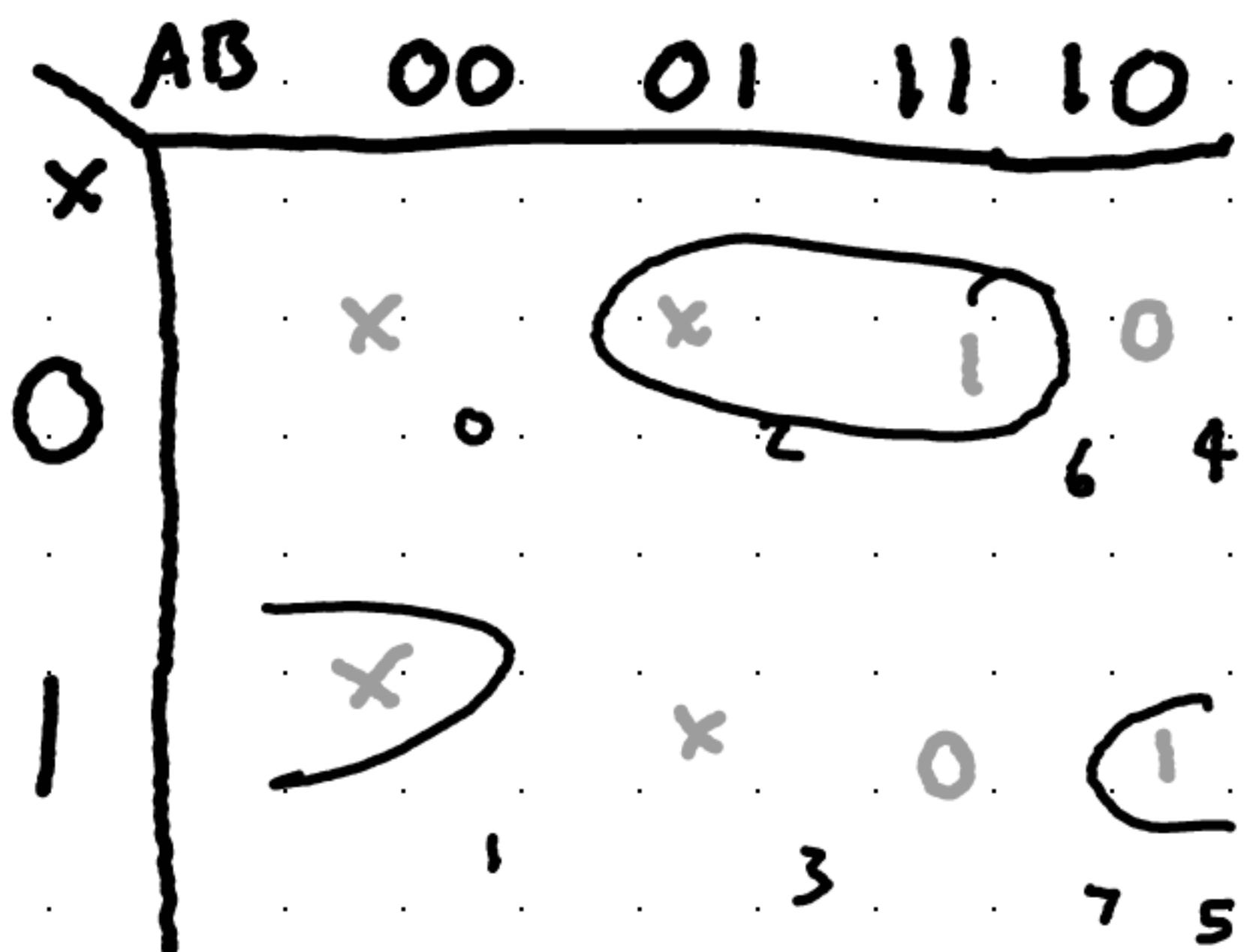
A	B	x	A^+	B^+	J_A	K_A	J_B	K_B
0 0	0	0	0	1	0	x	1	x
0 0	1	1	1	1	1	x	1	x
0 1	0	1	0	1	1	x	x	1
0 1	1	0	0	0	0	x	x	1
1 0	0	1	1	1	x	0	1	x
1 0	1	0	1	1	x	1	1	x
1 1	0	0	0	0	x	1	x	1
1 1	1	1	0	1	x	0	x	1

c)



J_A

$$\bar{J}_A = \bar{X}B + X\bar{B}$$



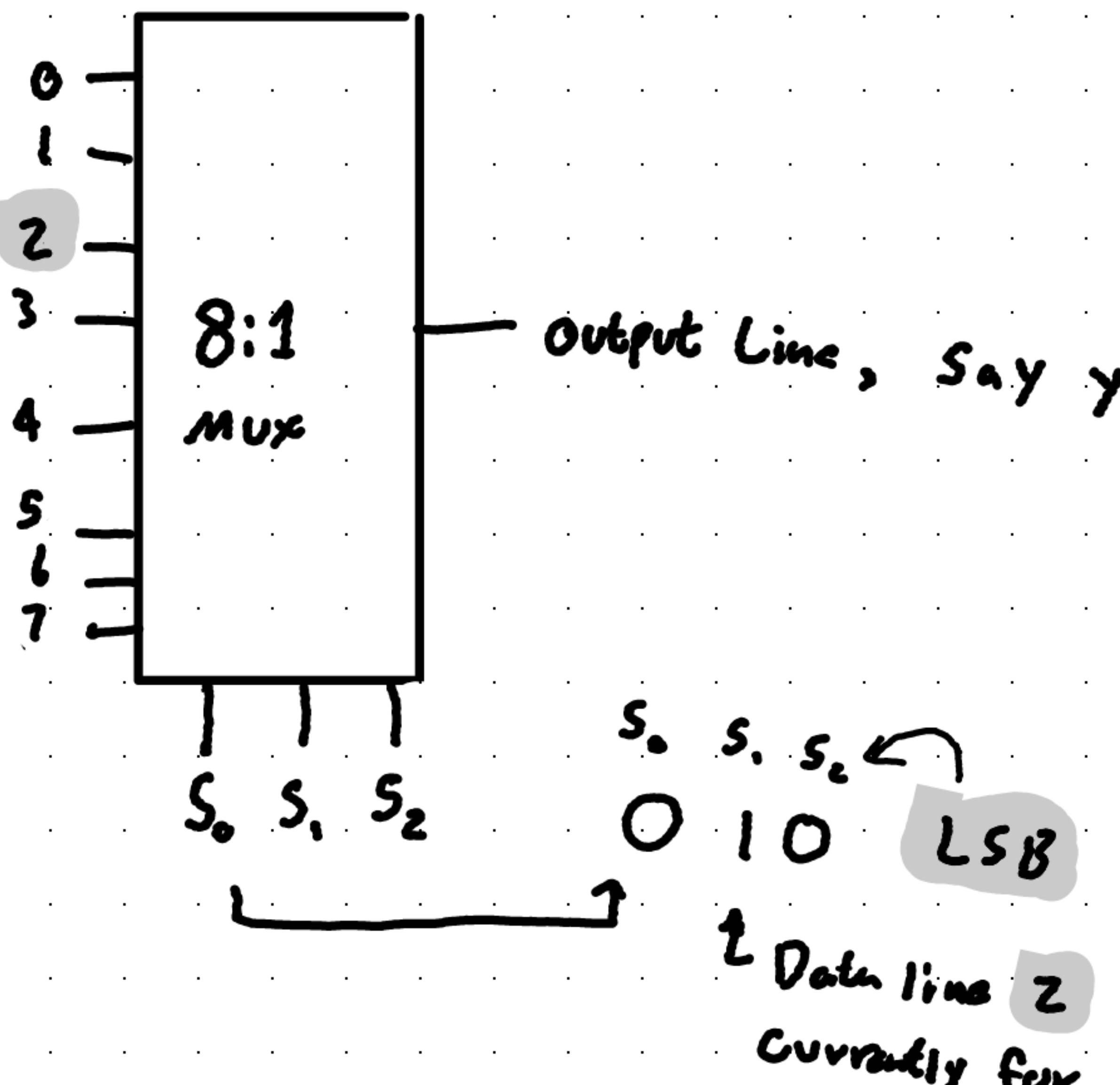
K_A

$$K_A = \bar{X}B + X\bar{0}$$

$$\bar{J}_B = 1$$

$$K_B = 1$$

Multiplexer Elements (MUX)



- A multiplexer Element acts as a traffic controller. It allows who can go, and who can't.
- In this case, we've allowed line z to go. We can change this by manipulating S_0 , S_1 , & S_2 . Say we want 5. Send 101.

Examples:

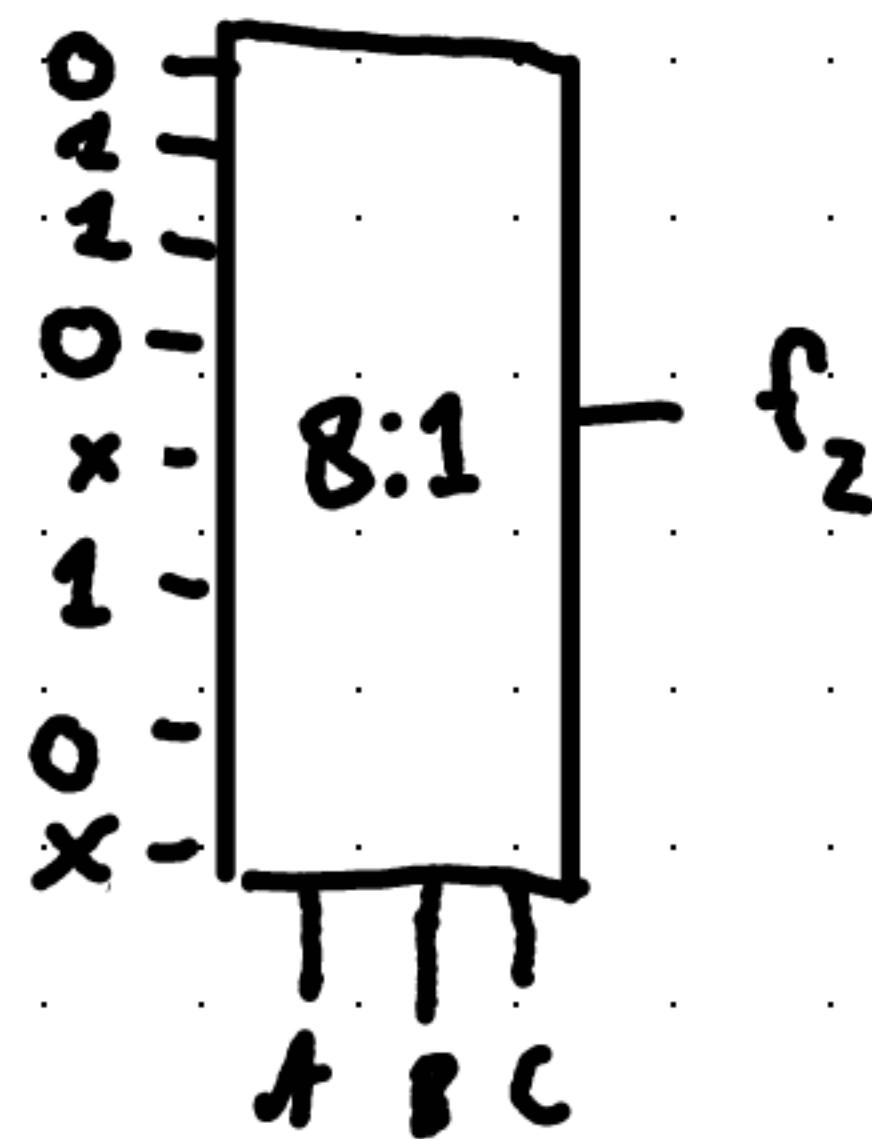
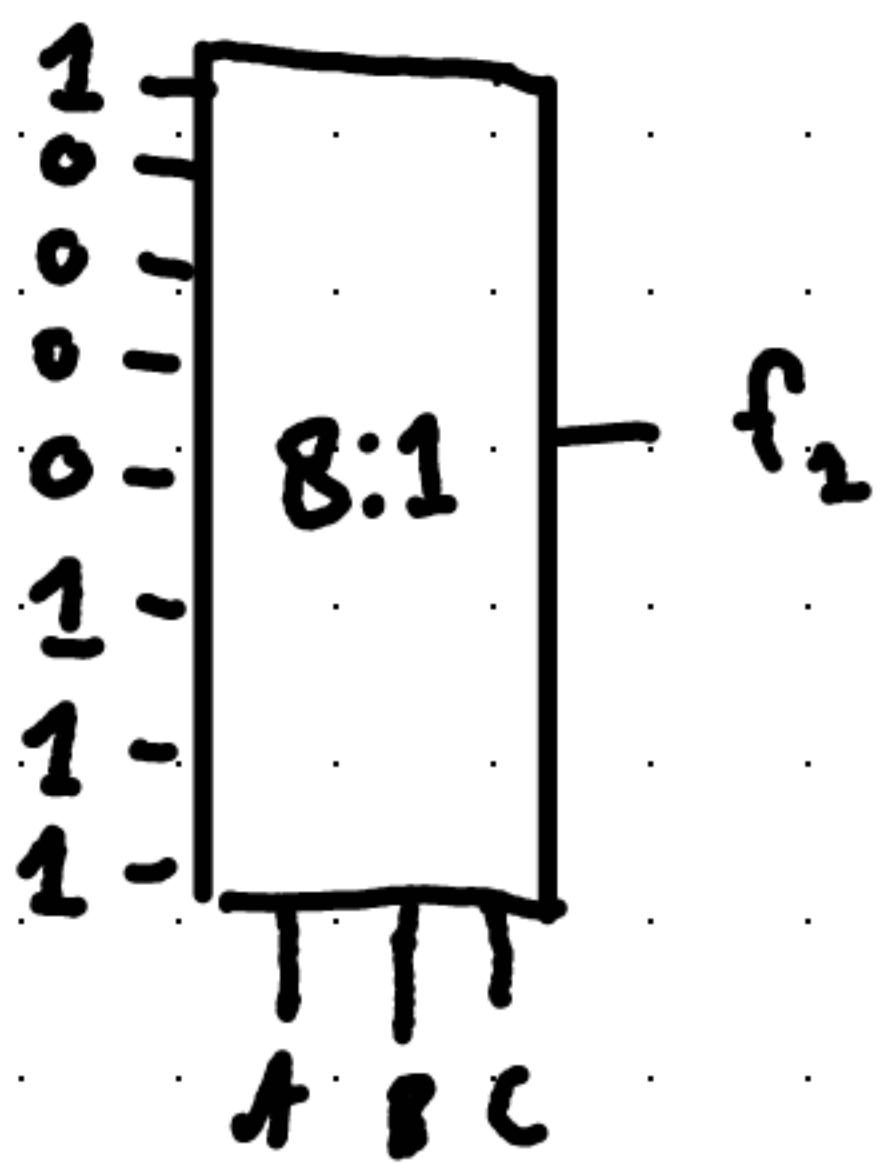
Implement the following Boolean functions using 8:1 multiplexer

$$\text{i)} \quad f_1(A, B, C) = \sum m: (0, 5, 6, 7) : \text{SOP}$$

$$\text{ii)} \quad f_2(A, B, C) = \overline{\text{TM}}_1(0, 3, 6) : \text{POS}$$

We are also told that the input combinations $A=100$ and $A=111$ are not of concern (don't care) for f_2 . ④

a)



b)

	A	B	C	f_1	f_2
0	0	0	0	1	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	0	1
4	1	0	0	0	0
5	1	0	1	0	x
6	1	1	0	1	0
7	1	1	1	1	x

b) Implement f_1 and f_2 on a 4:1 Mux

We need to implement 1's on $\sum m: (0, 5, 6, 7)$

- To do this, we need to consider each selection range

-
- 1. When $A=0, B=0$

* Possible Inputs $000(0), 001(1)$

When C is zero (\bar{C}), the 1 value is selected

- 2. When $A=0, B=1$

The output is always zero.

0

- 3. When $A=1, B=0$

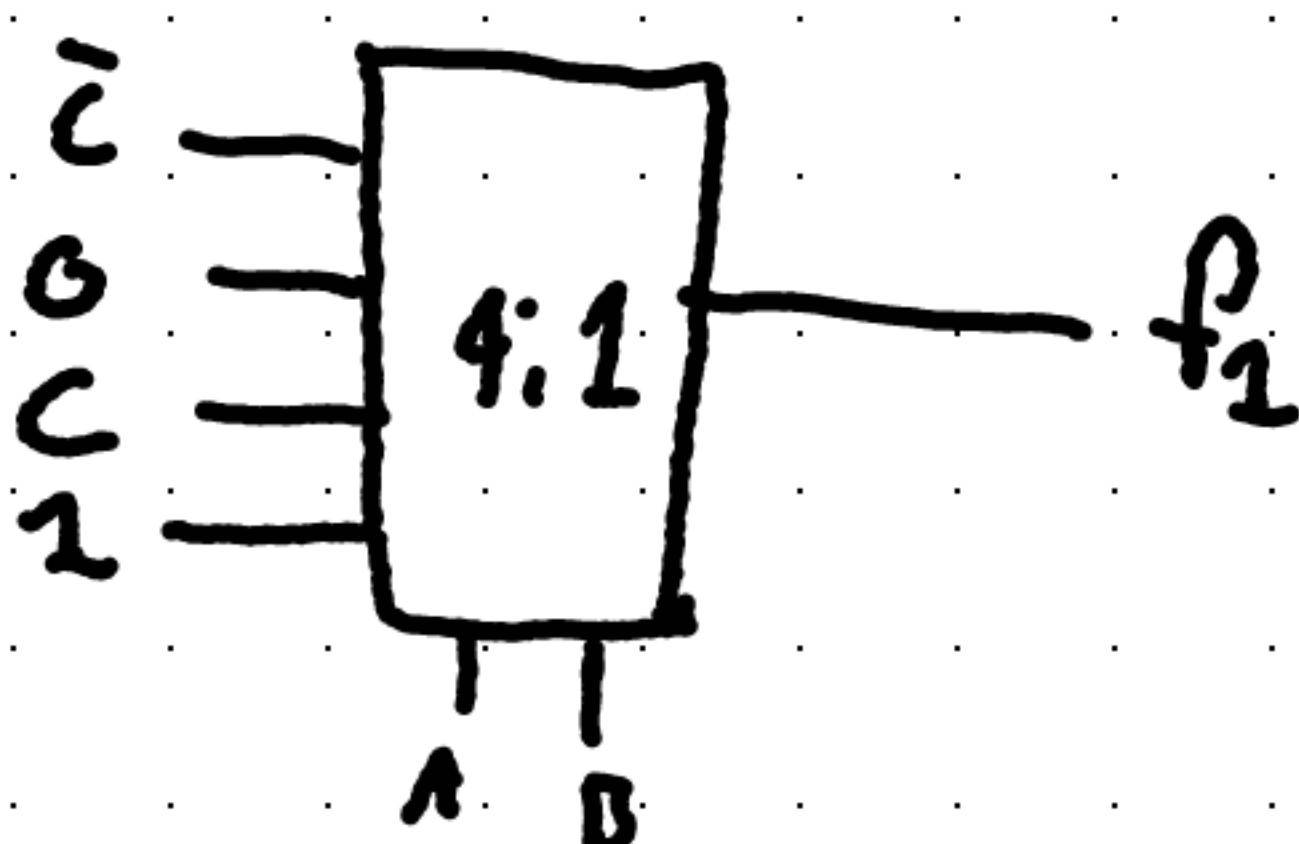
We get what we want when $C=1$

C

- 4. When $A=1, B=1$

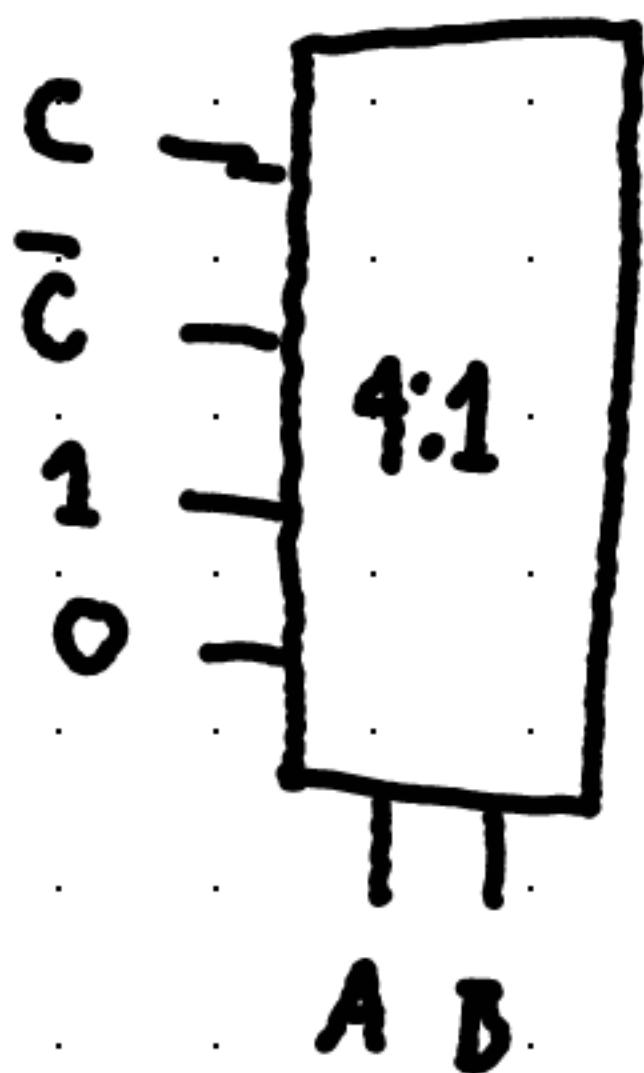
The output is always 1.

1



Implementation of f_2

$\overline{TM}_1(0,3,6)$



00	C
01	\bar{C}
10	1
11	0

c) Implement the following boolean functions using one 3:8 decoder and three OR gates.

$$i) f(A, B, C) = \sum m_1(5, 6, 7)$$

$$ii) f(A, B, C) = \bar{A} \cdot (B + \bar{C})$$

$$iii) f(A, B, C) = \bar{A} \cdot C + A \cdot \bar{B} \cdot \bar{C}$$

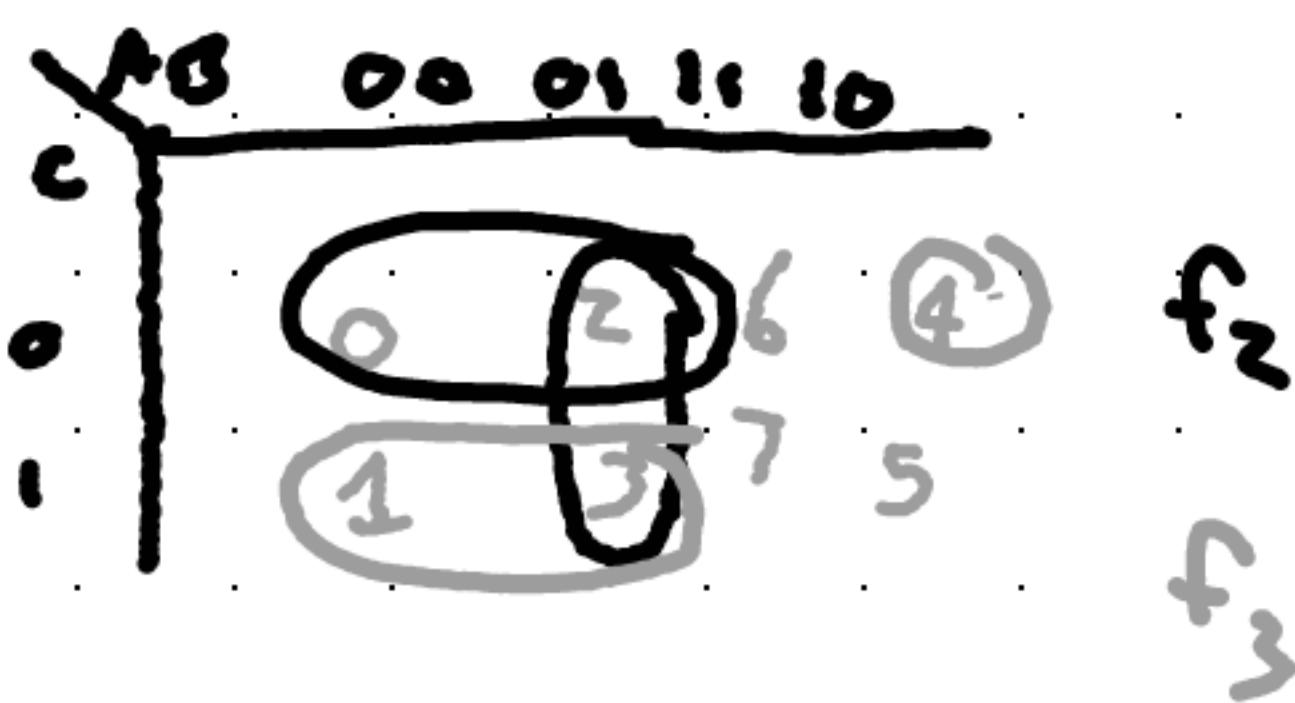
$$f_1 = \sum m_1(5, 6, 7)$$

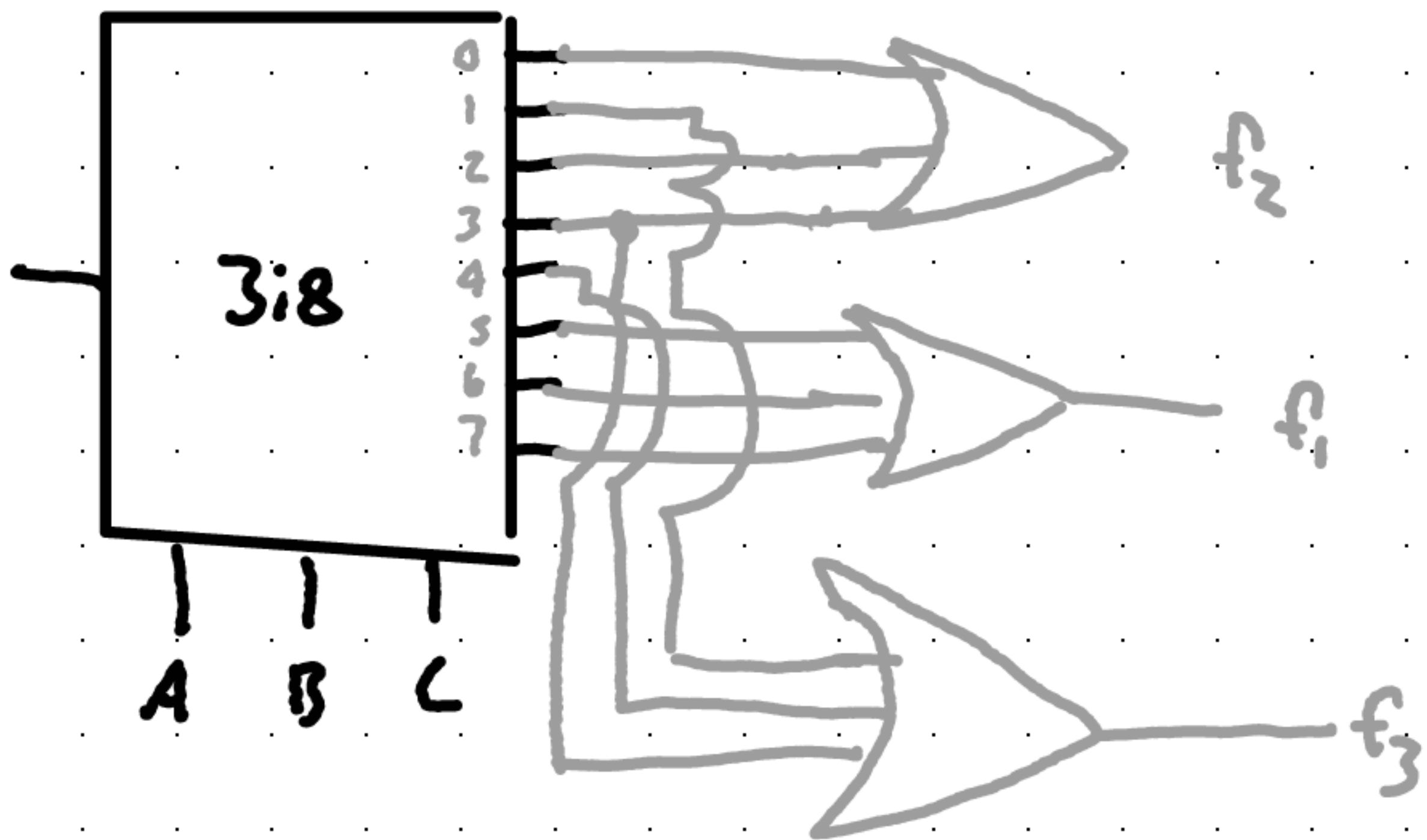
$$f_2 = \bar{A}B + \bar{A}\bar{C}$$

$$= \sum m_1(0, 2, 3)$$

$$f_3 = \bar{A}C + A\bar{B}\bar{C}$$

$$= \sum m_1(1, 3, 4)$$





$$f_1 = \sum m; (5, 6, 7)$$

$$\begin{aligned} f_2 &= \bar{A}B + \bar{A}\bar{C} \\ &= \sum m; (0, 2, 3) \end{aligned}$$

$$\begin{aligned} f_3 &= \bar{A}C + A\bar{B}\bar{C} \\ &= \sum m; (1, 3, 4) \end{aligned}$$

Example:

A half adder circuit has two inputs A and B, and two outputs, S and Co

Pattern detector

