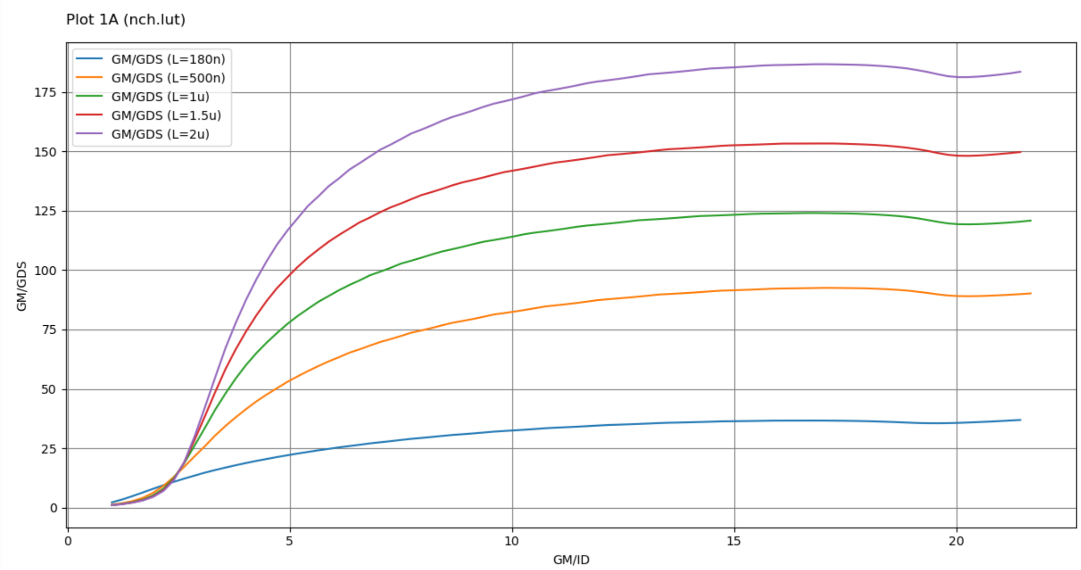
Analog IC Design

Lab 11

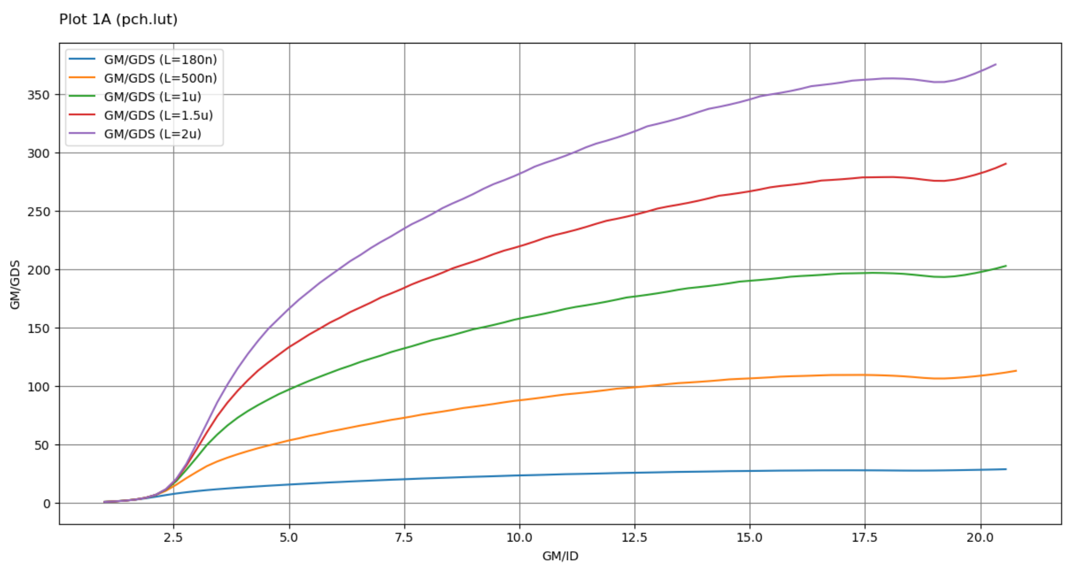
PART 1: gm/ID Design Charts

gm/gds

NMOS

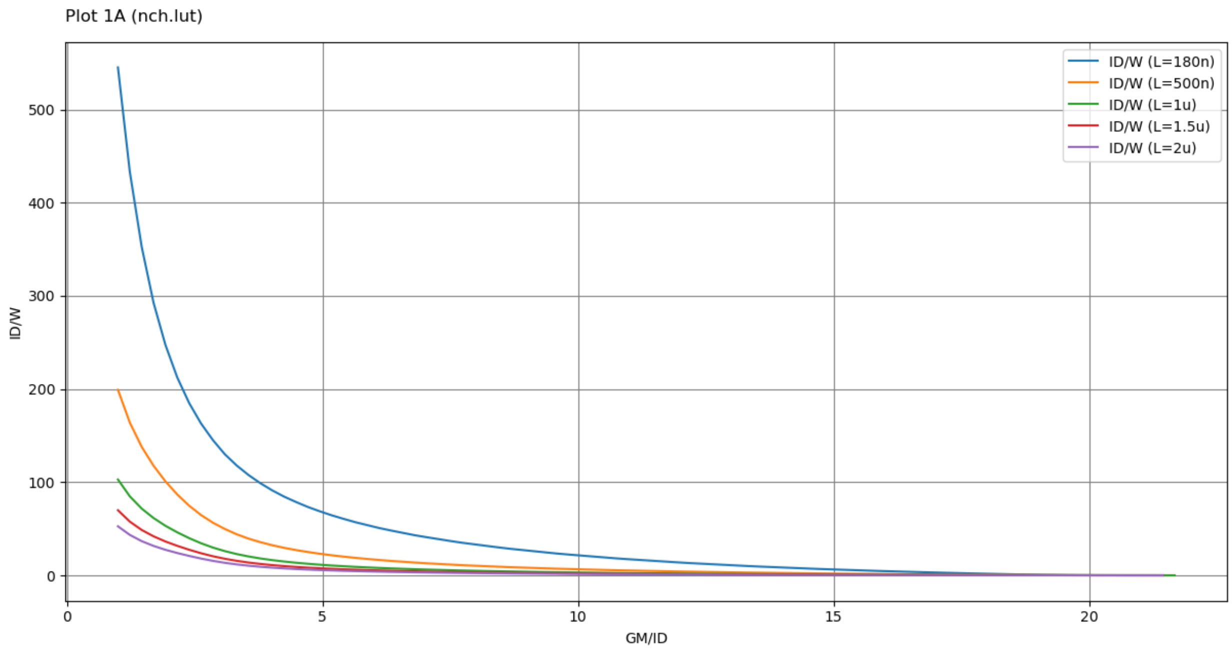


PMOS

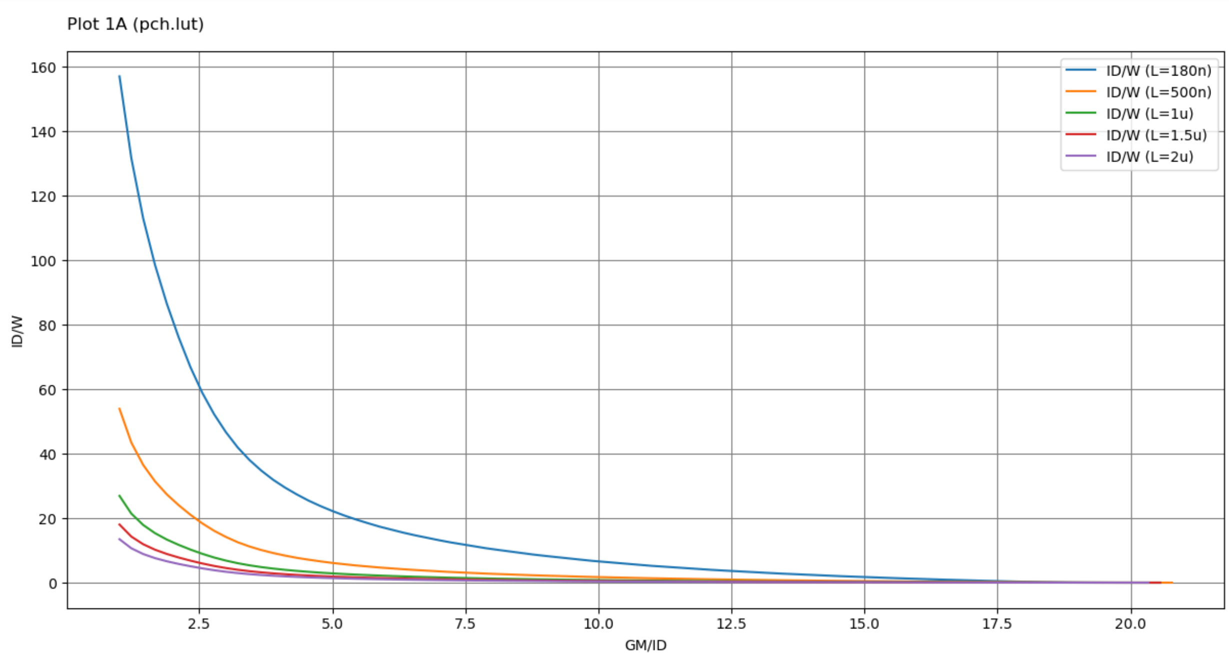


ID/W

NMOS

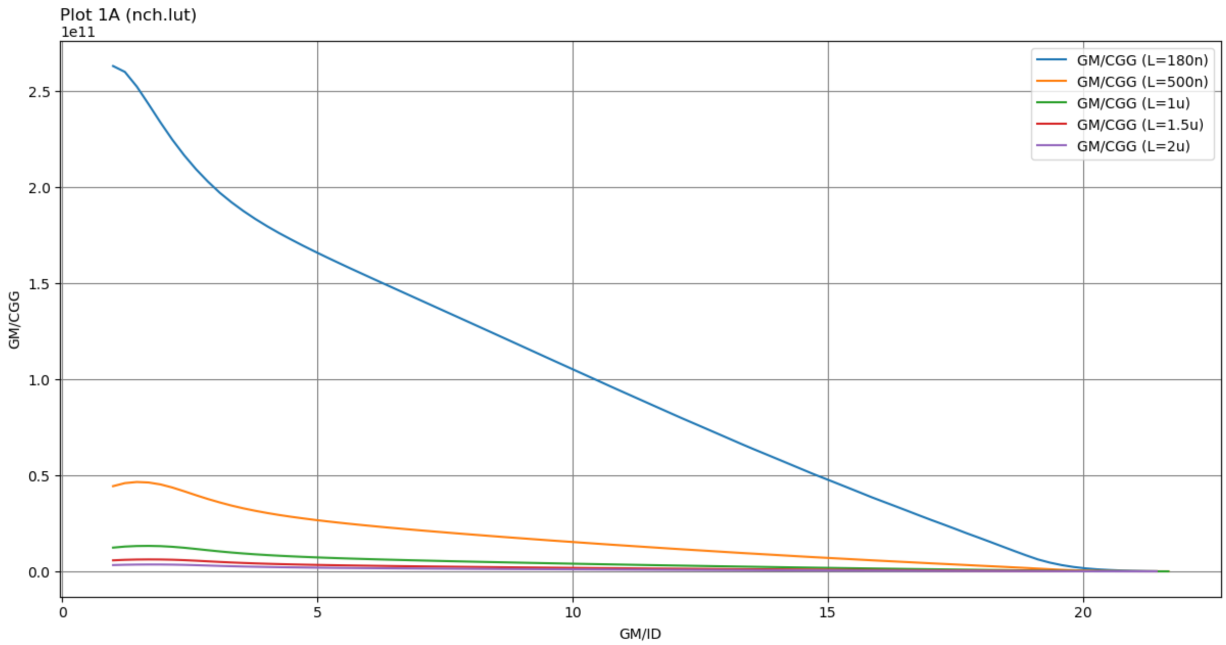


PMOS

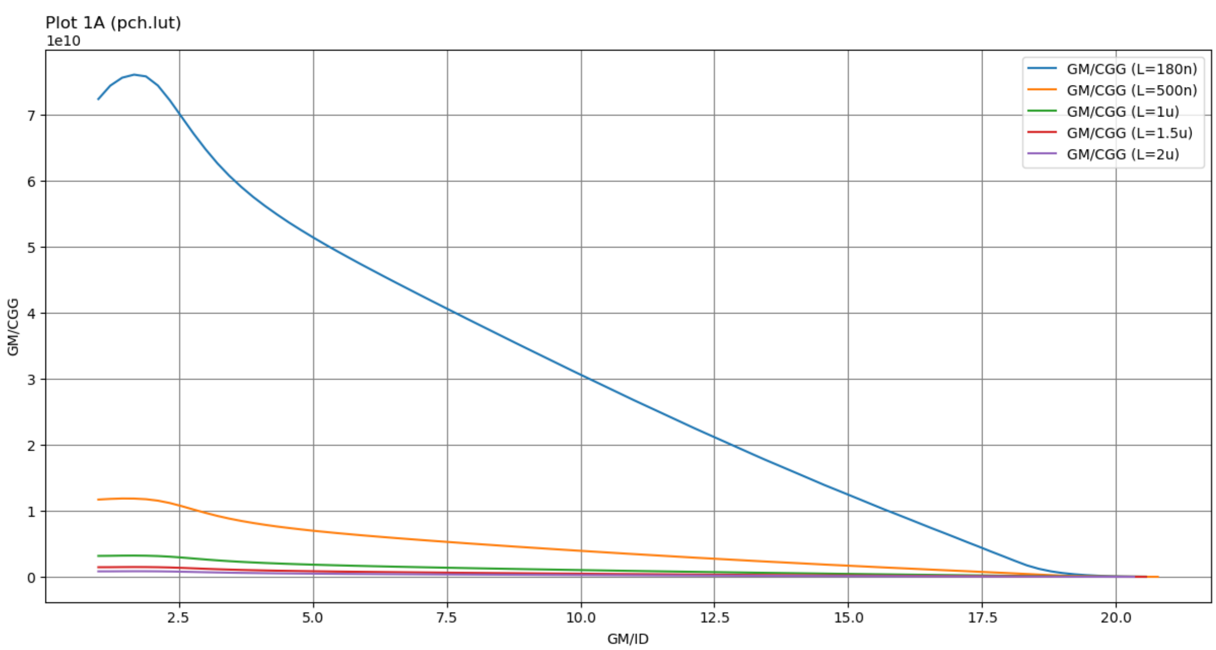


gm/Cgg

NMOS

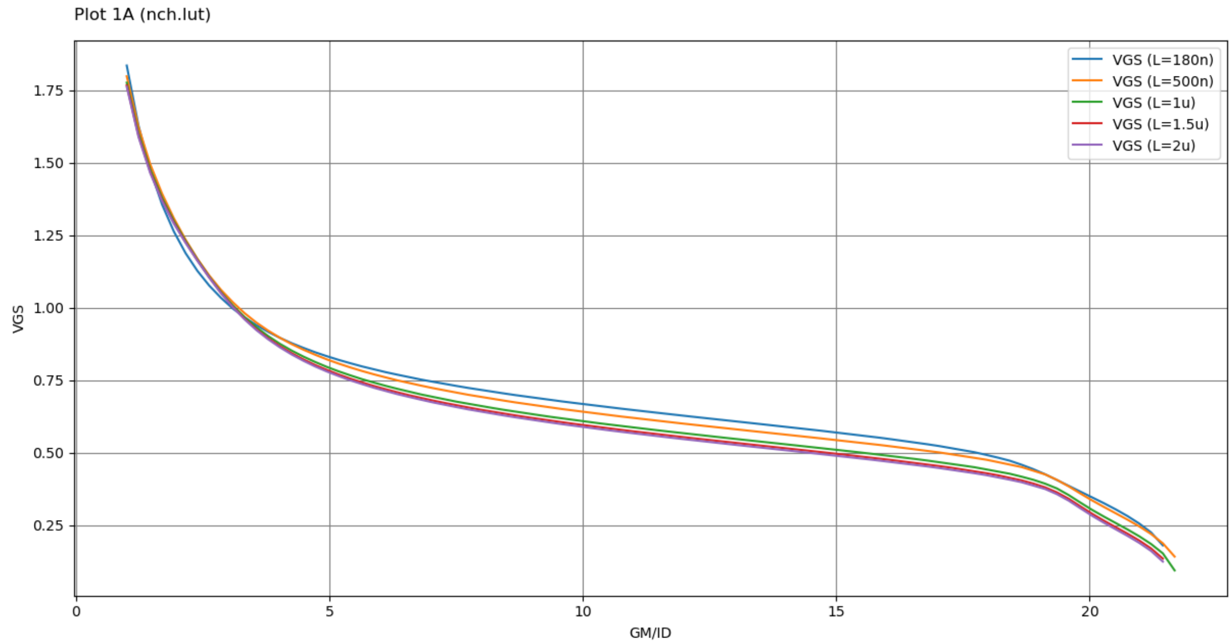


PMOS

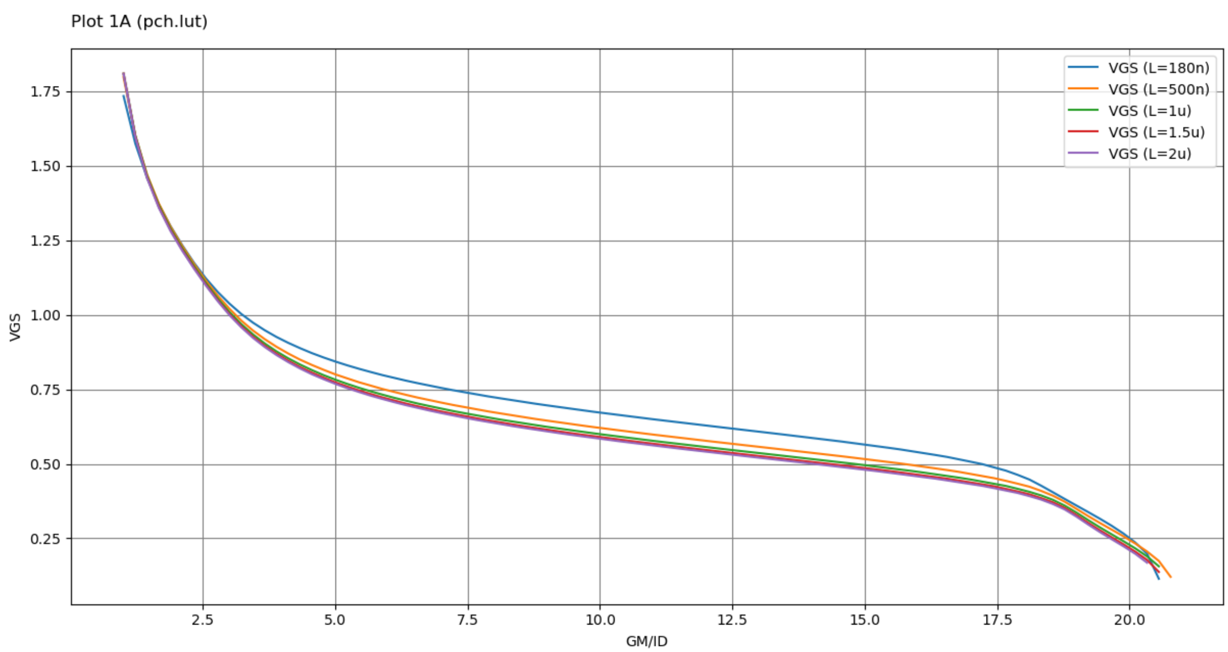


VGS

NMOS



PMOS



PART 2: OTA Design

General Hand Analysis

- Input pair should be PMOS because CMIR is closer to ground.
- ISS = 40uA for the input pair (CS), and 40uA for the cascode branches (CG). The NMOS current sources in the bottom needs to sink 80uA (2 x 40uA)

Differential PMOS Pair Sizing

- MI or WI & short L for optimum GBW and minimum capacitive loading.
- ID = 20u & gm/ID = 15

L = 200n & W = 6.36u

PMOS Tail Current Source Sizing

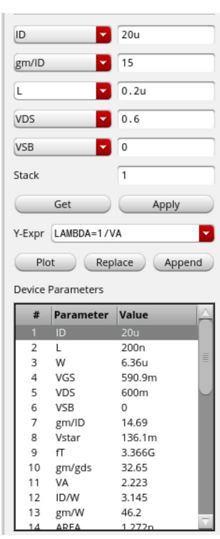
- SI & long L → lower noise contribution
- ID = 40u and gm/ID = 10

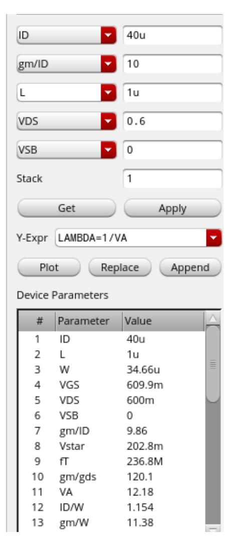
L = 1u & W = 34.66u

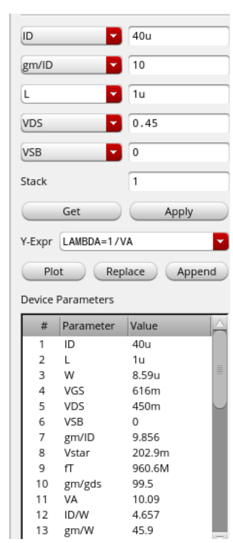
NMOS CM Sizing

- SI & long L
- ID = 40u and gm/ID = 10

L = 1u & W = 8.59u







PMOS CM Sizing

- SI & long L
- ID = 20u and gm/ID = 10

L = 1u & W = 17.47u

PMOS Cascode Sizing

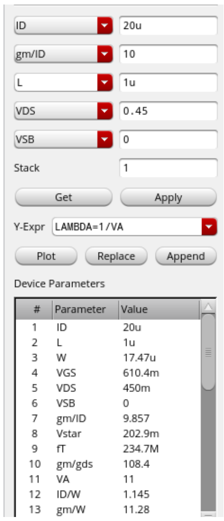
- MI or WI & moderate L
- ID = 20u and gm/ID = 15

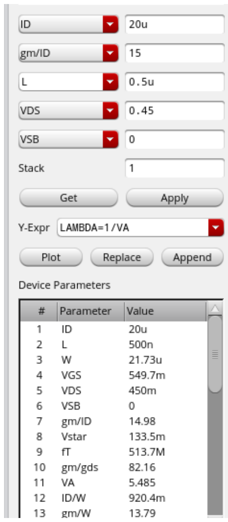
L = 0.5u & W = 21.73u

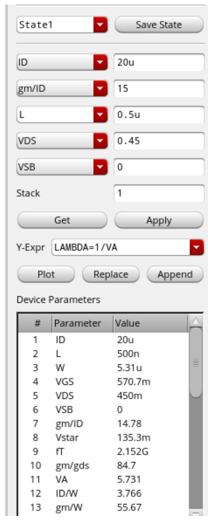
NMOS Cascode Sizing

- MI or WI & moderate L
- ID = 20u and gm/ID = 15

L = 0.5u & W = 5.31u





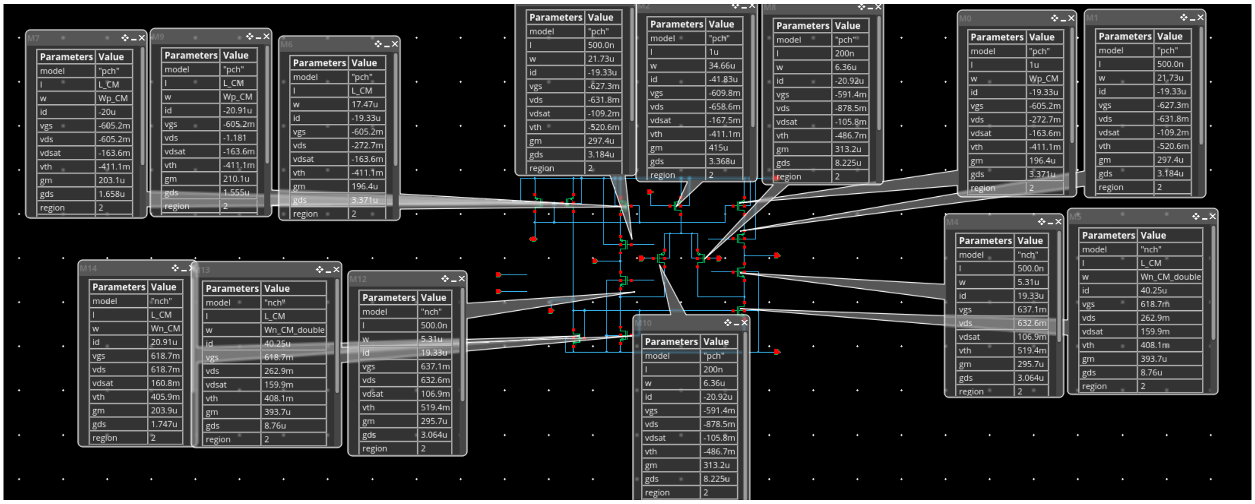


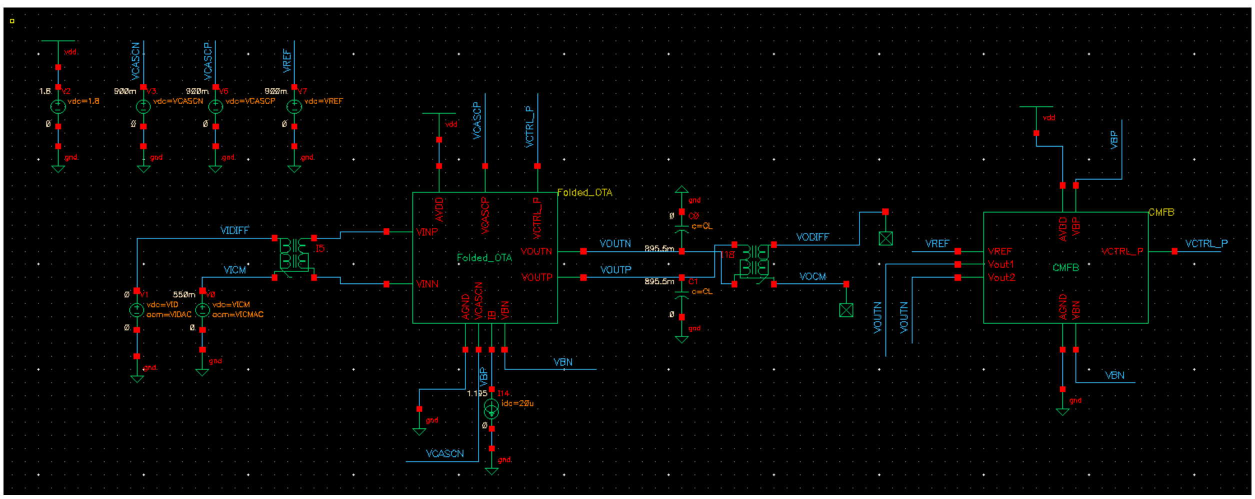
VCASCN & VCASCP Selection

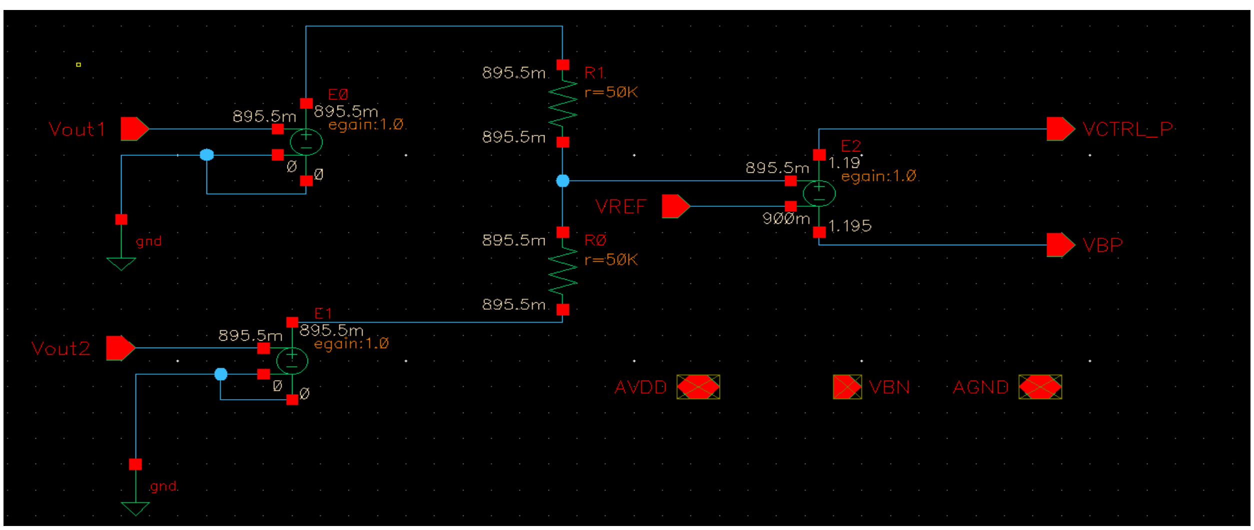
- VCASCN ≈ VGSN + V* = 0.5707 + 0.2029 = 0.77
- VCASCP ≈ VDD - |VGSP| - V* = 1.8 – 0.5497 – 0.2029 = 1.05
- Take margin for both (deeper in saturation) → VCASCN = VCASCP = 0.9V

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

DC OP







- V_{out_CM} = 895.5mV
- The differential input (4.5m) = differential output voltage (4.5m). The relation is the error amplifier gain.

Differential Small Signal

Circuit Parameters

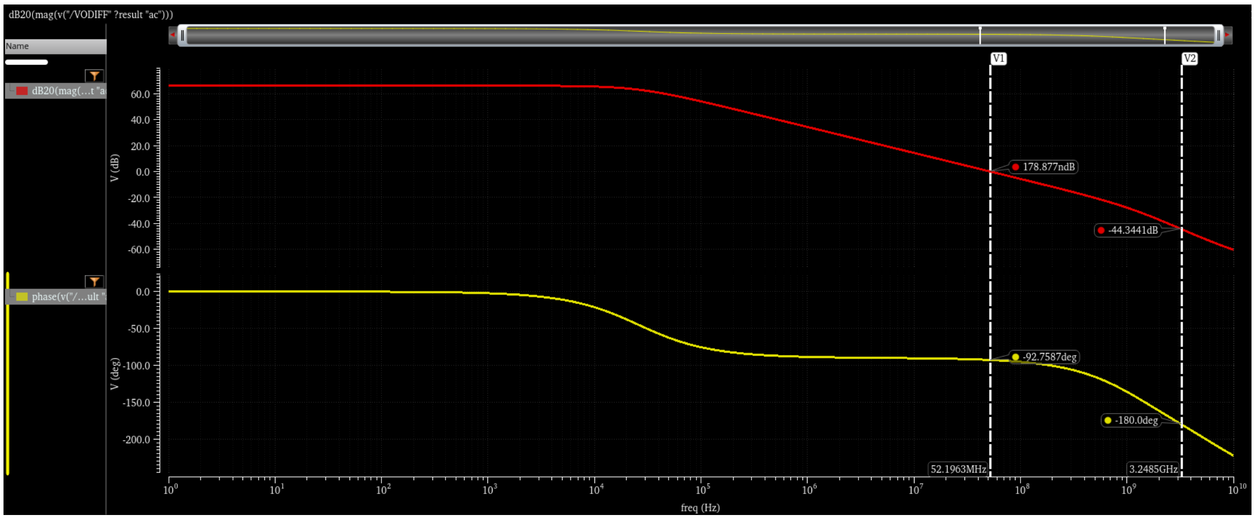
Name	Type	Details	Value
Ao	expr	ymax(mag(VF("/VODIFF")))	1.86K
Ao_dB	expr	dB20(ymax(mag(VF("/VODIFF"))))	65.39
BW	expr	bandwidth(VF("/VODIFF") 3 "low")	24.67K
UGF	expr	unityGainFreq(VF("/VODIFF"))	46.47M
GBW	expr	(Ao * BW)	45.87M
PM	expr	phaseMargin(v("/VODIFF" ?result "ac"))	87.87

Tuning:

- $ACL = \frac{AOL}{1+LG} \rightarrow AOL = 2(1+1000) = 2002$
- Increasing width of the input pair should increase the gain (W_{diff} = 10u).

Name	Type	Details	Value
Ao	expr	ymax(mag(VF("/VODIFF")))	2.011K
Ao_dB	expr	dB20(ymax(mag(VF("/VODIFF"))))	66.07
BW	expr	bandwidth(VF("/VODIFF") 3 "low")	25.86K
UGF	expr	unityGainFreq(VF("/VODIFF"))	52.4M
GBW	expr	(Ao * BW)	52.01M
PM	expr	phaseMargin(v("/VODIFF" ?result "ac"))	87.25

Differential Gain vs Frequency



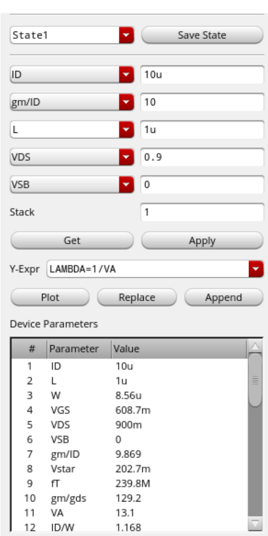
Hand Analysis

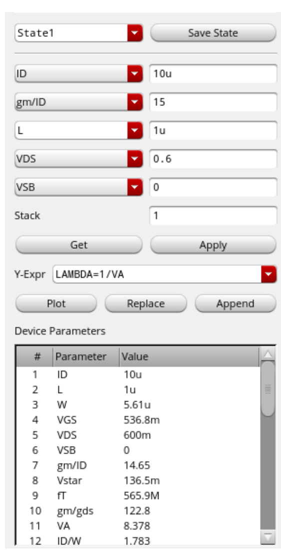
- $R_{out} = [ro_{casc_n}(1+(gm+gmb)(ro_{CM_n}||ro_{diff})] \;||\; \left[ro_{casc_p}\left(1+(gm+gmb)ro_{CM_p}\right)\right]$
- $R_{out} = [326.4k(1+(295.7+74)u*55.56k)]||[314k(1+(297.4+85.37)u*296.7k)]$ = 5.88MΩ
- Av$_{\text{diff}}$ $= gm_{diff} * R_{out} = 355.6u * 5.88M = 2091.2 = 66.4dB$
- $f_p \approx \frac{1}{2\pi * R_{out} * CL} = \frac{1}{2\pi(5.88M)(1p)}$ = 27.1K (parasitic capacitances are neglected in this calculation)
- GBW = UGF = Av*BW = 56.7 MHz
- PM = 90 - $\tan^{-1}\left(\frac{UGF}{\omega_{p_2}}\right)$ = 90 - $\tan^{-1}\left(\frac{52.2M}{3.25G}\right)$ = 89.1 deg

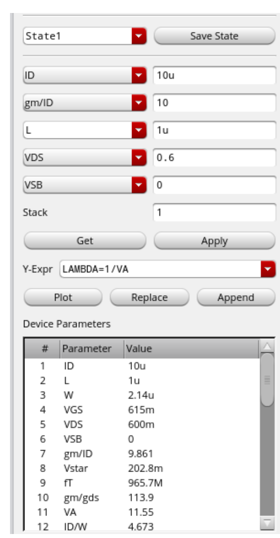
	Simulation	Hand Analysis
Av	2011	2091
Av (dB)	66.1	66.4
BW (KHz)	25.86	27.1
GBW (MHz)	52.0	56.7
UGF (MHz)	52.4	56.7
PM (deg.)	87.25	89.1

PART 4: Open-Loop OTA Simulation (Actual CMFB)

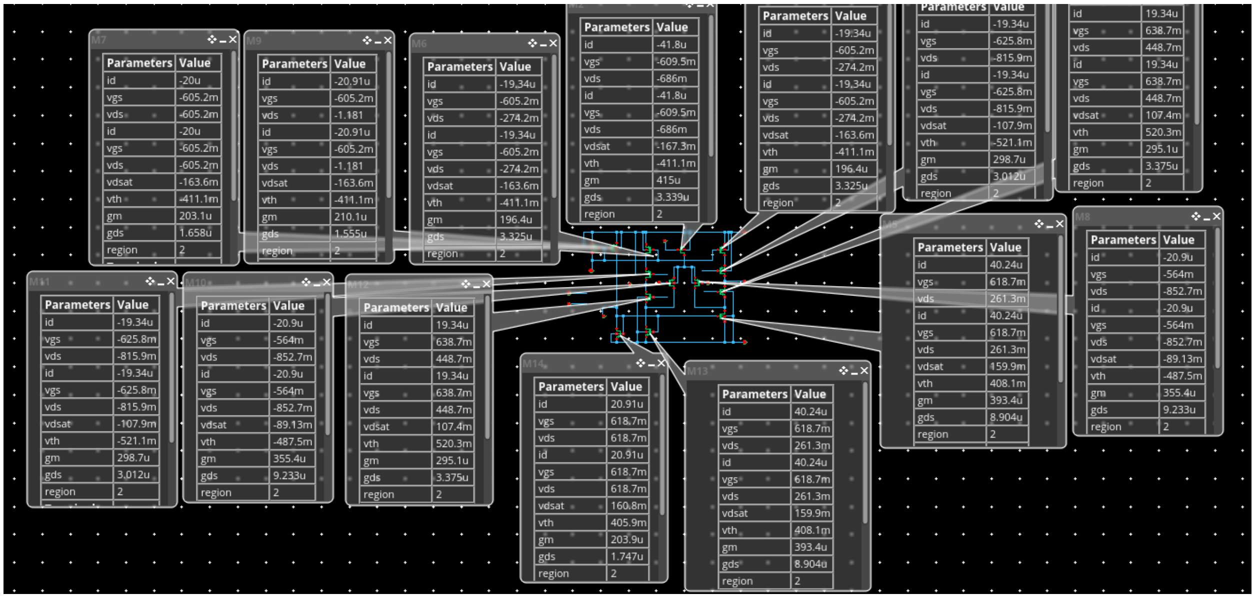
Sizing

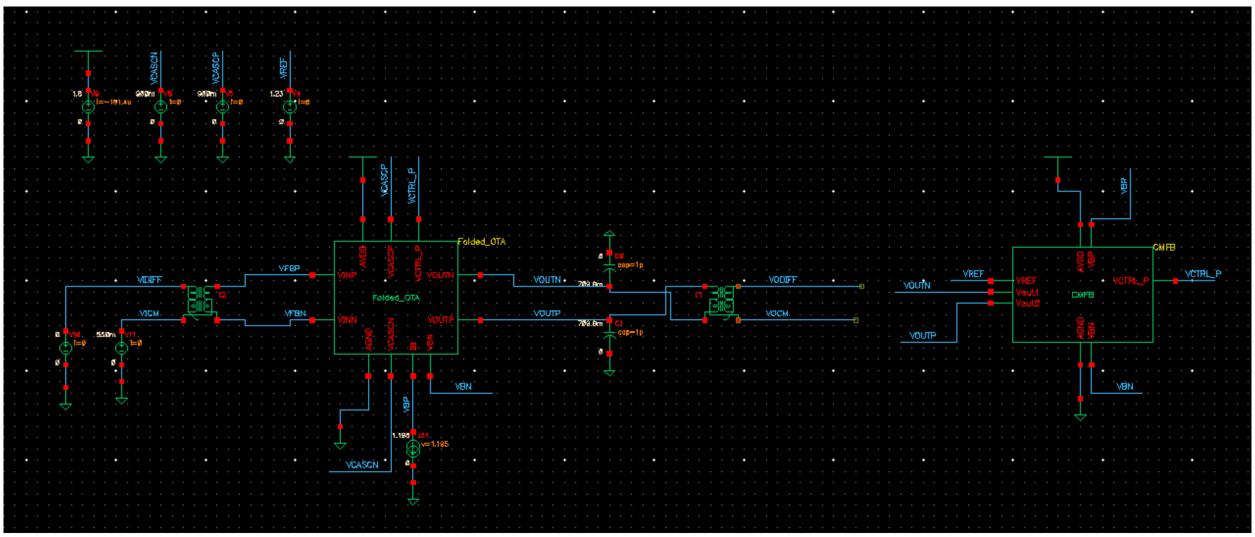


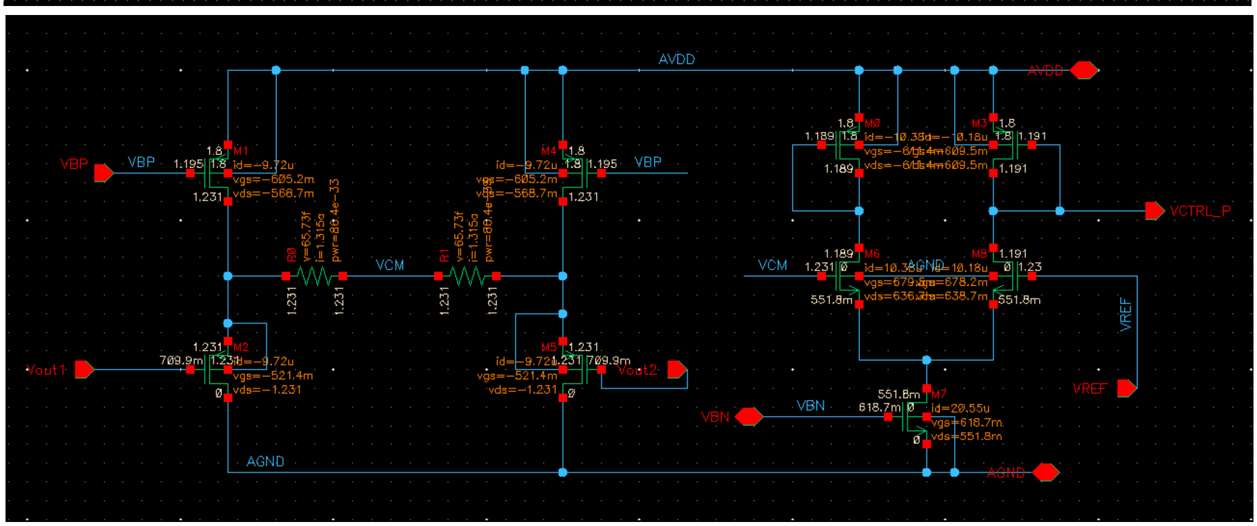




DC OP




Folded_OTA
VDIFF
VICM
VINP
VINN
VOUTN
VOUTP
VOCM
CMFB
VREF
VCTRL_P
VBN
VBP
VCASCN
VCASCP


AVDD
VBP
VCM
Vout1
Vout2
AGND
VCTRL_P
VREF
VBN

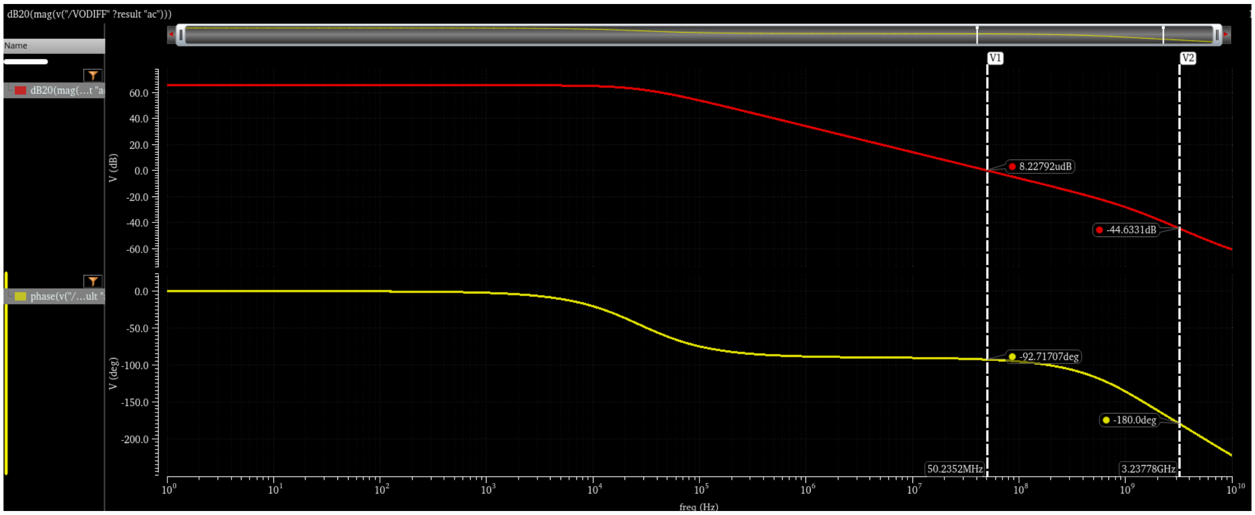
- Vref = 1.23V & VCM = 1.231v
- VOUTN = VOUTP = 709.mV
- The differential input (1m) & differential output voltage (4m). The relation is the error amplifier gain.

Differential Small Signal

Circuit Parameters

Name	Type	Details	Value
Av	expr	ymax(mag(VF("/VODIFF")))	1.858K
Av_dB	expr	dB20(ymax(mag(VF("/VODIFF"))))	65.38
BW	expr	bandwidth(VF("/VODIFF") 3 "low")	27.09K
GBW	expr	(Av * BW)	50.32M
UGF	expr	unityGainFreq(VF("/VODIFF"))	50.25M
PM	expr	phaseMargin(VF("/VODIFF"))	87.28

Differential Gain vs Frequency



Hand Analysis

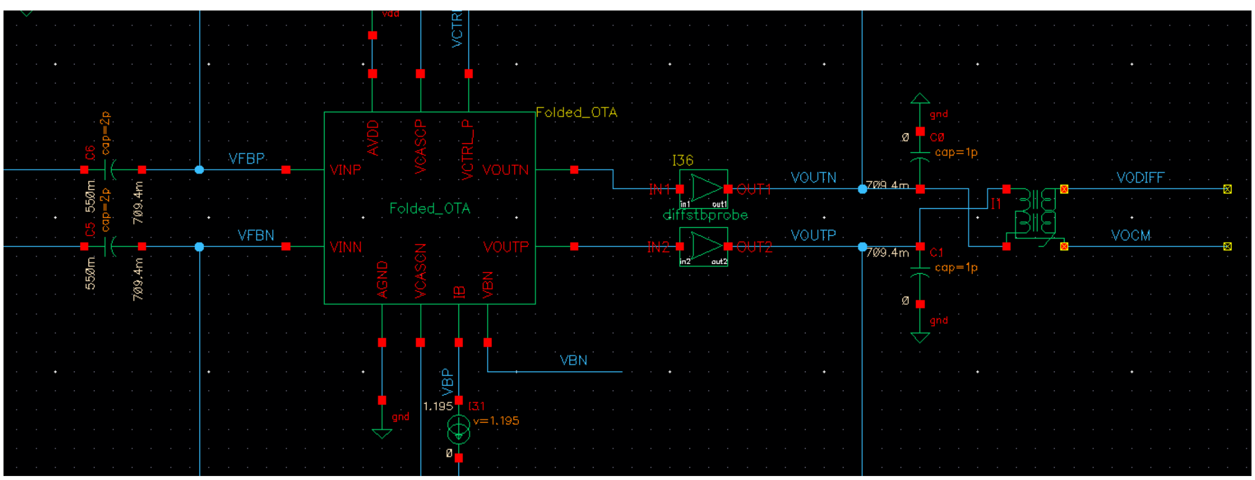
- $R_{out} = [ro_{casc_n}(1 + (gm + gmb)(ro_{CM_n}||ro_{diff})] \; || \; \left[ro_{casc_p}\left(1 + (gm + gmb)ro_{CM_p}\right)\right]$
- $R_{out} = [296.3k(1 + (295.1 + 73.9)u * 55.1k)]||[322k(1 + (298.7 + 84.2)u * 300.7k)]$ = 5.41MΩ
- Av$_{diff} = gm_{diff} * R_{out} = 355.4u * 5.41M = 1920 = 65.7dB$

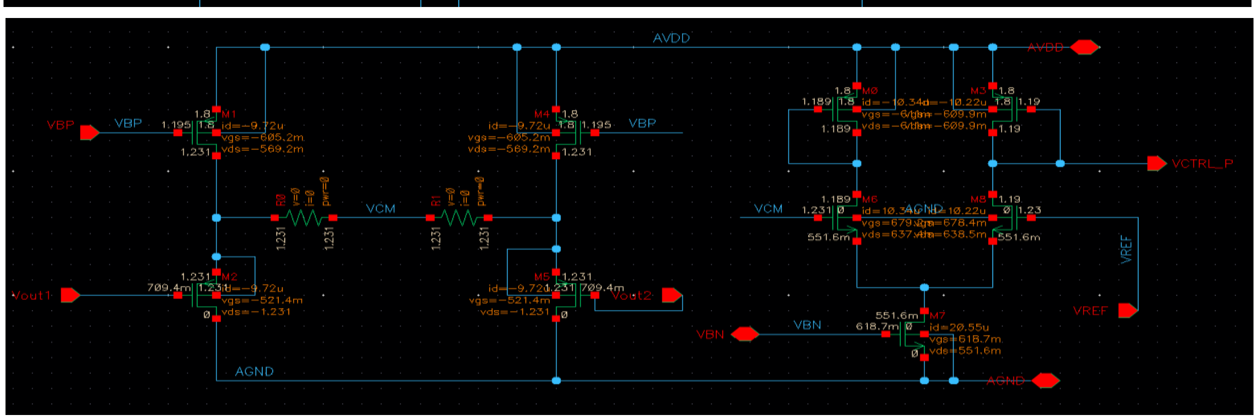
- $f_p \approx \frac{1}{2\pi * R_{out} * CL} = \frac{1}{2\pi(5.41M)(1p)}$ = 29.4K (parasitic capacitances are neglected in this calculation)
- GBW = UGF = Av*BW = 56.5 MHz
- PM = 90 - $\tan^{-1}\left(\frac{UGF}{\omega_{p_2}}\right) = 90 - \tan^{-1}\left(\frac{50.2M}{3.24G}\right)$ = 89.1 deg

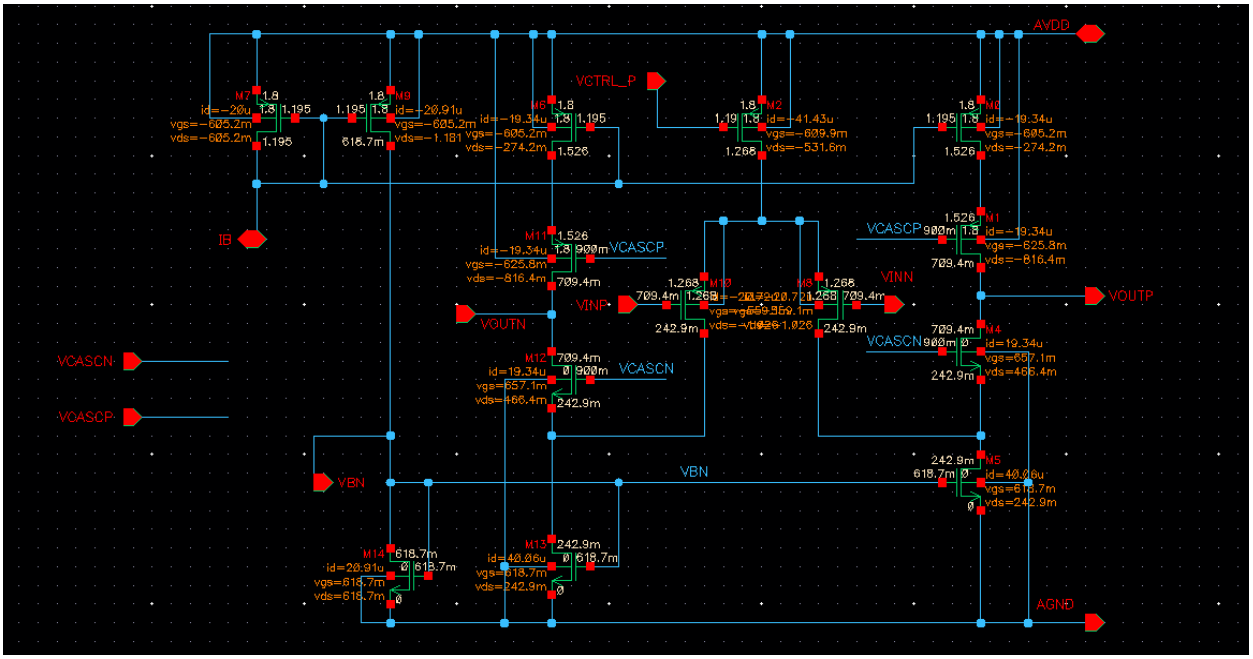
	Simulation	Hand Analysis
Av	1858	1920
Av (dB)	65.4	65.7
BW (KHz)	27.1	29.4
GBW (MHz)	50.3	56.5
UGF (MHz)	50.3	56.5
PM (deg.)	87.3	89.1

PART 5: Closed Loop Simulation (AC and STB Analysis)

DC OP







- V_{out_CM} = 709.4mV → CMFB will reduce error till CM = Vref.
- V_{in_CM} = 709.4mV → due to feedback V_{out_CM} = V_{in_CM}

Differential Closed-Loop Response

Name	Type	Details	Value
Av	expr	ymax(mag(VF("/VODIFF")))	1.997
Av_dB	expr	dB20(ymax(mag(VF("/VODIFF"))))	6.007
BW	expr	bandwidth(VF("/VODIFF") 3 "low")	10.9M
GBW	expr	(Av * BW)	21.77M
UGF	expr	unityGainFreq(VF("/VODIFF"))	19.35M
PM	expr	phaseMargin(VF("/VODIFF"))	96.14

Differential & CMFB Loops Stability (STB analysis)

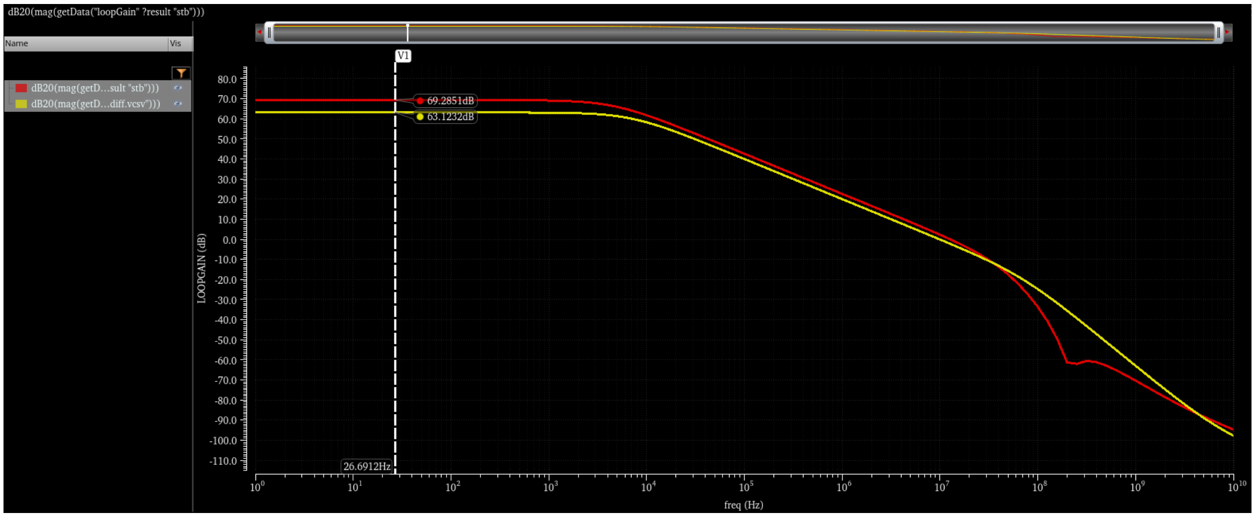
Note

After the first run, we didn't meet the loop gain spec, so we multiply L & W of NMOS cascode transistor with factor of 4 (W=21.24u & L=4u).

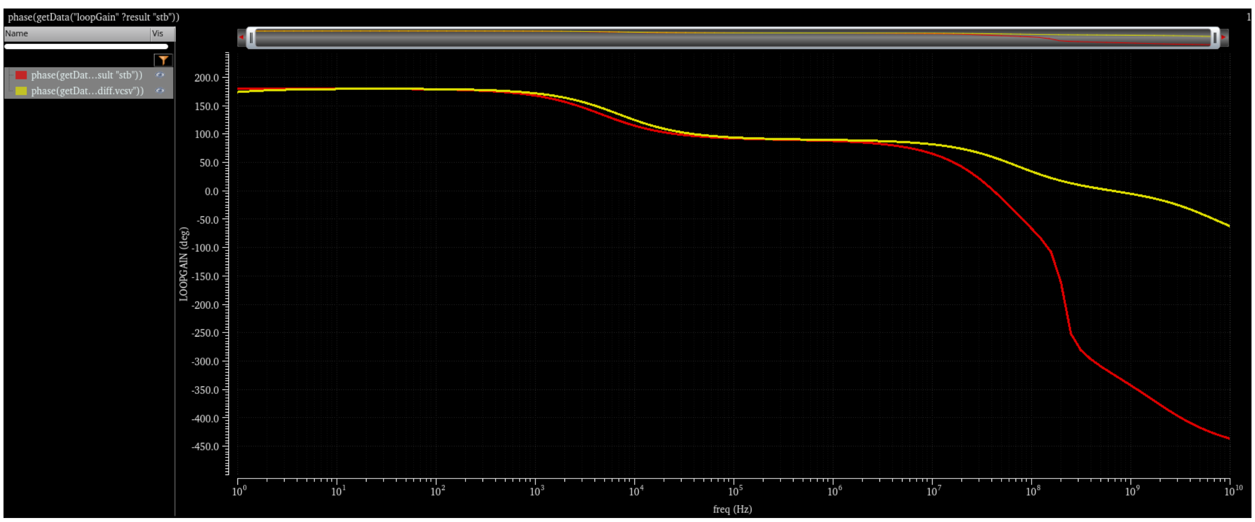
AC Parameters

Name	Type	Details	Value
Av	expr	ymax(mag(VF("/VODIFF")))	1.999
Av_dB	expr	dB20(ymax(mag(VF("/VODIFF"))))	6.015
BW	expr	bandwidth(VF("/VODIFF") 3 "low")	13.63M
GBW	expr	(Av * BW)	27.25M
UGF	expr	unityGainFreq(VF("/VODIFF"))	25.26M
PM	expr	phaseMargin(VF("/VODIFF"))	70.03

Magnitude (dB)



Phase



Differential

phaseMargin(getData("loopGain" ?r...

	Expression	Value	Expression	Value
1	gainBwProd(get...	9.899E6	phaseMargin(ge...	81.98

Common

gainBwProd(getData("loopGain" ?re...

	Expression	Value	Expression	Value
1	gainBwProd(get...	13.54E6	phaseMargin(ge...	59.04

Comparisons

	Differential Loop	Common Loop
GBW (MHz)	9.90	13.5
PM (deg.)	82	59

Comments: Both differential and common loops are stable (PM > 45 deg). Differential loop meets the phase margin spec. Common loop has a relatively poor phase margin. Common loop GBW is higher than differential GBW.

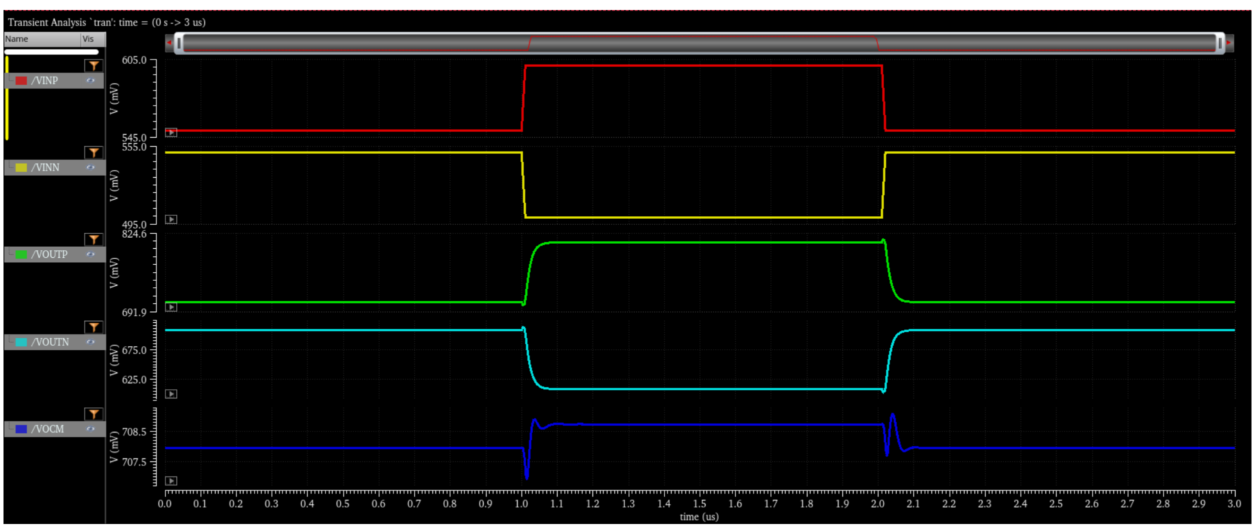
	STB	Open-Loop
GBW (MHz)	9.90	50.3
Loop Gain (dB)	63.1	66.2

Comments: Open-loop LG is higher than STB's LG because of the change in beta after adding the feedback capacitors. GBW is lower in closed loop due to decrease in gain.

PART 6: Closed Loop Simulation (Transient Analysis)

Differential & CMFB Loops Stability

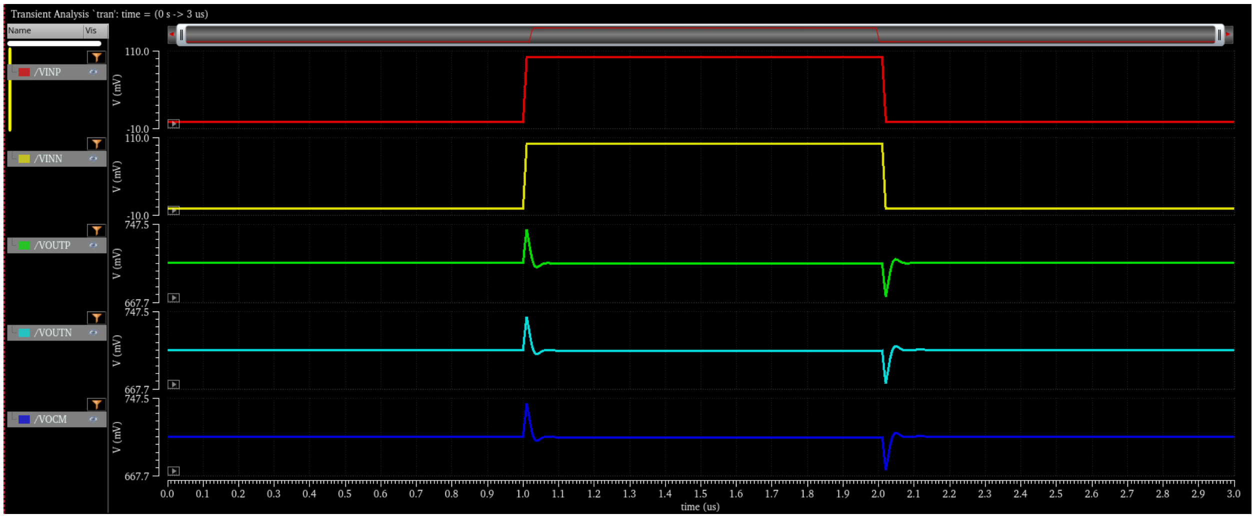
Differential Input



Comment: There is no ringing in differential loop, but there is ringing in the common loop.

There is no spec on common loop PM, but increasing PM would reduce the ringing.

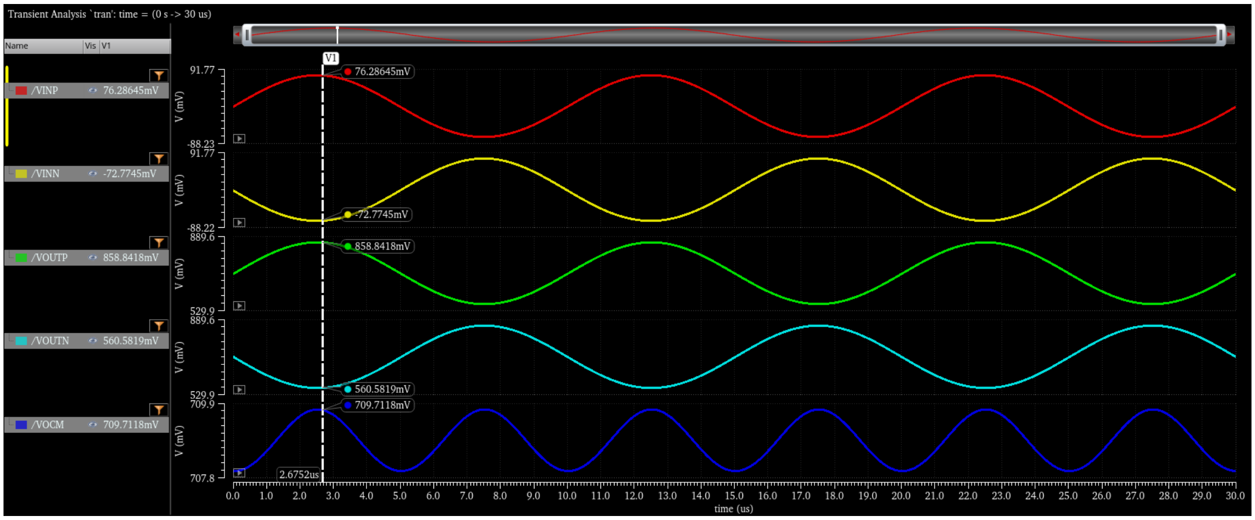
Common Input



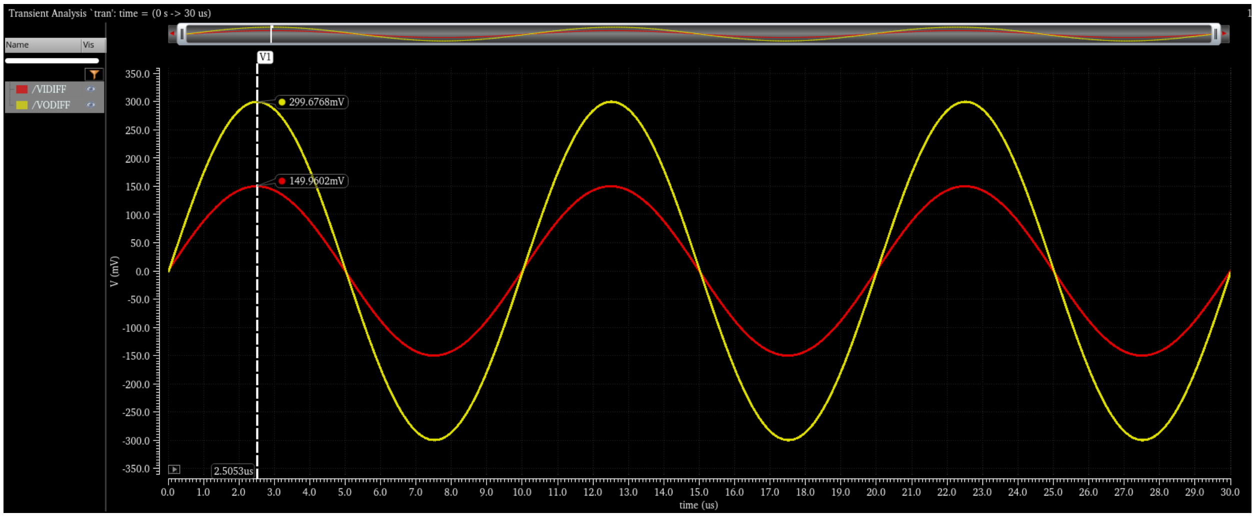
Comment: There is no ringing in differential loop, but there is small ringing in the common loop.

Output Swing

VINP, VINN, VOUTP, VOUTN, and VOCM



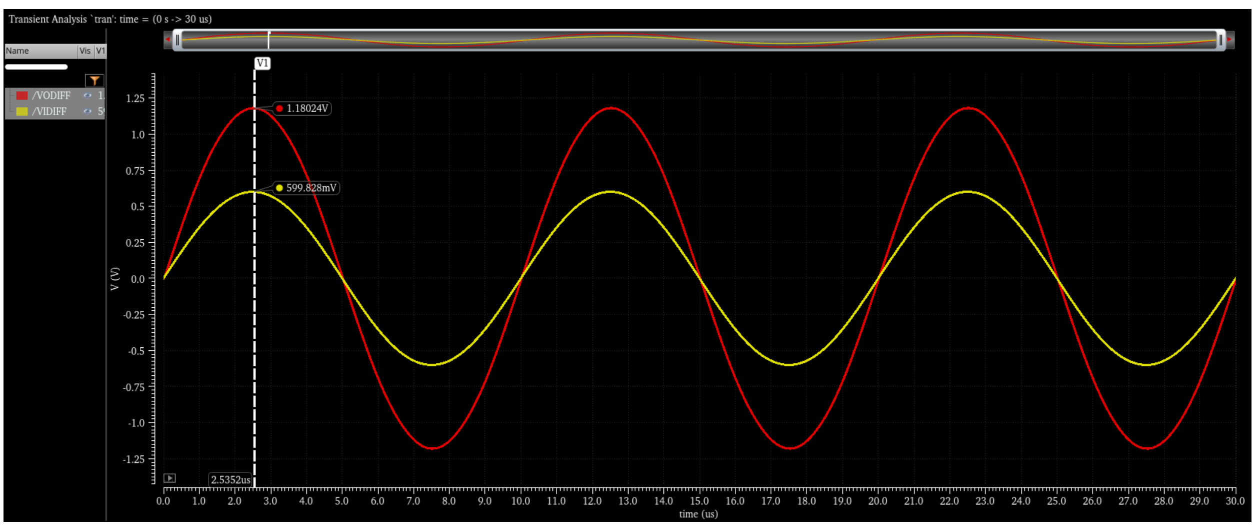
VIDIFF and VODIFF



Type	Details	Value
expr	peakToPeak(VT("/VIDIFF"))	300m
expr	peakToPeak(VT("/VODIFF"))	599.5m

ACL	expr	ymax(mag(VF("/VODIFF")))	1.999

Spec Check



We can achieve more than 1.2pk-to-pk swing.

Acknowledgments

As this is the final lab and project in the training, I would like to express my heartfelt gratitude to Dr. Hesham for his outstanding guidance and support throughout the past two months. He has been a great mentor and a source of inspiration for me. I also want to thank the teaching assistants, Eng. Roshan and Eng. Rawan, for their invaluable help in the labs. They have been very patient and helpful in debugging errors for everyone. Thank you for everything!