Analog IC Design

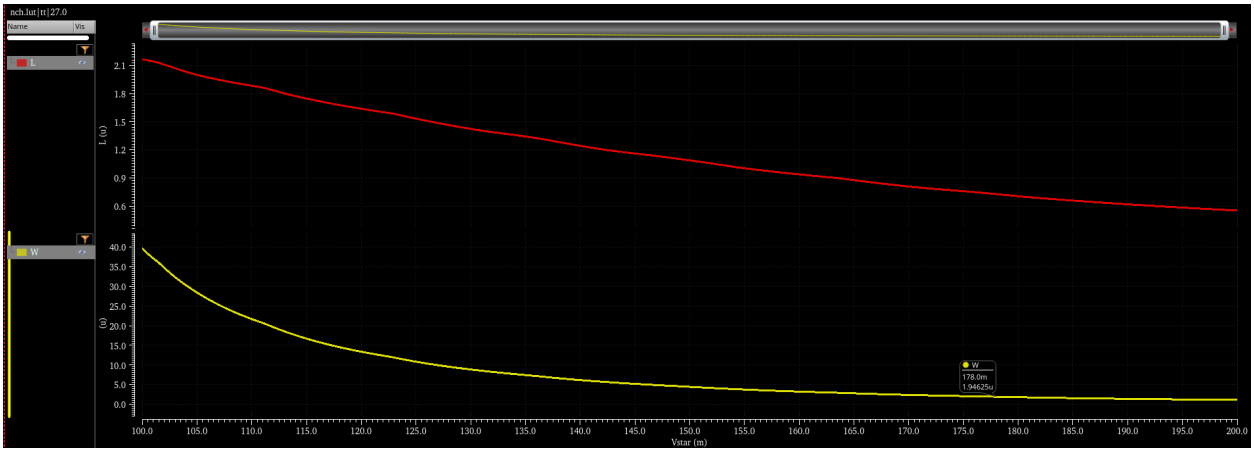
Lab 5

Part 1: Sizing Chart

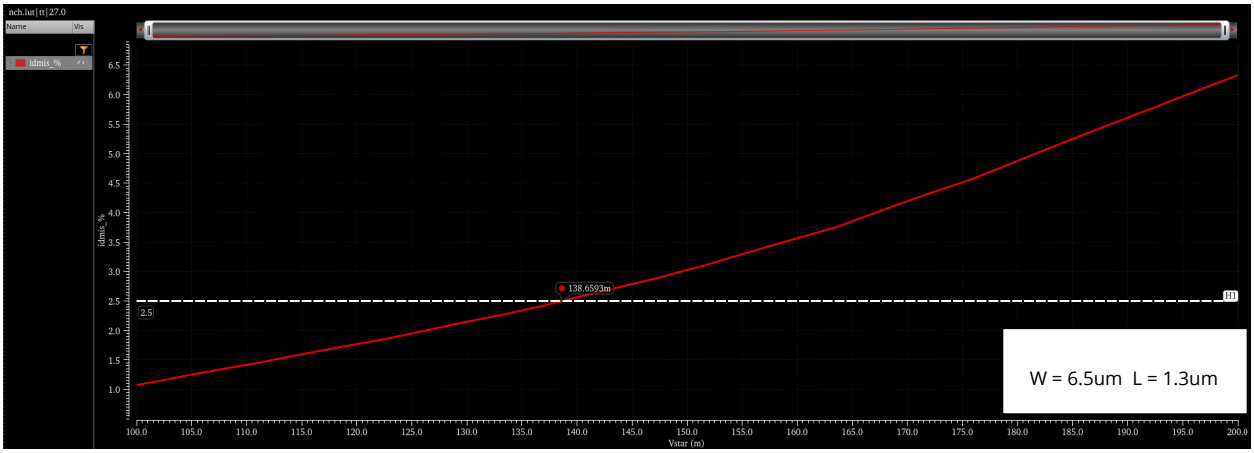
Answer The Following

- $\lambda = 0.1$
- **NMOS** sinks current.

L & W vs V*



Current Mismatch vs V*

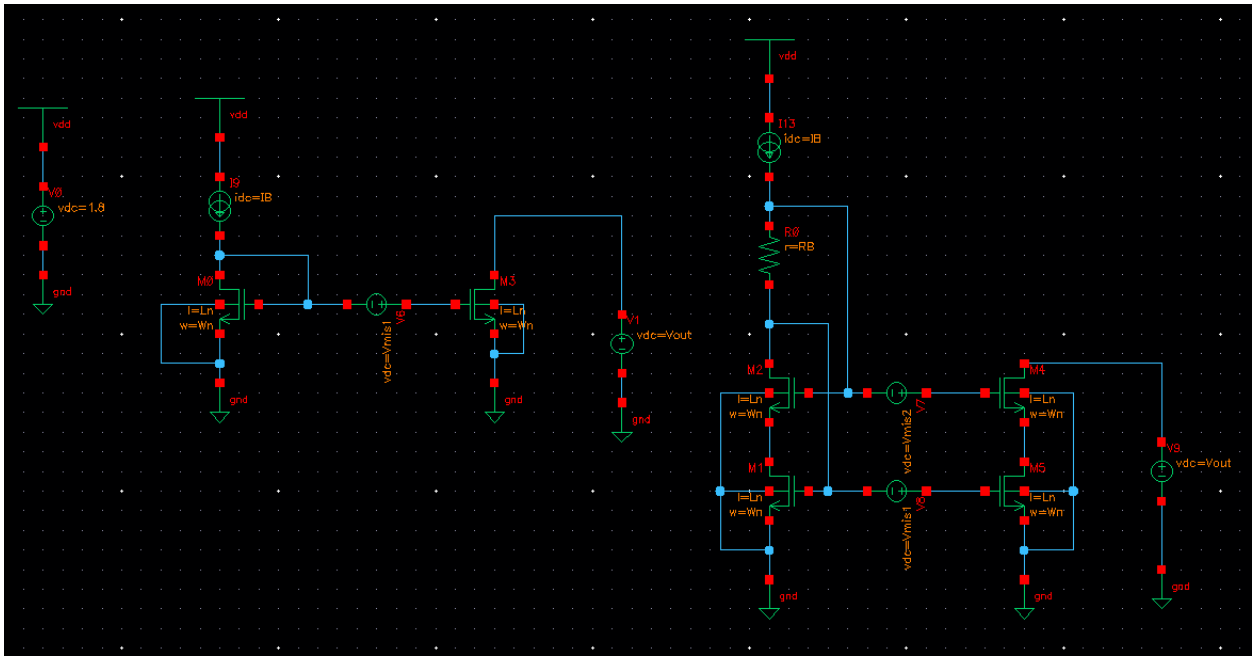


Is It Possible to Use Standard SPICE Simulators?

This is not possible, because standard SPICE simulators cannot keep λ constant as it depends on region of operation and how deep is the transistor in saturation.

Part 2: Current Mirror Simulation

Schematic



DC OP

RB Selection

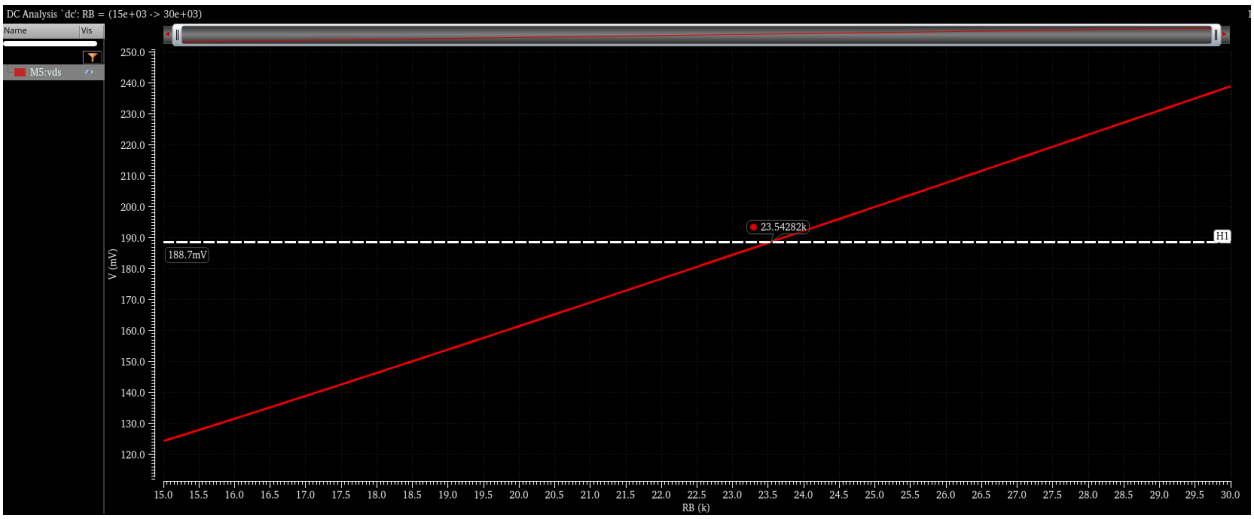
Theoretical: RB = (50m+138.7m)/10u = 18.87k ≈ 19 kΩ

Simulation: RB = 23.5 kΩ

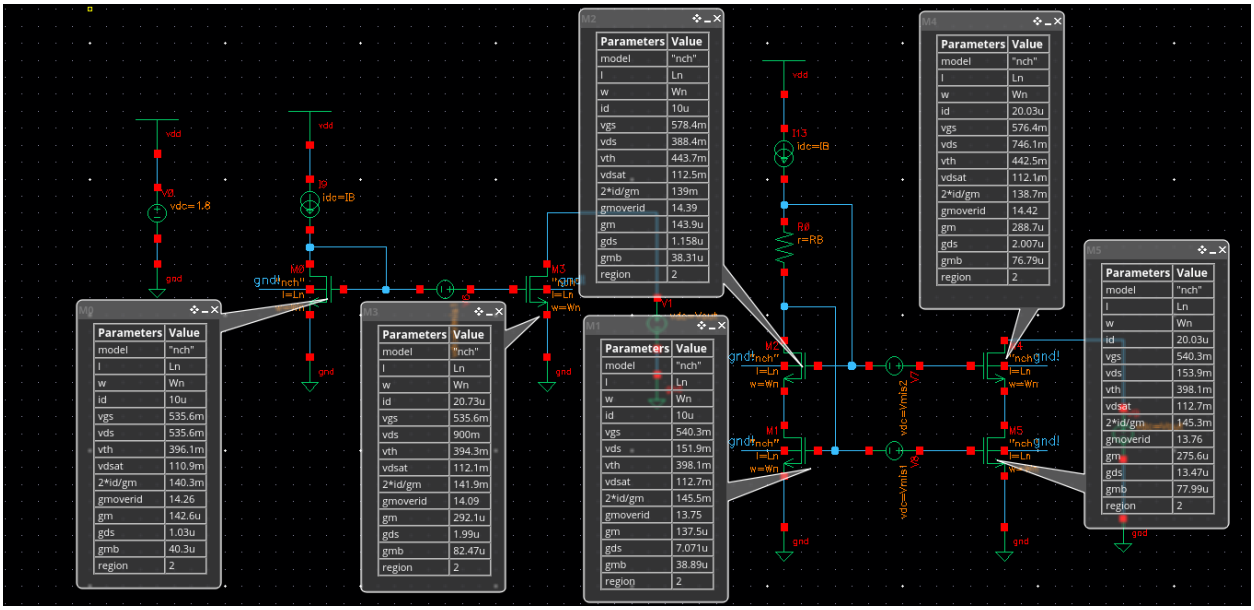
Comment: $RB_{simulation} > RB_{theoretical}$.

The theoretical calculation we assumed that (VGS1 = VGS2 in my schematic). However, this is not true because the source of M2 is not connected to ground.

RB = $(VGS2+VDS1-VGS1)$/IB → The accurate rule



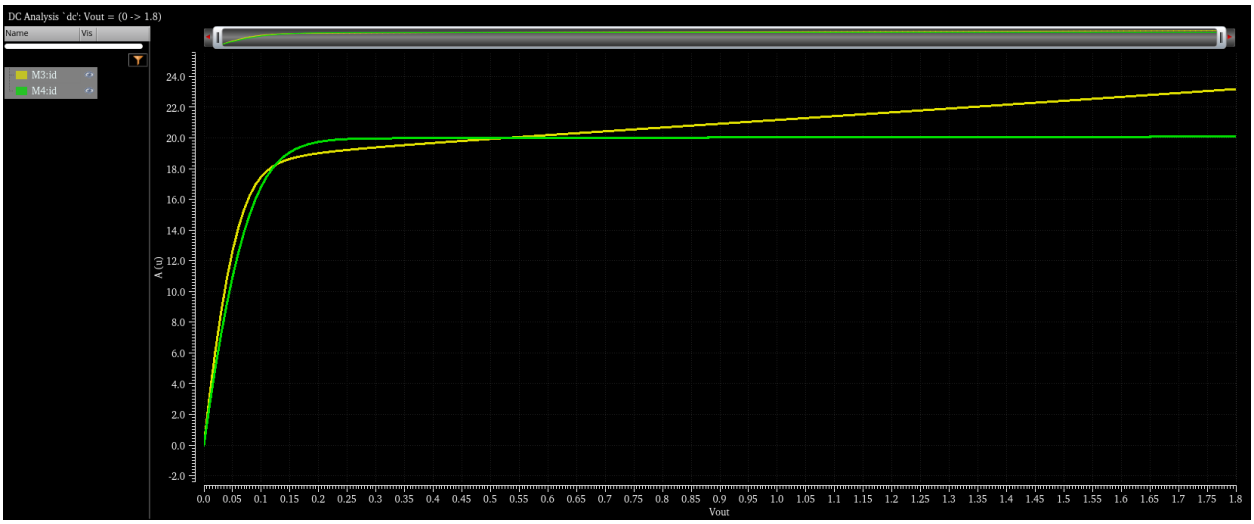
Parameters' Balloons



Comment: All transistors operate in saturation.

DC Sweep (I_{out} vs V_{out})

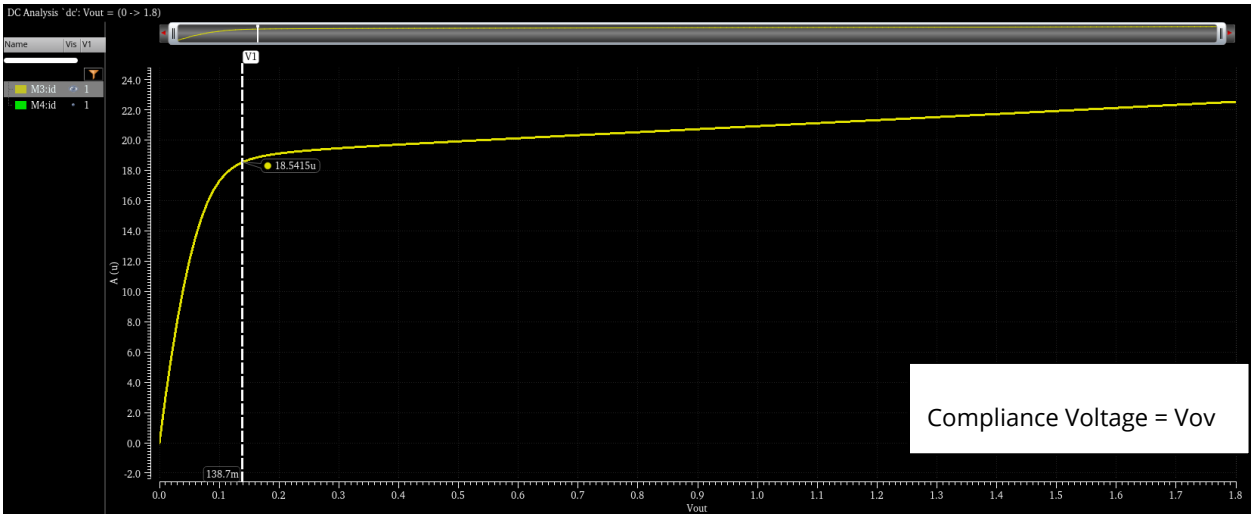
Overlaid Graphs



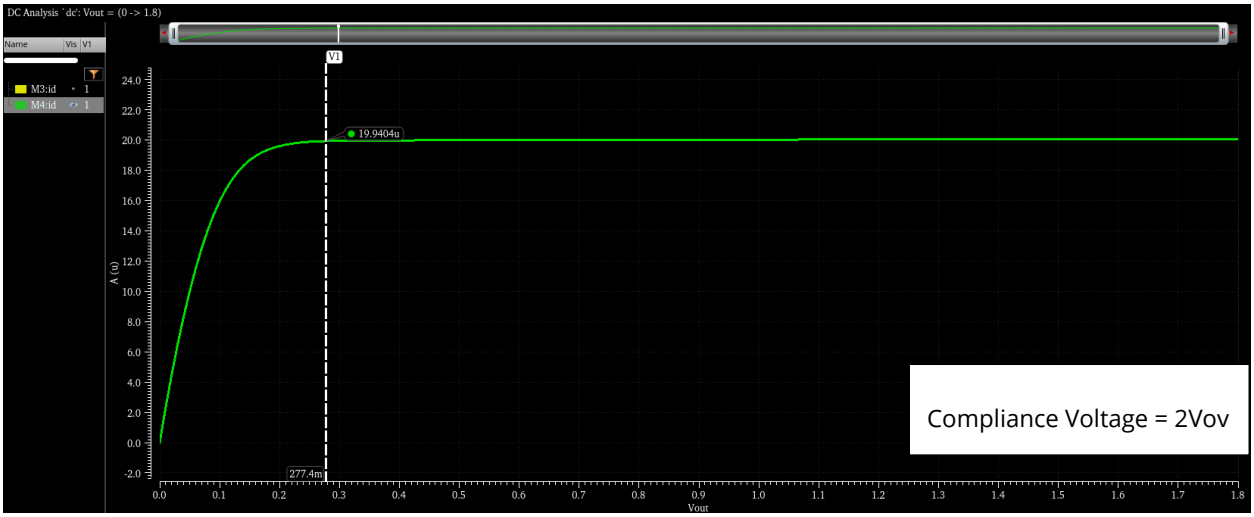
Comment:

There are more variations in Iout in the simple CM, as it has a higher slope in saturation region. This is due to the differences in Rout and VDS, which we will discuss below.

Current at Compliance Voltage (Simple CM)



Current at Compliance Voltage (Cascode CM)

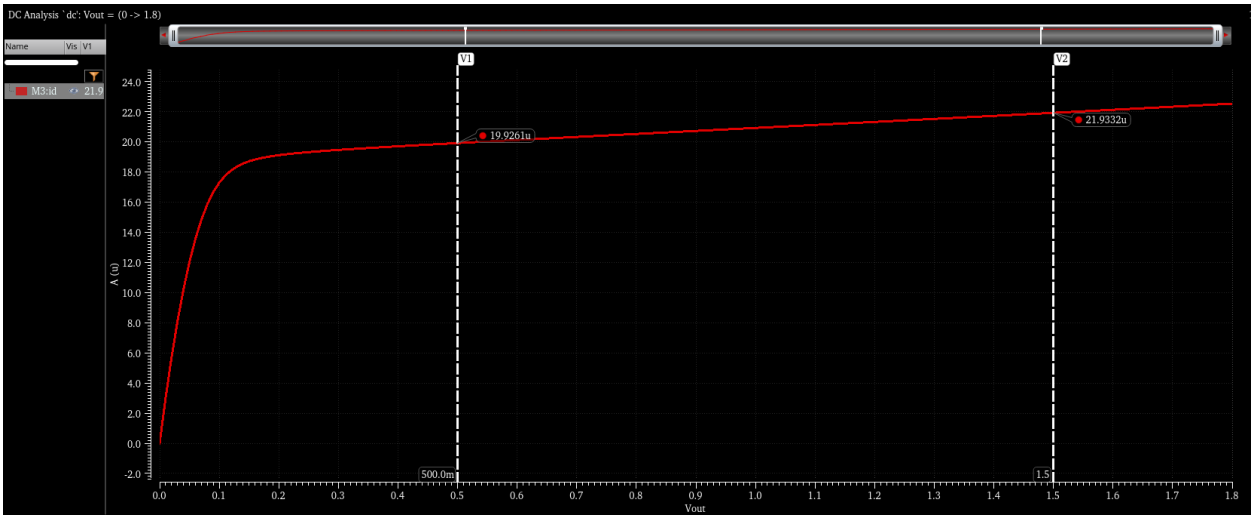


When does I_{out} = 2*IB exactly?

Iout = 20u at Vout = VGS, because VDS0 = VDS3 since:

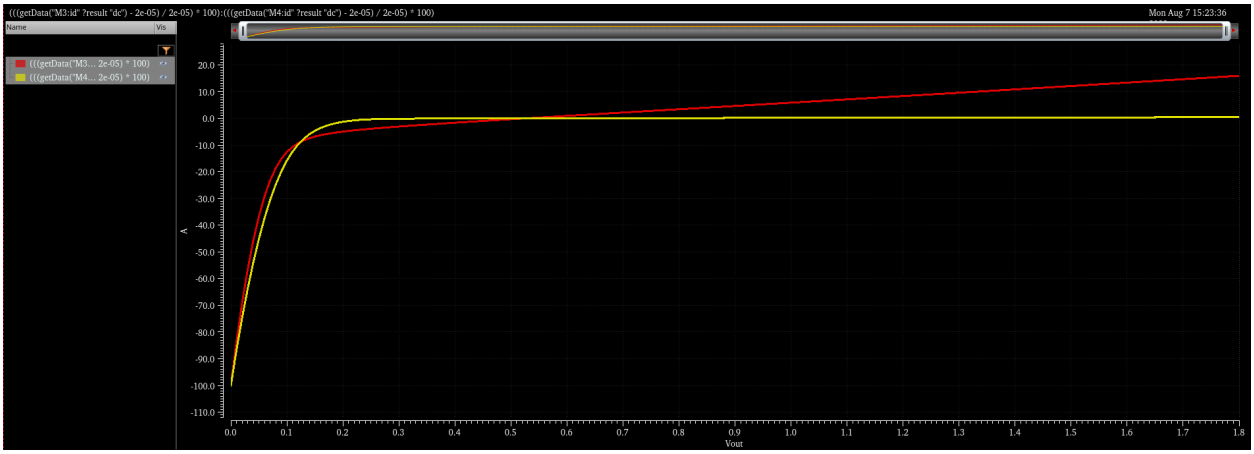
- VGS0 = VDS0 (diode-connected)
- VGS0 = VDS3 (direct connection)

Simple CM Current Change Percentage



$$\Delta I_{out} = \frac{(21.9u - 19.9u)}{20u} = 10\% \rightarrow > 2.5\% \text{ (In DC sweep not in DC OP)}$$

Error Percentage

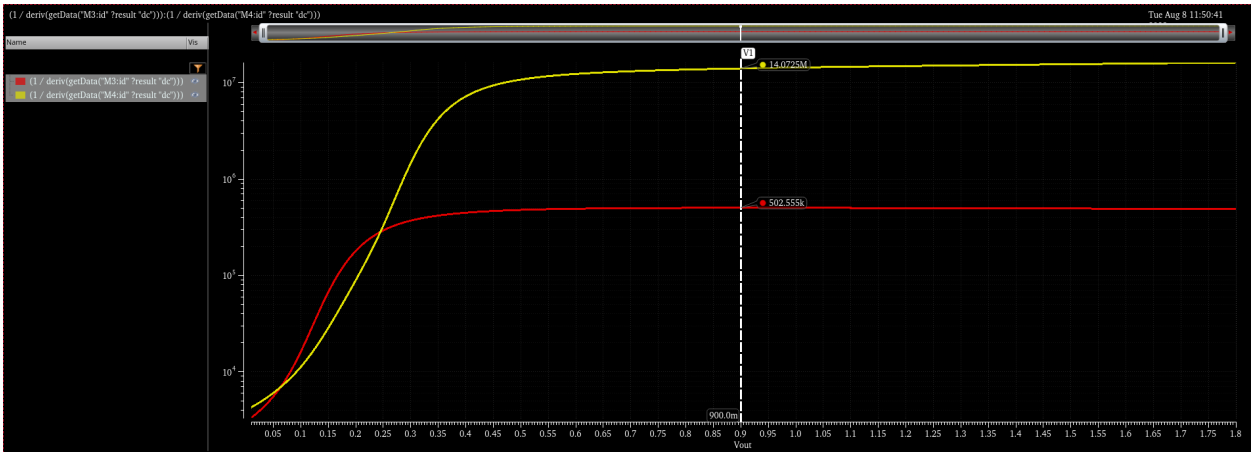


Comment:

As Vout increases, simple CM has higher error percentage, due to the current dependence on VDS. In cascode CM, M2 & M4 ensures that VDS of mirroring transistors are equal.

$$\frac{I_{out}}{I_{REF}} = \frac{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_B - V_{TH})^2(1 + \lambda_2 V_{DS2})}{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_B - V_{TH})^2(1 + \lambda_1 V_{DS1})}$$

Rout vs Vout



Comments:

- Rout cascode CM is much higher than the simple CM.
- Rout changes with Vout due to dependence of ro on VDS (VA = f(VDS) & ro = VA/ID).

Analytic Calculation of Rout

- **Simple CM:** Rout = ro_3 = 1/gds_3 = 500kΩ
- **Cascode CM:** Rout = $ro_4[1+(gm_4 + gmb_4)ro5]$ = 14.04MΩ

	Rout (Simulation)	Rout (Theoretical)
Simple CM	502.6k	500k
Cascode CM	14.07M	14.04M

Mismatch

Current Nominal Value Without Mismatch

M3:id M4:id

	Name	Value
1	M3:id	20.73E-6
2	M4:id	20.01E-6

CM Mismatch (Vmis1)

M3:id M4:id

	Name	Value
1	M3:id	21.24E-6
2	M4:id	20.49E-6

- **Simple CM:** $\frac{\Delta I_{out}}{I} = \frac{(21.24u-20.73u)}{20.73u} = 2.46\%$
- **Cascode CM:** $\frac{\Delta I_{out}}{I} = \frac{(20.49u-20.01u)}{20.01u} = 2.40\%$
- **Analytic Calculations:** $\frac{\Delta I_{out}}{I} = \frac{2*V_{mis}}{Vov} = \frac{2*1.72m}{(535.6-394.3)m} = 2.43\%$

Cascode Mismatch (Vmis2)

M4:id

	Name	Value
1	M4:id	20.02E-6

- **Cascode CM:** $\Delta I_{out} = \frac{(20.02u-20.01u)}{20.01u} = 0.05\%$
- **Analytic Calculations:** $\frac{\Delta I_{out}}{I} = \frac{Gm*V_{mis}}{I_{ref}} = \frac{gm*V_{mis}}{I_{ref}[1+(gm+gmb)ro]} = 0.09\ \%$

Comments

- Current mirror mismatch has a larger effect on the current's percentage change, because current in CM depends on the parameters' ratio between the reference source and the CM, so any change Vth would affect this ratio.
- Using larger W & L is better, as this decreases the standard deviation of Vth.