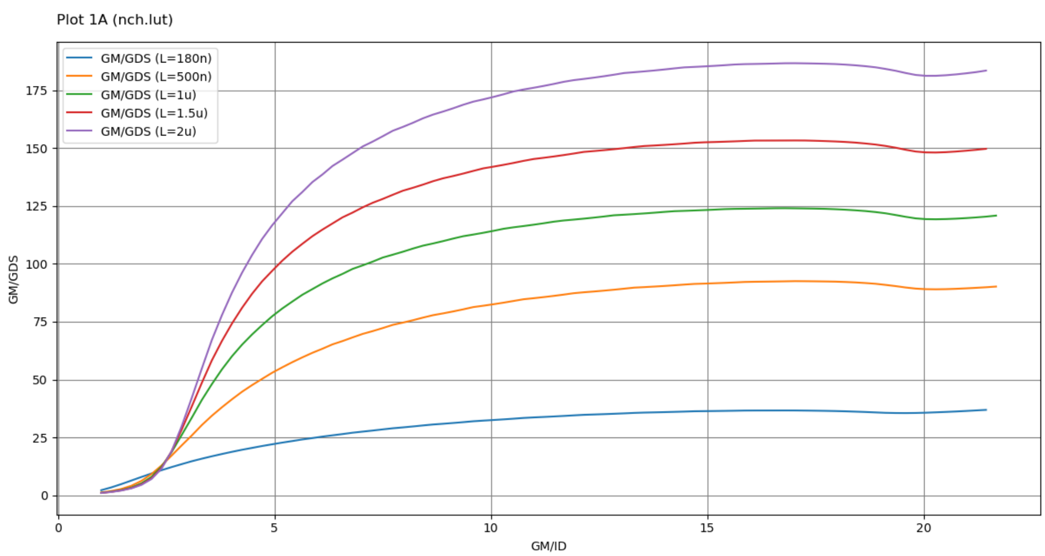
Analog IC Design

Lab 7

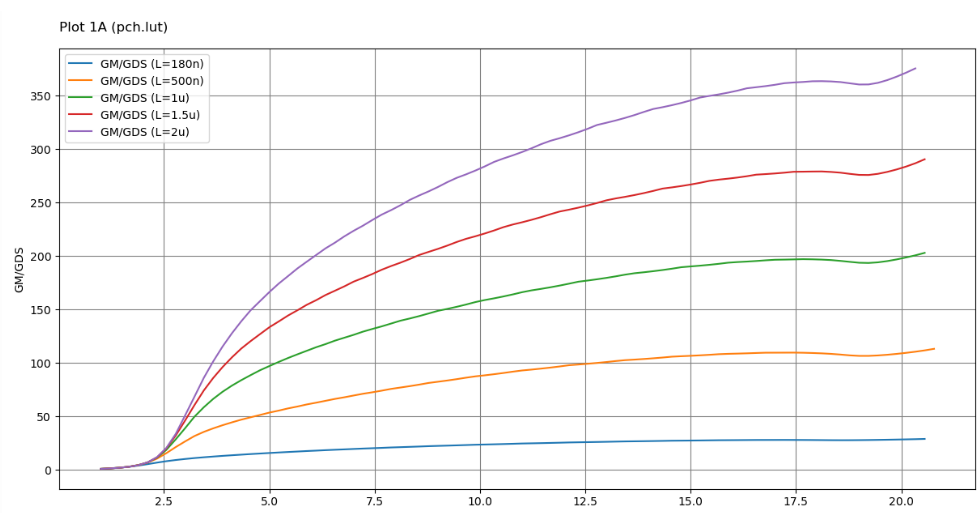
Part 1: gm/ID Design Charts

gm/gds

NMOS

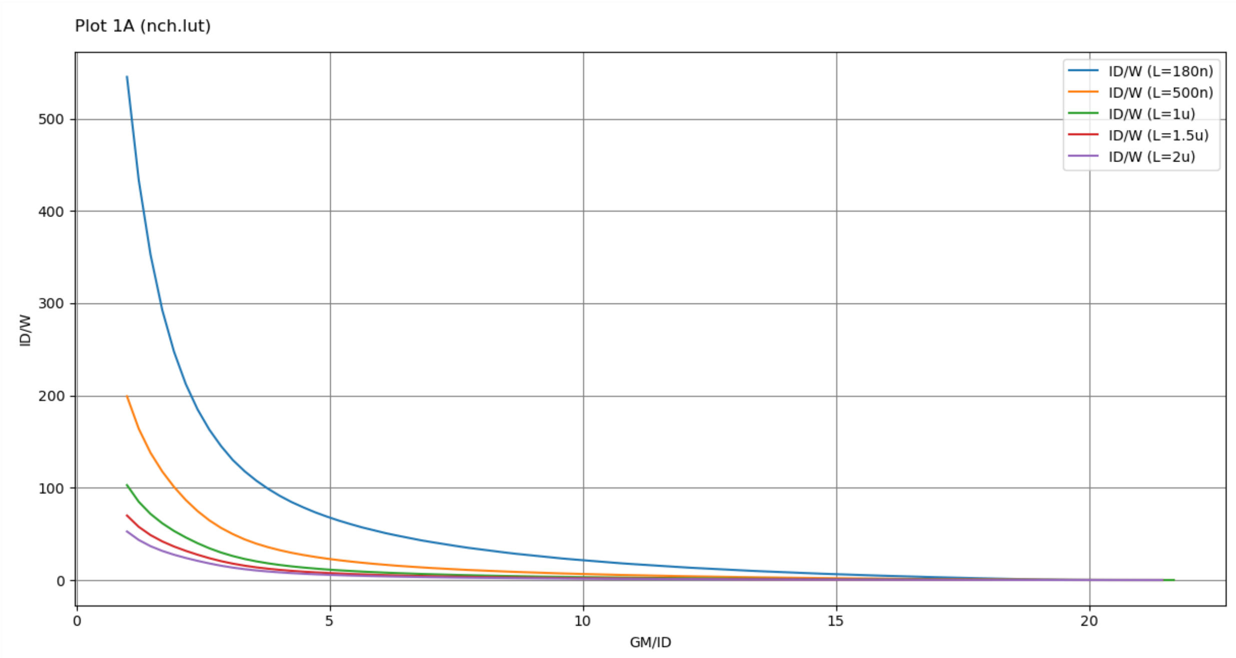


PMOS

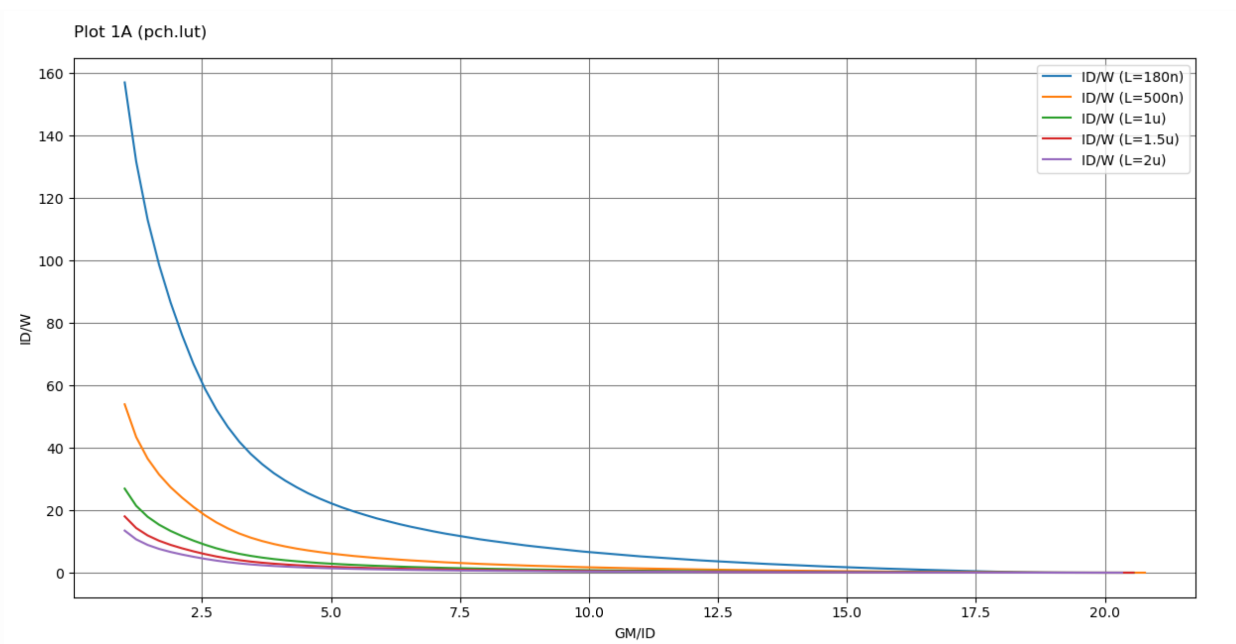


ID/W

NMOS

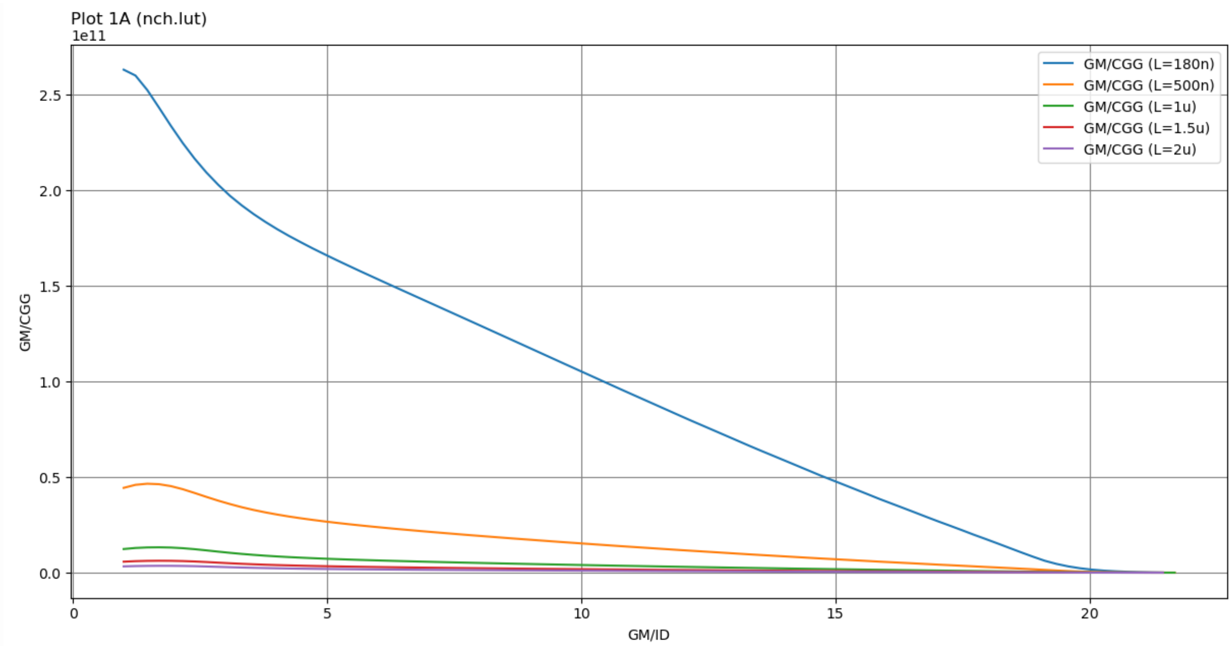


PMOS

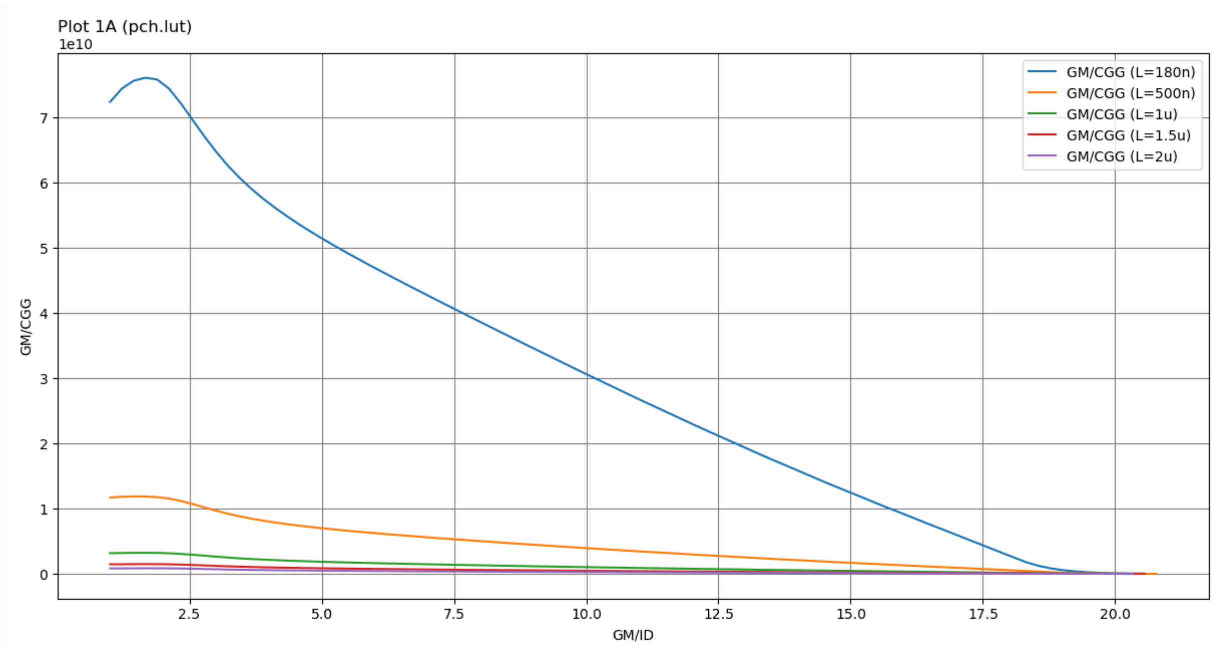


gm/Cgg

NMOS

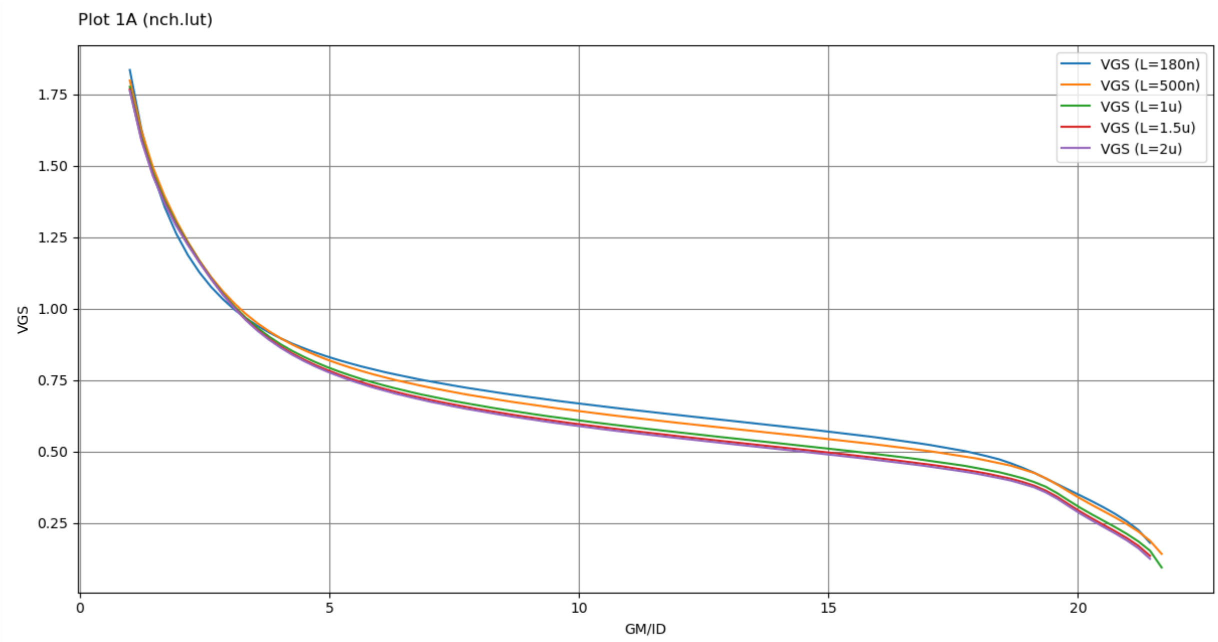


PMOS

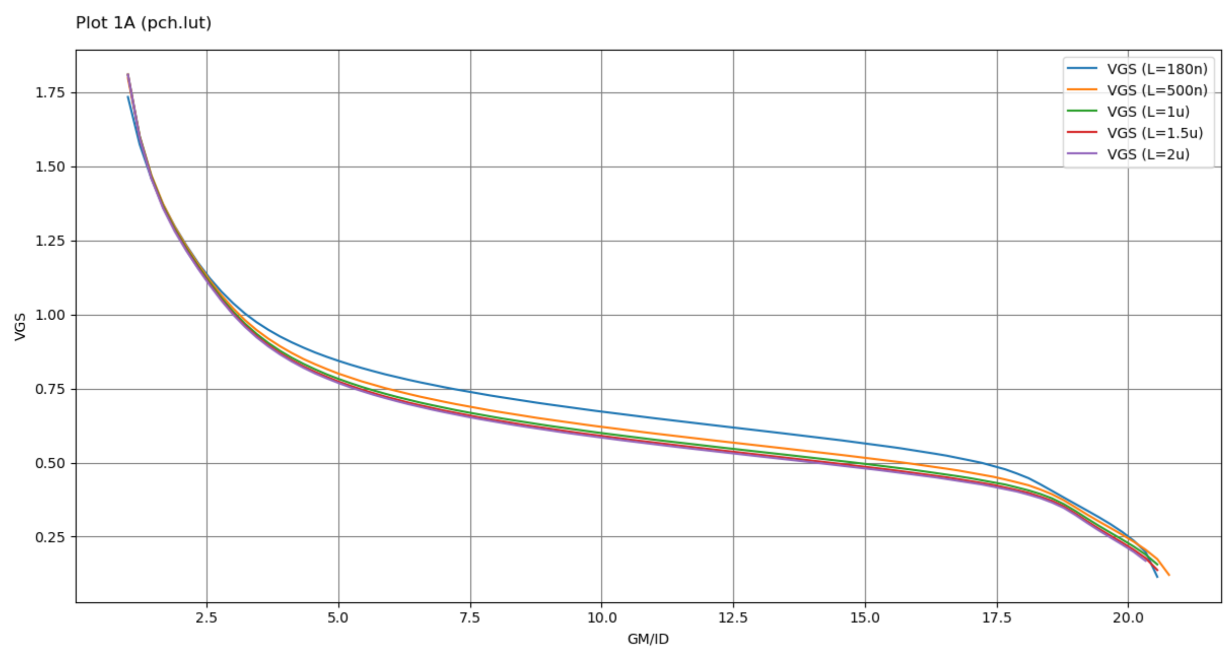


VGS

NMOS



PMOS

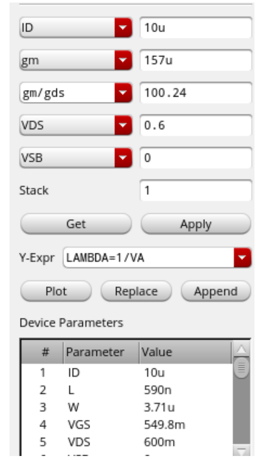


Part 2: OTA Design

Differential Pair Sizing

- GBW = $\frac{gm}{2\pi CL}$ → gm = 157uS
- ID = 10u → gm/ID = 15.7
- Av = gm*ro/2 = 34dB = 50.1 (assume ro_{diff} = ro_{PMOS})
- gm/gds = 100.24
- Assume VDS = 0.6V & VSB = 0V

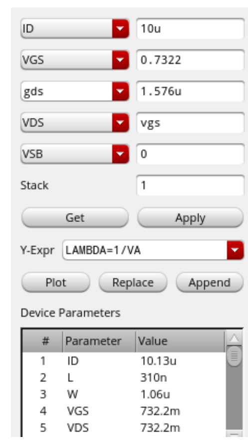
L = 590nm, W = 3.71u



Design Loads PMOS Sizing

- Since we assumed ro_{diff} = ro_{PMOS} → gds_{PMOS} = gds_{diff} = 1.576u
- VGS = VDS = VDD-[VCM_{max} – Vth] = 732.2mV
- ID = 10u
- VSB = 0

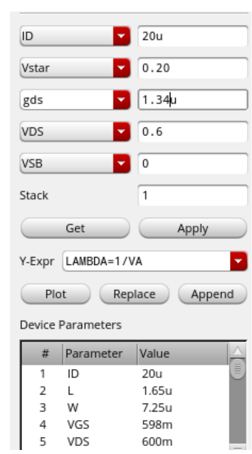
L = 310nm, W = 1.06u



Current Mirror Sizing

- Av_{CM} = 34 – 74 = -40dB = 0.01
- Av_{CM} = $\frac{gds_{CM}}{2*gm_{PMOS}}$ → gds_{CM} = 2*0.01*(66.79u) = 1.34u
- V* = VCM_{min} – VGS_{diff} = 0.8-0.5498 = 0.25V → use V* =200mV
- ID = 20uA
- VSB = 0 & VDS = 0.6

L = 1.65u W = 7.25u

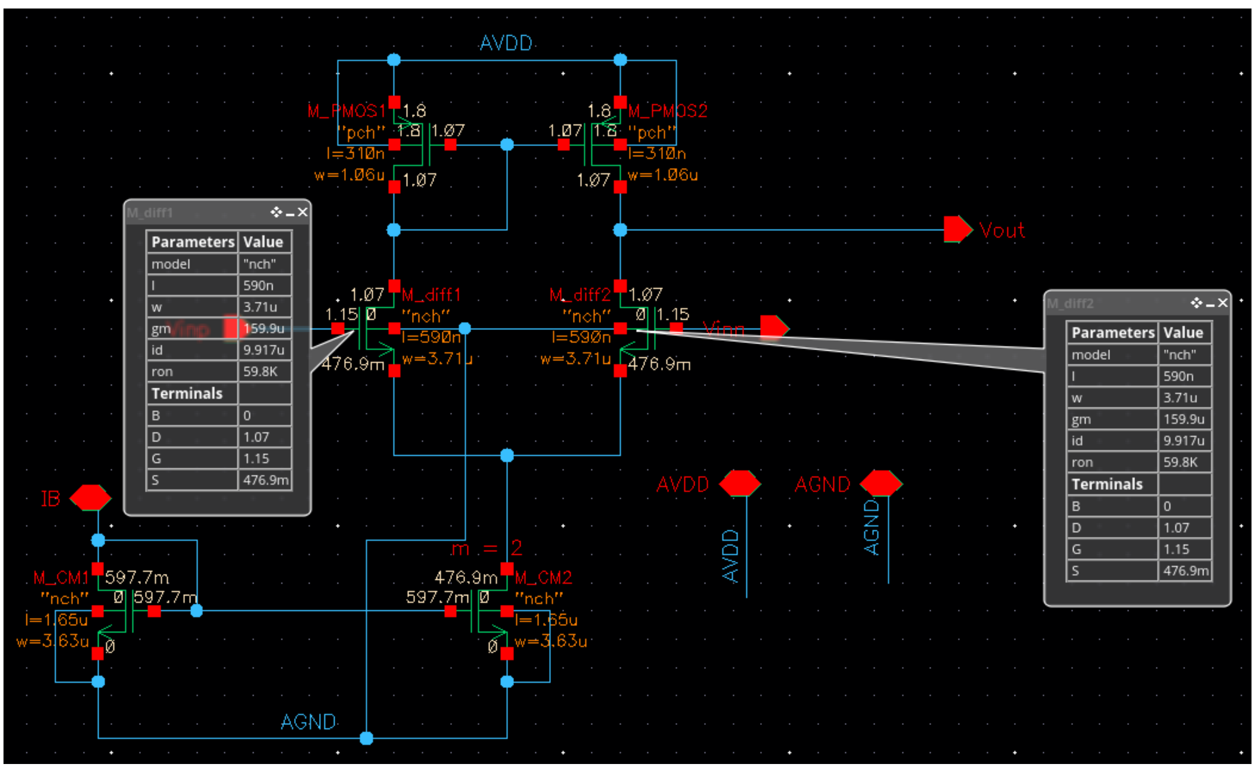


MOSFET Parameters

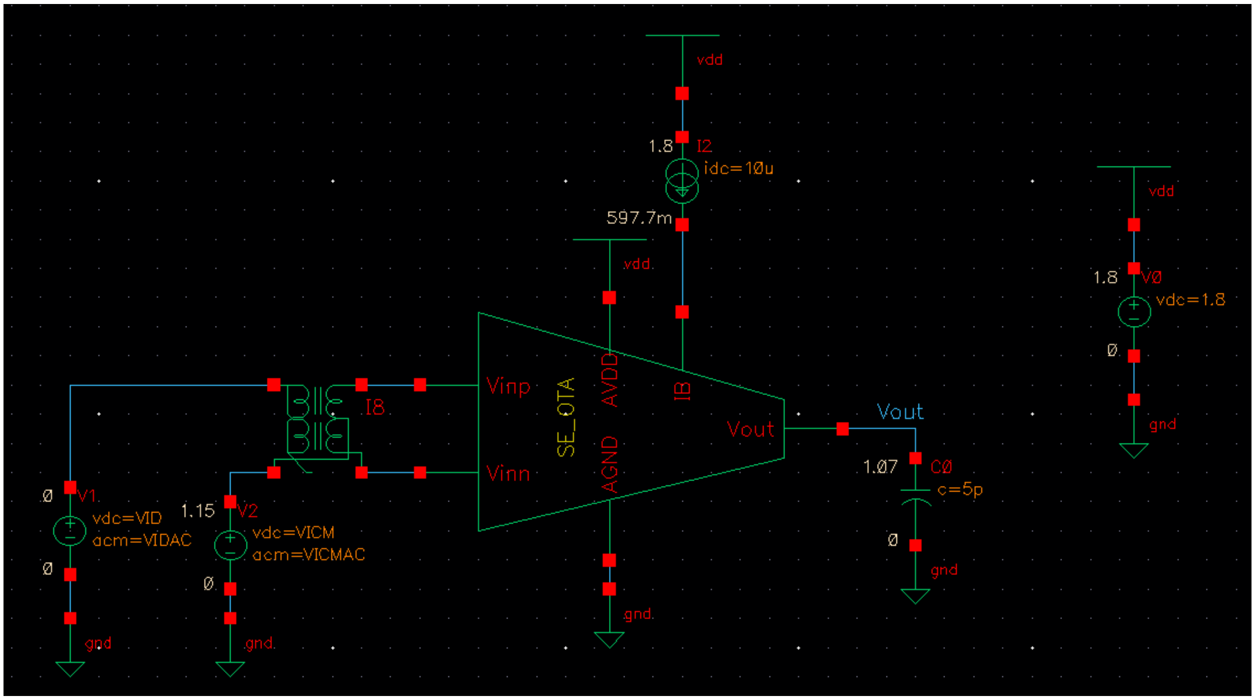
	Differential Pair	CM Load (PMOS) Pair	Current Mirror Pair
W (μm)	3.71	1.06	7.25
L (nm)	590	310	1650
gm (μS)	157.3	66.79	199.6
ID (μA)	10	10.13	20
gm/ID	15.73	6.593	9.979
VDS_{sat} (mV)	98.54	227	157.1
Vov (mV)	117.6	281.6	209.9
V* (mV)	127.1	303.3	200

Part 3: Open-Loop OTA Simulation

Schematic



- ID & gm are exactly equal in the input pair.
- Vout = 1.07V, because at DC OP where is no differential input, Vout = VDD - VGS_{PMOS} = 1.07V.



Differential Small Signal

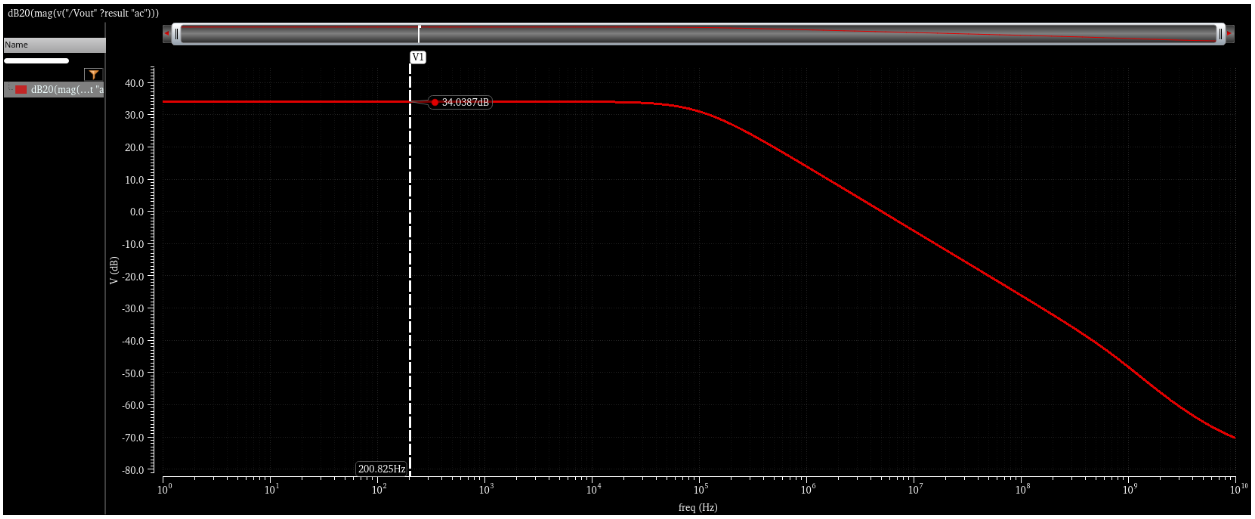
Circuit Parameters

Name	Type	Details	Value
Ao	expr	ymax(mag(VF("/Vout")))	50.01
Ao_dB	expr	dB20(ymax(mag(VF("/Vout"))))	33.98
BW	expr	bandwidth(VF("/Vout") 3 "low")	99.09K
UGF	expr	unityGainFreq(VF("/Vout"))	4.974M
GBW	expr	(BW * Ao)	4.955M

In order to meet the specs, we tune the width to of input pair to be 3.85u.

Name	Type	Details	Value
Ao	expr	ymax(mag(VF("/Vout")))	50.34
Ao_dB	expr	dB20(ymax(mag(VF("/Vout"))))	34.04
BW	expr	bandwidth(VF("/Vout") 3 "low")	99.59K
UGF	expr	unityGainFreq(VF("/Vout"))	5.027M
GBW	expr	(BW * Ao)	5.014M

Differential Gain vs Frequency



I1.M_PMOS2:rout I1.M_diff2:rout I1....

	Name	Value
1	I1.M_PMOS2:rout	632.3E3
2	I1.M_diff2:rout	626.7E3
3	I1.M_diff2:gm	161.8E-6

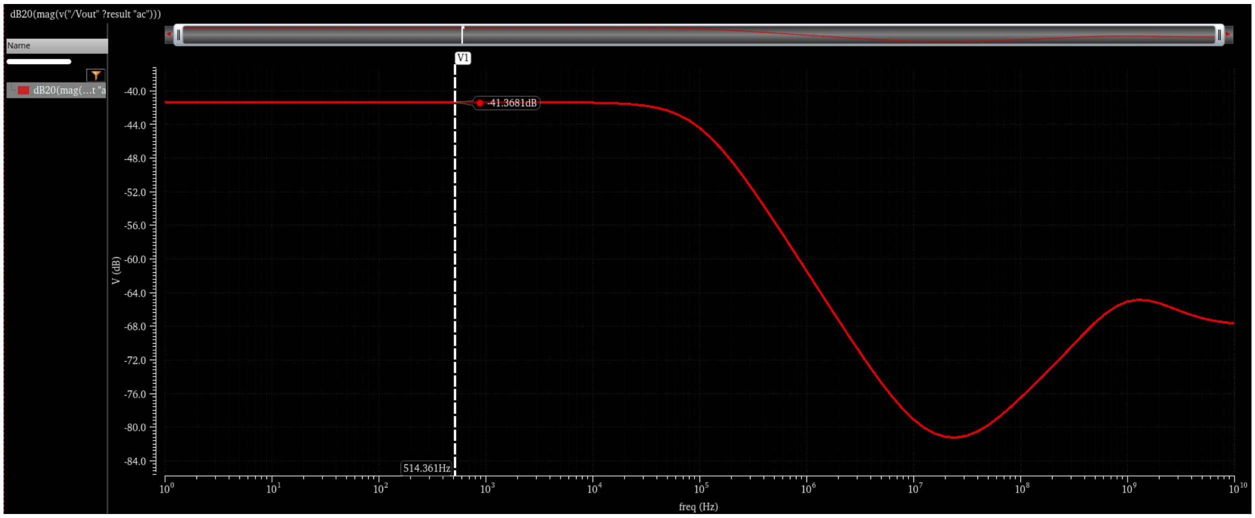
Hand Analysis

- $Av_{diff} = gm_{diff}(ro_{PMOS2} \,||\, ro_{diff2})$ = 161.8u*(632.3k || 626.7k) = 50.9 = 34.14dB
- $\omega_p \approx \frac{1}{(\mathrm{ro_{PMOS2}} \,||\, \mathrm{ro_{diff2}})CL} = \frac{1}{(314.7k)(5p)}$ = 635.4K → BW = $\frac{\omega_p}{2\pi}$ = 101.1 KHz (parasitic capacitances are neglected in this calculation)
- GBW = UGF = Av*BW = 5.15 MHz

	Simulation	Hand Analysis
Av (dB)	34.04	34.14
BW (KHz)	99.6	101.1
GBW (MHz)	5.01	5.15
UGF (MHz)	5.03	5.15

Common-Mode Small Signal

CM Gain vs Frequency



Hand Analysis

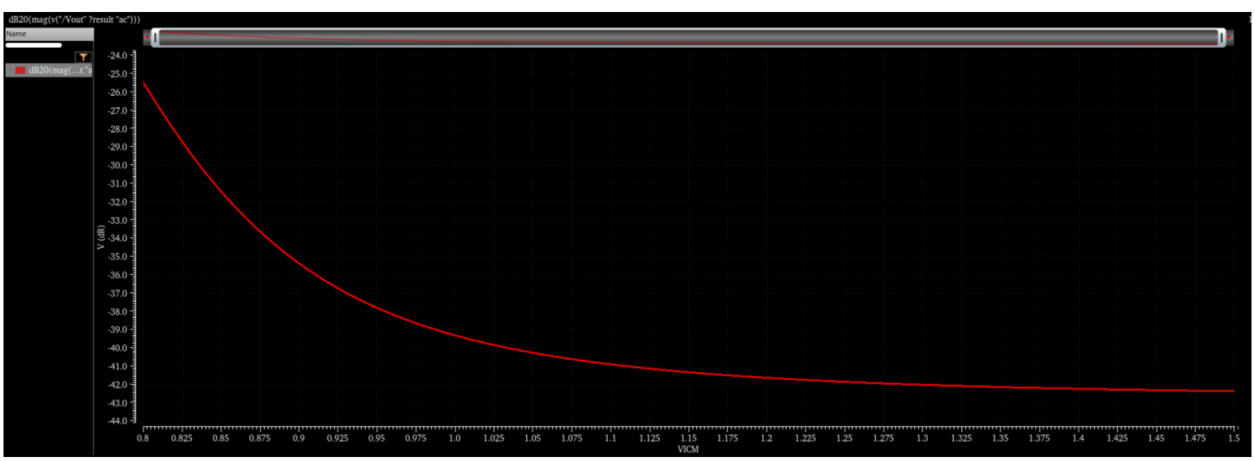
$$Av_{CM} \approx \frac{1}{2 * gm_{PMOS} * ro_{CM}} = \frac{1}{2*(66.04u)*(632.3k)} = 11.97m = -38.4dB$$

I1.M_PMOS2:gm I1.M_PMOS1:rout

	Name	Value
1	I1.M_PMOS2:gm	66.04E-6
2	I1.M_PMOS1:rout	632.3E3

	Simulation	Hand Analysis
Av (dB)	-41.4	-38.4

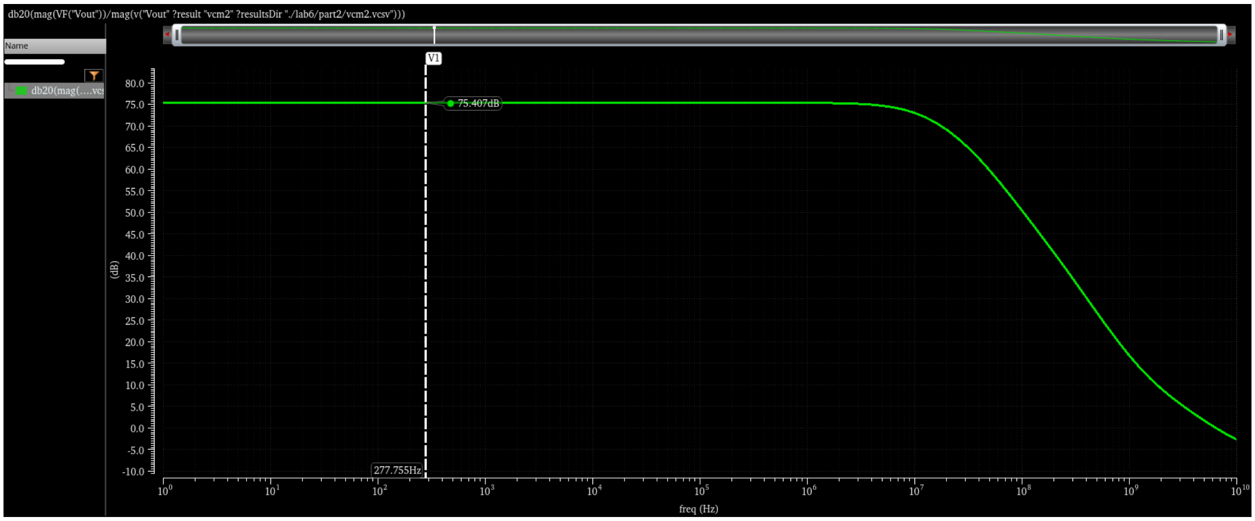
Av$_{CM}$ vs VICM



Comment: As VICM increases, the common mode gain decreases until it saturates.

Common-Mode Rejection Ratio (CMRR)

CMRR vs Frequency

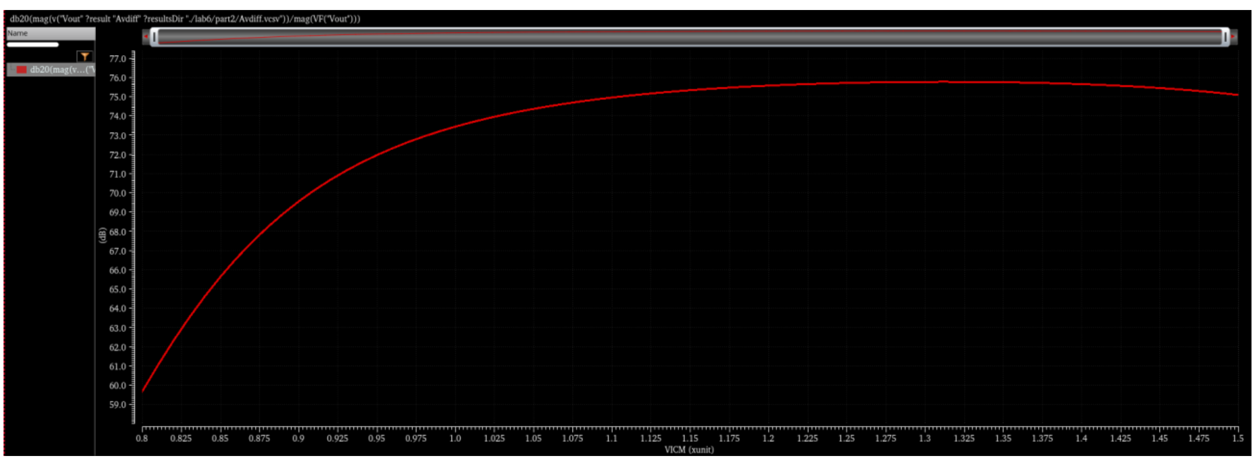


Hand Analysis

CMRR = Av_{diff}/Av_{CM} = 50.9/11.97m = 4252 =72.57 dB

	Simulation	Hand Analysis
CMRR (dB)	75.4	72.57

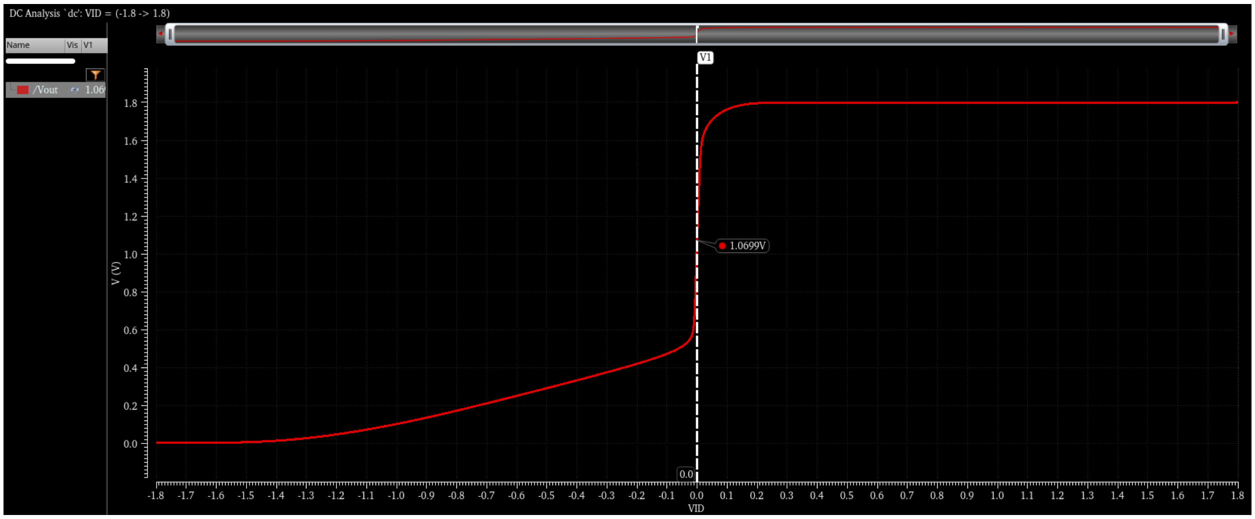
CMRR vs VICM



Comment: As VICM increases, CMRR increases because AV_{CM} decreases.

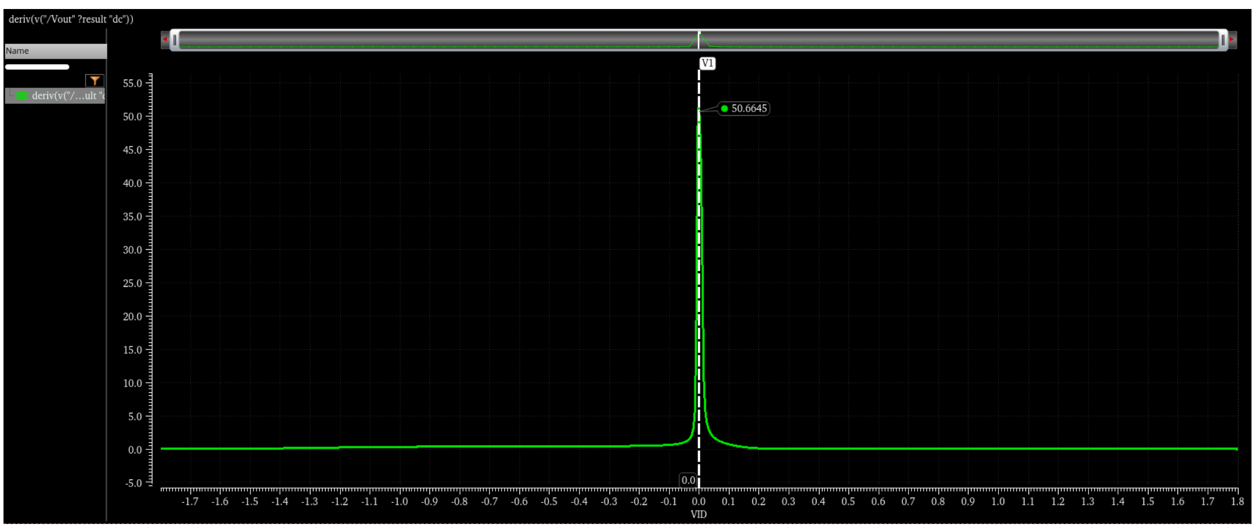
Differential Large Signal

Vout vs VID



- Vout = 1.07V at VID = 0
- At VID = 0, there is no differential signal, so there is no change in output. Therefore, Vout = VF = VDD - VGS_{PMOS} = 1.07V as simulated in DC OP.

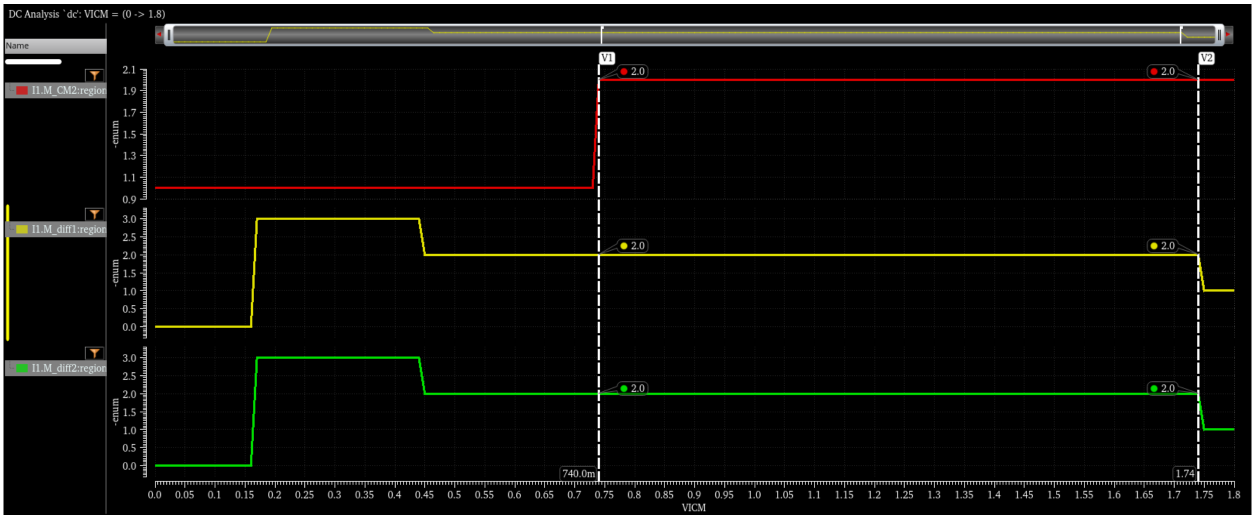
Derivative of Vout vs VID



Comment: Peak of the graph ≈ Av_{diff}.

Common-Mode Large Signal

Region vs VICM



Comparison

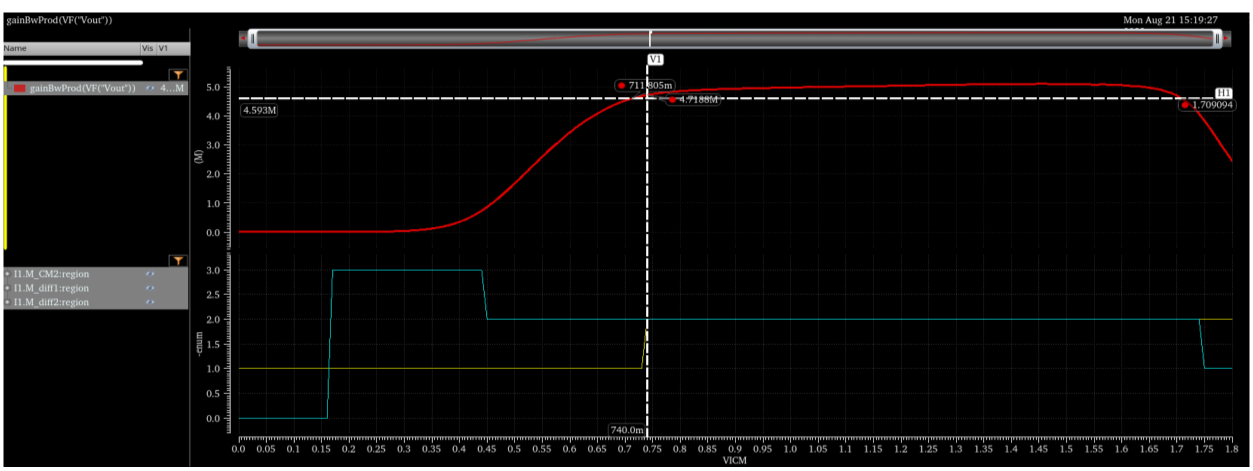
$CMIR_{simulation}$ = 1.74 - 0.74 = 1V

$CMIR_{hand\ analysis} = VDD - V_{thp} - V^*_{PMOS1} - V^*_{diff1} - V^*_{CM}$ = 1.8 - 0.45 - 0.3 - 0.12 - 0.2 = 0.73V

(numbers used are from DC OP)

	Simulation	Hand Analysis
CMIR (V)	1.0	0.73

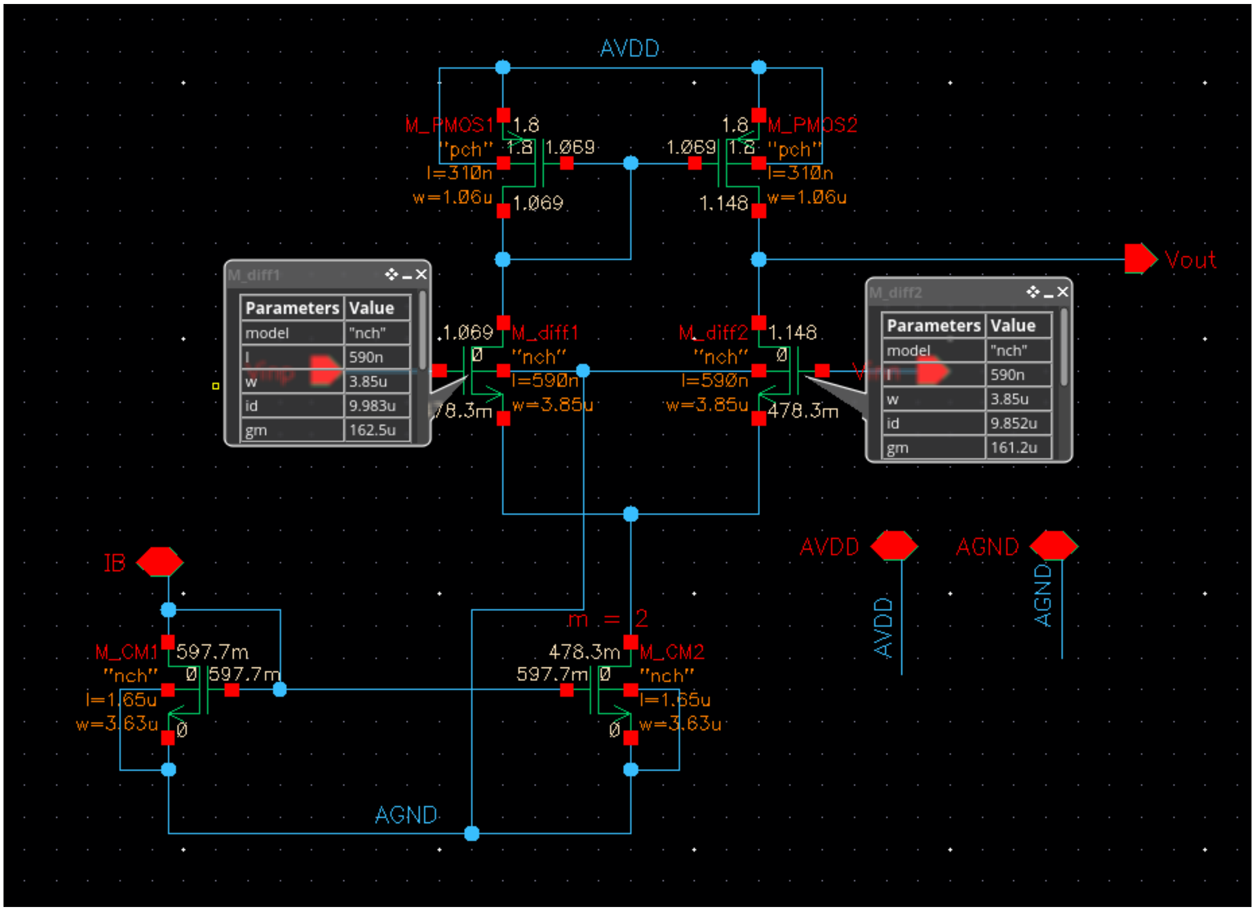
GBW vs VICM



CMIR = 1.71 – 0.71 = 1V

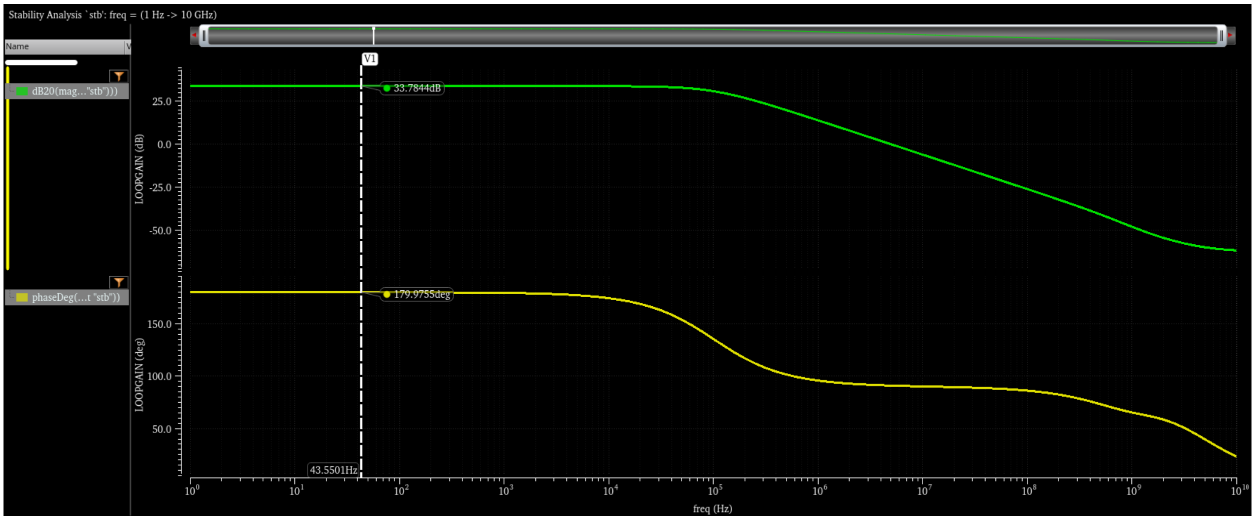
Part 4: Closed-Loop OTA Simulation

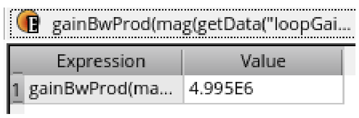
DC OP



- Current and gm are not exactly equal due to the mismatch in the circuit after feedback connection.
- Current mismatch = $9.983u - 9.852u$ = 0.131uA
- gm mismatch = 162.5u – 161.2u = 1.3uS

Loop Gain





	STB Simulation	Open Loop Simulation
DC Gain (dB)	33.78	34.04
GBW (MHz)	5.00	5.01

Hand Analysis

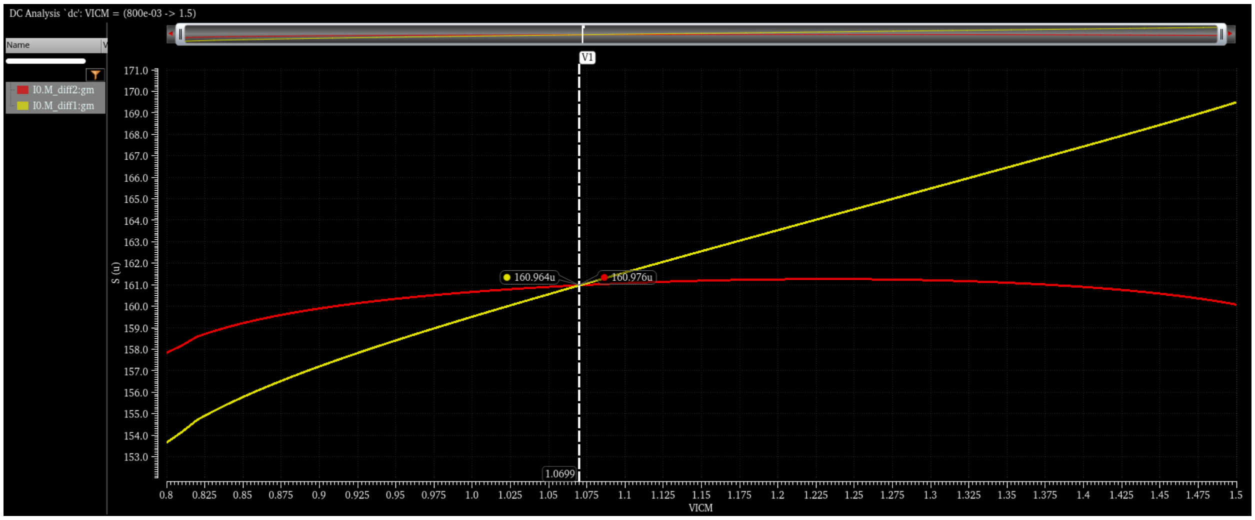
Loop Gain = βAOL → $\beta = 1$ & AOL is the same as calculated in part 3 = 34.14dB

	STB Simulation	Hand Analysis
DC Gain (dB)	33.78	34.14
GBW (MHz)	5.00	5.15

Part 5: Effect of Mismatch on CMRR

CM Small Signal

Input Pair gm vs VICM



- gm1 = gm2 at Vin = VF = 1.07, because at this value there is no mismatch in the circuit.
- Ideally → AvCM = 0
- Actual → AvCM = $-\frac{1}{2(\mathrm{gm})(\mathrm{ro_{CM}})} = -\frac{1}{2(160.96\mathrm{u})(692.3\mathrm{k})}$ = 4.49m = -46.96 dB

I0.M_CM2:rout

	Name	Value
1	I0.M_CM2:rout	692.3E3