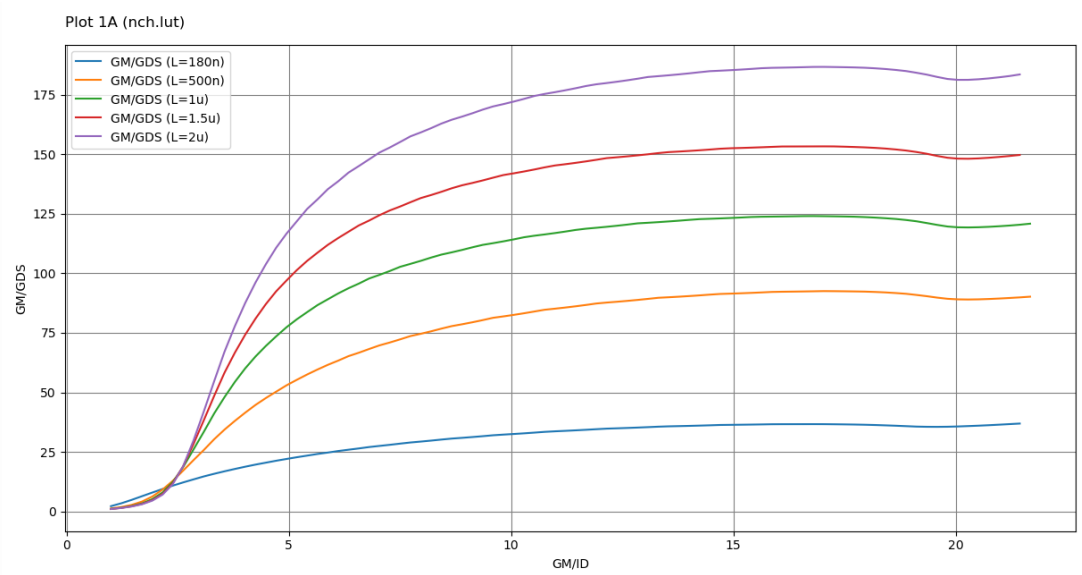
Analog IC Design

Lab 9

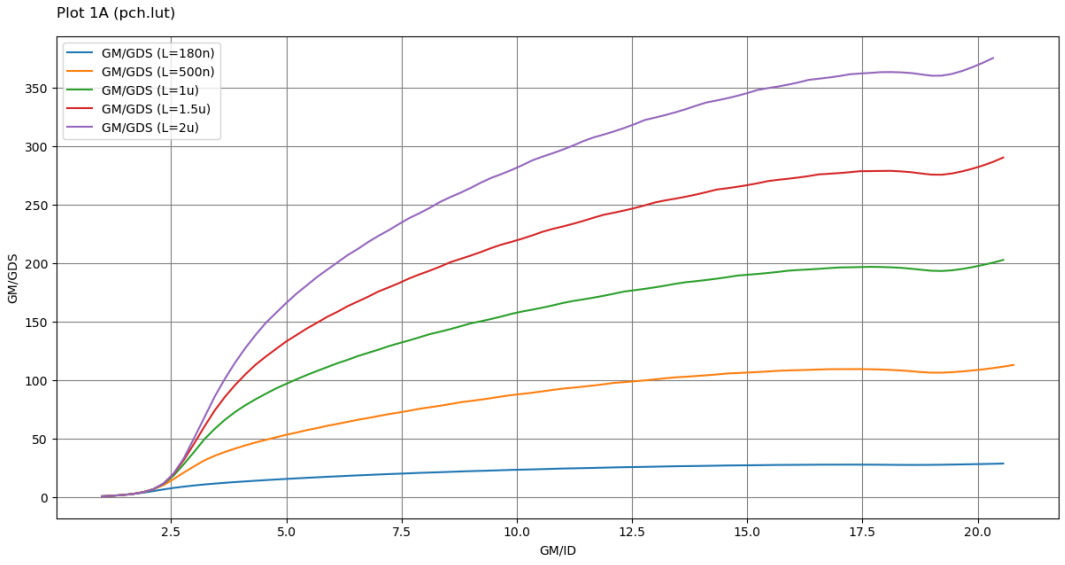
PART 1: gm/ID Design Charts

gm/gds

NMOS

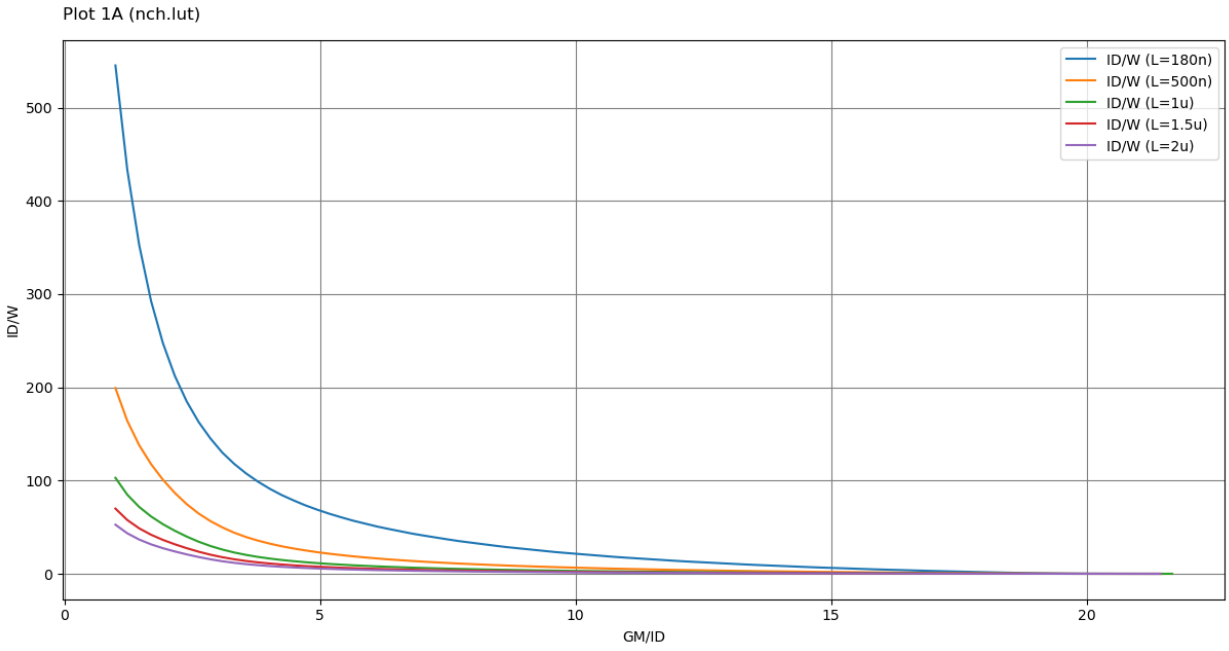


PMOS

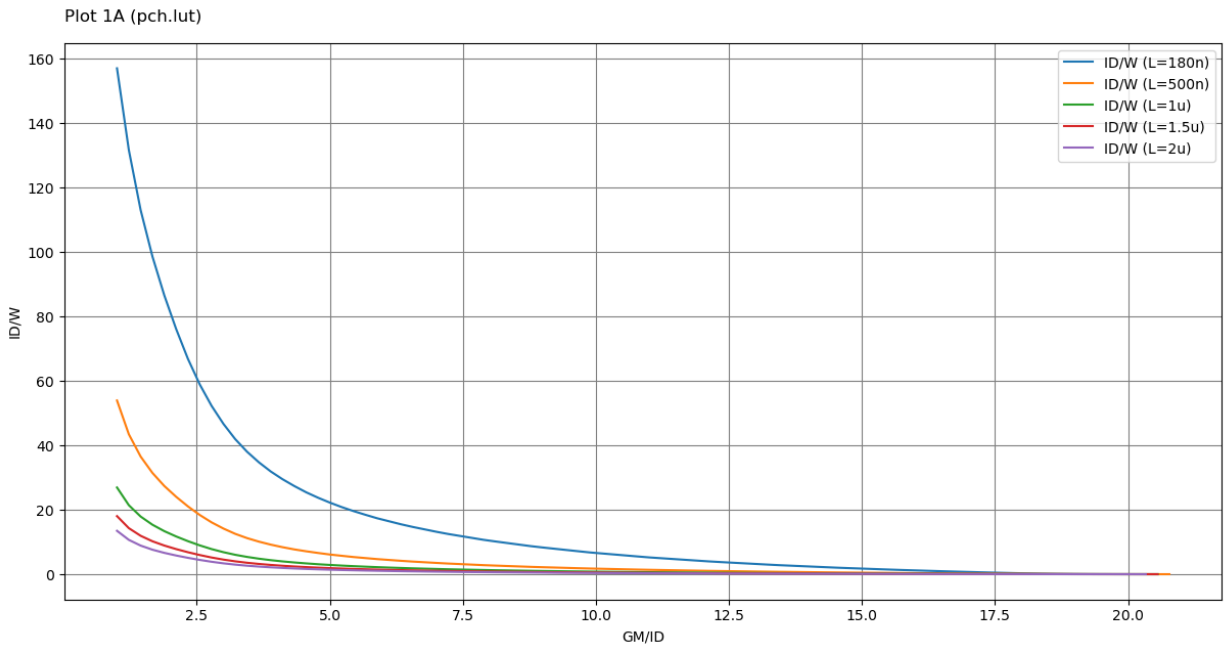


ID/W

NMOS

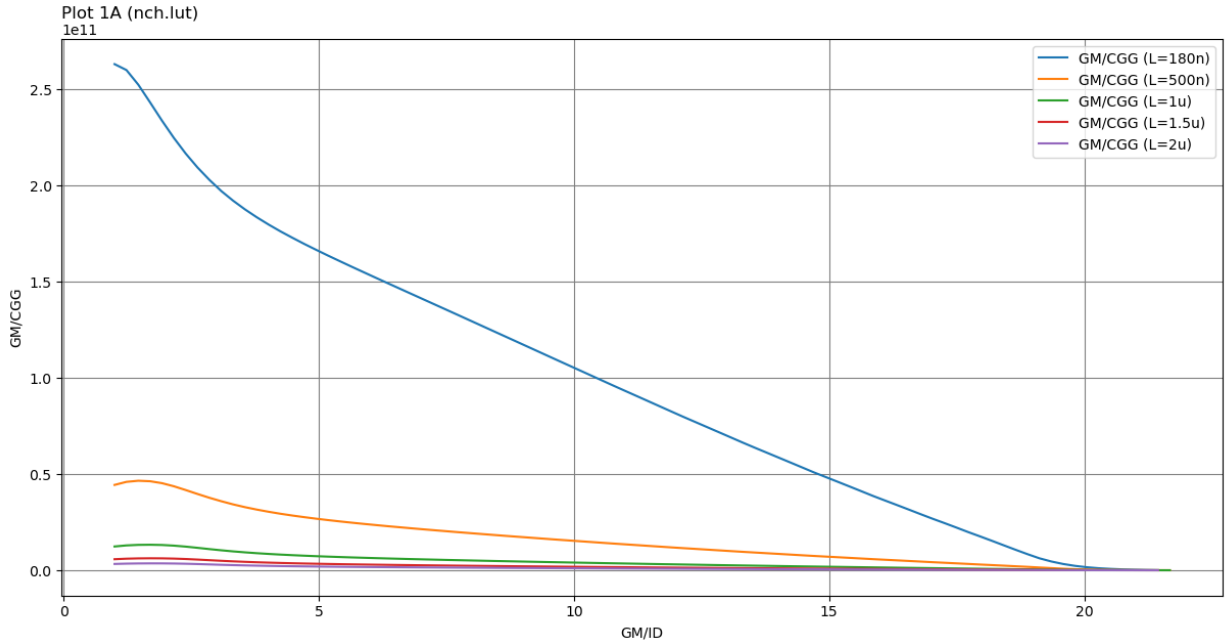


PMOS

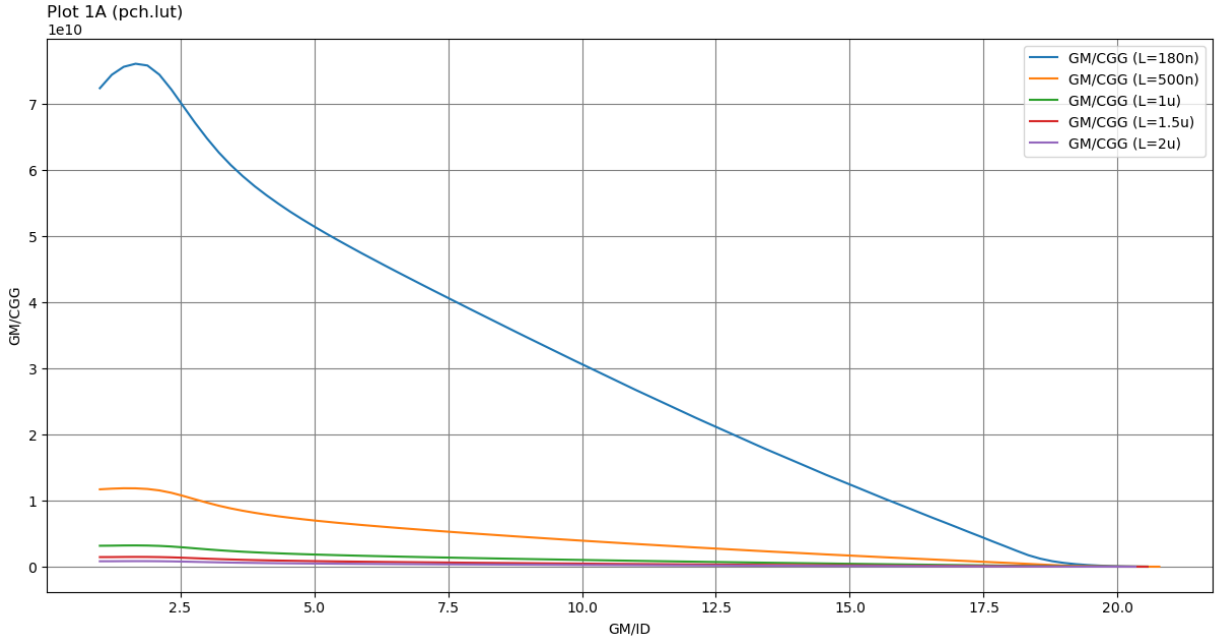


gm/Cgg

NMOS

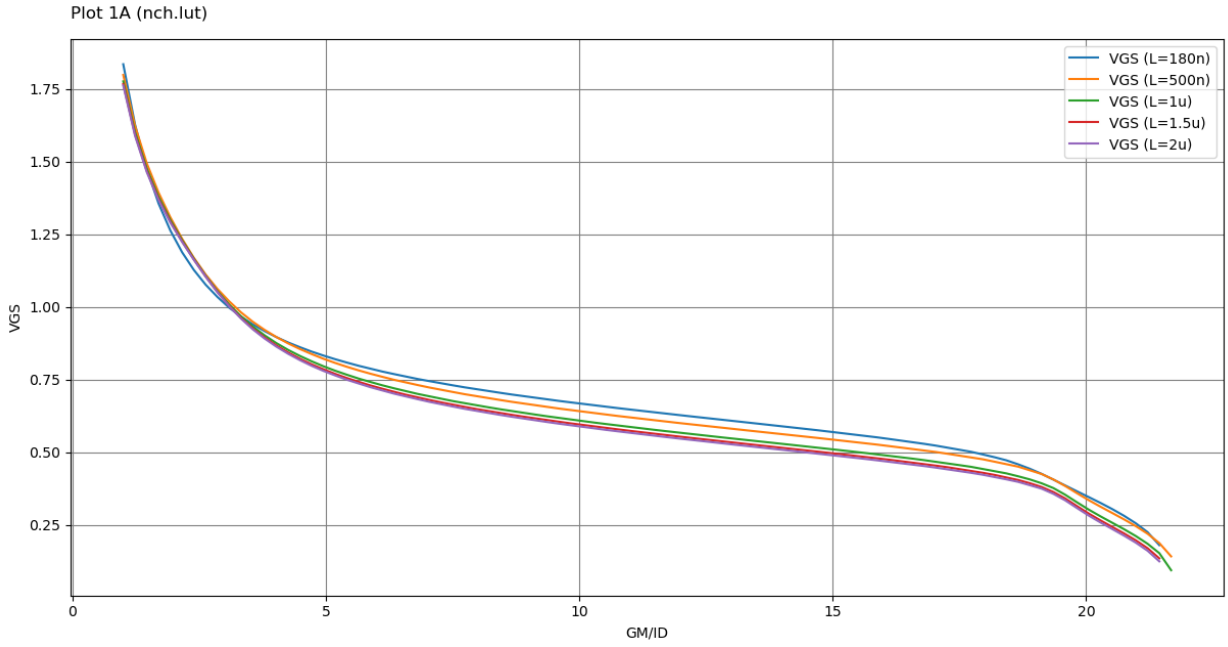


PMOS

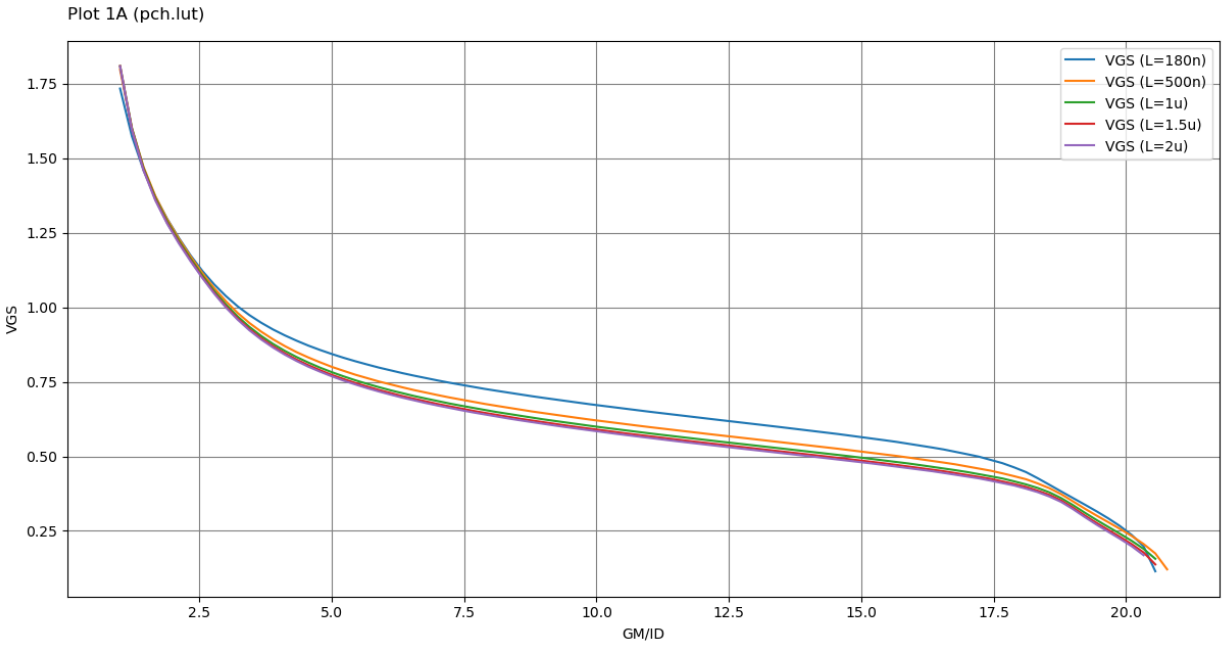


VGS

NMOS



PMOS

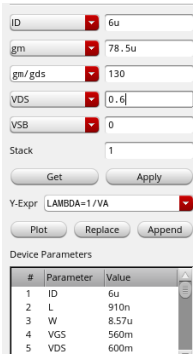


PART 2: OTA Design

General Hand Analysis

- Static gain error = 0.05% → LG = 2000 = β.AOL & β (buffer connection) → AOL = 2000
- $\omega_{p2} = 4\omega_u$ → $\frac{gm2}{CL} = \frac{gm1}{Cc}$ → gm2 = 4gm1
- $I_{B2} = 4I_{B1}$ → IB1 =12uA & IB2 = 48uA
- The first stage would have double the gain of the second stage (Av1 = $20\sqrt{10}$ = 63.2 & Av2 = $10\sqrt{10}$ = 31.6)
- Rise time = 2.2τ = 70ns → τ = 31.8ns = RC
- GBW = UGF = $\frac{1}{2\pi\tau}$ = 5MHz
- From SR = IB1/Cc → Cc = 2.4pF
- Input pair of first stage should be PMOS because CMIR is closer to ground.
- Input pair of second stage should be NMOS because CMIR is closer to ground.

Differential PMOS Pair Sizing



- Assume ro2 = ro4 → AOL = gmro/2 → Intrinsic gain = 126.4 ≈ 130
- ID = 12u → ID_{branch} = 6u
- Assume VDS = 0.6V & VSB = 0V
- GBW = $\frac{gm1,2}{2\pi Cc}$ → gm_{diff} = 78.5uS

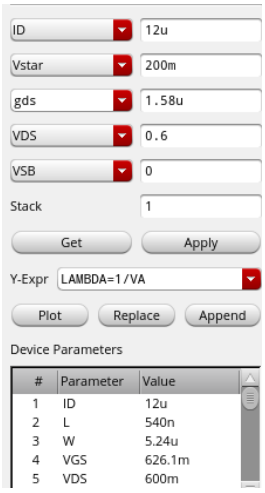
gm/ID = 12.83, L = 910n, W = 8.57u

NMOS Design Loads Sizing

- Since we assumed, ro_{diff} = ro_{load} → gds_{diff} = gds_{load} = 595.5n
- ID = 6u
- VSB = 0
- VGS_{load} = VDS_{load} = VCM_{low} + Vth = 0.2 + 0.4125 = 0.6125v

L = 800n & W = 1.12u

First Stage Tail Current Source Sizing



- Avdiff = 65 = 36dB
- Av_{CM} = 36 – 74 = -38dB = 0.0126
- $Av_{CM} = \frac{gds_{CM}}{2*gm_{load}}$ → gds_{CM} = 2*0.0126*(62.53u) = 1.58u
- V* = VDD-[$VICM_{high}$ + VGS_{diff}] = 1.8-(1+0.56) = 0.24V → use V* = 200mV
- VSB = 0 & VDS = 0.6
- ID = 12u

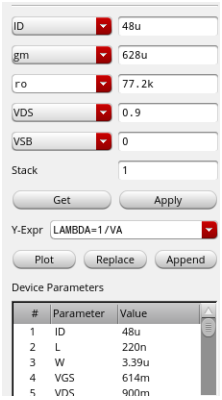
L = 540n W = 5.24u

Second Stage Load

- ID = 48u
- VDS = 0.9 & VSB = 0
- L = 540n
- W = 4*(5.24u) = 20.96u

ro = 177.5kΩ

Second Stage Common Source Sizing



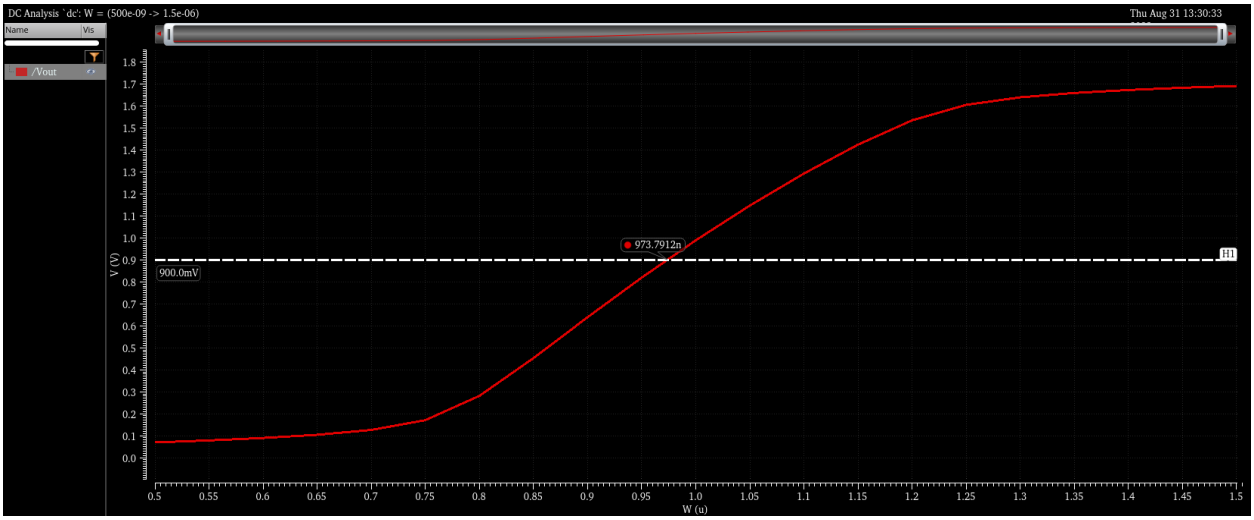
- $gm_{CS} = 8 * gm_{diff} = 628u$
- Av = $10\sqrt{10}$ = 31.6 = $gm_{CS} * (ro_{current\ mirror} \,||\, ro_{CS})$
- ro_{CS} = 70.22k
- VDS = 0.9 & VSB = 0
- ID = 48u

L = 220n W = 3.39u

Rz Selection

$$R_z = \frac{1}{Gm_2} = 1.6K\Omega$$

Removing Systematic Offset



After this step, ID of stage 2 becomes higher than 50u, so we reduce the width of the second stage PMOS load then reiterate the previous step → W_{NMOS_load} = 1.034u.

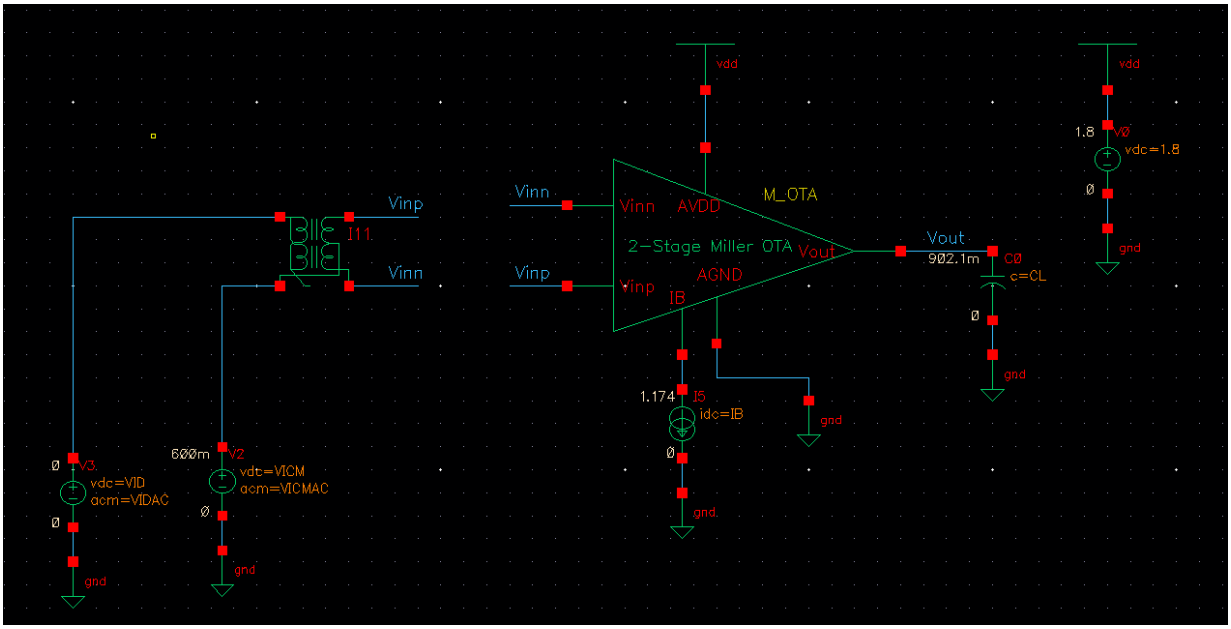
MOSFET Parameters

	Differential Pair	NMOS Load Pair	CS Amplifier	Tail Current Source	Current Mirror	CS Load
W (µm)	9.1	1.034	3.39	5.244	4.37	19.5
L (nm)	910	800	220	540	540	540
gm (µS)	78.93	59.86	601	119.5	100.7	466.7
ID (µA)	5.91	5.91	46.62	11.82	10	46.62
gm/ID	13.36	10.13	12.89	10.11	10.07	10
VDS_{sat} (mV)	128.5	154.4	116.2	163.7	163.3	165.6
Vov (mV)	133.8	204.1	142.6	193.1	193.6	192.6
V* (mV)	149.7	197.4	155.1	197.9	198.6	199.8

Note: These values are after modifications in part 3.

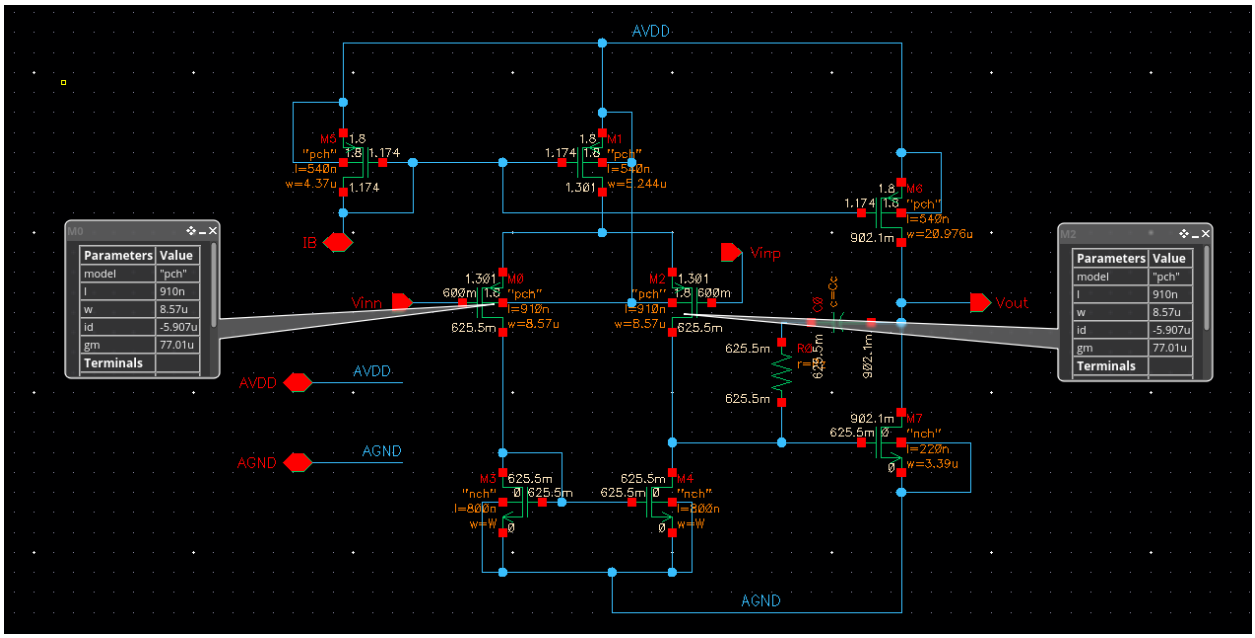
PART 3: Open-Loop OTA Simulation

Schematic



DC OP

DC Node Voltages



Comments

- The current and gm of the input pair are exactly equal, as there is no differential signal.
- Vout1 = VF = VGS_{load} = 625.5mV
- Vout2 = 0.9V → for maximum signal swing, Vout is set for VDD/2 (as designed)

Differential Small Signal

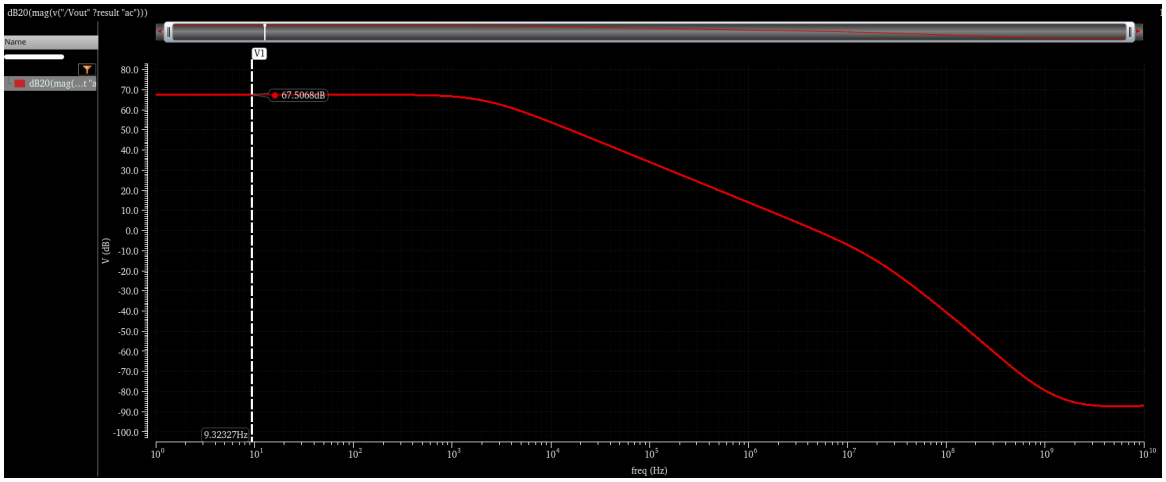
Circuit Parameters

Name	Type	Details	Value
Ao	expr	ymax(mag(VF("/Vout")))	2.324K
Ao_dB	expr	dB20(ymax(mag(VF("/Vout"))))	67.32
BW	expr	bandwidth(VF("/Vout") 3 "low")	2.102K
UGF	expr	unityGainFreq(VF("/Vout"))	4.792M
GBW	expr	(Ao * BW)	4.884M

In order to meet the GBW spec, we increase the width of differential pair to 9.1um.

Ao	expr	ymax(mag(VF("/Vout")))	2.373K
Ao_dB	expr	dB20(ymax(mag(VF("/Vout"))))	67.51
BW	expr	bandwidth(VF("/Vout") 3 "low")	2.11K
UGF	expr	unityGainFreq(VF("/Vout"))	4.881M
GBW	expr	(Ao * BW)	5.007M

Differential Gain vs Frequency



I0.M2:gm I0.M2:rout I0.M4:rout

	Name	Value
1	I0.M2:gm	78.93E-6
2	I0.M2:rout	1.776E6
3	I0.M4:rout	1.757E6

I0.M6:rout I0.M7:gm I0.M7:rout

	Name	Value
1	I0.M6:rout	184.9E3
2	I0.M7:gm	601.0E-6
3	I0.M7:rout	82.24E3

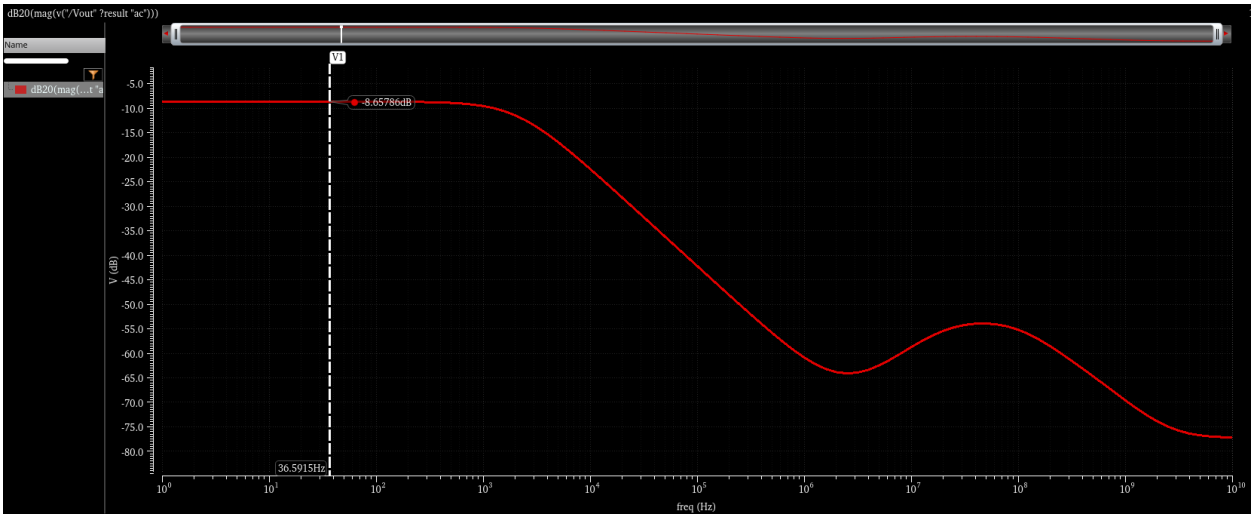
Hand Analysis

- $Av_{diff} = gm_{diff}(ro_{load} \,||\, ro_{diff}) = 78.93u*(1.8M \,||\, 1.8M) = 69.7$
- $Av_{CS} = gm_{CS}*(ro_{load} \,||\, ro_{CS}) = 601u*(184.9k \,||\, 82.24k) = 34.21$
- $Av_{OTA} = Av_{diff} * Av_{CS} = 2384 = 67.5dB$
- $BW \approx \frac{1}{2\pi(Rout_1)(Gm_2Rout_2)(C_c)} = \frac{1}{2\pi(883k)(601u*56.9k)(2.4p)} = 2.20K$
- GBW = UGF = Av*BW = 5.24 MHz

	Simulation	Hand Analysis
Av (dB)	67.5	67.5
BW (KHz)	2.11	2.20
GBW (MHz)	5.01	5.24
UGF (MHz)	4.88	5.24

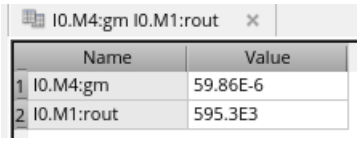
CM Small Signal

CM Gain vs Frequency



Hand Analysis

$Av_{CM} \approx \frac{1}{2*gm_{load}*ro_{tail}} = \frac{1}{2*(59.86u)*(595.3k)} = 0.014 = -37dB$

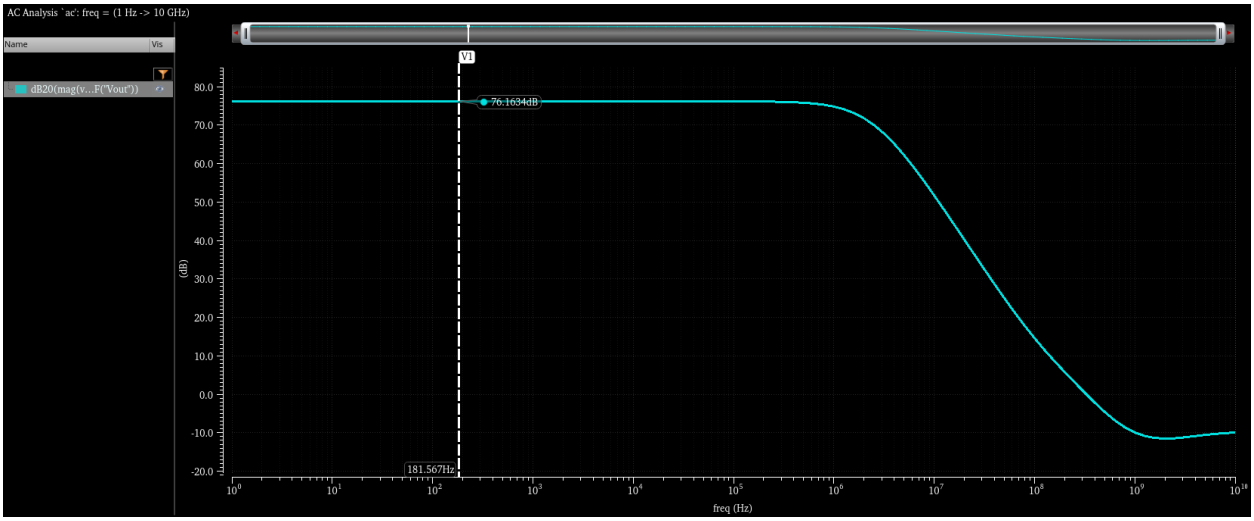


$Av_{CM\_OTA} = Av_{CM} * Av_{CS} = 0.014*34.21 = -6.39$

	Simulation	Hand Analysis
Av (dB)	-8.66	-6.39

CMRR (Optional)

CMRR vs Frequency



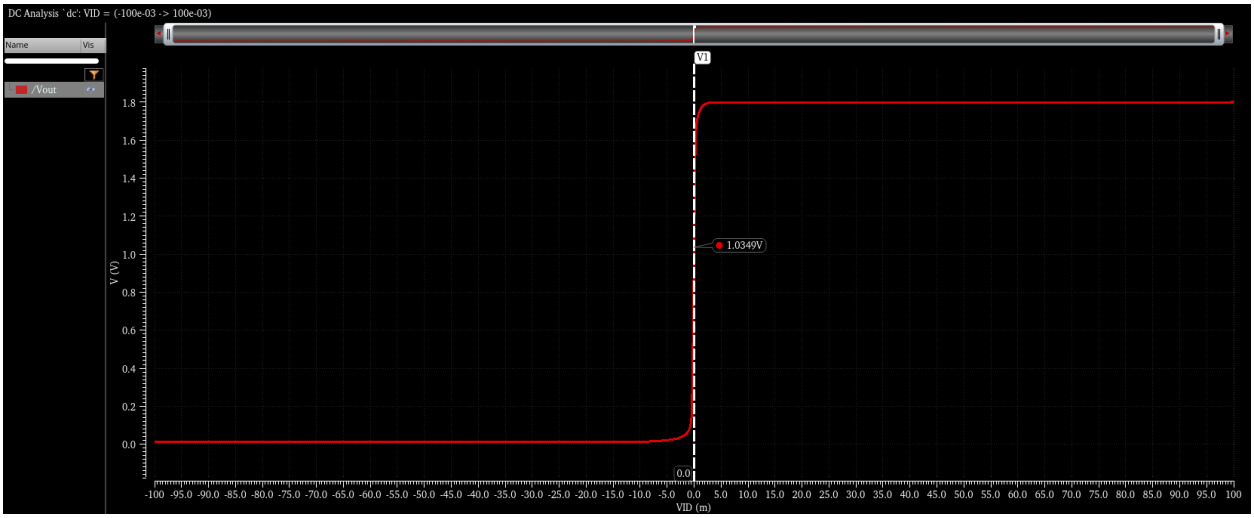
Hand Analysis

CMMR = Av_{diff}/Av_{CM} = 69.7/0.014 = 4980 =73.9dB

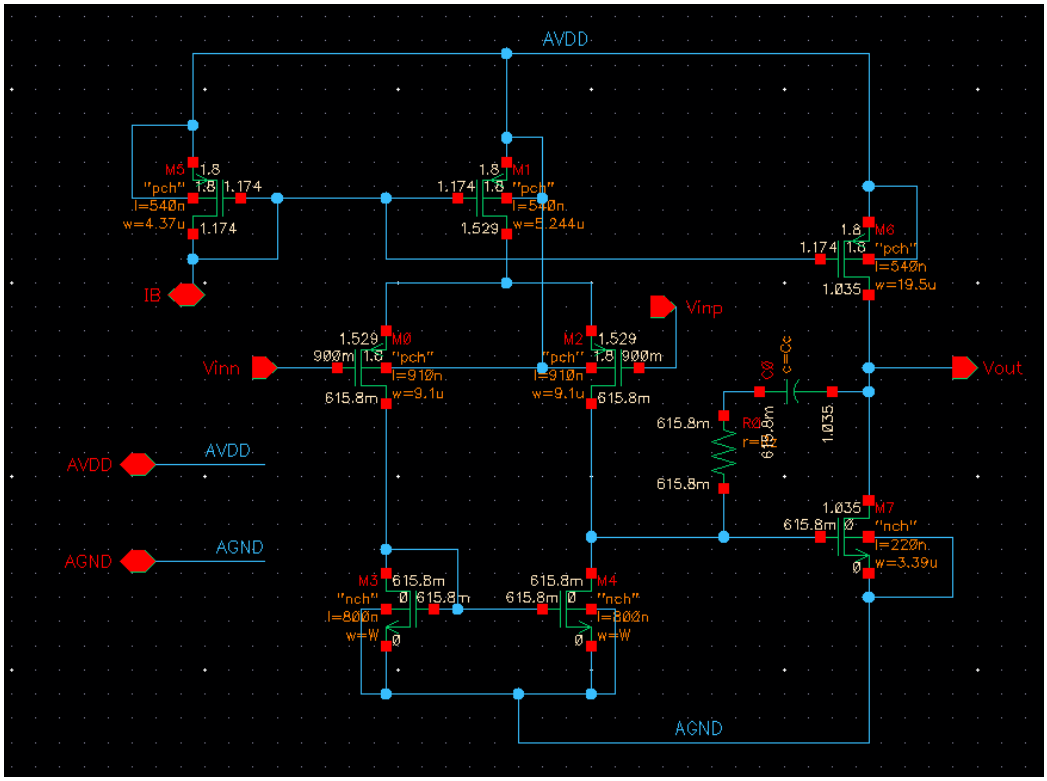
	Simulation	Hand Analysis
CMMR (dB)	76.2	73.9

Differential Large Signal (Optional)

Vout vs VID



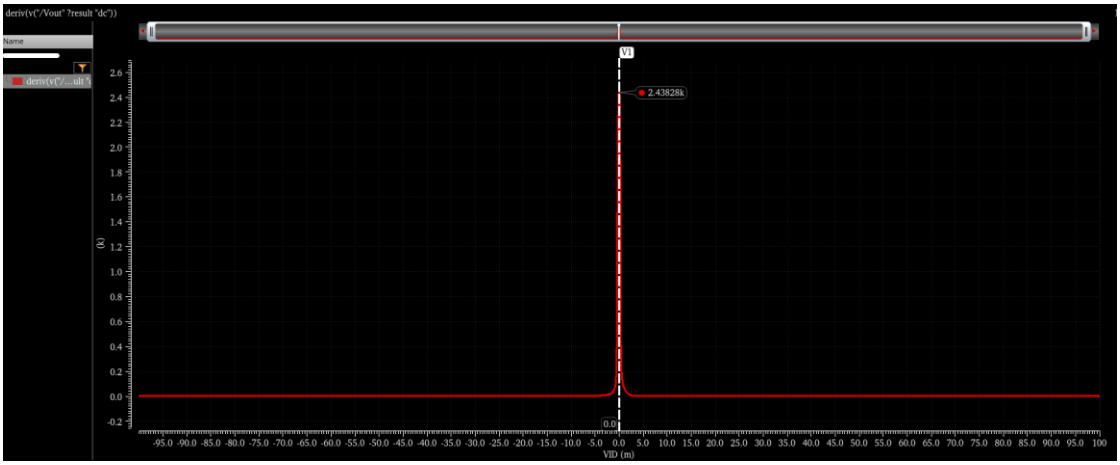
DC OP at VICM = 0.9V



Comments

- At VID = 0, Vout = 1.035V as simulated in DC OP.

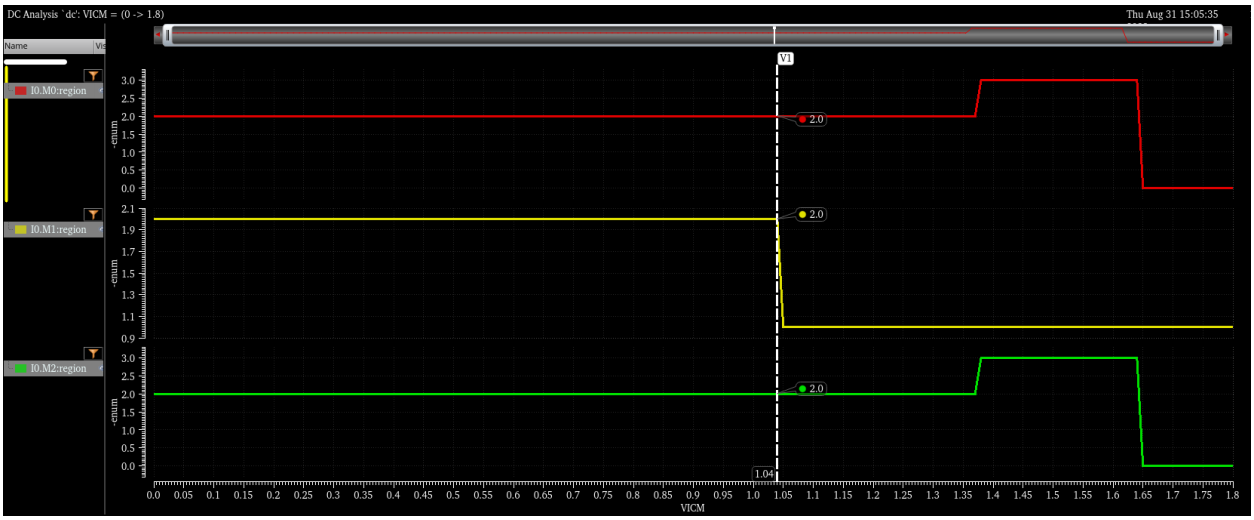
Derivative of Vout vs VID



Comment: Peak of the graph ≈ Av_{diff} = 2.4k

Common-Mode Large Signal

Region vs VICM



Comparison

$CMIR_{simulation}$ = 1.04V

$CMIR_{hand\ analysis} = VDD - V_{thp} - V^*_{load1} - V^*_{diff1} - V^*_{tail}$ = 1.8 - 0.564 + 0.15 - 0.13 - 0.16 = 1.096V

(numbers used are from DC OP)

	Simulation	Hand Analysis
CMIR (V)	1.04	1.10

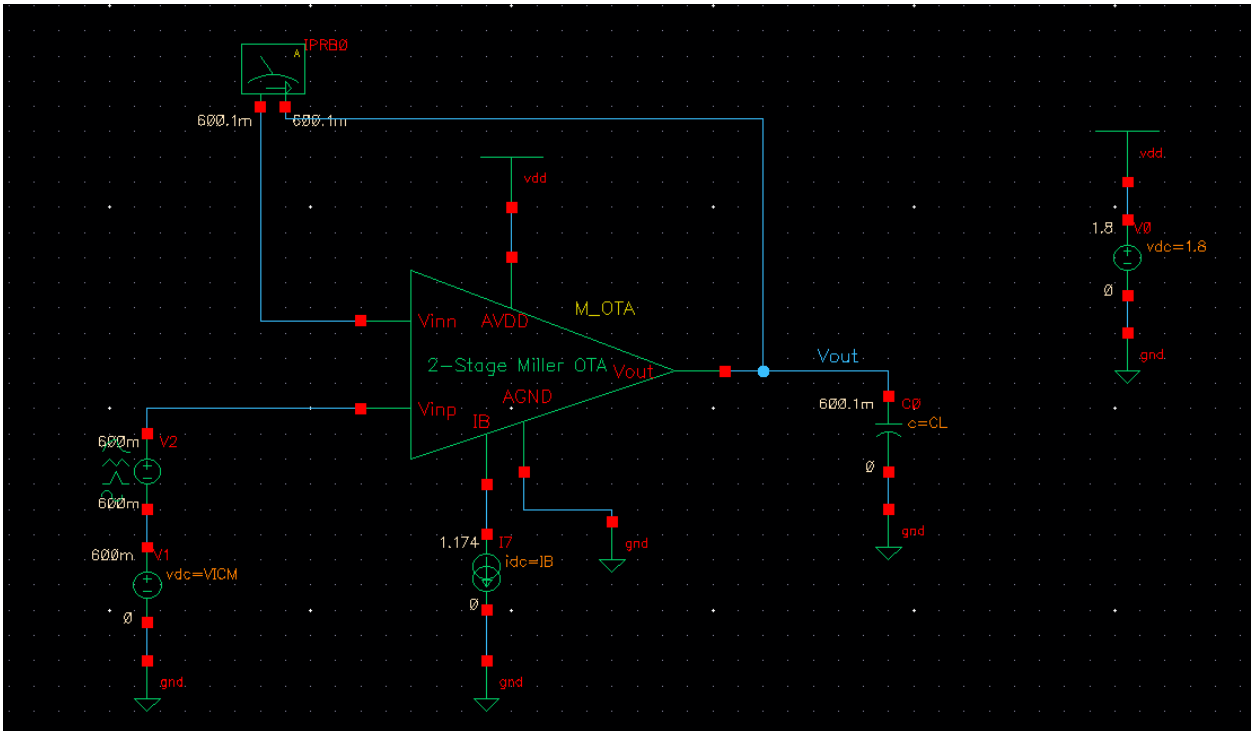
GBW vs VICM

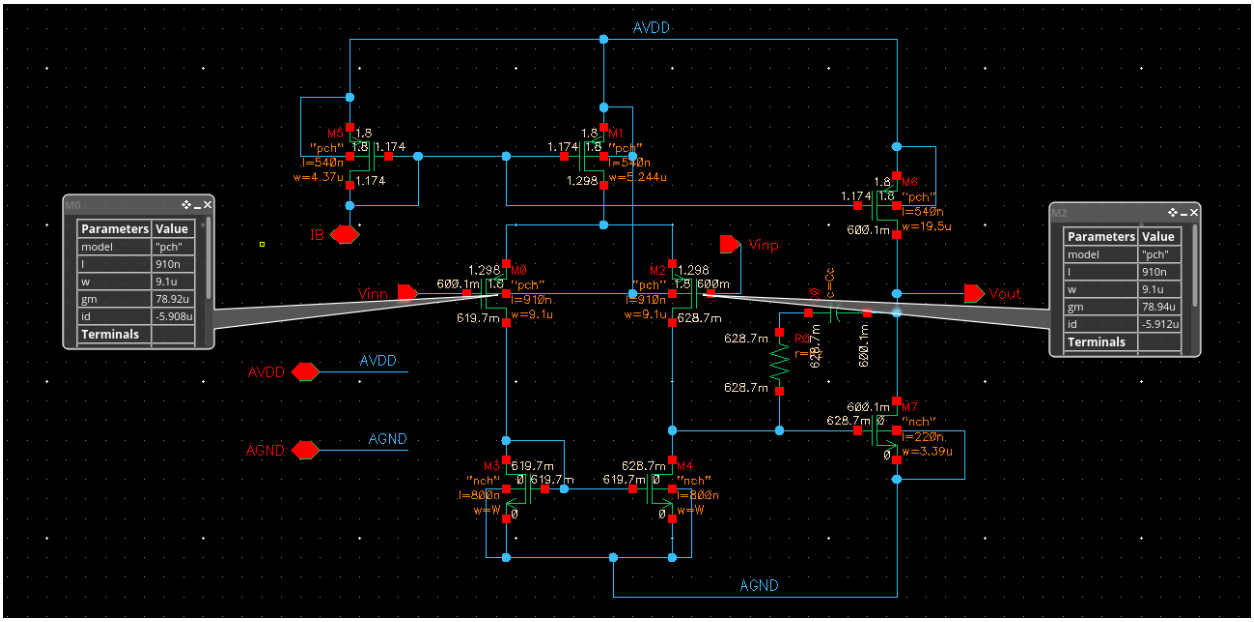
CMIR = 1.1V

PART 4: Closed-Loop OTA Simulation

DC OP

Schematics





Comments

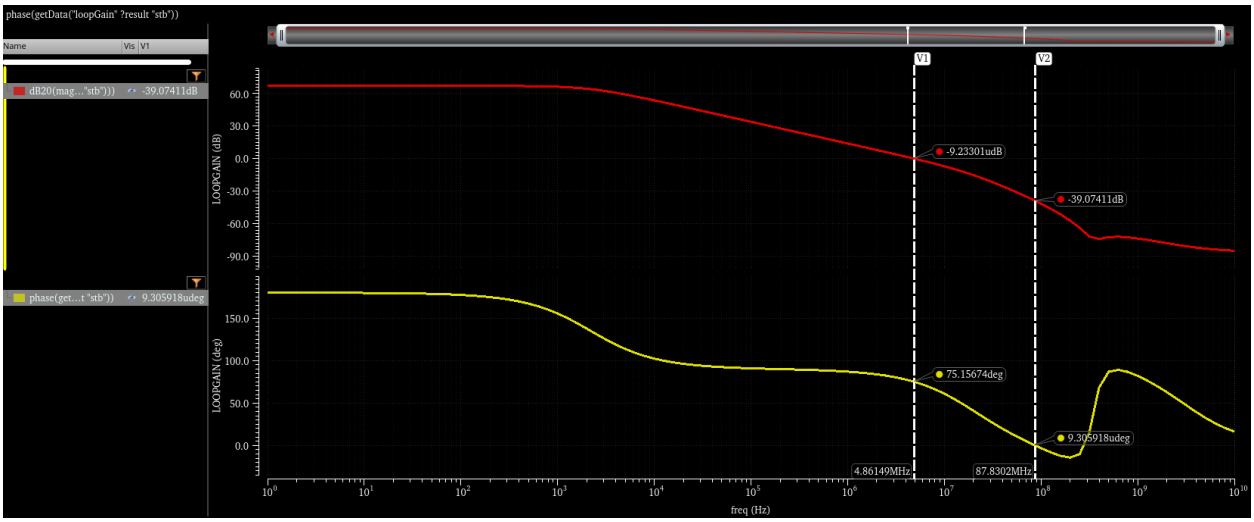
- The DC voltages at the input terminals of the op-amp are not exactly equal due to systematic offset; we designed for output of 0.9V, but due to the feedback connection, Vout ≈ 0.6V. Assuming ideal values:

$$\text{Voffset} = \frac{\text{Vout}_{\text{offset}}}{\text{Av}} = \frac{0.3}{2000} = 0.15mV$$

- The DC voltage at the output of the first stage (628.7mV) is not exactly equal to the value in the open-loop simulation (625.5mV), because of systematic offset, the circuit changes the VGS of both NMOS load & CS input.
- The current and gm of the input transistors are not exactly equal, because the circuit is not symmetrical anymore after the feedback connection; the negative terminal of OTA sees higher capacitance (CL) than the positive terminal, so it will have lower current.

Loop Gain

Loop Gain & Phase vs Frequency



ymax(dB20(mag(getData("loopGain...

	Expression	Value	Expression	Value	Expression	Value
1	ymax(dB20(mag...	67.12	unityGainFreq(g...	4.877E6	gainBwProd(get...	5.017E6

Open Loop Simulation vs Loop Gain Simulation

	STB Simulation	Open Loop Simulation
DC Gain (dB)	67.12	67.51
UGF (MHz)	4.88	4.88
GBW (MHz)	5.02	5.01

Comment: Note that UGF < GBW because UGF calculations are based on asymptotes of the curve.

Phase Margin

Simulation: From graph → PM = 75.2 deg

phaseMargin(getData("loopGain" ?r...

	Expression	Value
1	phaseMargin(ge...	75.20

Hand Analysis: PM = 90 - $\tan^{-1}\left(\frac{UGF}{\omega_{p_2}}\right)$ = 90 - $\tan^{-1}\left(\frac{4.88}{87.8/2\pi}\right)$ = 70.7 deg

	Simulation	Hand Analysis
Phase Margin (deg)	75.2	70.7

Comment: PM > 70deg → We meet the spec & the system is stable (far from oscillation).

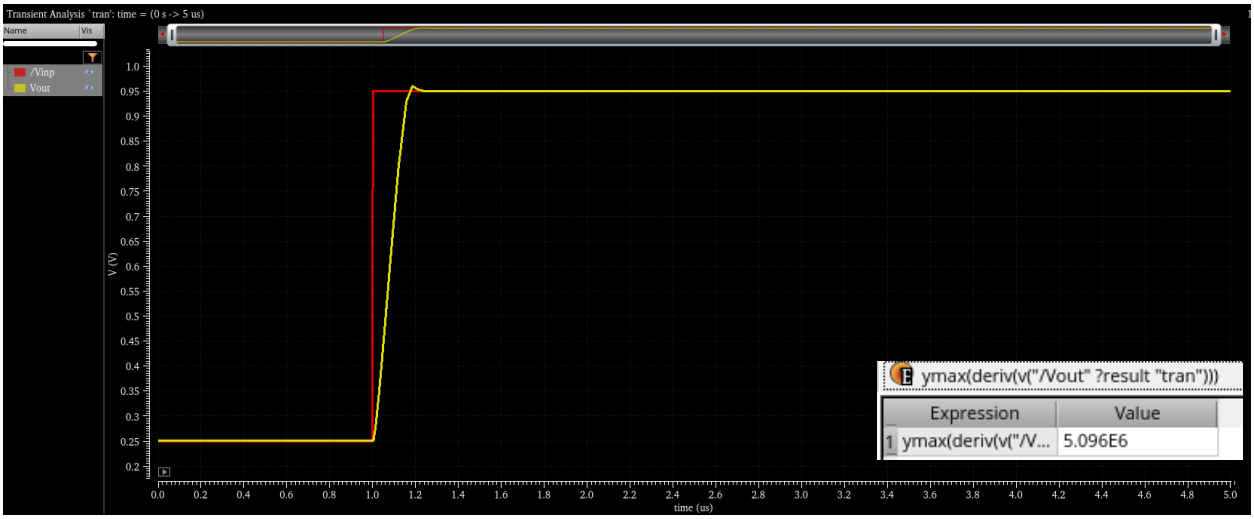
Hand Analysis

Loop Gain = βAOL → $\beta = 1$ & AOL is the same as calculated in part 3 = 67.5dB

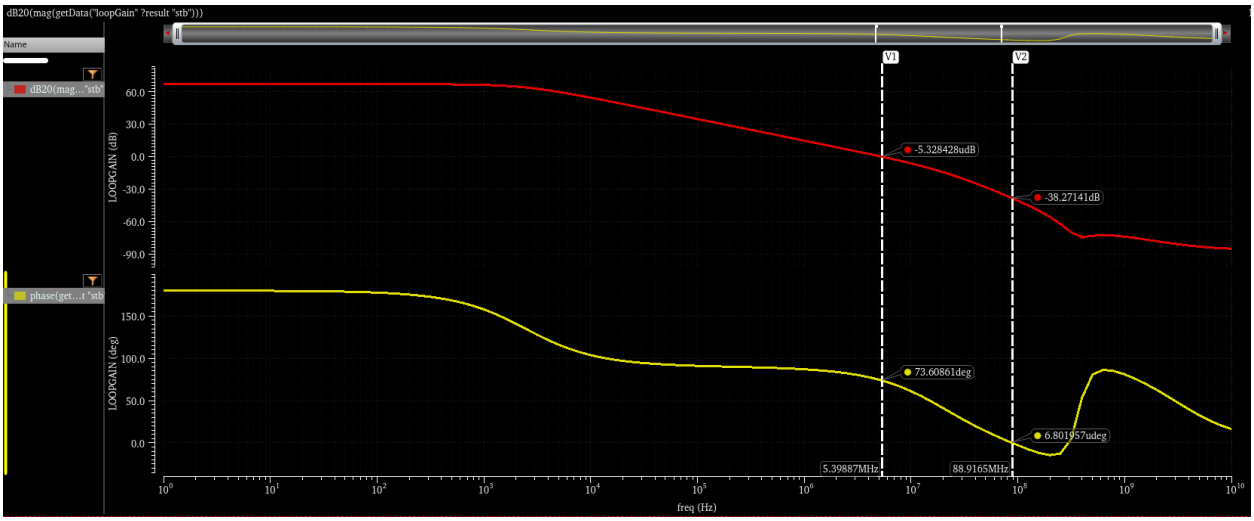
	Simulation	Hand Analysis
DC Gain (dB)	67.12	67.5
GBW (MHz)	5.02	5.24

Slew Rate

In order to meet the spec, we reduce Cc → Cc_{new} = 2.15pF



We need to check on phase margin



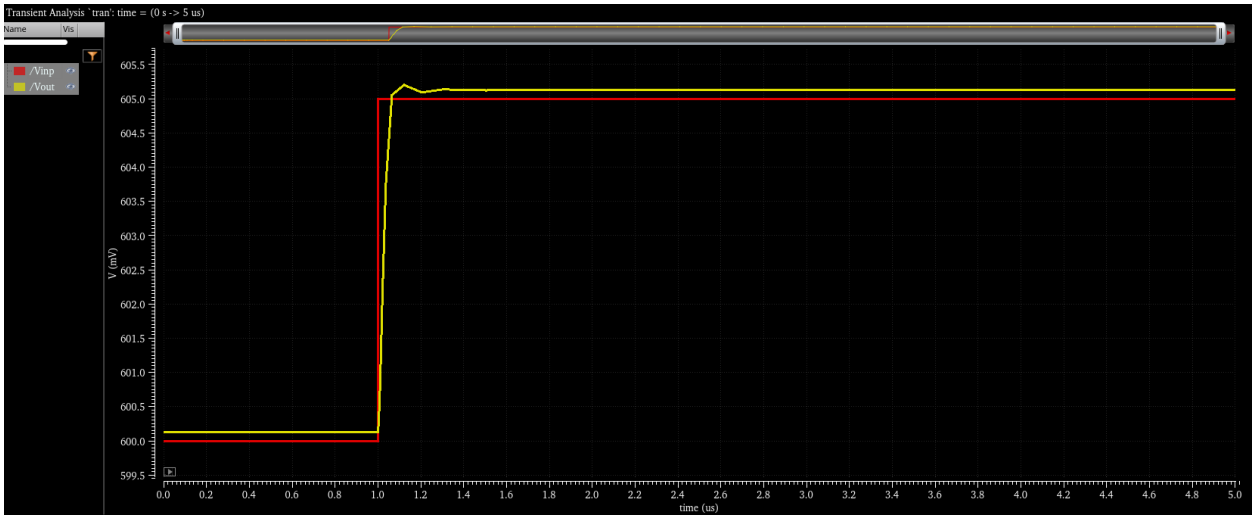
Phase margin = 73.6deg → we still meet the spec.

Hand Analysis

$$SR = \frac{I_{B1}}{C_c} = \frac{12u}{2.15p} = 5.58V/\mu s$$

	Simulation	Hand Analysis
SR (V/μs)	5.01	5.58

Settling Time



riseTime(v("/Vout" ?result "tran") 60...

	Expression	Value
1	riseTime(v("/Vou...	47.84E-9

Hand Analysis

- UGF after Cc modification = 5.4MHz = $\frac{1}{2\pi\tau}$ → τ = 29.5ns
- Rise time = 2.2τ = 64.8ns

	Simulation	Hand Analysis
Rise Time (ns)	47.84	64.8

Comments

- Rise time of simulation is better because using t_{rise} = 2.2τ is based on first-order model, while this a 2nd order, critical-damped system, which is faster from over-damped system.
- There is no ringing, because we designed our circuit for critical-damped response ($\omega p2$=4$\omega u1$). However, there is an overshoot because the error is multiplied with the gain.

Part 5: DC Closed Loop AC Open-Loop OTA Simulation