وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Dr. Hesham Omran
Ain Shams University – Master Micro LLC

Analog IC Design – Cadence Tools & SA
Lab 06
Differential Amplifier

Intended Learning Objectives

In this lab you will:

- Design a differential amplifier circuit using the Sizing Assistant (SA).
- Learn how to simulate the small-signal differential characteristics of a differential amplifier.
- Learn how to simulate the small-signal common-mode characteristics of a differential amplifier.
- Learn how to simulate the large-signal differential characteristics of a differential amplifier.
- Learn how to simulate the large-signal common-mode characteristics of a differential amplifier.

NOTE: To get access to the Sizing Assistant (SA) please register at https://adt.master-micro.com/ and create a support ticket from your dashboard. Verified instructors may also request access to an editable MS Word version of the labs and the model answers.

NOTE: The values and charts used in the lab document assume the provided 180 nm educational device models and 1.8 V supply. Other models/technologies can be used by applying reasonable adjustments to the lab values.

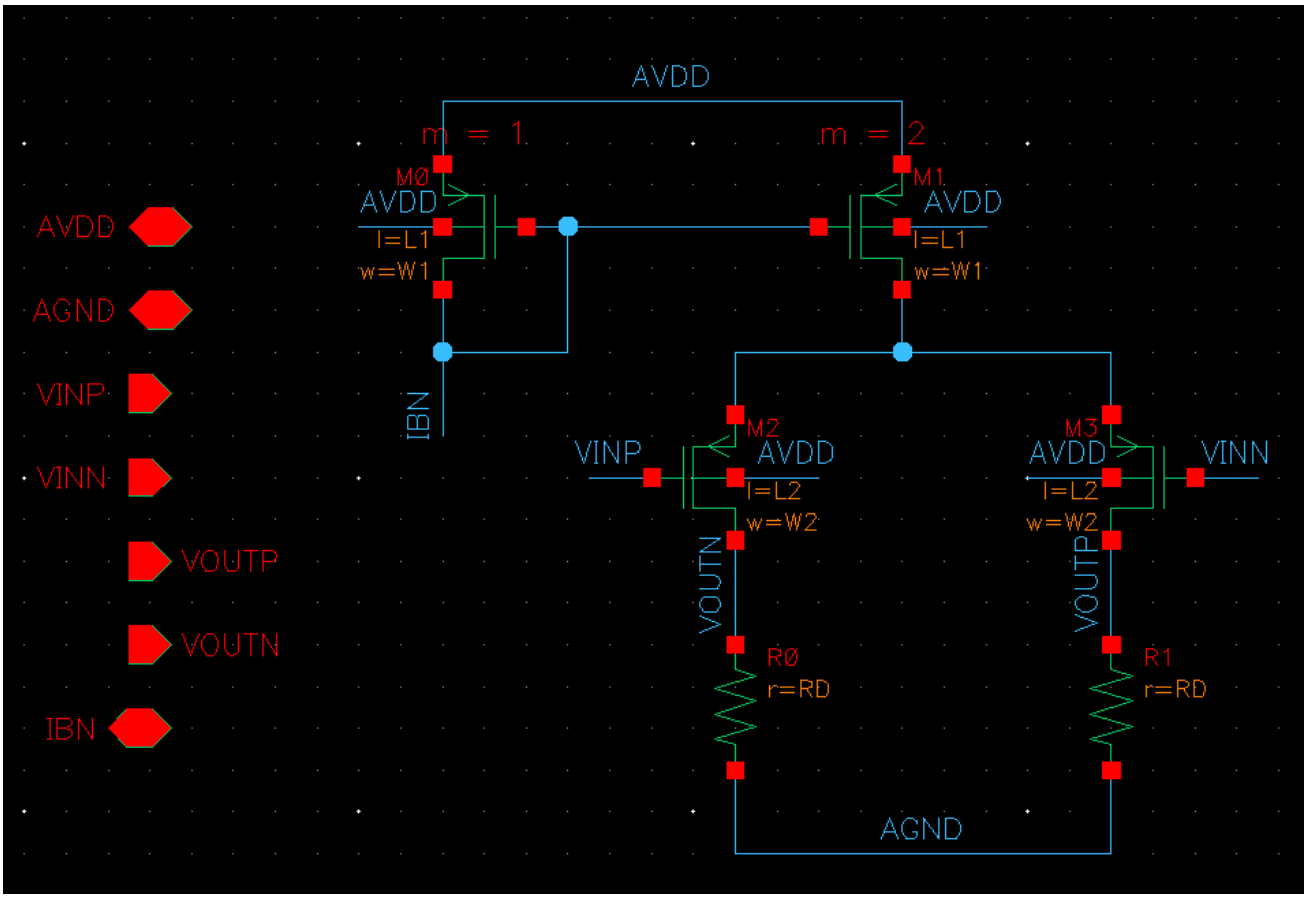
Part 1: Differential Amplifier Design

1) We want to design a resistive loaded differential amplifier with the specifications below.
   NOTE: that the bias current is split between two transistors; each transistor gets $I_D = 20\mu A$.

Parameter	
Supply (V_{DD})	$1.8V$
Bias current (I_{SS})	$40\mu A$
Differential gain	8
CM output level[1]	$V_{DD}/3$
Load capacitance	$1pF$

[1] Note that $I_{SS}R_D = 2V_{out-CM}$ must be smaller than $(V_{DD} - V_{dsat3})$ for proper large signal characteristics (why?).

2) Since the output level is closer to the ground rail, we will use a PMOS input stage. Assume the PMOS will not be placed in a dedicated well to save the area. Assume we will use a simple current mirror for biasing.
   - ➔ Cadence Hint: You can add labels (names) to nets (wires) using the hotkey "l" and create ports using the hotkey "p".
   - ➔ Cadence Hint: We will put the circuit under test in a schematic, create a symbol, then create a new schematic for the testbench. For design variables (e.g., WN and LN), you can use pPar("VariableName"), which passes the variable to the upper level of hierarchy. The variables will appear when you instantiate the cell in the upper-level schematic.



3) **Choose R_D** to meet the CM output level spec.
4) The differential amplifier gain is given by

$$|A_v| \approx g_m(R_D||r_o)$$

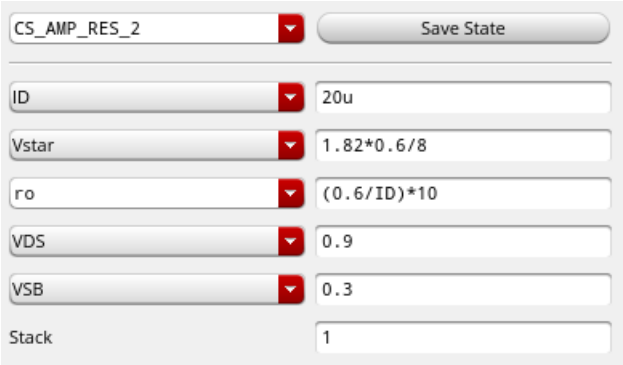
5) We will choose L to set $r_o \gg R_D$ → $r_o = 10 \times R_D$

$$|A_v| \approx 0.91 \times g_m R_D = 0.91 \times \frac{2I_D}{V^*} \times R_D = \frac{1.82V_{R_D}}{V^*}$$

6) **Choose V^*** to meet the differential gain spec.

$$V^* = \frac{1.82V_{R_D}}{|A_v|}$$

7) Assume we will set V_{DS} of the tail current source to $300mV$ to allow more output swing. **Report the input pair sizing using SA.**



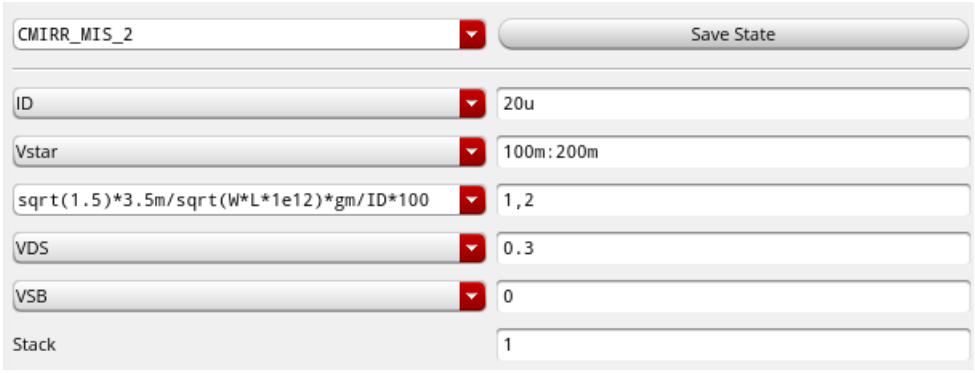
8) Give the above assumption, calculate the CM input level. **Calculate** the min and max CM input levels. Is the selected CM input level in the valid range?
9) The tail current source has the following specifications:

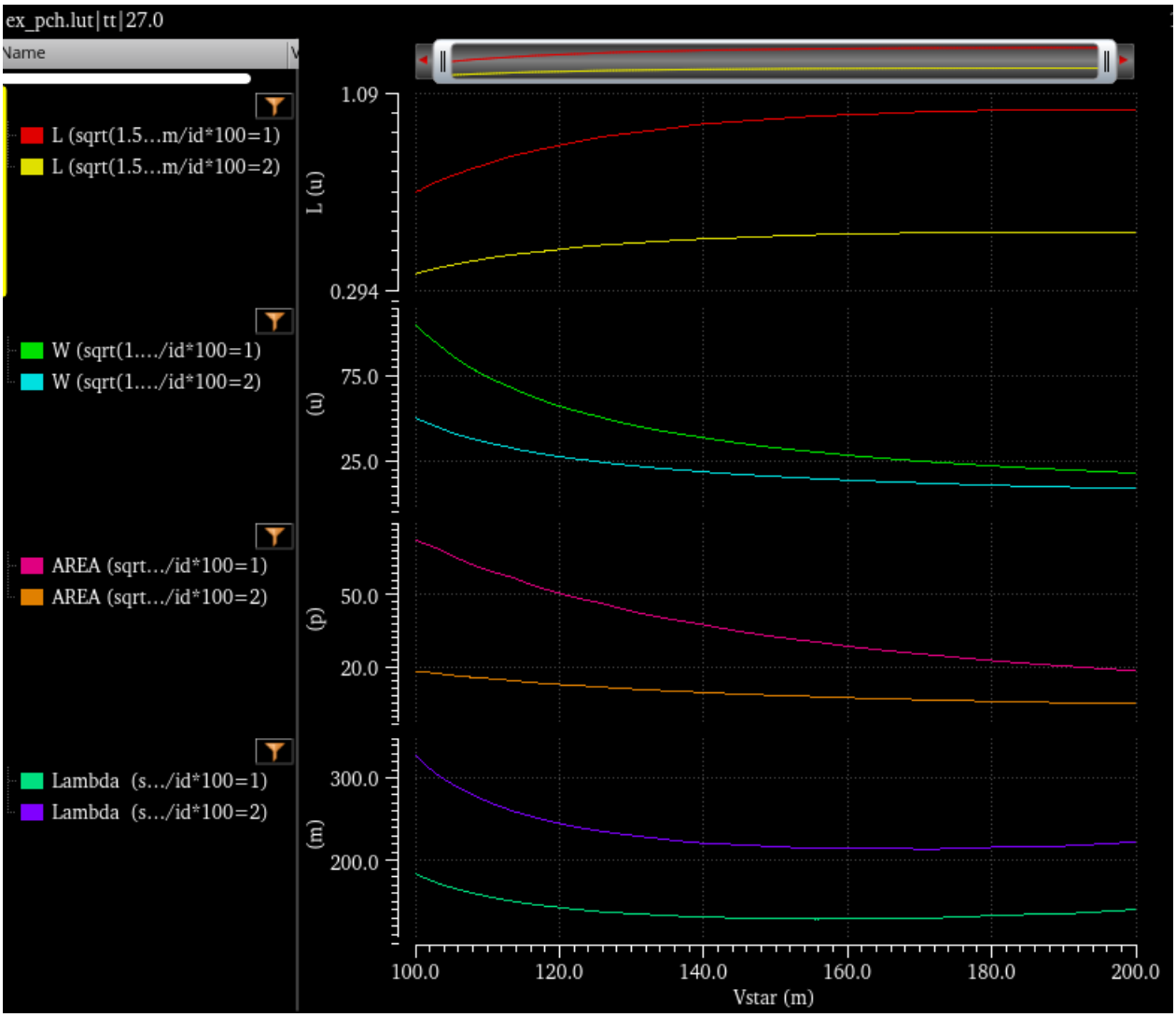
Parameter	
Input current	$20\mu A$
Percent mismatch: $\boldsymbol{\sigma(I_{out})/I_{out}}$	$\leq 2\%$
Compliance voltage	$\leq 200mV$
Area	Minimize

10) Use SA to plot the sizing at a constant $\boldsymbol{\sigma(I_{out})/I_{out}}$.

$$\frac{\boldsymbol{\sigma(I_{out})}}{\boldsymbol{I_{out}}} = \frac{\sqrt{\mathbf{1}+\frac{\mathbf{1}}{\boldsymbol{m}}} \times \frac{\boldsymbol{A_{V_T}}}{\sqrt{WL}} \times \boldsymbol{mg_m}}{\boldsymbol{mI_D}} \times \mathbf{100}$$

Where m is the mirroring ratio, $\boldsymbol{A_{V_T}} = \mathbf{3.5mV \cdot \mu m}$ is Pelgrom's coefficient, and the $\sqrt{1+\frac{1}{m}}$ factor is due to taking the difference between two random variables (V_{TH} of the two current mirror transistors).

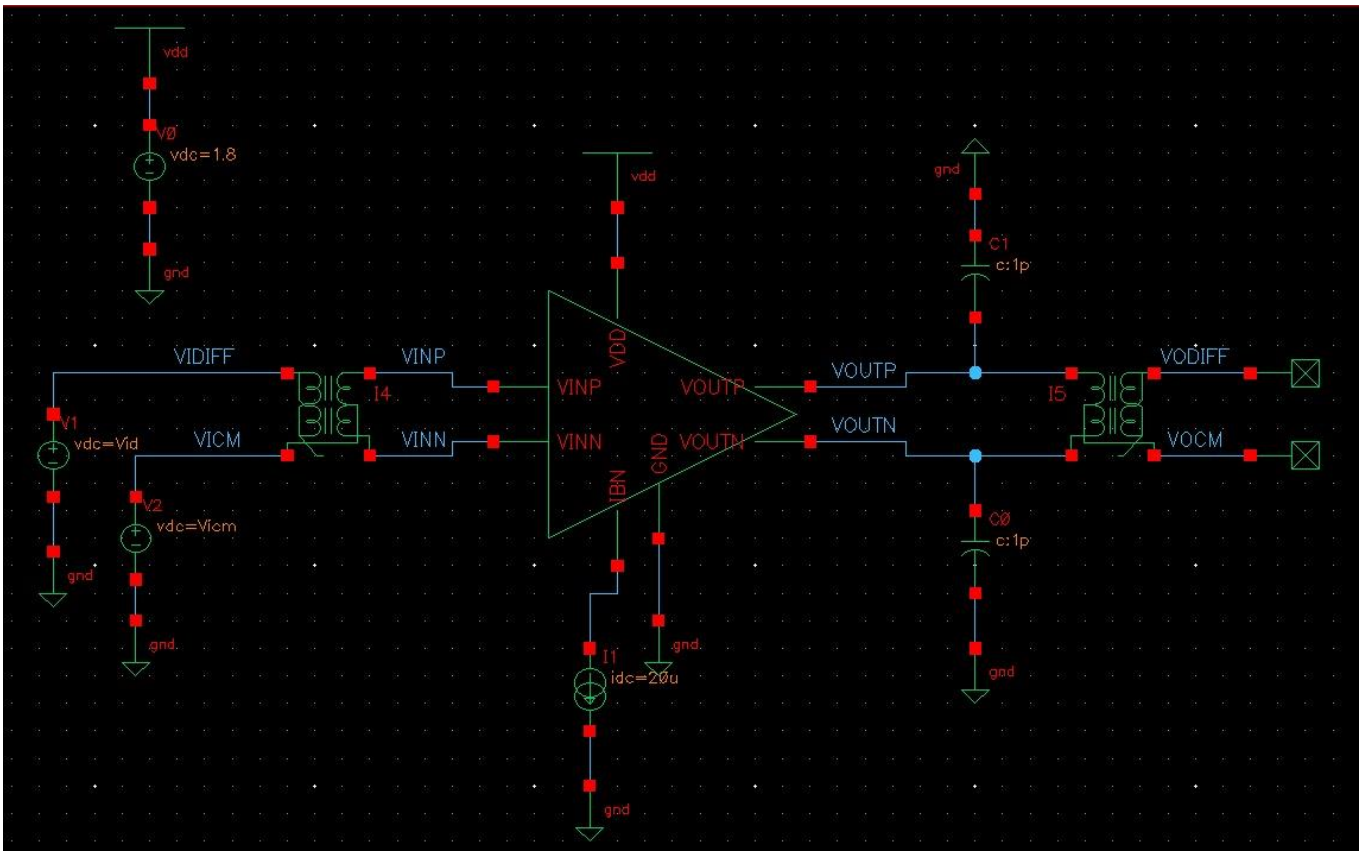




11) As seen in the plot, for a given mismatch requirement, the minimum area is achieved at the max V^*. Similarly, for a given area requirement, the minimum mismatch is achieved at the max V^*. That's why current mirrors are commonly biased in strong inversion.
12) Given the compliance voltage spec, **report** the above figure with a cursor added to the selected design point.

Part 2: Differential Amplifier Simulation

1) Create the schematic of a differential amplifier "lab_06_diff_amp".
2) Create a symbol for the diff pair. Edit the symbol to look as shown below in the testbench schematic.
   ➔ Cadence Hint: Use Create -> Cellview -> From Cellview.
3) Create a new cell for the testbench "lab_06_diff_amp_tb". Create the testbench schematic as shown below.
   ➔ Cadence Hint: Use ideal_balun from analogLib to separate common-mode and differential signals.



4) Set the transistor sizing and Vicm as designed in Part 1. Unless otherwise stated, set Vid = 0 (this is the large signal differential input voltage).
   NOTE: Use IB = 20uA (the CM multiplies this by 2, so each half in the diff pair gets IB).
5) Connect floating wires to avoid floating signal warnings.
   ➔ Cadence Hint: Use the noConn instance from basic library

Report the following:

1) OP simulation.
   - Report the schematic of the diff pair with DC OP point clearly annotated.

ID
VGS
VDS
VTH
VDSAT
Vstar = 2/(gm/ID)
gm/ID
GM
GDS
GMB
Region

   - Check that all transistors operate in saturation.
2) Diff small signal ccs:
   - Use AC magnitude = 1 for the diff source (and AC magnitude = 0 for the CM source).
   - Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
   - Report the Bode plot of small signal diff gain.
   - Compare the DC diff gain and BW with hand analysis in a table.
3) CM small signal ccs:

- Use AC magnitude = 1 for the CM source (and AC magnitude = 0 for the diff source).
- Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
- Report the Bode plot of small signal CM gain.
- Compare the DC CM gain with hand analysis in a table. Is it smaller than "1"? Why?
- Justify the variation of Avcm vs frequency.
- Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table.
  - ➔ Cadence Hint: In adexl you can access the results of the last 10 simulation runs from the "History" tab. We want to access the last two simulation runs in order to compare Avd and Avcm. Open both simulations in the Results Browser.
  - ➔ Cadence Hint: Note that xf analysis cannot be used in this case because we have two outputs (Diff and CM). xf analysis is useful for the case of single-ended output op-amp where there is only one output terminal. It is also useful for fully diff op-amp to calculate CMRR(SE2diff), but not Avd/Avcm.
- Justify the variation of Avd/Avcm with frequency.

4) Diff large signal ccs:
   - Use dc sweep (not parametric sweep) for Vid = -VDD:10m:VDD.
   - Report diff large signal ccs (VODIFF vs VIDIFF). Compare the extreme values with hand analysis in a table.
5) CM large signal ccs (region vs VICM):
   - We will use the region parameter to know the operating region of each transistor vs sweep variable.
     - ➔ Cadence Hint: The "region" parameter meaning is as follows:
       0: cut-off
       1: triode
       2: sat
       3: subth
       4: breakdown
   - Use DC sweep (not parametric sweep) for Vicm = 0:10m:VDD (no need to run AC sim)
     - ➔ Cadence Hint: To save the "region" parameter, add this this line to your save.scs file (in Model Libraries):
       save *:region sigtype=dev.
   - Disable ac analysis.
   - Plot "region" OP parameter vs Vicm for the input pair and the tail current source.
   - Find the CM input range (CMIR). Compare with hand analysis in a table.
   - Note that the drawback of this method is that the "region" parameter cannot be experimentally measured in the lab and is not quantitively related to circuit specifications.
6) CM large signal ccs (GBW vs Vicm):
   - Use ac analysis (start = 1, stop = 1, pts(linear) = 1) to get Avd. Use parametric sweep (not dc sweep) for Vicm = 0:20m:VDD.
     - ➔ Cadence Hint: Instead of using parametric sweep, a better alternative in Cadence is to use AC sweep but sweep a design variable (Vicm) instead of sweeping the frequency. The frequency is set at 1 Hz (or any other small value) to get the low frequency gain (DC gain).
     - ➔ Cadence Hint: Use the following expression in adexl to calculate Avd: ymax(mag(VF("/VODIFF")))
   - Report CM large signal ccs (Avd vs Vicm). Assume the valid range for Vicm (CMIR) is defined by the condition that Avd is within 90% of the max gain, i.e., 10% drop in gain.
     NOTE: The bandwidth of this circuit is determined by RD and CL, i.e., it is independent of Vicm, thus Avd variation is itself GBW variation.

- Plot the results overlaid on the results of the previous method (region parameter). Find the CM input range. Compare with the previous method in a table.

Lab Summary

- In Part 1 you learned:
  - How to design a resistive-loaded differential amplifier.
- In Part 2 you learned:
  - How to use an ideal balun to test a differential amplifier.
  - How to simulate the small-signal differential gain of a differential amplifier.
  - How to simulate the small-signal common-mode gain of a differential amplifier.
  - How to simulate the large-signal differential characteristics of a differential amplifier.
  - How to simulate the large-signal common-mode characteristics of a differential amplifier.

Acknowledgements

Thanks to all who contributed to these labs. Special thanks to Dr. Sameh A. Ibrahim for reviewing and editing the labs. If you find any errors or have suggestions concerning these labs, please contact Hesham.omran@eng.asu.edu.eg.