

Analog IC Design – Cadence Tools & SA**Lab 05****Simple vs Wide Swing (Low Compliance) Cascode Current Mirror****Intended Learning Objectives**

In this lab you will:

- Explore current mirror sizing trade-offs using Sizing Assistant (SA).
- Bias a cascode device using a series resistance.
- Design and simulate simple and wide swing (low-voltage) current mirrors.
- Compare simple and low-voltage current mirrors.

NOTE: To get access to the Sizing Assistant (SA) please register at <https://adt.master-micro.com/> and create a support ticket from your dashboard. Verified instructors may also request access to an editable MS Word version of the labs and the model answers.

NOTE: The values and charts used in the lab document assume the provided 180 nm educational device models and 1.8 V supply. Other models/technologies can be used by applying reasonable adjustments to the lab values.

Part 1: Exploring Sizing Tradeoffs Using SA

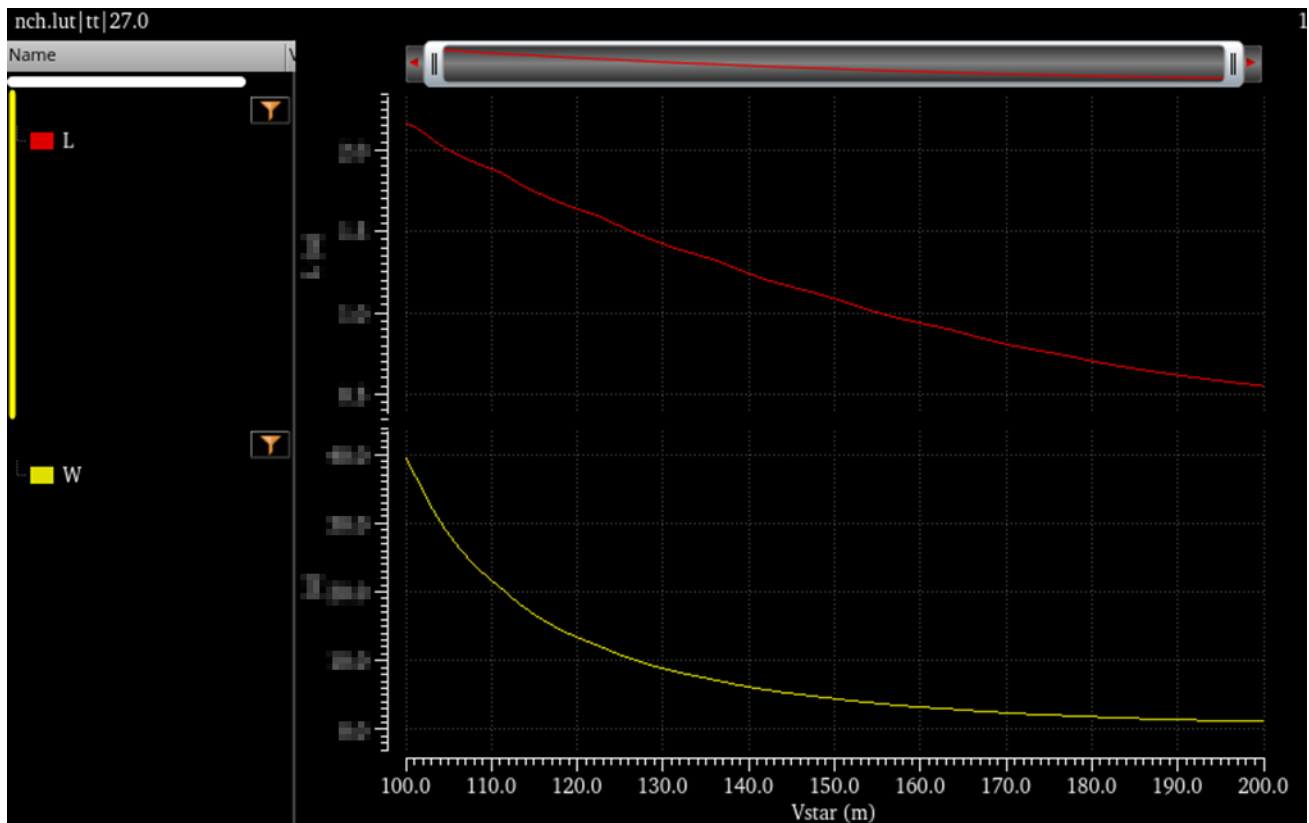
- 1) We want to design a simple current mirror with the following specs.

Parameter	
Input Current	10 μA
Output Current	20 μA
% Change in Current for $\Delta V_{out} = 1V$	< 10%
Current direction (source/sink)	Sink

Answer the following:

- 2) The % Change in current translates to a spec on the $\lambda = 1/V_A$ of the device. How much is the required λ ?
- 3) Sinking current means which device type? NMOS or PMOS?
- 4) The higher the g_m/I_D (the lower the V^*) the higher the headroom (the available swing), but the larger the area. Examine this trade-off using SA as shown below. Report L and W vs Vstar.

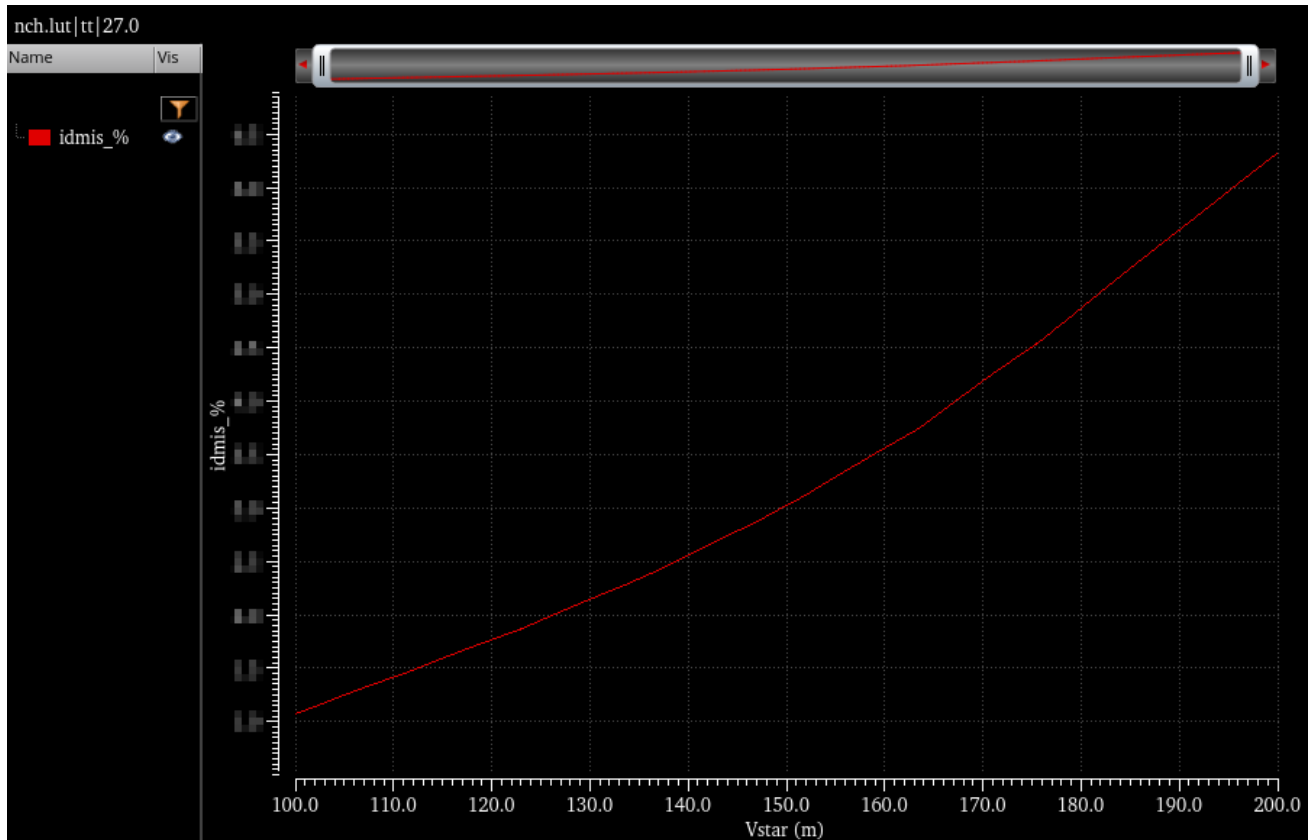
CMIRR_CLM	Save State
ID	10u
Vstar	100m:200m
1/VA	0.1
VDS	1
VSB	0
Stack	1



- 5) Another related tradeoff is the random mismatch, which is inversely proportional to the device area. Assume Pelgrom's coefficient for V_{TH} random mismatch is $5mV \cdot \mu m$. Plot the % rms (standard deviation, i.e., sigma) change in current vs Vstar using this expression in SA:

$$\text{idmis}_{\%} = 5m / \sqrt{W \cdot L \cdot 1e12} \cdot \text{gm} / \text{ID} \cdot 100$$

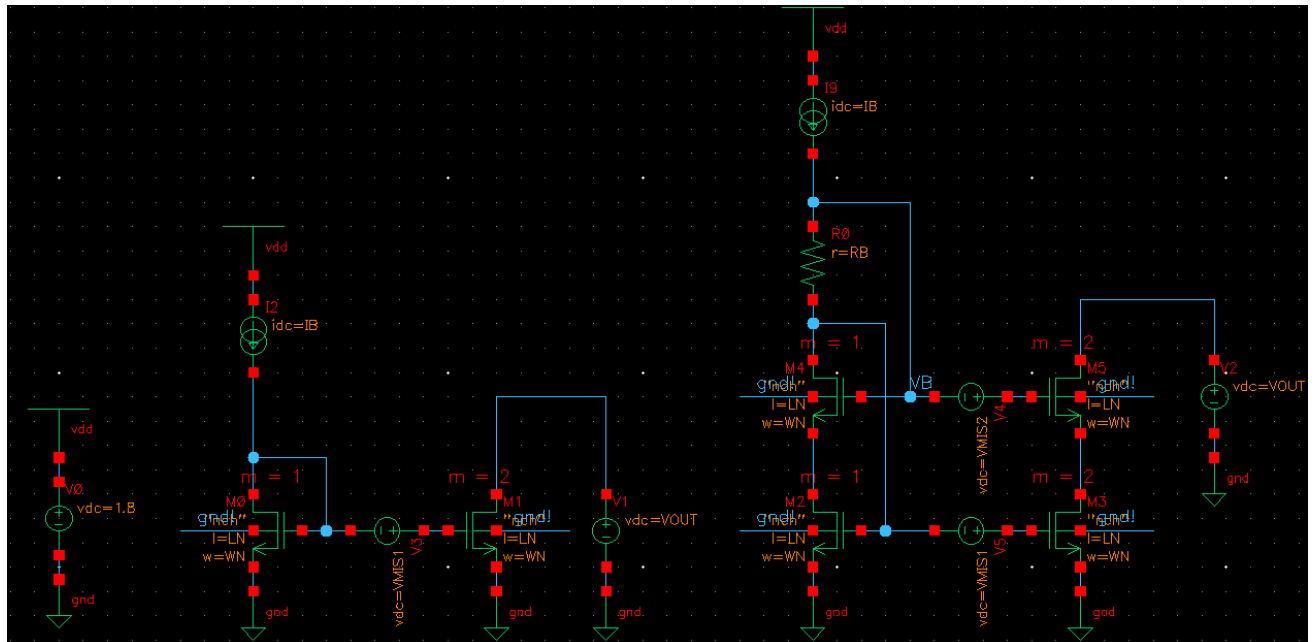
➔ ADT Hint: If the LUT contains mismatch data, we can directly use the parameter `idmis` in SA to get the standard deviation of the current random variations. The mismatch data can be added to any LUT using ADT by using an appropriate Monte Carlo mismatch model file.



- 6) Pick a bias point (V_{star}) that gives $idmis < 3\%$. Determine W and L . We will use these sizing parameters for the cascode current mirror as well.
- 7) Can we do the previous design trade-offs exploration sweeps using a standard SPICE simulator, i.e., sweep V_{star} at a constant λ ? Why?

Part 2: Current Mirror Simulation

- 1) Create a new schematic. Construct the circuit shown below. or using the toolbar.
 - ➔ Cadence Hint: You can add labels (names) to nets (wires) using the hotkey “l” and create ports using the hotkey “p”.
 - ➔ Cadence Hint: You can put the circuit under test in a schematic, create a symbol, then create a new schematic for the testbench. For design variables (e.g., W_N and L_N), you can use `pPar(“VariableName”)`, which passes the variable to the upper level of hierarchy. The variables will appear when you instantiate the cell in the upper level schematic.
- 2) The current mirror takes input current I_B and generates output current $= 2 \cdot I_B$ (note the multiplier setting in the output branch).
- 3) Instead of using a wide-swing bias transistor (a magic battery) to generate V_B , we use a resistor R_B in series with the input branch.
- 4) Unless otherwise stated, set $V_{OUT} = V_{DD}/2$ and $V_{MIS1} = V_{MIS2} = 0$.



1. Design and OP (Operating Point) Analysis

- 1) Assume we want to set a $50mV$ saturation margin for M2 and M3, i.e., $V_{DS2} \approx V_{DS3} \approx V^* + 50mV$. Ignore the body effect and **calculate** a rough value for R_B .

Hint:
$$R_B = \frac{V_{GS4} + V_{DS2} - V_{GS2}}{I_B} \approx \frac{V_{DS2}}{I_B}$$

Hint: The purpose of doing rough analysis is not to reach a final design point, but to calculate a value that makes sense and can be used to determine a reasonable range for a simulator sweep.

- 2) Perform DC sweep (not parametric sweep) for R_B . Choose a reasonable sweep range given the rough value computed in the previous step. **Report** V_{DS3} vs R_B . **Choose** R_B to satisfy the $50mV$ saturation margin requirement. Is the selected R_B value larger or smaller than the rough analytical value? Why?

➔ Cadence Hint: The DC sweep is performed in a simulator inner loop, so it is very fast and takes small disk space. The parametric sweep is an outer loop repetitive calling of the simulator, so it is much slower and takes much larger disk space.

- 3) Simulate the OP point. Report a snapshot clearly showing the following parameters.

➔ Cadence Hint: You can use Info Balloons (View -> Info Balloons) to show the device parameters. Use (View -> Annotations -> Setup) to customize the Info Balloons.

➔ Cadence Hint: You can add expressions to the Info Balloons, e.g., $V_{star} = 2/(gm/ID)$.

ID
VGS
VDS
VTH
VDSAT
$V_{star} = 2/(gm/ID)$
gm/ID
GM
GDS
GMB
Region

- 4) Do all transistors operate in saturation?

2. DC Sweep (I_{out} vs V_{OUT})

- 1) Perform DC sweep (not parametric sweep) using $V_{OUT} = 0:10m:V_{DD}$. Report I_{out} vs V_{OUT} for the two CMs overlaid in the same plot.
 - Comment on the difference between the two circuits.
 - From the plot, find an estimate for the compliance voltage of each current mirror.
 - I_{out} of the simple CM is exactly equal to $I_B \cdot 2$ at a specific value of V_{OUT} . Why?
- 2) For the simple current mirror, calculate the percent change in I_{out} when V_{OUT} changes from 0.5V to 1.5V (i.e., 1V change). Compare the result to the value expected from Part 1.
- 3) Report the percent of error in I_{out} vs V_{OUT} (ideal I_{out} should be $I_B \cdot 2$) for the two CMs in the current mirror operating region ($V_{OUT} \approx V^*$ to V_{DD}) overlaid in the same plot.
Hint: Calculate percent of error as $(\text{simulated} - \text{ideal}) / \text{ideal} \cdot 100$
 - Comment on the difference between the two circuits.
- 4) Report R_{out} vs V_{OUT} (take the inverse of the derivative of I_{out} plot) for the two CMs in the current mirror operating region ($V_{OUT} \approx V^*$ to V_{DD}) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at $V_{OUT} = V_{DD}/2$.
 - Comment on the difference between the two circuits.
 - Does R_{out} change with V_{OUT} ? Why?

➔ Cadence Hint: R_{out} can be also simulated using AC analysis. The value we used here should be the same as the AC analysis result at low frequencies.
- 5) Analytically calculate R_{out} of both circuits at $V_{OUT} = V_{DD}/2$. Compare with simulation results in a table.

3. Mismatch

NOTE: Practically, we study the mismatch using Monte Carlo simulation. However, since the educational device model we are using does not include a mismatch model, we will manually add mismatch in the circuit.

- 1) Set $VMIS1 = 5m/\sqrt{W \cdot L}$ and $VMIS2 = 0$. This models the standard deviation of the mismatch in V_{TH} for the current mirror devices. Run OP simulation. Find the percent change in I_{out} .
- 2) Analytically calculate the percent change in I_{out} and compare it to the simulation result.
Hint: The voltage change at the gate can be considered as a small signal. Thus, the change in the current can be calculated using the G_m of the circuit. In this case, the circuit can be considered as a cascode amplifier.
- 3) Set $VMIS1 = 0$ and $VMIS2 = 5m/\sqrt{W \cdot L}$. This models the standard deviation of the mismatch in V_{TH} for the cascode devices. Run OP simulation. Find the percent change in I_{out} .
- 4) Analytically calculate the percent change in I_{out} and compare it to the simulation result.
Hint: The voltage change at the gate can be considered as a small signal. Thus, the change in the current can be calculated using the G_m of the circuit. In this case, the circuit can be considered as a **degenerated** common source amplifier.
- 5) Which mismatch contribution is more pronounced? Why?
- 6) Which design decision is better: setting the same W and L for the mirror and cascode devices? Or using larger W and L for the current mirror devices? Why?

Lab Summary

In Part 1 you learned:

- How to use SA to examine current mirror design trade-offs.
- How to design a simple current mirror.

In Part 2 you learned:

- How to design a wide swing (low-voltage) current mirror.
- How the behavior of a simple current mirror changes with the output voltage.
- How the behavior of a low-voltage current mirror changes with the output voltage.

Acknowledgements

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