Static Timing Analysis

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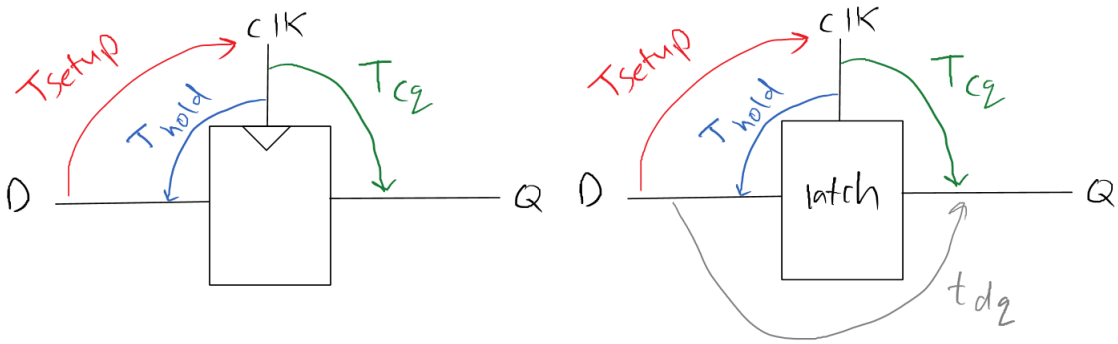
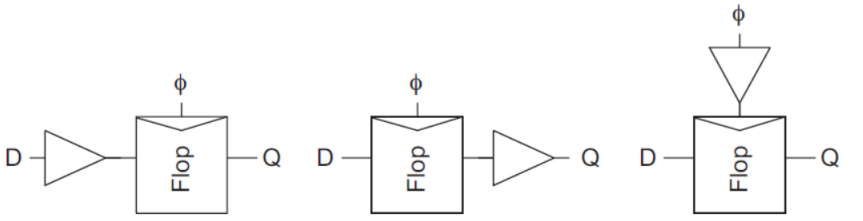
Timing Definitions

Contamination Delay: Output may begin to change or glitch.
Propagation Delay: Output must have settled to final value.
Setup Time: The time the input data signals are stable before the active clock edge occurs (D to CLK).
Hold Time: The time the input data signals are stable after the active clock edge occurs (CLK to D).
Aperture Time: Setup time + hold time
Sequencing Overhead: $t_{pcq} + t_{setup} + t_{skew}$
Recovery Time: The reset/set signal has to return to its normal state before the clock edge for this duration, similar to the setup time.
Removal Time: The reset/set signal has to remain in the reset/set state after the clock edge for this duration, similar to the hold time.



Notes:

- Tcq is useful when Q is CLK-sensitive like in FF (all cases) or in latch (when D is constant and latch toggles from opaque to transparent).
- We can achieve negative hold time by delaying the input (D). We can achieve a smaller setup time by delaying the CLK.
- The smaller the t_s, t_h and T_c, the bettter.
- t_{cq} can be different for the same FF cell due to different load capacitance.



$t'_{setup} = t_{setup} + t_{buf}$ $t'_{pcq} = t_{pcq}$ $t'_{hold} = t_{hold} - t_{buf}$

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Timing Analysis

Note: We measure clock period from a point to the same exact point in the next cycle (i.e, from CLK to CLK (same edge: -ve to -ve or +ve to +ve) or D to D).

Clock Skew & Jitter:

- **Clock Skew:** Spatial variation across chip
  - **Positive Skew:**
    - CLK's edge of FF2 is later than FF1.
    - CLK drivers are in the same direction as the combinational logic.
    - Difference between 2 CLK edges is increased.
    - Bad for hold time, since data must be preserved for a longer time (waiting for the delayed FF2's CLK edge).
  - **Negative Skew:**
    - CLK's edge of FF2 is earlier than FF1.
    - CLK drivers are in the opposite direction as the combinational logic.
    - Difference between 2 CLK edges is reduced.
    - Bad for setup time, since actual clock period is reduced for a given clock frequency.
- **Clock Jitter:** Temporal variation at the same element (random)
  - **Worst case (setup):** When launching FF is late & capturing FF is early. Actual clock period is reduced (for a given frequency).
  - **Worst case (hold):** When launching FF is early & capturing FF is late. Data is held for a longer time.

Max-delay constraints:

- Maximum propagation delay (data didn't settle before CLK edge)
- Setup time failure
- $T_c + t_{skew} > T_{pcq} + t_{pd} + t_s$ (t_{skew} is a negative number for worst case)

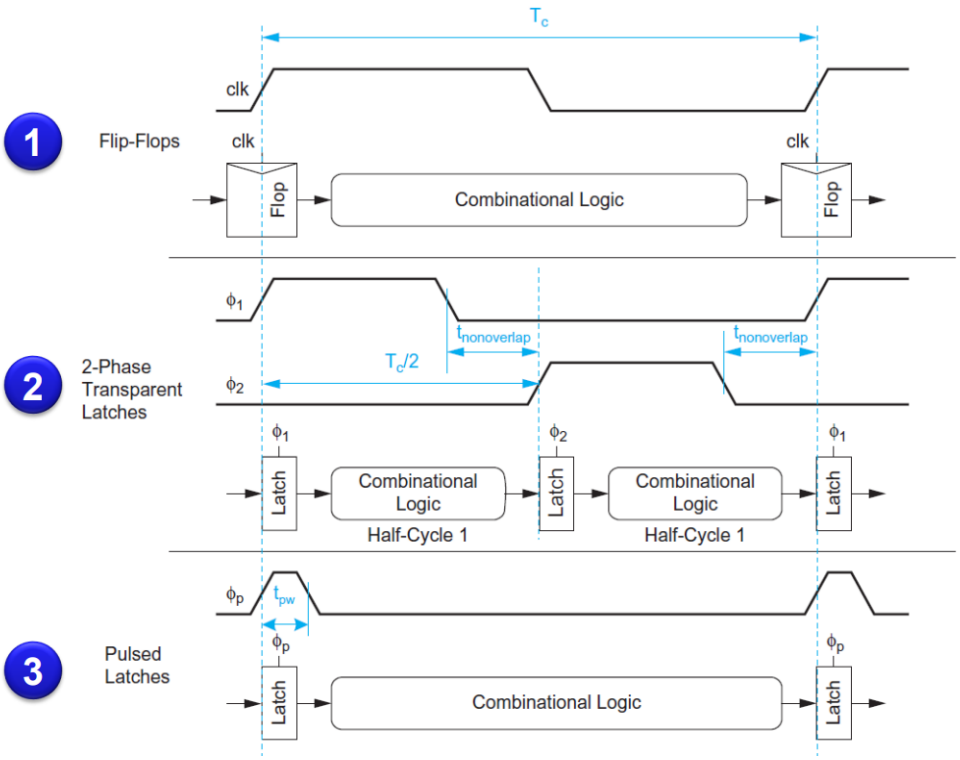
Min-delay constraints:

- Minimum contamination delay (early change of data after CLK edge or data is so fast that it passes through several FFs during the same clock cycle.)
- Hold time failure (race condition)
- $t_h + t_{skew} < t_{ccq} + t_{cd}$ (t_{skew} is a positive number for worst case)

Note:

- In synthesis tool, we set input delay constraint from launching FF's CLK to the design block's input. The output delay is set from the design block's output to the capturing FF's CLK.
- Slack = Required time - Arrival time.
  - **Setup:** slack = $(T_{clk} - t_{setup}) - (T_{pcq} + t_{pd})$
  - **Hold:** slack = $(T_{ccq} + t_{cd}) - T_{hold}$.

Extra: Latch-Based Systems



Maximum delay is given by:

- **2-phase transparent latch:** $T_c > T_{pdq1} + t_{pd1} + T_{pdq2} + t_{pd2}$
- **Pulsed Latch (D changes during pulse):** $T_c > T_{pdq} + t_{pd}$ $(t_{pw} > t_s)$
- **Pulsed Latch (D constant during pulse):** $T_c > T_{pcq} + t_{pd} + t_s - t_{pw}$ (from +ve edge CLK) $(t_{pw} < t_s)$

Minimum delay is given by:

- **2-phase transparent latch:** $t_h < t_{ccq} + t_{cd} + t_{nonoverlap}$
- **Pulsed Latch:** $t_h + t_{pw} < t_{ccq} + t_{cd}$
- **Note:** No timing violation for min delay if hold time is negative.

Time Borrowing:
Time borrowing is only valid when system is latch-based (not FF), because it is not edge-sensitive, so data can be late and will still pass when latch is transparent.

- Max borrowing time:
  - **2-phase latch:** $t_{borrow} < T_c/2 - (t_s + t_{nonoverlap})$
  - **Pulsed latch:** $t_{borrow} < t_{pw} - t_s$
- Actual borrowing time:
  - **2-phase latch:** $t_{borrow} = t_{pdq} + t_{pd} - T_c/2$
  - **Pulsed latch:** $t_{borrow} = t_{pdq} + t_{pd} - T_{pw}$

Clock Skew:

- **2-phase latch:** It reduces $t_{nonoverlap}$.
- **Pulsed latch:** It reduces t_{pw}.
- Therefore, skew increases hold time and reduces borrowing time.