Afolabi Ige: afolabiige.me | aige3@gatech.edu

Education

GRAD: PHD & MASTERS. ECE MAJOR, CS MINOR. FALL 2020 – SUMMER 2025. **GEORGIA TECH**
UNDERGRAD: ECE & CS DOUBLE MAJOR. FALL 2015 – SPRING 2020. **LSU**

Industry Experience

APPLE | PHYSICAL DESIGN ENGINEERING INTERN - GPU | MAY 2024 – AUGUST 2024

- Cannot discuss project specifics but worked to improve PPA metrics by implementing optimization techniques across placement and CTS.

APPLE | DESIGN FOR TEST INTERN | MAY 2021 – AUGUST 2021

- Converted the DFT-DV testbench to a simulator agnostic design by implementing another Verilog simulator while also implementing new testbench features at request of DV methodology team.

AMAZON | SOFTWARE ENGINEER INTERN | JUNE 2020 – AUGUST 2020

- Implemented an Audit trail into a massive customer facing application and worked across the full stack.
- This required setting up a new data store, creating backend functions, creating an internal API, working with many AWS resources, and pulling information from the API to display with typescript on a React website.

AMAZON | SOFTWARE ENGINEER INTERN | JUNE 2019 – AUGUST 2019

- Built metric dashboard from scratch in React with Elastic Search as a data store.
- Setup a data pipeline that used an internal wrapper on Elastic Map Reduce to aggregate billions of records and write to Kinesis FireHose which funneled into Elastic search.

CHEVRON | SOFTWARE ENGINEER INTERN | MAY 2018 – AUGUST 2018

- Automated CI/CD deployment process to Dev, QA and Prod servers using the Jenkins tool.
- Implemented and enhanced automated maintenance scripts for over 30+ servers.

CHEVRON | SOFTWARE ENGINEER INTERN | JUNE 2017 – AUGUST 2017

- Analyzed 30+ applications on site to extract interface patterns and created a cloud deployment plan that avoided downtime.

Academic Projects

ANALOG COMPUTING SYNTHESIS TOOLCHAIN

- Journal: **Ige, A**.; Yang, L.; Yang, H.; Hasler, J.; Hao, C. “Analog System High-Level Synthesis for Energy-Efficient Reconfigurable Computing.” J. Low Power Electron. Appl. 2023, 13, 58.
- Best Paper runner-up: L. Hanks, C. Lonergan, K. Richardson, J. Hasler, P. Mathews, **A. Ige**. “Analog High-Level Synthesis for Field Programmable Analog Arrays” in 2024 IEEE International Opportunity Research Scholars Symposium (ORSS)
- CRNCH Fellowship award and Design Automation Conference poster

ANALOG STANDARD CELL LIBRARIES

- Journal: J. Hasler; P. Ayyappan; **A. Ige**; P. Mathews “A 130nm CMOS Programmable Analog Standard Cell Library”. Transactions on Circuits and Systems I: Regular Papers.
- Journal: P. O. Mathews, P. Raj Ayyappan**, A. Ige**, S. Bhattacharyya, L. Yang and J. O. Hasler, "A 65 nm CMOS Analog Programmable Standard Cell Library for Mixed-Signal Computing," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 32, no. 10, pp. 1830-1840, Oct. 2024
- CICC: P. Mathews; P. Ayyapan; **A. Ige**; S. Bhattacharyya; L. Yang; “A 65nm and 130nm CMOS programmable analog standard cell library for scalable system synthesis”. IEEE Custom Integrated Circuits Conference 2024.

FULLY ANALOG MACHINE LEARNING

- **A. Ige** and J. Hasler, “Efficient implementation of a fully analog neural network on a reconfigurable platform,” in 2023 IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS).