Afolabi Ige

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Education

M.S | GEORGIA INSTITUTE OF TECHNOLOGY | ELECTRICAL ENGINEERING | DEC 2021
B.SC | LOUISIANA STATE UNIVERSITY | MAY 2020

Double Major - Electrical Engineering and Computer Science

Work Experience

HARDWARE ENGINEER INTERN | APPLE | MAY – AUG 2021

- Documented complex features of DFT verification environment for the DV team
- Implemented new testbench features at request of DV methodology team
- Converted the DFT-DV testbench to a simulator agnostic design by implementing support for another Verilog simulator

SOFTWARE DEVELOPMENT ENGINEER INTERN | AMAZON | YEAR 1 AND 2

Remote Work | Year 2 | June – August 2020

- Implemented an Audit trail into a massive customer facing application and worked across the full stack.
- This required setting up a new data store, creating backend functions, creating an internal API, working with many AWS resources, and pulling information from the API to display with typescript on a React website.

Seattle, WA | Year 1 | June – August 2019

- Built metric dashboard from scratch in React with Elastic Search as a data store.
- Setup a data pipeline that used an internal wrapper on Elastic Map Reduce to aggregate billions of records and write to Kinesis FireHose which funneled into Elastic search.

Research Work

CREATING AN ANALOG STANDARD CELL LIBRARY | GATECH | AUG 2020 – MAY 2021

The ICE lab under Dr Hasler has been developing the field of analog computation by leveraging floating gates(FG). One of the fruits of the lab is a Field Programmable Analog Array (FPAA) like the FPGA counterpart.

- I implemented the core FG cell, a 4x2 FG bias cell, transconductance amplifier and many variations of the FG cell.
- For the layouts above, they passed DRC checks and I implemented schematics that passed LVS as well.

ATOMIC FORCE MICROSCOPE | LSU | JAN – MAY 2020

Description: As part of the research work in the Applied Hybrid Electronic Materials & Structures (AHEMS) lab, my professor asked me to continue the building of an AFM that would be cheaper than commercially available.

- I disassembled a complex circuit and simulated all the major parts.
- I made upgrades and changes to the design as part of a goal to increase accessibility of the AFM.
- Designed a PCB circuit for the device and created documentation detailing work done.

School Work

13-BIT TWO STAGE PIPELINED ADC | GATECH | ANALOG SYSTEM DESIGN

The project for our 6414 class required the design of a 12-bit ENOB ADC down to transistor level. This entailed design of a 6-bit MDAC first stage and 8-bit SAR second stage.

- I implemented a CDAC array and SAR Logic for both 6- and 8-bit stages.
- I implemented a strong-arm latch comparator as well as various lower-level gates (nor, D & JK flops, and etc)
- I implemented clock generation for the phi early, phi 1, phi 2 and SAR logic signals for both stages from a master clock.

6 TRANSITOR SRAM CELL | GATECH | ADVANCED VLSI

- I implemented the layout and schematic of a 6T SRAM cell.
- The layout passed design rule check (DRC) as well as layout versus schematic (LVS) checks.

Projects

EMERSON WANTS TO PLAY BASEBALL | LSU | SEP 2019 – MARCH 2020

Description: For my capstone project, my team was tasked with building a device that was able to give a 12-year-old girl with cerebral palsy, the ability to toss a baseball with friends and family.

- I designed and assembled the PCB which was responsible for controlling all electronics on board.
- I designed and created a remote that mounted to her wheelchair with large buttons tailored to her needs.