Albert Gafiyatullin

Compiler Engineer

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SUMMARY

Software Engineer with 2+ years of experience specializing in the development of programming language compilers and runtimes. Interested in system programming, LLVM, compiler technologies, operating systems, computer architecture.

EXPERIENCE

Samsung Research Russia
Moscow, Russia

- *NPU Compiler Engineer, SOC SW Lab*
Jul. 2023 - Present

  `C++`

Unipro
Novosibirsk, Russia

- *Compiler Engineer, Java Virtual Machine team*
Mar. 2021 - Jun. 2023

  `C++` `JVM` `Assembly Language` `JIT Compilers Design` `Garbage Collection` `GNU Debugger` `Perf`

  JVM Runtime and JIT Compiler development for Elbrus VLIW processor by MCST:

  - Adapted the C2 compiler for tiered compilation, which improved average startup performance by 50% compared to non-tiered compilation;
  - Designed and implemented a fast compiler named 'C0' for warmup compilation levels (instead of C1), taking into account the features of Elbrus VLIW CPU architecture. This resulted in a 25% improvement in average startup performance for machines with a small number of cores, compared to tiered compilation based on the adapted C2 compiler;
  - Improved performance for certain string and XML tasks by up to 8% using intrinsics;
  - Reduced runtime overhead by implementing platform-dependent improvements for implicit null checks.

PROJECTS & COURSES

COOL Compiler
- `C++` `LLVM` `Garbage Collection` `Compilers Design` `GNU Debugger`
Sep. 2021 - Feb. 2023

  Implementation of COOL compiler and runtime with LLVM:

  - AArch64 and x86-64 as target architectures;
  - Stop-The-World Mark-and-Sweep, Mark-and-Compact and Semispace Copying Garbage Collectors.

SOE.YCSCS1: Compilers
- `C++` `MIPS` `Compilers Design` `Assembly Language`
Oct. 2021

  Implementation of COOL compiler for SPIM emulator.

ENGR85A: Digital Design
- `SystemVerilog` `Circuit Design`
Apr. 2023

  Combinational and sequential circuits design.

ENGR85B: Computer Architecture
- `RISC-V` `Computer Architecture` `SystemVerilog` `Embedded Systems` `Circuit Design`
Jun. 2023

  Implementation of multicycle RICS-V CPU, introduction to pipelined CPU design.

EDUCATION

Novosibirsk State University
Novosibirsk, Russia

- *Master's degree in Computer Science*
2021 - 2023

  - **Thesis**: The tiered JIT compilation in Java Virtual Machine for Elbrus platform.

Novosibirsk State University
Novosibirsk, Russia

- *Bachelor's degree in Computer Science*
2017 - 2021

  - **Thesis**: Development of a computational module for the simulation of fast-neutron reactor core destruction.
  - **GPA**: 4.8/5.0, graduated with honors

PROGRAMMING SKILLS

- **Languages**: C++, C, Assembly Languages, Java, Python.
- **Technologies**: JVM internals, Compilers Design, CPU Architecture.
- **Tools**: GNU Debugger, Bash, Perf, Intel VTune Profiler.