Albert Gafiyatullin

AI Compiler Engineer

Email: albert.gafiyatullin@outlook.com
Github: a-gafiyatullin
LinkedIn: Albert G.

Summary

Software Engineer specializing in the development of programming language compilers and runtimes. Interested in system programming, compiler technologies, operating systems, computer architecture.

Experience

Samsung Research Russia — Moscow, Russia
- *AI Compiler Engineer, SOC SW Lab* — *Jul. 2023 - Present*

C++ | Compilers | Neural Networks | Optimizations

Development of the optimizing AI compiler for Samsung Exynos SoC NPU.

Unipro — Novosibirsk, Russia
- *JIT Compiler Engineer, Java Virtual Machine team* — *Mar. 2021 - Jun. 2023*

C++ | JVM | Assembly Language | Compilers | Garbage Collection

JVM Runtime and JIT Compiler development for Elbrus VLIW processor by MCST:

- Adapted the C2 compiler for tiered compilation, which improved average startup performance by 50% compared to non-tiered compilation;
- Designed and implemented a fast compiler named 'C0' for warmup compilation levels (instead of C1), taking into account the features of Elbrus VLIW CPU architecture. This resulted in a 25% improvement in average startup performance for machines with a small number of cores, compared to tiered compilation based on the adapted C2 compiler;
- Improved performance for certain string and XML tasks by up to 8% using intrinsics;
- Reduced runtime overhead by implementing platform-dependent improvements for implicit null checks.

Projects & Courses

- **COOL Compiler** — *Sep. 2021 - Mar. 2024*

C++ | LLVM | Garbage Collection | Compilers | ARM

Implementation of COOL compiler and runtime with LLVM:

- AArch64 and x86-64 as target architectures;
- Stop-The-World Mark-and-Sweep, Mark-and-Compact and Semispace Copying Garbage Collectors.

- **SOE.YCSCS1: Compilers** — *Oct. 2021*

C++ | MIPS | Compilers | Assembly Language

Implementation of COOL compiler for SPIM emulator.

- **ENGR85A: Digital Design** — *Apr. 2023*

SystemVerilog | Circuit Design

Combinational and sequential circuits design.

- **ENGR85B: Computer Architecture** — *Jun. 2023*

RISC-V | Computer Architecture | SystemVerilog | Embedded Systems | Circuit Design

Implementation of multicycle RICS-V CPU, introduction to pipelined CPU design.

Education

- **Novosibirsk State University** — Novosibirsk, Russia
  Master's degree in Computer Science — *2021 - 2023*
  - **Thesis**: The tiered JIT compilation in Java Virtual Machine for Elbrus platform.
- **Novosibirsk State University** — Novosibirsk, Russia
  Bachelor's degree in Computer Science — *2017 - 2021*
  - **Thesis**: Development of a computational module for the simulation of fast-neutron reactor core destruction.
  - **GPA**: 4.8/5.0, graduated with honors

Programming Skills

- **Languages**: C++, C, Assembly Languages, Python.
- **Technologies**: JVM internals, Compilers, Computer Architecture.