

Motivation

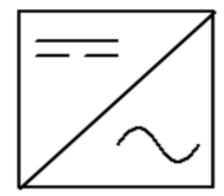
What is Inverter?

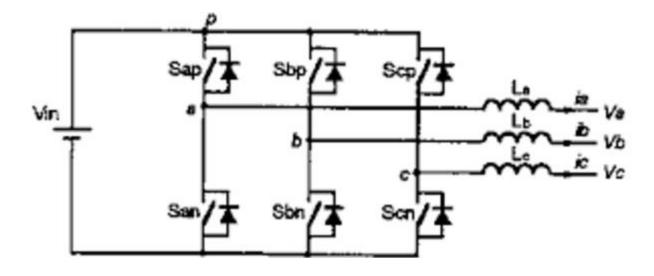
What are the applications of Inverters?

What does the inverter circuit look like?

What is the main disadvantage of it?

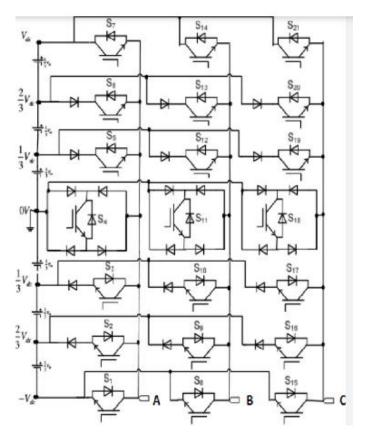
How to solve it?

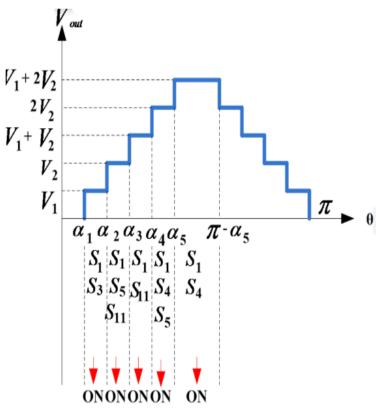




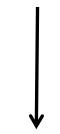
Problem Statement

A new kind of inverter topology was introduced to tackle the disadvantages of the traditional inverter.





However, the increased number of switches makes controlling the converter extremely difficult.

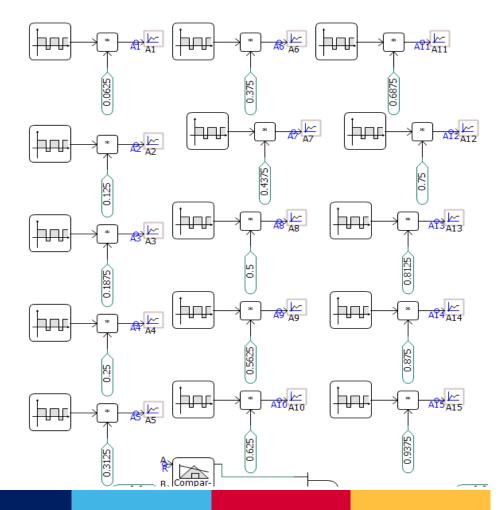


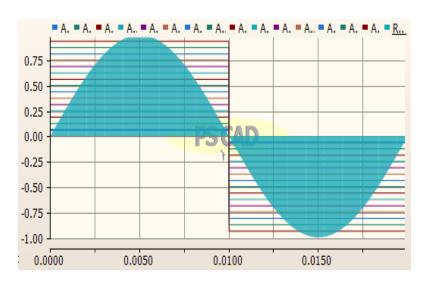
So, How do we control it?

Control Technique

Nearest Level Control:

We compare voltage reference and constant voltage levels to produce the pulses for gates.





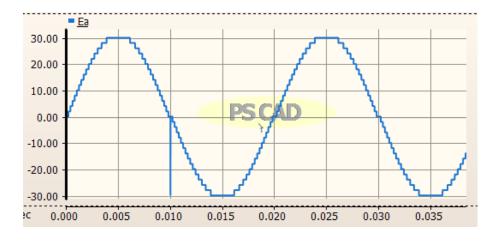
Overview of Implemented Control Method:

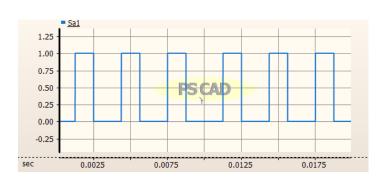
$$\begin{split} S_{a_{1}} &= A_{0}A_{4}\overline{A}_{8} + A_{0}A_{14} + \overline{A}_{0}\overline{A}_{4}A_{8} + \overline{A}_{0}\overline{A}_{14} \\ S_{b_{1}} &= A_{0}A_{1}\overline{A}_{2} + A_{0}A_{3}\overline{A}_{4} + A_{0}A_{5}\overline{A}_{6} + A_{0}A_{7}\overline{A}_{8} + A_{0}A_{9}\overline{A}_{10} + A_{0}A_{11}\overline{A}_{12} + A_{0}A_{13}\overline{A}_{14} \\ &\quad + \overline{A}_{0}\overline{A}_{1}A_{2} + \overline{A}_{0}\overline{A}_{3}A_{4} + \overline{A}_{0}\overline{A}_{5}A_{6} + \overline{A}_{0}\overline{A}_{7}A_{8} + \overline{A}_{0}\overline{A}_{9}A_{10} + \overline{A}_{0}\overline{A}_{11}A_{12} + \overline{A}_{0}\overline{A}_{13}A_{14} \\ S_{i} &= A_{0}A_{6} + \overline{A}_{0}\overline{A}_{6} \end{split}$$

$$\begin{split} H_1 &= A_0 A_6 + A_0 A_{10} + \overline{A}_0 \overline{A}_2 + \overline{A}_0 \overline{A}_6 A_{12} \\ H_2 &= A_0 A_2 + A_0 A_6 A_{12} + \overline{A}_0 A_6 + \overline{A}_0 \overline{A}_{10} \\ H_3 &= A_0 A_6 \overline{A}_{10} + \overline{A}_0 \overline{A}_2 A_6 + \overline{A}_0 \overline{A}_{12} \\ H_4 &= A_0 A_2 \overline{A}_6 + A_0 \overline{A}_{12} + \overline{A}_0 \overline{A}_6 A_{10} \\ \end{split} \qquad \begin{split} H_1' &= A_0 + \overline{A}_0 (A_1 + \overline{A}_2 A_3 + \overline{A}_4 A_5) \\ H_2' &= A_0 (\overline{A}_1 + A_2 \overline{A}_3 + A_4 \overline{A}_5) + \overline{A}_0 \\ H_3' &= \overline{A}_0 (\overline{A}_1 A_2 + \overline{A}_3 A_4 + \overline{A}_5) \\ H_4' &= A_0 (A_1 \overline{A}_2 + A_3 \overline{A}_4 + A_5) \end{split}$$

Results

The control method is tested under various loads. (inductive and resistive)





Voltage Output Under inductive load



Sa1

Sb1

Conclusion

- These new topologies of inverters increase the reliability of the converter, especially in power systems where reliability is crucial.
- This control method is implemented on PSCAD EMTDC and its functionality is proved.
- The number of logic gates is reduced in this simulation.
- This control method is tested under high inductive load.