EECE 3324

Summer 2022

Final Project

(Written by Dr. J Marpaung)

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Overall Guidelines of the Project:

1. You are only allowed to complete this assignment individually.

2. You are NOT allowed to work/collaborate/show your work with/to other people.

3. Your work must be your own. Should you be found guilty of using someone else's work (either fully or partly), an "F" will be assigned as your overall course grade for the semester.

4. You must submit all your files and report to Canvas.

5. Read, understand, and follow Northeastern Honor Code.

6. You are NOT allowed to receive help from anyone. Your course instructor and teaching assistants will not help you in building and debugging your design. Your work must be your own and it must be original. This is your final project, not your TA's final project.

7. All work must be done using Xilinx Vivado software. Failure to do this will result in a zero as the final grade of this assignment.

8. **The use of * (star symbol) in Verilog is strictly prohibited**. Using a * (star symbol) will result in a zero as the final grade of this assignment.

9. The deadline for this project can be found on Canvas. No extension will be given.

10. Failure to demonstrate your work to your course instructor or grader will result in a zero as the final grade of this assignment.

11. Do not procrastinate. Issues often happen to those who procrastinate.

1. Purpose

The purpose of this assignment is to build a fully working 5-stage CPU pipeline using ARM LEGV8 instruction set based on the MIPS CPU model provided to you on the previous assignments. Your CPU needs to run at a 20 MHz clock rate (a full clock cycle is 50 nsec. and a half cycle is 25 nsec.). The LEGV8 instruction reference card can be found at:

http://booksite.elsevier.com/9780128017333/content/Green%20Card.pdf

2. Instructions to Be Implemented

Implement the instructions found in Table 1 using the ARM LEGV8 data sheet. The new OPCODE can also be found in Table 1.

Instruction	Opcode	Opcode Size	Instruction Format
ADD	00101000000	11	R-format
ADDS	00101000001	11	R-format
AND	00101000010	11	R-format
ANDS	00101000011	11	R-format
EOR	00101000100	11	R-format
ENOR	00101000101	11	R-format
LSL	00101000110	11	R-format
LSR	00101000111	11	R-format
ORR	00101001000	11	R-format
SUB	00101001001	11	R-format
SUBS	00101001010	11	R-format
ADDI	1000100000	10	I-format
ADDIS	1000100001	10	I-format
ANDI	1000100010	10	I-format
ANDIS	1000100011	10	I-format
EORI	1000100100	10	I-format
ENORI	1000100101	10	I-format
ORRI	1000100110	10	I-format
SUBI	1000100111	10	I-format
SUBIS	1000101000	10	I-format
LDUR	11010000000	11	D-format
STUR	11010000001	11	D-format
MOVZ	110010101	9	IM-format
B	000011	6	B-format
CBZ	11110100	8	CB-format
CBNZ	11110101	8	CB-format
B.EQ	01110100	8	CB-format
B.NE	01110101	8	CB-format
B.LT (Signed)	01110110	8	CB-format
B.GE (Signed)	01110111	8	CB-format

Table 1. Instructions to be implemented and Opcode Table

Note:

All other op-codes should be treated as NOP's. The reset input should clear the PC (set the PC register to all 0's). It is acceptable for all the other registers to remain undefined until something is clocked into them. All branch instructions must be resolved in the Decode stage.

3. Deliveries:

You must turn in your final write-up directly to Canvas before you are interviewed by Dr. Marpaung/the grader for the course. The interview will be recorded. A set of time blocks will be given to you in advance. You need to upload your final-write up, your full Verilog code, and your full test bench file.

1. Draw the interconnections of pipeline block diagram for this assignment in great details. You can find an example of it in Assignment 5 - Figure 2.

2. You need to **elaborate**/explain your **CPU** extensively via writing. You need to tell your course instructor how your CPU works at each stage extensively. You will be judged based on the depth of your knowledge, and your course instructor will do so based on what is written on the report.

3. You need to have at least a total of **210** instructions on your test bench file **to test all instructions extensively**. You need to thoroughly explain your test bench file to a point where your course instructor can understand what you are doing with ease and make changes to further test your CPU. No points shall be awarded should your course instructor fail to understand your work/writing/test bench file. Your course instructor will also run his own test bench file against your CPU module and this test bench file will NOT be released prior to the due date, hence it is in your best interest to debug your module thoroughly. **Providing an incorrect test bench file in any ways will result in a Zero for the overall assignment.** Your work will also be judged by the complexity of your modified test bench file. The more complex and rigorous your test bench file in testing different scenarios, the more points you earn.

4. **Follow the final report template** at the end of this document. Points will be taken off for failure to follow the template.

5. You must type your final write-up using a **software**. Using any form of handwriting (either directly or scanned) is not accepted for your final write-up.

6. Make sure to label your top module for this project as cpu5arm.v and your testbench file as cpu5armtb.v.

7. Make sure you have the following ports for your cpu5arm.v:

Name of the port	Size of the port
ibus	32 bits
clk	1 bit
reset	1 bit
daddrbus	64 bits
databus	64 bits
iaddrbus	64 bits

8. A screenshot of your **Trace Receipt** that shows you have completed the Trace evaluation. Upload the screenshot as a separate file.

10. Any similarities found on your work against other student(s) will be thoroughly investigated by the **Office of Student Conduct and Conflict Resolution** (OSCCR).

11. The writing in this document can be interpreted in many different ways. **This document will be interpreted in the way your course instructor interprets it**. Should you encounter anything that is not clear about this document, and you would like this document to be updated please **email your course instructor as soon as possible**. Your course instructor may update this assignment at any time. Questions regarding this document must be directed to the course instructor before the due date. Comments such as "I don't fully understand the rules …" or "I thought you meant …" or "The TA said that …" will not be valid because it is your duty to ask questions to clarify things. Be active in asking questions.

Extra Note:

You may find some inconsistencies within the ARM LEGV8 data sheet. For example: see how the CondBranchAddr is calculated in relation to the CB instruction. Please feel free to contact the course instructor about any inconsistencies you may find in the ARM LEGV8 data sheet.

John Doe

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I. Brief Description of the assignment

The purpose of this assignment is …

II. Schematic

a. Detailed Pipeline Interconnections

b. Block Diagram Overview of your top module

III. Extensive Explanation about CPU

a. Stage 1 (or you can say Stage Instruction Fetch …)

…

b. Stage 2

…

c. Stage 3

…

d. Stage 4

…

e. Stage 5

…

III. Verilog – Code (with heavy comments) (Do NOT forget to attach your code on a separate file)

IV. Test Bench (Do NOT forget to attach your test bench on a separate file)

IV. New Acquired skills/knowledge

I have learned ….