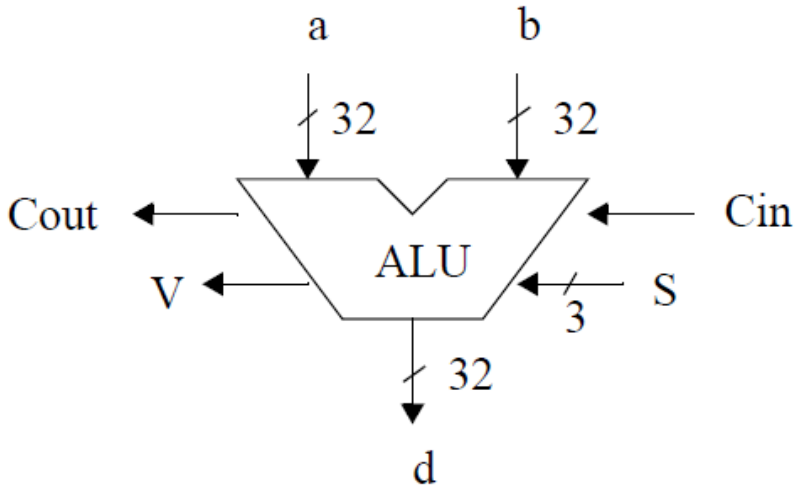
EECE 3324
Summer 2022
Assignment 1

Use the Xilinx Vivado synthesizer to design a 32-bit ALU with a worst case delay of 20 nano seconds. The ALU needs to have the following inputs and outputs.



All busses shall be numbered with 0 as the least significant bit. The inputs and outputs are defined as follows.

a, b are 32 bit input busses

d is the 32 bit output bus

Cin is the carry into bit 0

Cout is the carry out of bit 31

V is the overflow output

S is the 3-bit function select input

The d, Cout and V outputs should implement the correct function according to the following code for the S input.

S	ALU Function
000	a xor b
001	a xnor b
010	a + b
011	a - b
100	a or b
101	a nor b
110	a and b
111	X

The ALU function X means that we "don't care" what the ALU output is for these values of S. You will erroneously generate latches in your ALU if you leave the outputs undefined for these S inputs. Set the outputs to something, e.g. '0'; never leave them undefined.

A Verilog testbench file to provide inputs to your design will be provided by your course instructor. A similar file may be used to grade your design.

Your highest-level Verilog file needs to be named **alu32.v** to be compatible with the testbench file.

Create your own the testbench file that fully tests your design with at least 32 test scenarios covering the range of **S** from 000 to 110 as evenly as possible. You must provide comments on your testbench file so that others can follow your work. You will post your testbench to Assignment 1 Discussion on Canvas. Your classmates will review your testbench and provide feedback about it. Your classmates will also grade/rate your testbench file.

Please submit all your Verilog files including your new testbench file to Assignment 1 Link on Canvas. For your initial post to Assignment 1 Discussion, you only need to post your new testbench file.

Rules of Engagement:

1. You are only allowed to complete this assignment individually/as a group as assigned by the course instructor.
2. You are NOT allowed to work/collaborate/show your work to other people.
3. Your work must be your own. Should you be found guilty of using someone else's work (either full or partly), an "F" will be assigned as your overall course grade for the semester.
4. Read, understand, and follow NU Honor Code.
5. After you have completed your work, you must submit all your files to Canvas. Once you have submitted all your code to Canvas, you then need to be live interviewed by your TA/course instructor to verify all your work for this assignment using Xilinx Vivado. Failure to demonstrate your work to your grader or course instructor will result in a zero as the final grade of this assignment.
6. All work must be done using Xilinx Vivado software. Failure to do this will result in a zero as the final grade of this assignment.
7. **The use of * (star symbol) in Verilog is strictly prohibited**. Using a * (star symbol) will result in a zero as the final grade of this assignment.

Lab Submission:

You must show a live **working demo** to your course instructor or grader to receive a grade. The demo must be completed individually/as a group as instructed by the course instructor. Questions will be asked during the demo. Points will be deducted from your Lab grade should you fail to answer any questions. Comments such as "I cannot remember why I did that" will not help you. Come prepared.

Upload all the Verilog files used and the improved test bench file to Canvas. Make sure that your Verilog files (including the test bench file) are heavily commented as it is part of the grading. Your work will also be judged by the complexity of your modified test bench file. The more complex and rigorous your test bench file in testing different scenarios, the more points you earn.

Do not zip all your files together.

An automatic zero will be assigned for anyone who fails to show a live working demo to your course instructor or grader.