EECE 3324
Summer 2022
Assignment 5

For this assignment, you will design a simplified 3-stage 32-bit pipelined CPU. Figure 1 shows an overview design of how the **CPU should look like**. Figure 1 shows an overview design of how the **CPU should look like**. Figure 1 is used to give you a visual/an overall idea of how the design should look like without all the little details. **Your job is to fill in all the small details**.

At this point in time, you must remember the function of the following signals from the previous Assignments: Aselect, Bselect, and Dselect. Remember that **Dselect** signal is being used to write the result of an instruction back to a register, which means that you must delay Dselect signal so that the final value in dbus can be written back into the correct register (as pointed by Dselect) at the correct time.

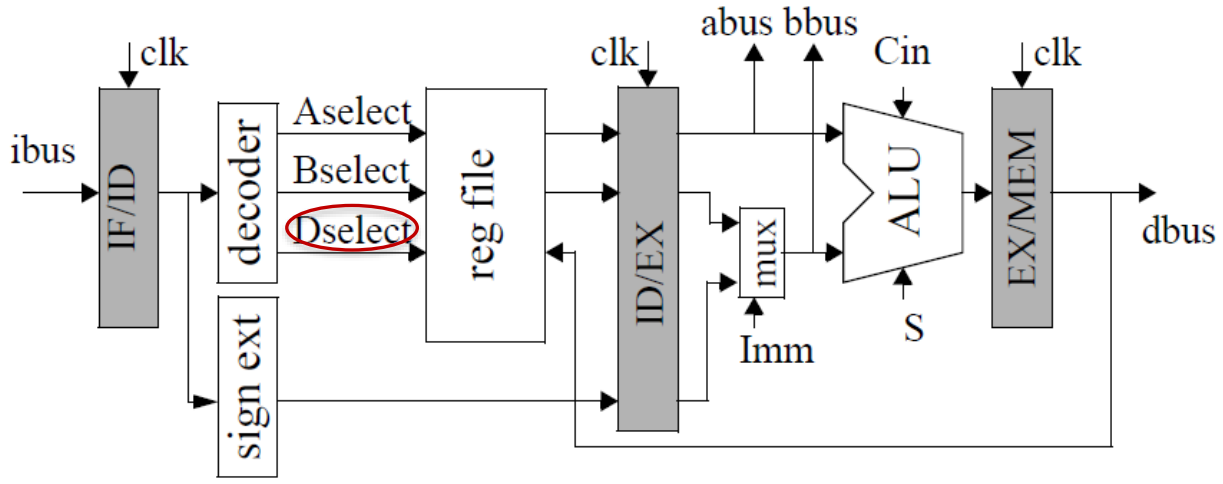

Figure 1. Overview of Pipeline Block Diagram

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Figure 2 shows ALL the interconnections that you need to make.

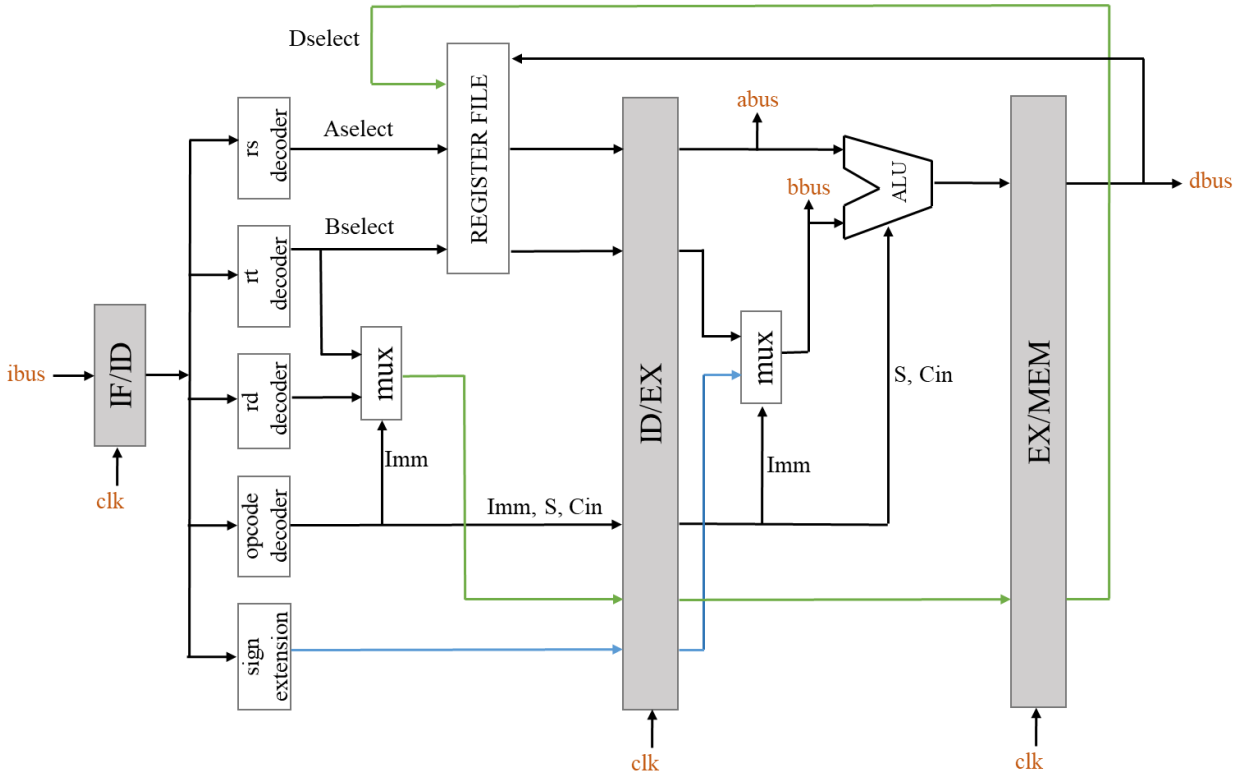

Figure 2. Interconnections of Pipeline Block Diagram

Starting on Assignment 6, you are expected to draw and derive your interconnections from the overview design.

Design decision: Now, you need to make a judgement call on how to proceed. You can use your controller.v from Assignment 4 as a starting point or you can start from scratch. You are the designer, not the course instructor.

TIPS:

1. The sign extension logic extends the lower order 16-bits of the instruction to 32 bits

   https://en.wikipedia.org/wiki/Sign_extension

2. Add a MUX on the ALU B-input such that the sign extension output is selected for I format.

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Each instruction will stay on the ibus for one clock cycle. It is acceptable for all the registers in the register file to remain undefined until something is clocked into them.

To facilitate testing of your design, the IF/ID register inputs will be connected to the instruction bus which will be made available as an external terminal. Your design should have the terminals shown in Figure 2.

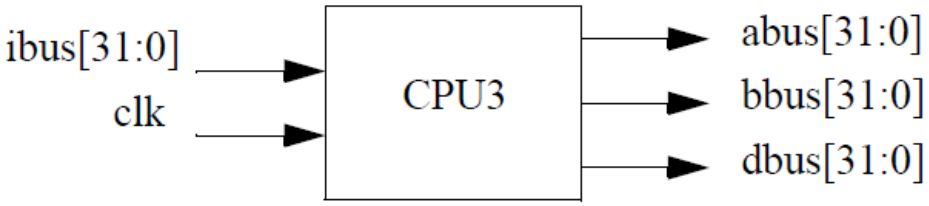

Figure 3. CPU Terminals

Before you start designing the hardware as shown in Figure 2 using Verilog, fill out the table on the next page and find the value of the wires and output ports at each clock cycle. The purpose of filling out the table is to check your basic understanding of the hardware. If you believe the output is undefined, then use Xs to denote it, for example 32'hxxxxxxxx.

You must use a software such as Microsoft Word or Microsoft Excel to fill out the table. Using your own handwriting will not earn you any points.

Submit this table as part of your final submission to Canvas.

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Clock Status	ibus	Asel	Bsel	abus	bbus	Imm	S	Cin	Dsel	dbus
clk = 0	32’b00000000000000000110100000000010									
↑	32’b00000000000000000110100000000010									
clk = 1	32’b00000000000000000110100000000010									
↓	32’b00000000000000000110100000000010									
clk = 0	32'b00001100000000010000000000000000									
↑	32'b00001100000000010000000000000000									
clk = 1	32'b00001100000000010000000000000000									
↓	32'b00001100000000010000000000000000									
clk = 0	32'b00001100000000001111111111111111									
↑	32'b00001100000000001111111111111111									
clk = 1	32'b00001100000000001111111111111111									
↓	32'b00001100000000001111111111111111									
clk = 0	32'b00001100001111101010111111000000									
↑	32'b00001100001111101010111111000000									
clk = 1	32'b00001100001111101010111111000000									
↓	32'b00001100001111101010111111000000									
clk = 0	32'b00000000000000000000000000000010									

Table 1. CPU3 Table

A Verilog testbench file to provide inputs to your design will be provided by your course instructor. A similar file will be used to grade your design. Your highest-level Verilog file needs to be named **cpu3.v** to be compatible with the testbench file.

Create your own the testbench file that fully tests your design with at least 32 test scenarios. You must provide comments on your testbench file so that others can follow your work. You will post your testbench to Assignment 5 Discussion on Canvas. Your classmates will review your testbench and provide feedback about it. Your classmates will also grade/rate your testbench file.

Please submit all your Verilog files including your new testbench file to Assignment 5 Link on Canvas. For your initial post to Assignment 5 Discussion, you only need to post your new testbench file.

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Rules of Engagement:

1. You are only allowed to complete this assignment individually/as a group as assigned by the course instructor.
2. You are NOT allowed to work/collaborate/show your work to other people.
3. Your work must be your own. Should you be found guilty of using someone else's work (either full or partly), an "F" will be assigned as your overall course grade for the semester.
4. Read, understand, and follow NU Honor Code.
5. After you have completed your work, you must submit all your files to Canvas. Once you have submitted all your code to Canvas, you then need to be live interviewed by your TA/course instructor to verify all your work for this assignment using Xilinx Vivado. Failure to demonstrate your work to your grader or course instructor will result in a zero as the final grade of this assignment.
6. All work must be done using Xilinx Vivado software. Failure to do this will result in a zero as the final grade of this assignment.
7. **The use of * (star symbol) in Verilog is strictly prohibited**. Using a * (star symbol) will result in a zero as the final grade of this assignment.

Lab Submission:

You must show a live **working demo** to your course instructor or grader to receive a grade. The demo must be completed individually/as a group as instructed by the course instructor. Questions will be asked during the demo. Points will be deducted from your Lab grade should you fail to answer any questions. Comments such as "I cannot remember why I did that" will not help you. Come prepared.

Upload all the Verilog files used and the improved test bench file to Canvas. Make sure that your Verilog files (including the test bench file) are heavily commented as it is part of the grading. Your work will also be judged by the complexity of your modified test bench file. The more complex and rigorous your test bench file in testing different scenarios, the more points you earn.

Do not zip all your files together.

An automatic zero will be assigned for anyone who fails to show a live working demo to your course instructor or grader.

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