Abdul Muizz ECSE 6680 - Advanced VLSI Design

FIR Filter Design and Implementation

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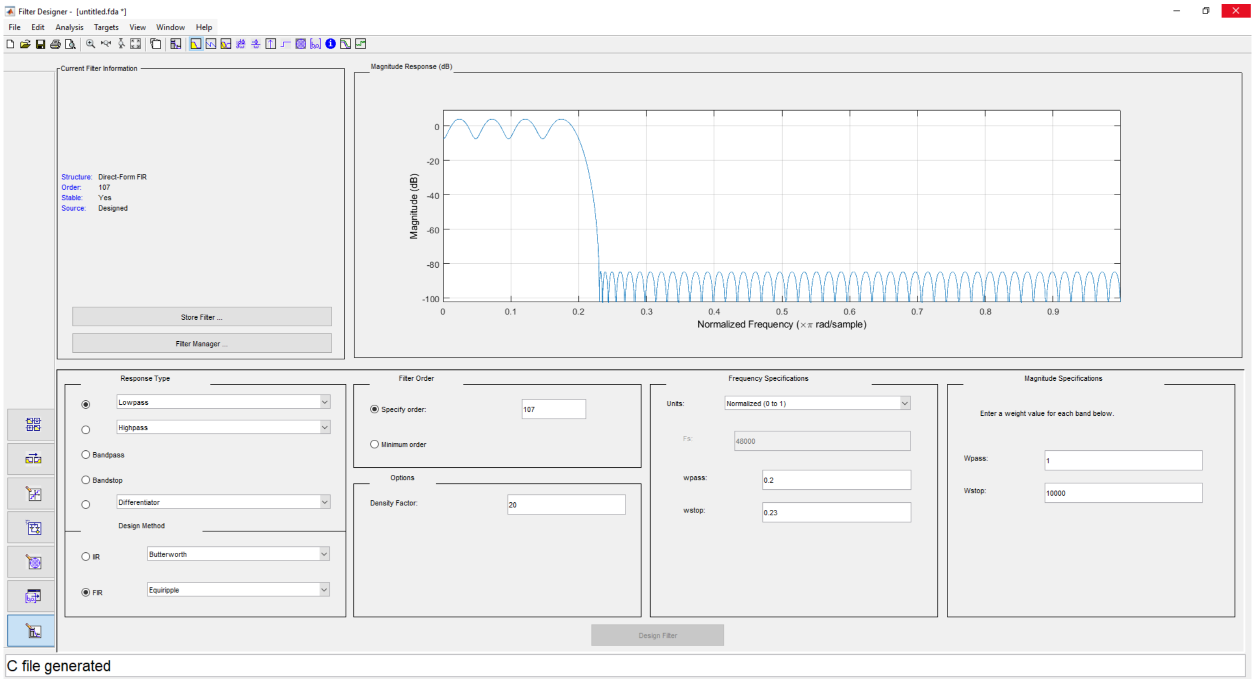
1. Project Outline

The objective of this course project is to design and implement a low-pass FIR filter. This filter should have at least 100 taps, a transition region of 0.2pi-0.23pi rad/sample, and a stopband attenuation of at least 80 dB. To achieve performance gains, filter coefficients can be quantized, and the hardware implementations can include pipelining and/or parallelization.

2. MATLAB FIR Filter Design, Quantization, Frequency Response

i. FIR Filter Design

MATLAB's Filter Designer was used to design an unquantized 108-tap low-pass FIR Filter. I chose 108-tap because it exceeds the 100-tap requirement, while still divisible by two and three. This will be important when we look to add two, or three levels of parallelization.



Structure: Direct-Form FIR
Order: 107
Stable: Yes
Source: Designed

● Lowpass
○ Highpass
○ Bandpass
○ Bandstop
○ Differentiator

○ IIR Butterworth
● FIR Equiripple

● Specify order: 107
○ Minimum order

Density Factor: 20

Units: Normalized (0 to 1)
Fs: 48000
wpass: 0.2
wstop: 0.23

Enter a weight value for each band below.
Wpass: 1
Wstop: 10000

C file generated

Figure 1: MATLAB Filter Designer

ii. Unquantized (Original) vs. Quantized

To determine the Filter's frequency response, we used another MATLAB script that allows us to view the filter's passband. Both an unquantized (original) and quantized filter were used in this test. My quantization method involved converting the filter taps (originally double-precision floats) into a signed 24-bit representation. I also challenged the issue of arithmetic overflow by properly scaling inputs and using intermediate registers during MAC stages in the architecture. The figure below shows that the stopband attenuation is at least 80 dB, and that the transition region occurs at around 2.23pi rad/sample. The overlap between the Quantized and unquantized response is very large, indicating near identical performance.

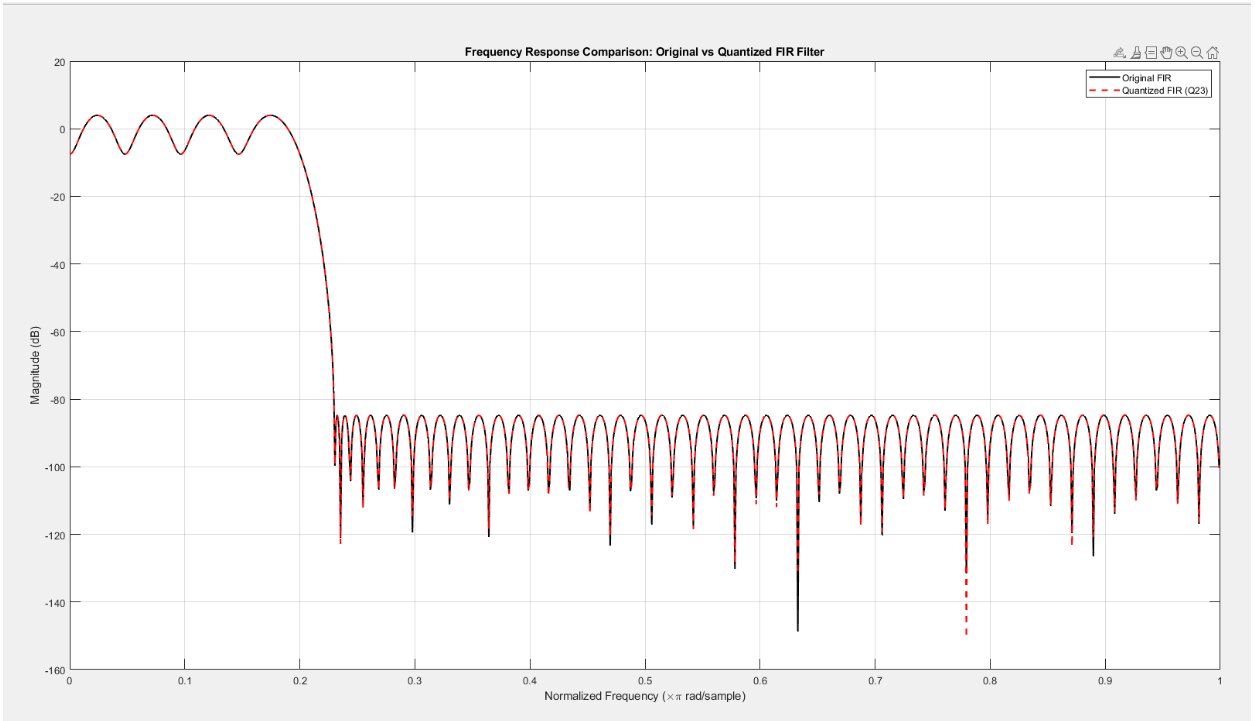


Figure 2: Unquantized (original) vs. Quantized

iii. Benchmark Input Signal

For simulation setup, and to determine the FIR filter’s effectiveness, I passed in a sine wave (1 kHz) containing noise. This signal was generated through MATLAB and saved as a .data or .txt file. This allows us to determine the FIR filter’s ability to remove noise and preserve key signal shaping. This sine wave will be simplified to 16-bit integer inputs.

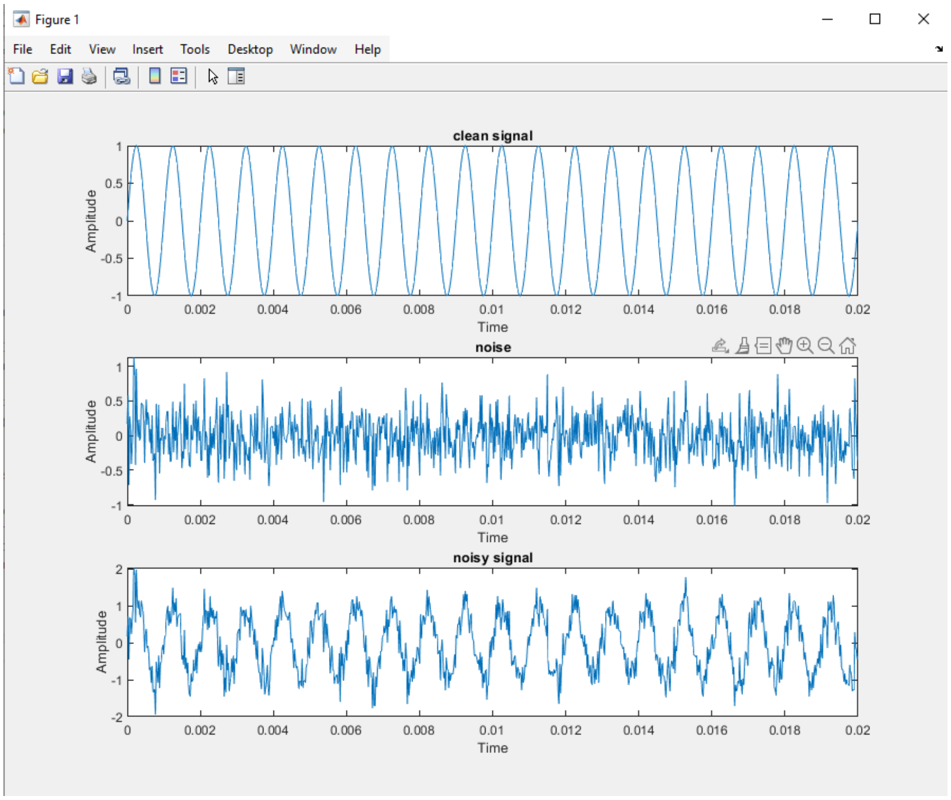


Figure 3: Noisy Sine Wave Input Generation

3. FIR Hardware Architecture

i. Baseline Design

Four hardware implementations for this lab were created. This includes a pipelined variant, N=2 level parallelization, N=3 level parallelization, and pipelined N=3 level parallelization. The first image below highlights the baseline requirement for implementing an FIR filter. This approach uses Multiply-Accumulate (MAC) blocks to delay sample progression. This architecture has a very long critical path, which means there is significant room for improvement.

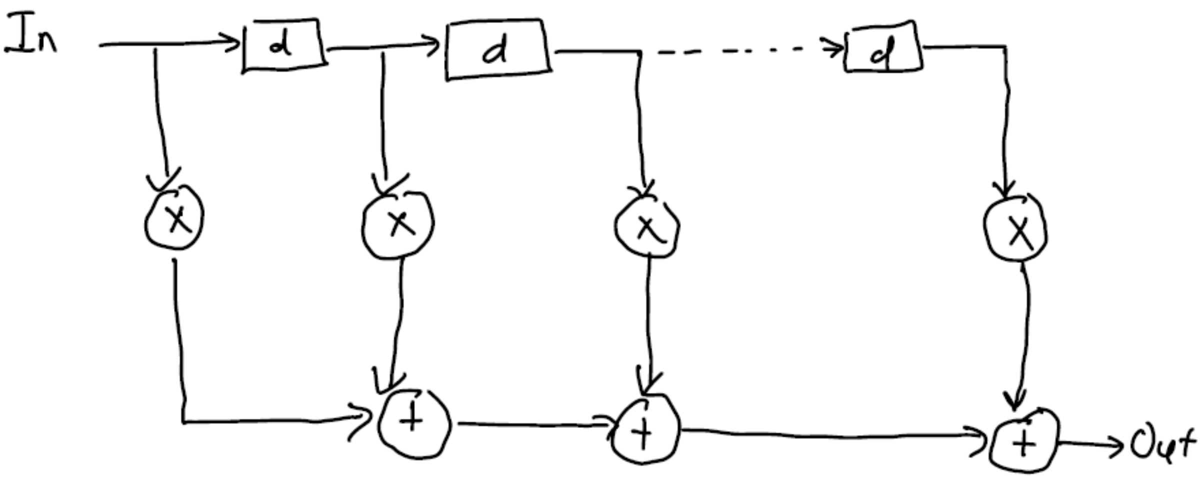


Figure 4: Baseline Implementation

ii. Fully Pipeline Design

The next image below illustrates the ideal full pipelining. Using vertical (MAC) and horizontal (Adder) pipelining limits the critical path to a single multiplier or adder. This allows for throughput to be drastically increased, compared to waiting for one pass at a time.

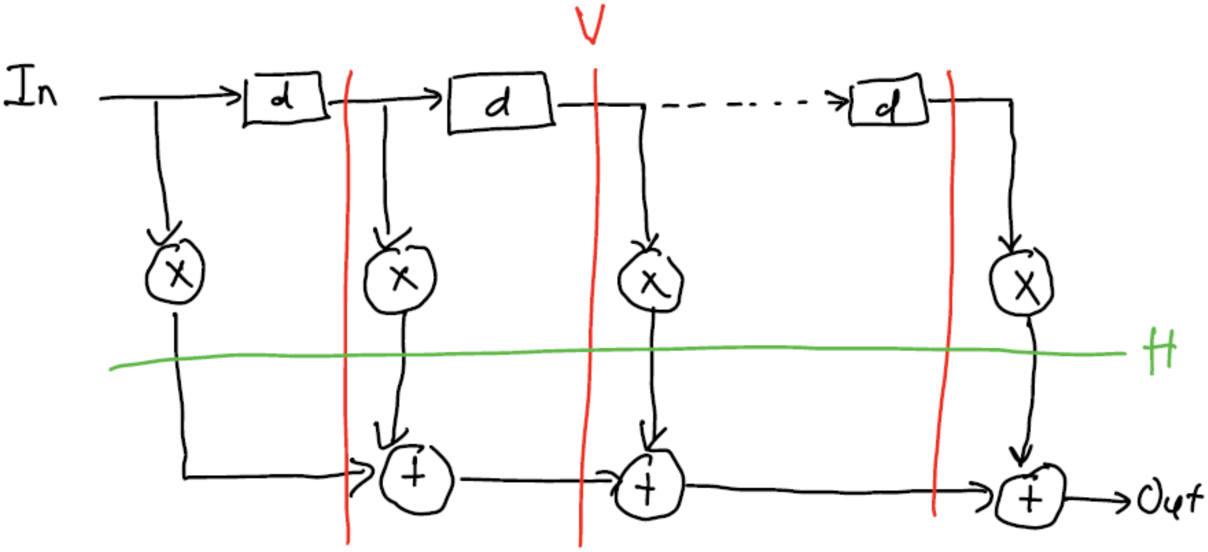


Figure 5: Fully Pipelined Implementation

iii. Simple Pipeline Design

Implementation issues with vertical pipelining (affecting output smoothing clarity) led to a simplified pipelining variation, specifically using horizontal pipelining only. While this still improves the performance, the critical path is still high (up to a “tap count” number of adders.

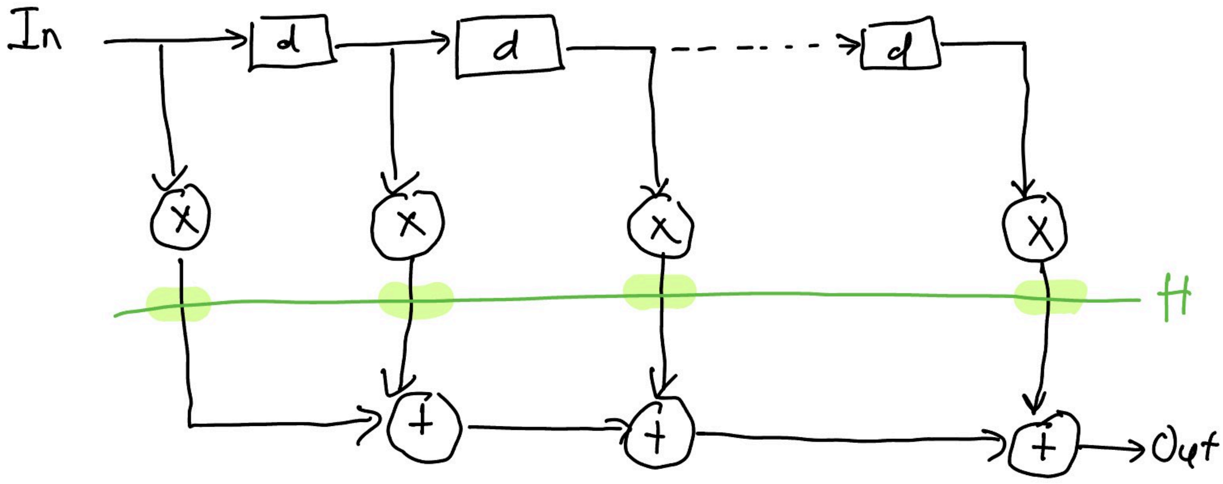


Figure 6: Horizontal Pipeline Implementation

iv. Parallelization (N=2 and N=3)

Parallelization allows for the ability to split the workload across multiple lines, allowing for a multi-faceted hardware approach for this filter. The two images below show an N=2 and N=3 parallelization implementation. The 108 taps (coefficients) were split across each line through a process known as polyphase decomposition.

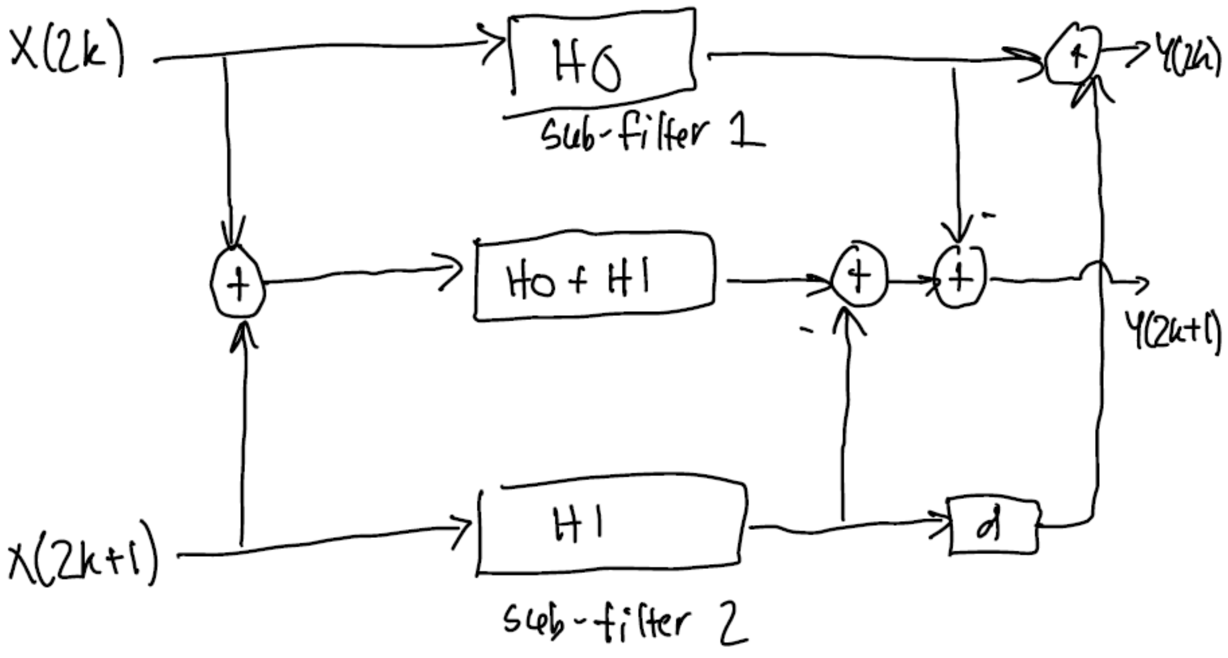


Figure 7: Parallelization (N=2)

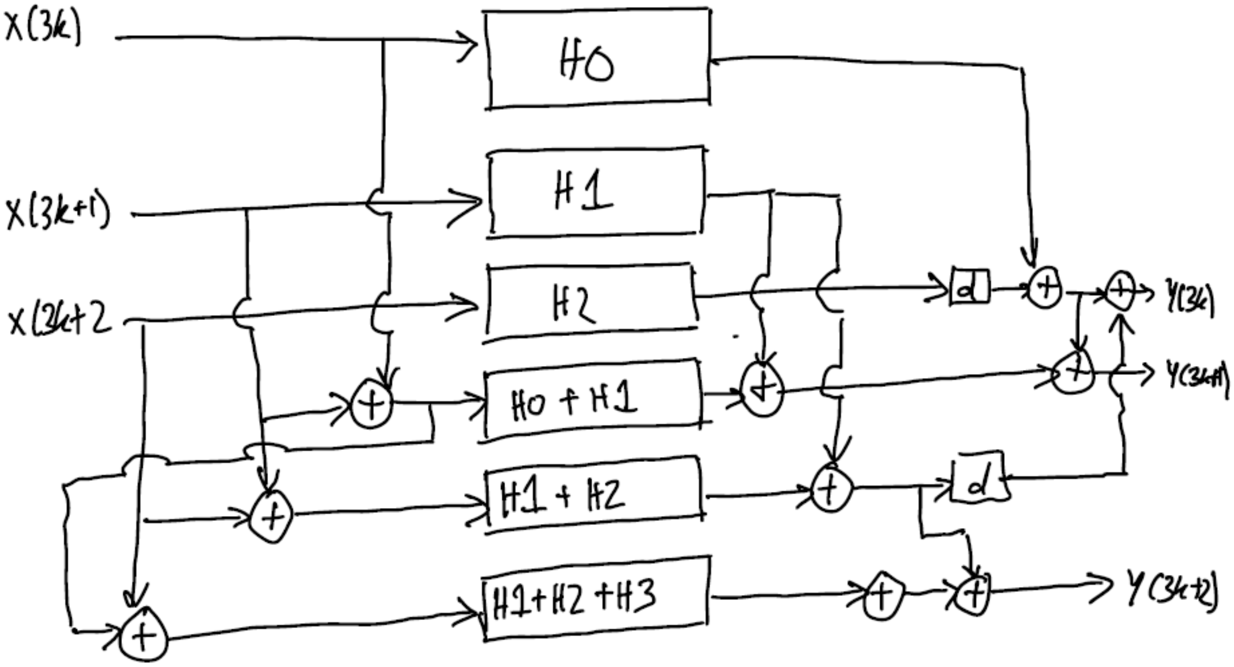


Figure 8: Parallelization (N=3)

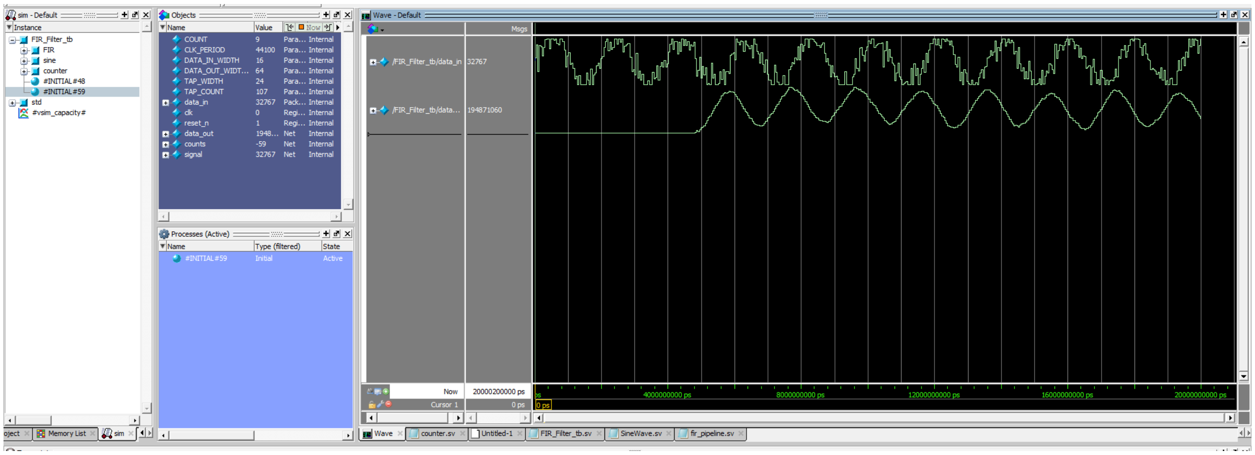
v. Pipelining and Parallelization (N=3)

Combining pipelining and L=3 parallel allows for even higher performance. Implementing pipelining into three subfilters allows for increased pipelining throughput across a split workload.

4. HDL Code Structure

The SystemVerilog structure for this project (for each of the 4 filter implementations) includes the filter design file (and sometimes an adjacent top.sv), a testbench file (ran for simulation), a sine wave input signal file coupled with binary signal data (generated from the noisy sine wave MATLAB file), and a counter file to continually increment and pass time. The measured values were input and output data, showing the original noisy sine wave input compared to a smoother, refined output. The results for each of the 4 implementations can be seen below. For the examples containing parallelization, the input and output are split into multiple groups, based on the parallelization level.

i. Pipelining



Name	Value		
COUNT	9	Para...	Internal
CLK_PERIOD	44100	Para...	Internal
DATA_IN_WIDTH	16	Para...	Internal
DATA_OUT_WIDT...	64	Para...	Internal
TAP_WIDTH	24	Para...	Internal
TAP_COUNT	107	Para...	Internal
data_in	32767	Pack...	Internal
clk	0	Regi...	Internal
reset_n	1	Regi...	Internal
data_out	1948...	Net	Internal
counts	-59	Net	Internal
signal	32767	Net	Internal

Name	Type (filtered)	State
#INITIAL#59	Initial	Active

/FIR_Filter_tb/data_in 32767

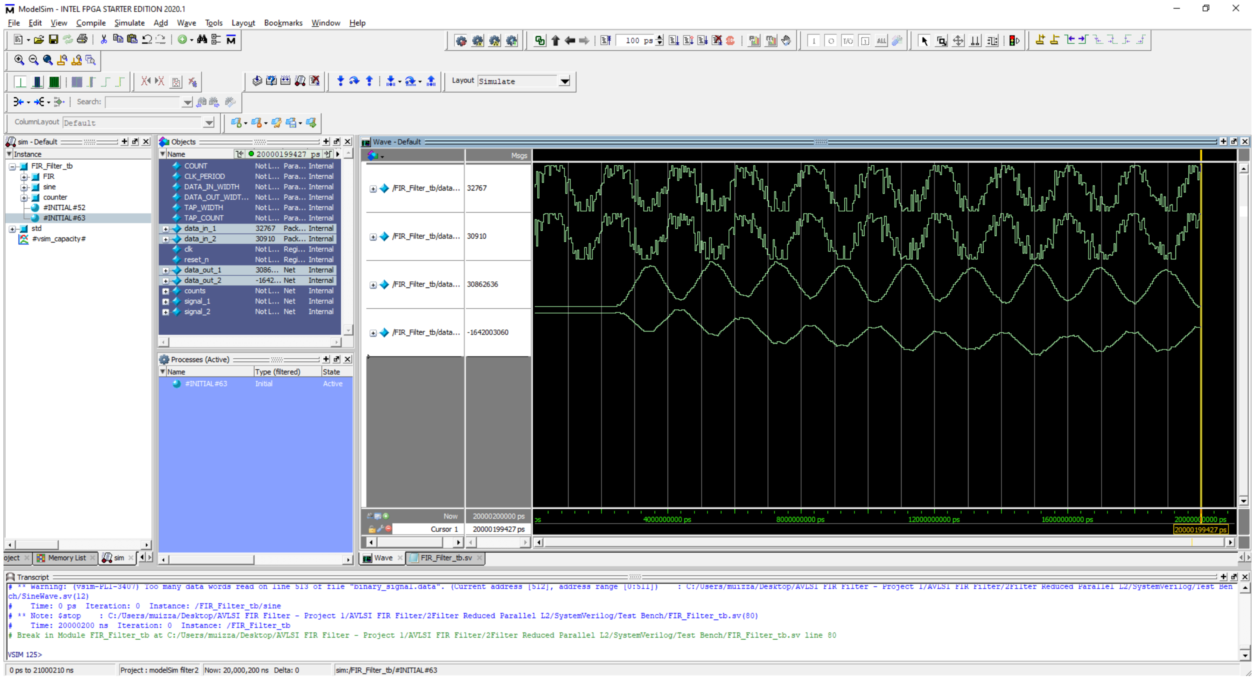
/FIR_Filter_tb/data... 194871060

Now 20000200000 ps

Cursor 1 0 ps

Figure 9: Pipeline ModelSim

ii. Parallelization, N=2



Name	Value	Kind	Mode
COUNT	Not L...	Para...	Internal
CLK_PERIOD	Not L...	Para...	Internal
DATA_IN_WIDTH	Not L...	Para...	Internal
DATA_OUT_WIDT...	Not L...	Para...	Internal
TAP_WIDTH	Not L...	Para...	Internal
TAP_COUNT	Not L...	Para...	Internal
data_in_1	32767	Pack...	Internal
data_in_2	30910	Pack...	Internal
clk	Not L...	Regi...	Internal
reset_n	Not L...	Regi...	Internal
data_out_1	3086...	Net	Internal
data_out_2	-1642...	Net	Internal
counts	Not L...	Net	Internal
signal_1	Not L...	Net	Internal
signal_2	Not L...	Net	Internal

```
/FIR_Filter_tb/data...   32767
/FIR_Filter_tb/data...   30910
/FIR_Filter_tb/data...   30862636
/FIR_Filter_tb/data...   -1642003060

Now       20000200000 ps
Cursor 1  20000199427 ps
```

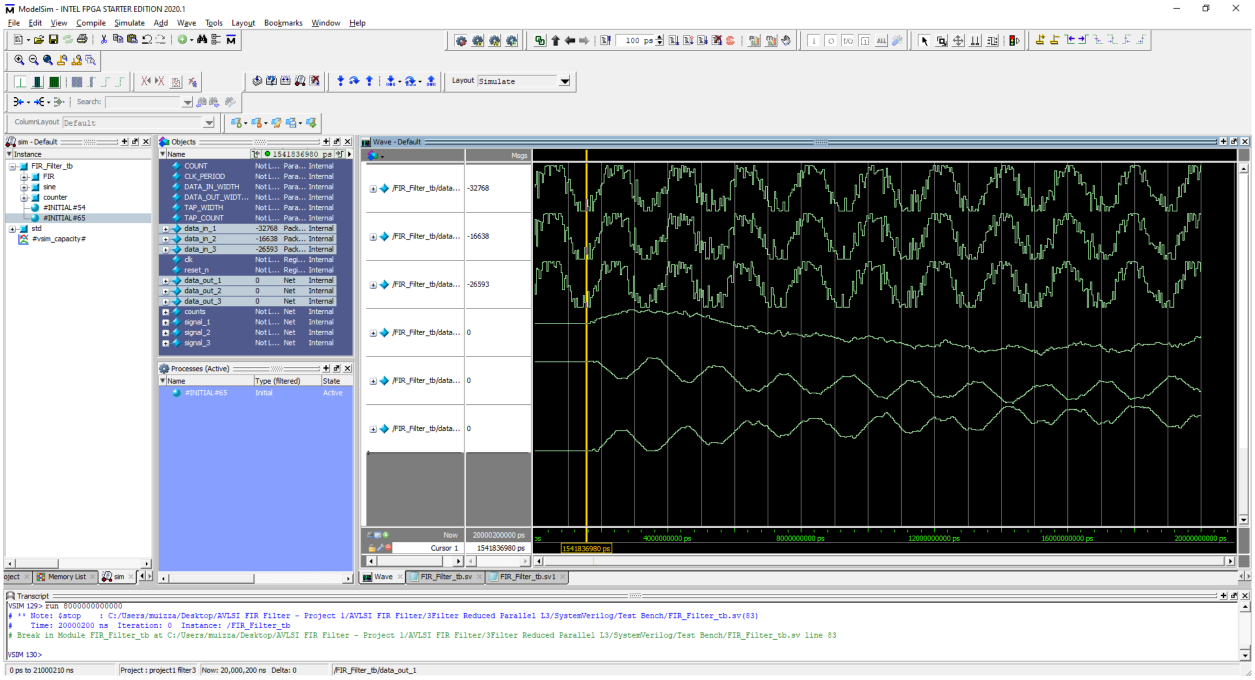
```
# ** Warning: (vsim-PLI-3407) Too many data words read on line 513 of file "binary_signal.data". (Current address [512], address range [0:511])    : C:/Users/muizza/Desktop/AVLSI FIR Filter - Project 1/AVLSI FIR Filter/2Filter Reduced Parallel L2/SystemVerilog/Test Bench/SineWave.sv(12)
#    Time: 0 ps  Iteration: 0  Instance: /FIR_Filter_tb/sine
# ** Note: $stop    : C:/Users/muizza/Desktop/AVLSI FIR Filter - Project 1/AVLSI FIR Filter/2Filter Reduced Parallel L2/SystemVerilog/Test Bench/FIR_Filter_tb.sv(80)
#    Time: 20000200 ns  Iteration: 0  Instance: /FIR_Filter_tb
# Break in Module FIR_Filter_tb at C:/Users/muizza/Desktop/AVLSI FIR Filter - Project 1/AVLSI FIR Filter/2Filter Reduced Parallel L2/SystemVerilog/Test Bench/FIR_Filter_tb.sv line 80

VSIM 125>
```

```
0 ps to 21000210 ns    Project : modelSim filter2    Now: 20,000,200 ns  Delta: 0    sim:/FIR_Filter_tb/#INITIAL#63
```

Figure 10: Parallelization (N=2) ModelSim

iii. Parallelization, N=3



Name	Value	Kind	Mode
COUNT	Not L...	Para...	Internal
CLK_PERIOD	Not L...	Para...	Internal
DATA_IN_WIDTH	Not L...	Para...	Internal
DATA_OUT_WIDT...	Not L...	Para...	Internal
TAP_WIDTH	Not L...	Para...	Internal
TAP_COUNT	Not L...	Para...	Internal
data_in_1	-32768	Pack...	Internal
data_in_2	-16638	Pack...	Internal
data_in_3	-26593	Pack...	Internal
clk	Not L...	Regi...	Internal
reset_n	Not L...	Regi...	Internal
data_out_1	0	Net	Internal
data_out_2	0	Net	Internal
data_out_3	0	Net	Internal
counts	Not L...	Net	Internal
signal_1	Not L...	Net	Internal
signal_2	Not L...	Net	Internal
signal_3	Not L...	Net	Internal

```
/FIR_Filter_tb/data...   -32768
/FIR_Filter_tb/data...   -16638
/FIR_Filter_tb/data...   -26593
/FIR_Filter_tb/data...   0
/FIR_Filter_tb/data...   0
/FIR_Filter_tb/data...   0

Now       20000200000 ps
Cursor 1  1541836980 ps
```

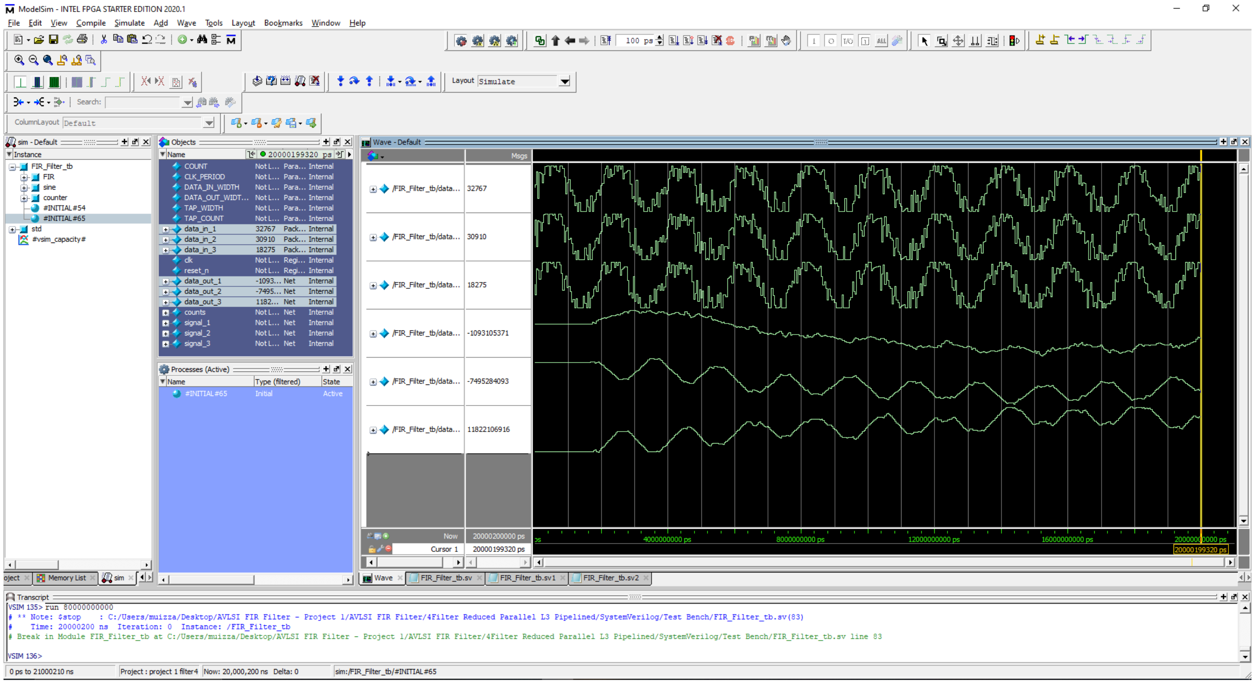
```
VSIM 129> run 8000000000000
# ** Note: $stop    : C:/Users/muizza/Desktop/AVLSI FIR Filter - Project 1/AVLSI FIR Filter/3Filter Reduced Parallel L3/SystemVerilog/Test Bench/FIR_Filter_tb.sv(83)
#    Time: 20000200 ns  Iteration: 0  Instance: /FIR_Filter_tb
# Break in Module FIR_Filter_tb at C:/Users/muizza/Desktop/AVLSI FIR Filter - Project 1/AVLSI FIR Filter/3Filter Reduced Parallel L3/SystemVerilog/Test Bench/FIR_Filter_tb.sv line 83

VSIM 130>
```

```
0 ps to 21000210 ns    Project : project1 filter3    Now: 20,000,200 ns  Delta: 0    /FIR_Filter_tb/data_out_1
```

Figure 11: Parallelization (N=3) ModelSim

iv. Pipelining & Parallelization, N=3



Name	● 20000199320 ps		
COUNT	Not L...	Para...	Internal
CLK_PERIOD	Not L...	Para...	Internal
DATA_IN_WIDTH	Not L...	Para...	Internal
DATA_OUT_WIDT...	Not L...	Para...	Internal
TAP_WIDTH	Not L...	Para...	Internal
TAP_COUNT	Not L...	Para...	Internal
data_in_1	32767	Pack...	Internal
data_in_2	30910	Pack...	Internal
data_in_3	18275	Pack...	Internal
clk	Not L...	Regi...	Internal
reset_n	Not L...	Regi...	Internal
data_out_1	-1093...	Net	Internal
data_out_2	-7495...	Net	Internal
data_out_3	1182...	Net	Internal
counts	Not L...	Net	Internal
signal_1	Not L...	Net	Internal
signal_2	Not L...	Net	Internal
signal_3	Not L...	Net	Internal

Name	Type (filtered)	State
#INITIAL#65	Initial	Active

	Msgs
/FIR_Filter_tb/data...	32767
/FIR_Filter_tb/data...	30910
/FIR_Filter_tb/data...	18275
/FIR_Filter_tb/data...	-1093105371
/FIR_Filter_tb/data...	-7495284093
/FIR_Filter_tb/data...	11822106916
Now	20000200000 ps
Cursor 1	20000199320 ps

```
VSIM 135> run 80000000000
# ** Note: $stop    : C:/Users/muizza/Desktop/AVLSI FIR Filter - Project 1/AVLSI FIR Filter/4Filter Reduced Parallel L3 Pipelined/SystemVerilog/Test Bench/FIR_Filter_tb.sv(83)
#    Time: 20000200 ns  Iteration: 0  Instance: /FIR_Filter_tb
# Break in Module FIR_Filter_tb at C:/Users/muizza/Desktop/AVLSI FIR Filter - Project 1/AVLSI FIR Filter/4Filter Reduced Parallel L3 Pipelined/SystemVerilog/Test Bench/FIR_Filter_tb.sv line 83

VSIM 136>
```

```
0 ps to 21000210 ns    Project : project 1 filter4   Now: 20,000,200 ns  Delta: 0    sim:/FIR_Filter_tb/#INITIAL#65
```

Figure 12: Pipelining & Parallelization (N=3) ModelSim

5. Hardware Implementation Results

Hardware Implementation Results were carried out through AMD's Vivado software. The implementations were all run on device ID "xc7k70tfbv676-1", which was chosen for its higher port/pin count. The implementations were analyzed for area (cell count), power consumption, and timing (speed and performance). Screenshots of in-depth results can be found below and in the "Analysis" subfolder under each implementation folder (1Filter Pipelined, 2Filter Reduced Parallel L2, 3Filter Reduced Parallel L3, 4Filter Reduced Parallel L3 Pipelined). At the end, there is a table summarizing all of the data. Note that for the Vivado simulations, the architectures were synthesized with a clock period of 21276 nanoseconds (47 kHz).

i. Pipelining Hardware Implementation Results

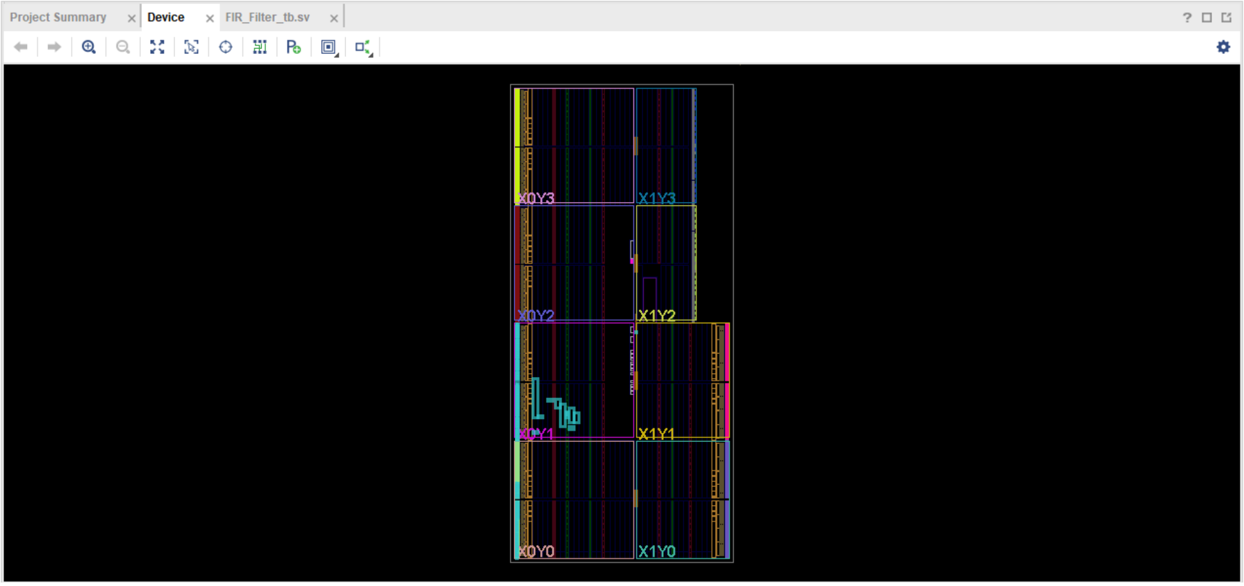
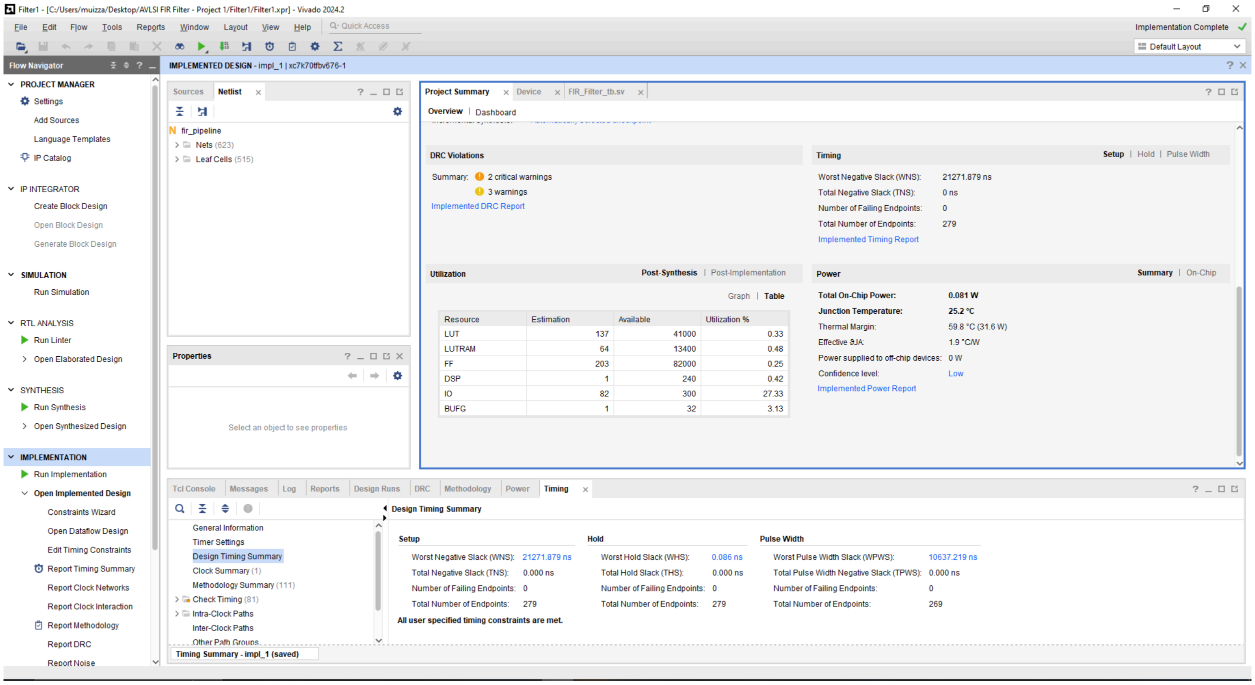


Figure 13: Pipelining Device Layout



IMPLEMENTED DESIGN - impl_1 | xc7k70tfbv676-1

fir_pipeline
Nets (623)
Leaf Cells (515)

Select an object to see properties

DRC Violations

Summary: 2 critical warnings
3 warnings
Implemented DRC Report

Timing — Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	21271.879 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	279

Implemented Timing Report

Utilization — Post-Synthesis | Post-Implementation

Graph | Table

Resource	Estimation	Available	Utilization %
LUT	137	41000	0.33
LUTRAM	64	13400	0.48
FF	203	82000	0.25
DSP	1	240	0.42
IO	82	300	27.33
BUFG	1	32	3.13

Power — Summary | On-Chip

Total On-Chip Power:	**0.081 W**
Junction Temperature:	**25.2 °C**
Thermal Margin:	59.8 °C (31.6 W)
Effective ϑJA:	1.9 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Methodology Summary (111)
Check Timing (81)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups

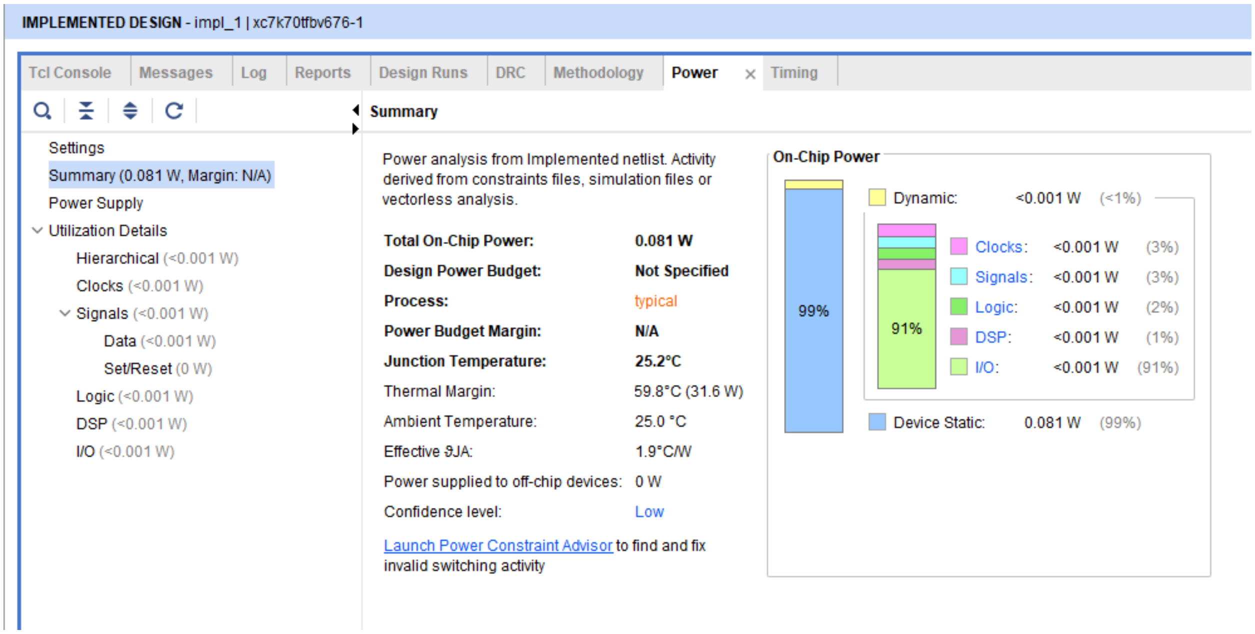
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	21271.879 ns	Worst Hold Slack (WHS):	0.086 ns	Worst Pulse Width Slack (WPWS):	10637.219 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	279	Total Number of Endpoints:	279	Total Number of Endpoints:	269

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

Figure 14: Pipelining Cell Count & Summary



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

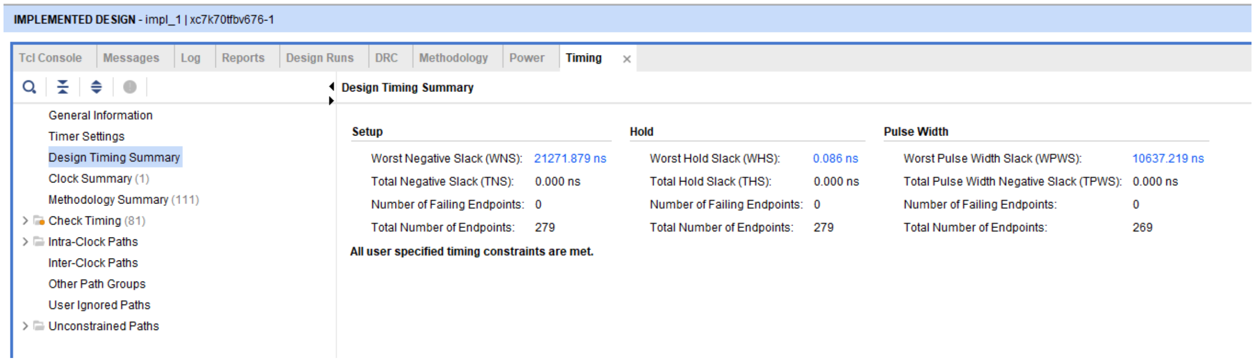
Total On-Chip Power:	**0.081 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	<0.001 W	(<1%)
Clocks:	<0.001 W	(3%)
Signals:	<0.001 W	(3%)
Logic:	<0.001 W	(2%)
DSP:	<0.001 W	(1%)
I/O:	<0.001 W	(91%)
Device Static:	0.081 W	(99%)

Figure 15: Pipelining Power



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	21271.879 ns	Worst Hold Slack (WHS):	0.086 ns	Worst Pulse Width Slack (WPWS):	10637.219 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	279	Total Number of Endpoints:	279	Total Number of Endpoints:	269

All user specified timing constraints are met.

Figure 16: Pipelining Timing

ii. Parallelization (N=2) Hardware Implementation Results

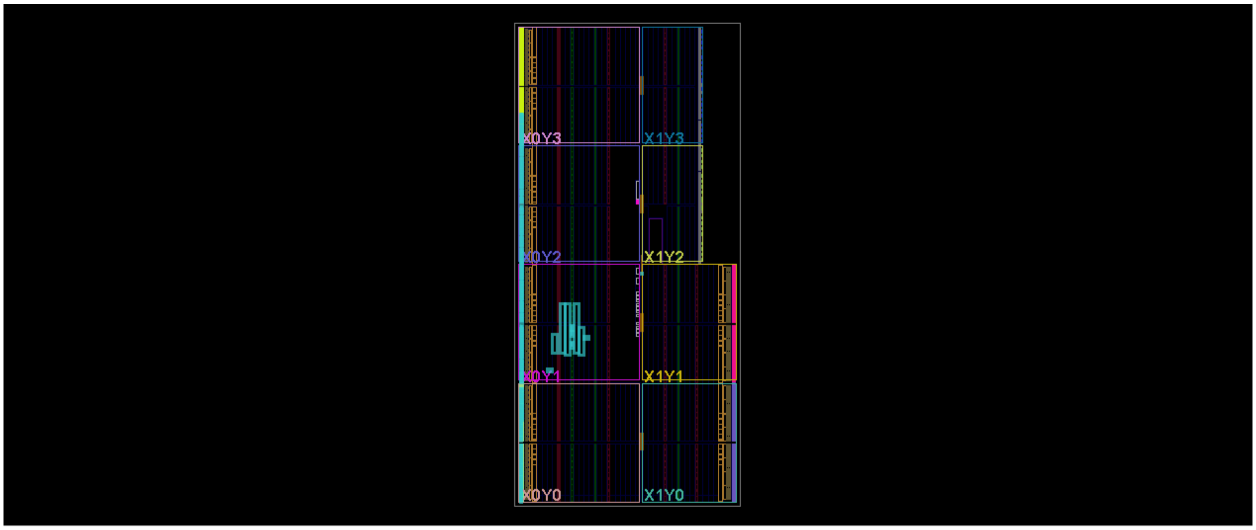
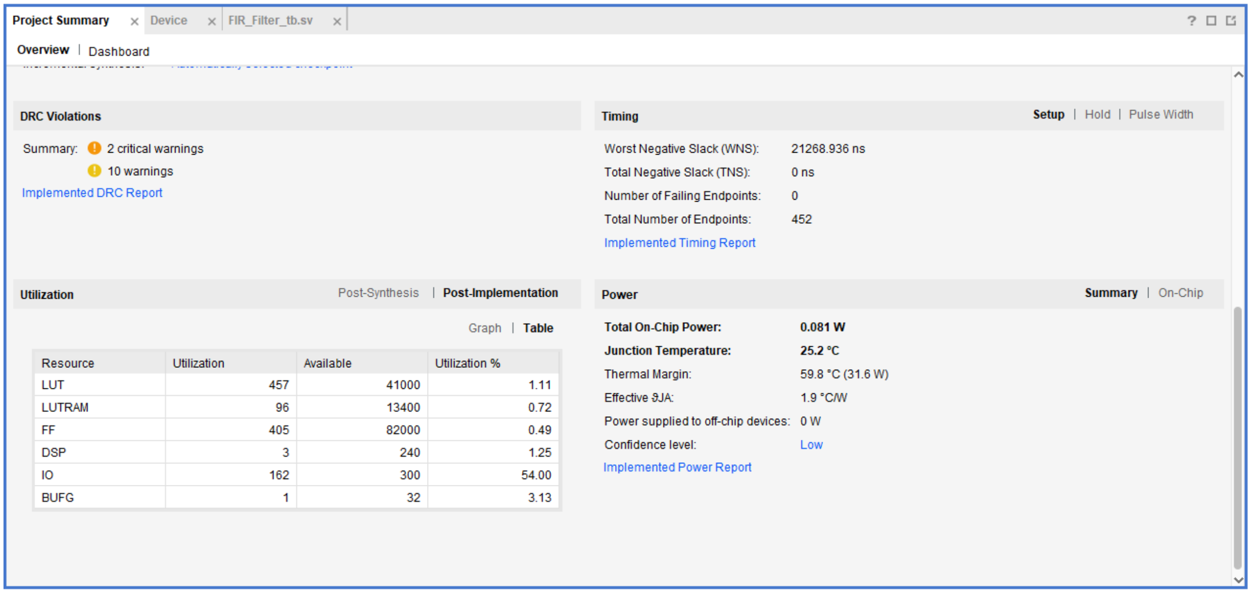


Figure 17: Parallelization (N=2) Device Layout



DRC Violations

Summary: 2 critical warnings
10 warnings

Implemented DRC Report

Timing

Worst Negative Slack (WNS):	21268.936 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	452

Implemented Timing Report

Utilization

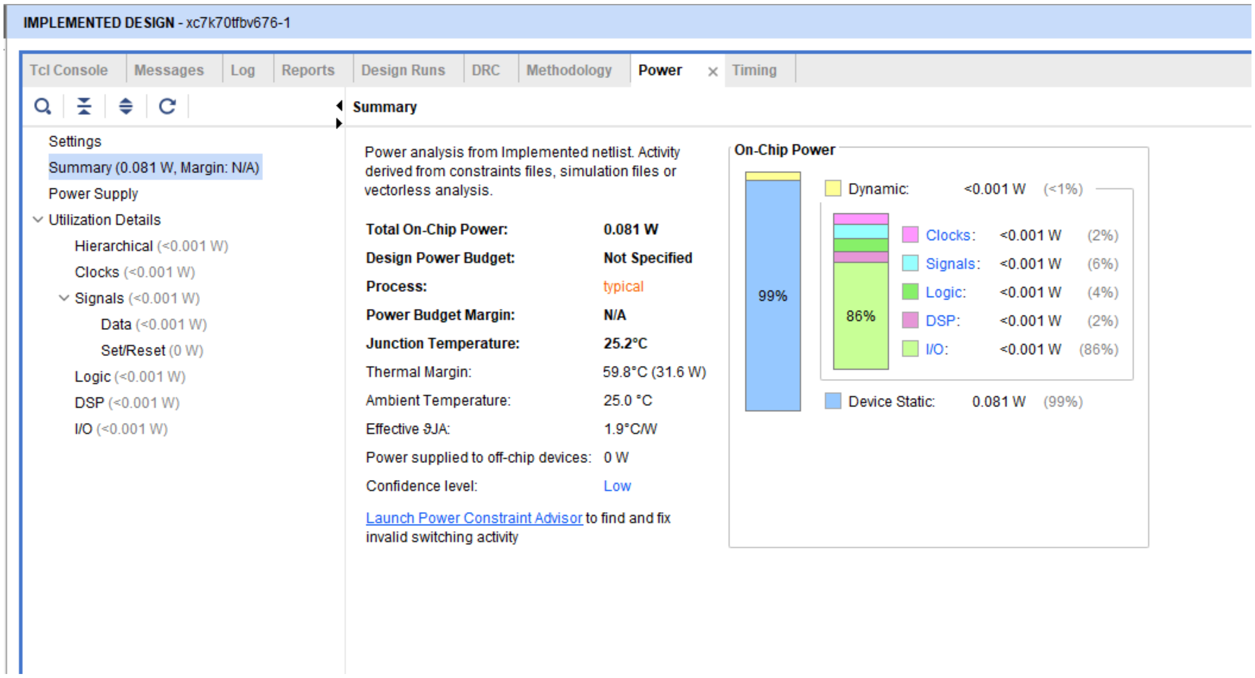
Resource	Utilization	Available	Utilization %
LUT	457	41000	1.11
LUTRAM	96	13400	0.72
FF	405	82000	0.49
DSP	3	240	1.25
IO	162	300	54.00
BUFG	1	32	3.13

Power

Total On-Chip Power:	**0.081 W**
Junction Temperature:	**25.2 °C**
Thermal Margin:	59.8 °C (31.6 W)
Effective ϑJA:	1.9 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

Figure 18: Parallelization (N=2) Cell Count & Summary



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

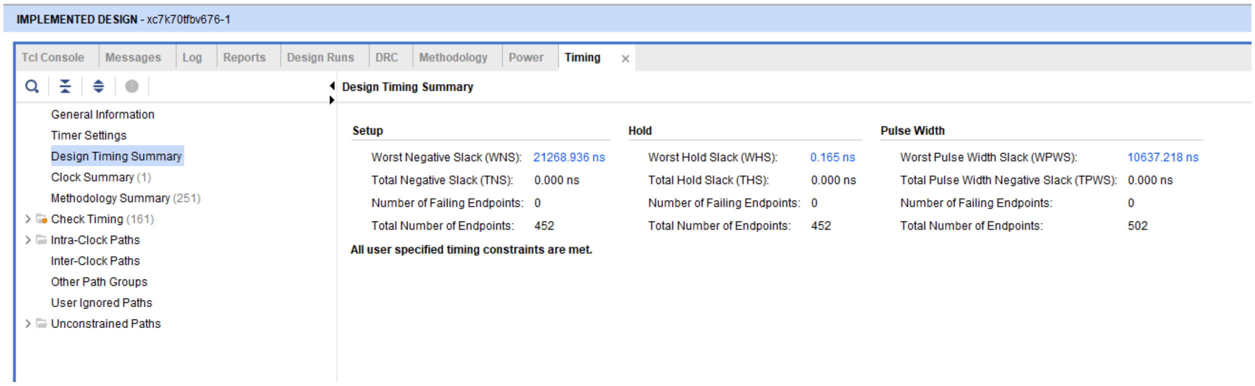
Total On-Chip Power:	**0.081 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	<0.001 W	(<1%)
Clocks:	<0.001 W	(2%)
Signals:	<0.001 W	(6%)
Logic:	<0.001 W	(4%)
DSP:	<0.001 W	(2%)
I/O:	<0.001 W	(86%)
Device Static:	0.081 W	(99%)

Figure 19: Parallelization (N=2) Power



Design Timing Summary

Setup		**Hold**		**Pulse Width**	
Worst Negative Slack (WNS):	21268.936 ns	Worst Hold Slack (WHS):	0.165 ns	Worst Pulse Width Slack (WPWS):	10637.218 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	452	Total Number of Endpoints:	452	Total Number of Endpoints:	502

All user specified timing constraints are met.

Figure 20: Parallelization (N=2) Power

iii. Parallelization (N=3) Hardware Implementation Results

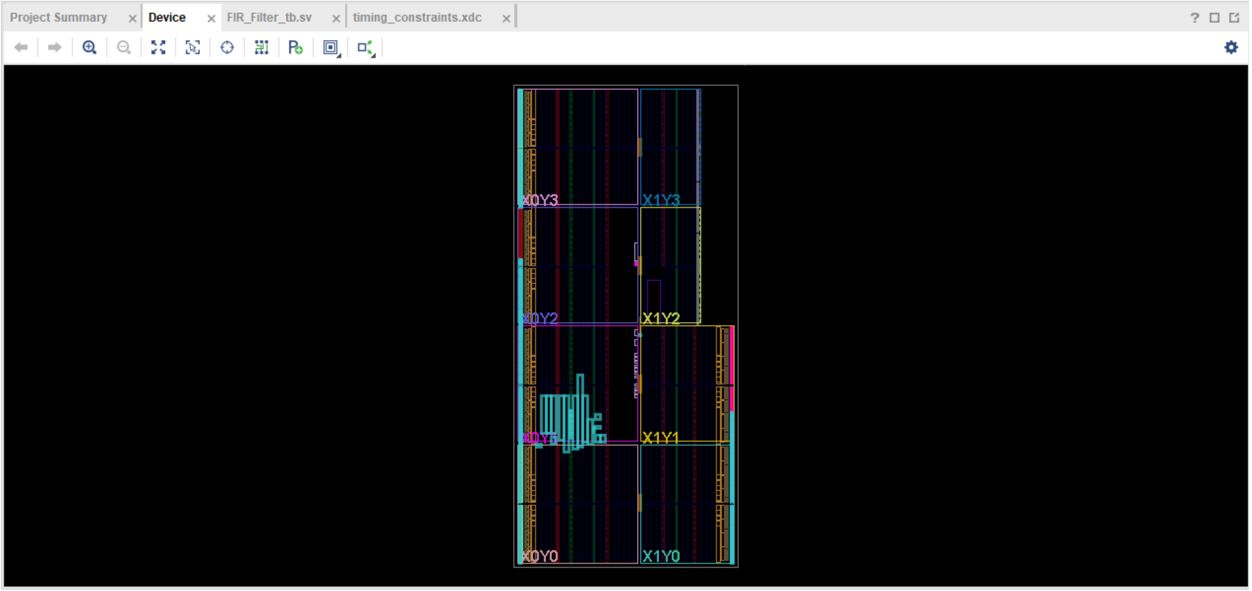
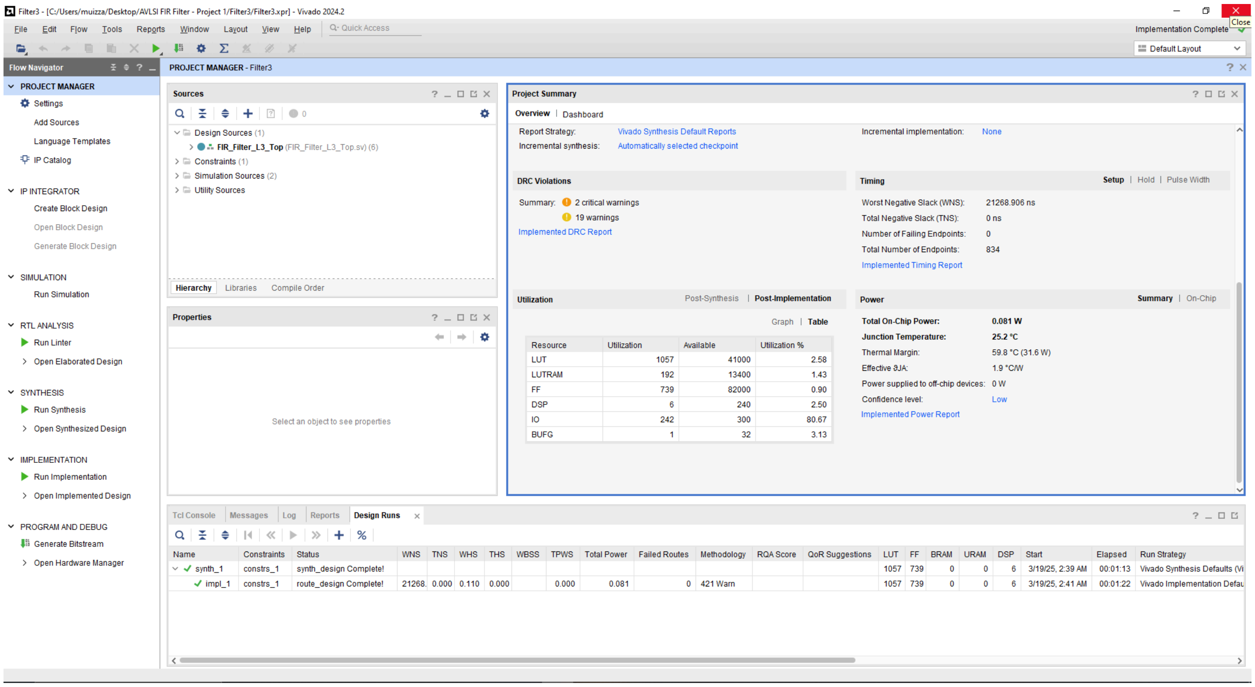


Figure 21: Parallelization (N=3) Device Layout



Filter3 - [C:/Users/muizza/Desktop/AVLSI FIR Filter - Project 1/Filter3/Filter3.xpr] - Vivado 2024.2

Implementation Complete ✓

PROJECT MANAGER - Filter3

Sources

- Design Sources (1)
  - FIR_Filter_L3_Top (FIR_Filter_L3_Top.sv) (6)
- Constraints (1)
- Simulation Sources (2)
- Utility Sources

Project Summary

Report Strategy: Vivado Synthesis Default Reports

Incremental synthesis: Automatically selected checkpoint

Incremental implementation: None

DRC Violations

Summary: 2 critical warnings
19 warnings

Implemented DRC Report

Timing

Worst Negative Slack (WNS):	21268.906 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	834

Implemented Timing Report

Utilization

Resource	Utilization	Available	Utilization %
LUT	1057	41000	2.58
LUTRAM	192	13400	1.43
FF	739	82000	0.90
DSP	6	240	2.50
IO	242	300	80.67
BUFG	1	32	3.13

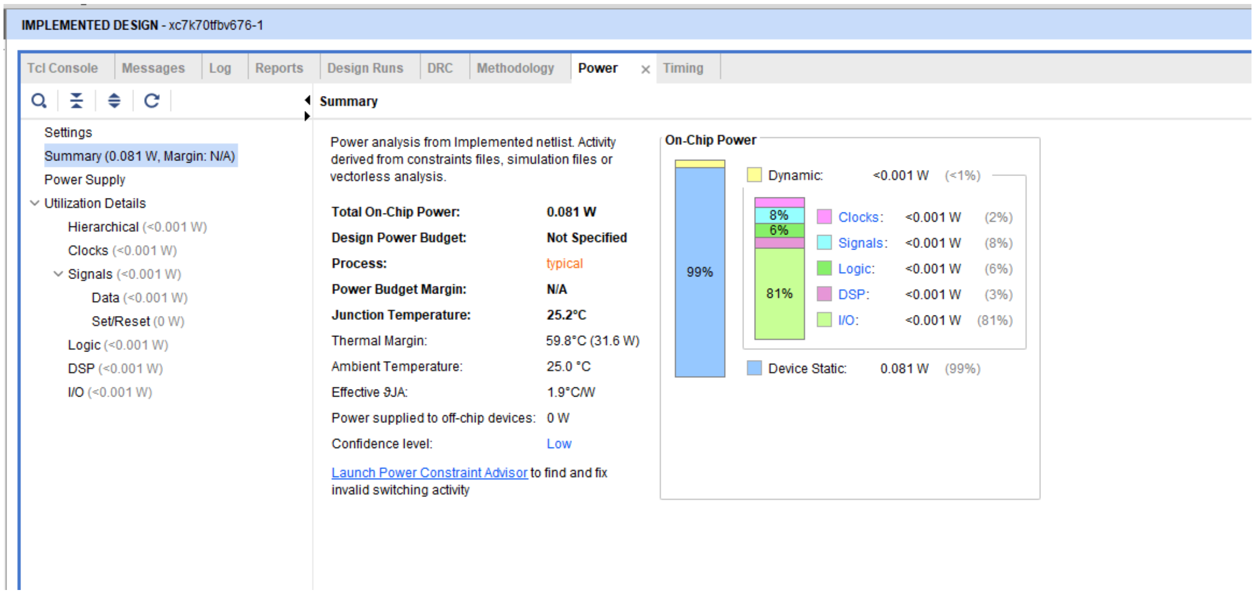
Power

Total On-Chip Power:	**0.081 W**
Junction Temperature:	**25.2 °C**
Thermal Margin:	59.8 °C (31.6 W)
Effective ϑJA:	1.9 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
✓ synth_1	constrs_1	synth_design Complete!												1057	739	0	0	6	3/19/25, 2:39 AM	00:01:13	Vivado Synthesis Defaults (Vi
✓ impl_1	constrs_1	route_design Complete!	21268.	0.000	0.110	0.000		0.000	0.081	0	421 Warn			1057	739	0	0	6	3/19/25, 2:41 AM	00:01:22	Vivado Implementation Defau

Figure 22: Parallelization (N=3) Cell Count & Summary



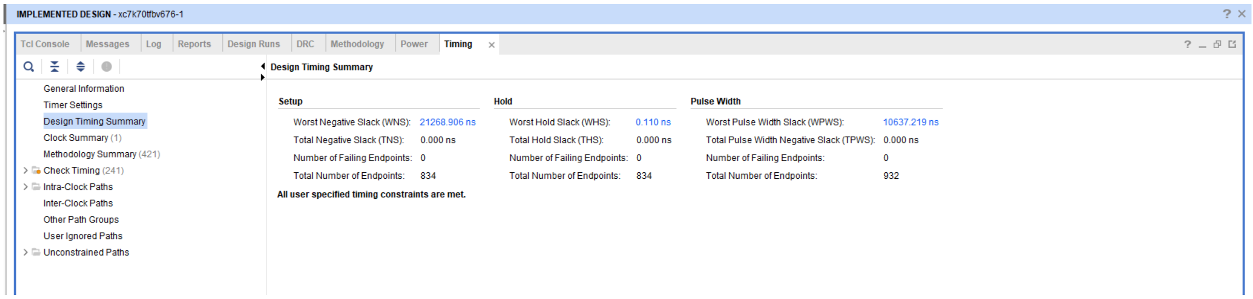
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.081 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

Dynamic:	<0.001 W	(<1%)
Clocks:	<0.001 W	(2%)
Signals:	<0.001 W	(8%)
Logic:	<0.001 W	(6%)
DSP:	<0.001 W	(3%)
I/O:	<0.001 W	(81%)
Device Static:	0.081 W	(99%)

Figure 23: Parallelization (N=3) Power



Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	21268.906 ns	Worst Hold Slack (WHS):	0.110 ns	Worst Pulse Width Slack (WPWS):	10637.219 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	834	Total Number of Endpoints:	834	Total Number of Endpoints:	932

All user specified timing constraints are met.

Figure 24: Parallelization (N=3) Timing

iv. Pipelining & Parallelization (N=3) Hardware Implementation Results

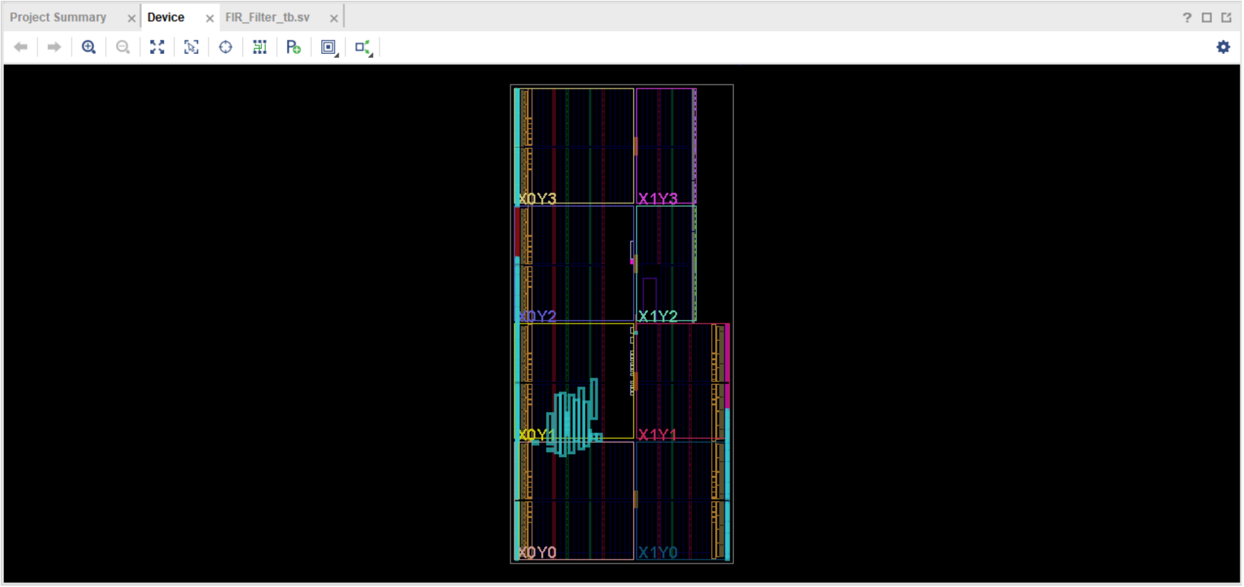
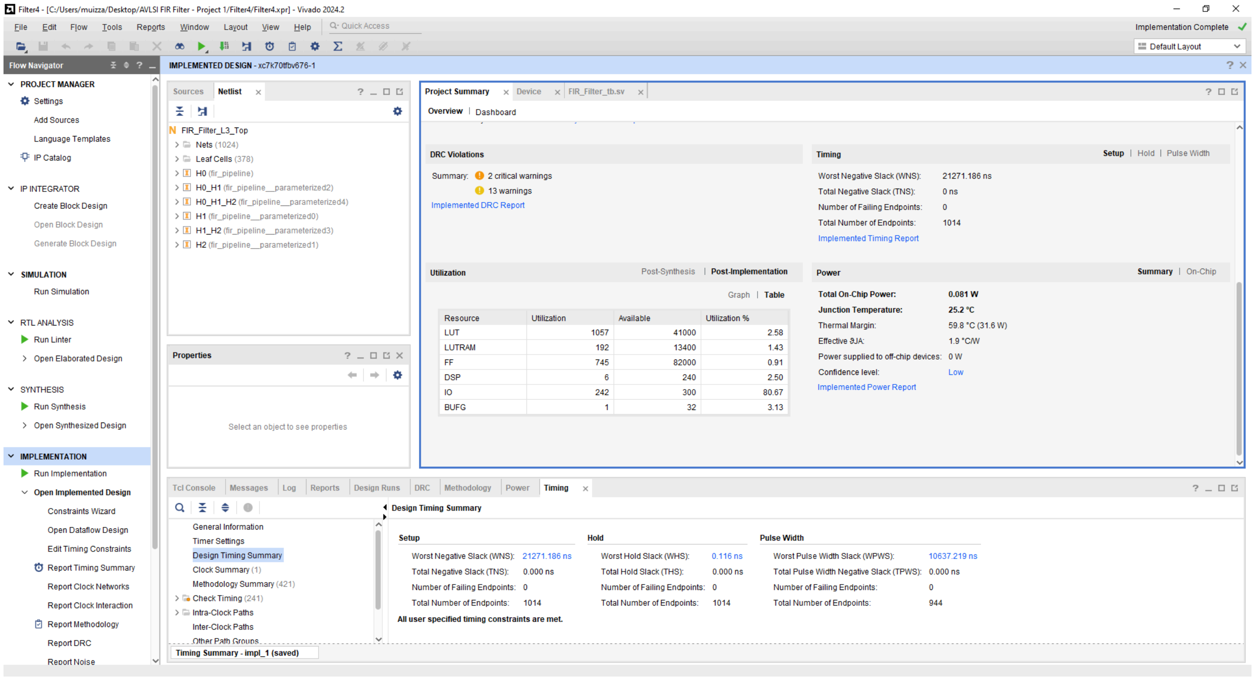


Figure 25: Pipelining & Parallelization (N=3) Device Layout



IMPLEMENTED DESIGN - xc7k70tfbv676-1

FIR_Filter_L3_Top
- Nets (1024)
- Leaf Cells (378)
- H0 (fir_pipeline)
- H0_H1 (fir_pipeline__parameterized2)
- H0_H1_H2 (fir_pipeline__parameterized4)
- H1 (fir_pipeline__parameterized0)
- H1_H2 (fir_pipeline__parameterized3)
- H2 (fir_pipeline__parameterized1)

Select an object to see properties

DRC Violations

Summary: 2 critical warnings
13 warnings
Implemented DRC Report

Timing

Worst Negative Slack (WNS): 21271.186 ns
Total Negative Slack (TNS): 0 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1014
Implemented Timing Report

Utilization

Resource	Utilization	Available	Utilization %
LUT	1057	41000	2.58
LUTRAM	192	13400	1.43
FF	745	82000	0.91
DSP	6	240	2.50
IO	242	300	80.67
BUFG	1	32	3.13

Power

Total On-Chip Power: **0.081 W**
Junction Temperature: **25.2 °C**
Thermal Margin: 59.8 °C (31.6 W)
Effective ϑJA: 1.9 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report

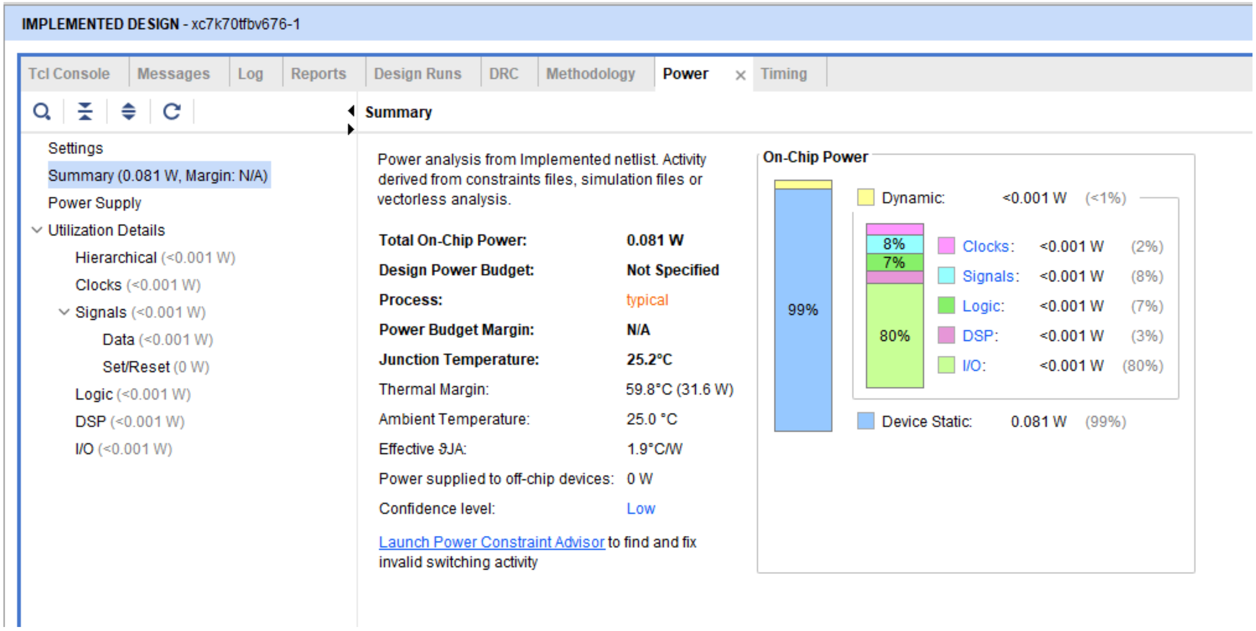
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	21271.186 ns	Worst Hold Slack (WHS):	0.116 ns	Worst Pulse Width Slack (WPWS):	10637.219 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1014	Total Number of Endpoints:	1014	Total Number of Endpoints:	944

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

Figure 25: Pipelining & Parallelization (N=3 Cell Count & Summary



IMPLEMENTED DESIGN - xc7k70tfbv676-1

- Settings
- Summary (0.081 W, Margin: N/A)
- Power Supply
- Utilization Details
  - Hierarchical (<0.001 W)
  - Clocks (<0.001 W)
  - Signals (<0.001 W)
    - Data (<0.001 W)
    - Set/Reset (0 W)
  - Logic (<0.001 W)
  - DSP (<0.001 W)
  - I/O (<0.001 W)

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

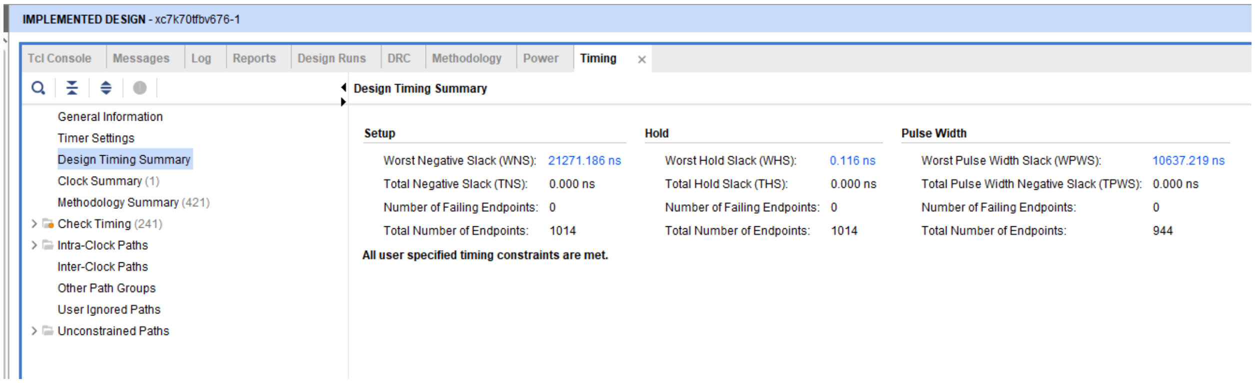
Total On-Chip Power:	**0.081 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	<0.001 W	(<1%)
🟪	Clocks:	<0.001 W	(2%)
🟦	Signals:	<0.001 W	(8%)
🟩	Logic:	<0.001 W	(7%)
🟪	DSP:	<0.001 W	(3%)
🟩	I/O:	<0.001 W	(80%)
🟦	Device Static:	0.081 W	(99%)

Figure 27: Pipelining & Parallelization (N=3 Power



IMPLEMENTED DESIGN - xc7k70tfbv676-1

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Methodology Summary (421)
- Check Timing (241)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths

Design Timing Summary

Setup

Worst Negative Slack (WNS):	21271.186 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	1014

Hold

Worst Hold Slack (WHS):	0.116 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	1014

Pulse Width

Worst Pulse Width Slack (WPWS):	10637.219 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	944

All user specified timing constraints are met.

Figure 28: Pipelining & Parallelization (N=3 Timing

Table 1: Hardware Implementation Summary

	Area (Total Cell Count)	On-Chip Power (Watt/area)	Worst Hold Slack (nsec)
Pipelined	488	0.081	0.086 ns
Parallel (N=2)	1,124	0.081	0.165 ns
Parallel (N=3)	2,237	0.081	0.110
Pipelined and Parallel (N=3)	2,243	0.081	0.116

6. Analysis & Conclusion

This project highlights the tradeoff between performance and area. While you can achieve increased performance with processes like L=3 parallel architecture, it comes with a significant cost in total cell count, meaning a larger area is used on-chip. We also see an increase in overall power consumption, as the consistent power density is now calculated over a larger area. Timing can increase with pipelining and parallelization, but once again comes with the drawback of area, power, and complexity. This simplified pipelining does not provide the expected benefit that full pipelining should. The critical path of this pipeline provides some level of improvement, but it is still too much when compared to a fully efficient pipeline.

Quantization of filter coefficients provided immense value by decreasing the total number of bits per tap. Decreasing to 24-bit allowed us to reduce bitcount, while still retaining precision that matched with the double-floating values. Proper scaling and overflow management with delays ensured that MAC operations occurred successfully, without limiting filter operation.

This project illustrates the process and development of a low-pass FIR filter through MATLAB and HDL. This filter can be improved in areas such as timing with processes such as quantization, pipelining, and parallelization, but at the cost of increased power draw and cell area. The correct design choice will depend on user requirements, use case, and operational environment.