Flight Computer for IlliniSat-2

FINAL REPORT
ECE445 – Senior Design Laboratory

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ABSTRACT

This report discusses the design and implementation of a Printed Circuit Board (PCB) that resides in a CubeSat. The PCB, also referred to as the Carrier and Data Handling (C&DH) board, utilizes communication peripherals to facilitate the interaction between the on-board processor and rest of the satellite subsystems, such as the data collection units and various payloads.

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1. INTRODUCTION

The Illini CubeSat team is a group working towards building a small CubeSat that will be launched in the summer of 2016. The goal of the project is to develop a satellite that is scalable and flexible in design to allow for a variety of different missions. With that in mind, the satellites incorporate a specific design structure; this structure has a series of PCB's that are stacked on top of each other and form the backbone of the satellite itself. The various PCB's are designed to handle one or two requirements. This is an attempt to isolate functionality within the CubeSat structure itself; this design will aid in debugging and testing procedures, as well as improve the ability to modularize the design of future CubeSats.

One of the required PCB's for the CubeSat project is the Control and Data Handling board (also referred to as the C&DH board). The CubeSat group approached us with the task of designing and building this board, and is the focus of this final paper.

1.1 Purpose

The goal of this project is to design and develop a board that connects the brain of the satellite (an ARM processor) with the peripherals of the CubeSat and the other PCB's in the CubeSat's backbone structure. In essence it is a board that provides the necessary connections for the processor to communicate with all other parts of the satellite. The processor itself sits on a daughter card (commonly referred to as the MitySOM module, or the MitySOM daughter card) which mates with the C&DH board through a 204 pin SODIMM connector. Once connected, the processor gains access to all components on the satellite. The following functions and features are what the C&DH board offers per the design requirements [1].

1.2 Functions and Features

1.2.1 Functions

This board provides several functions that enable the processor to communicate with the rest of the satellite; further considerations were also made to allow the board to function efficiently in space. These functions are listed below:

- Provides access to SPI, UART, and USB communication connections for various payloads
- Provides access to the power circuitry of the CubeSat
- Provides power access to the MitySOM module
- Efficiently heat sinks the MitySOM module
- Provides fastener connections (such as screw holes) for more secure connections
- Provides the ability to access the ARM processor and debug applications on the processor

1.2.2 Features

- 2 USB Memory Controller IC's
- 2 NAND Flash IC's (16 GB each, total of 32 GB extra memory)
- 4 UART to RS422 transceivers (no CTS/RTS)
- 1 UART to RS232 transceiver with CTS/RTS handshaking
- 1 Debug Port (two TTL lines) for debugging and programming the MitySOM
- Backbone connector that links C&DH to rest of CubeSat board stack

1.3 Block Diagrams

1.3.1 High-Level Block Diagram Description

Block Diagram 1

Block Diagram 1 is the high level Communication diagram for the C&DH board. The MitySOM335x Module connects into the C&DH board through a 204 pin SODIMM connector. This connector provides access to all of the pins on the MitySOM335x, allowing the C&DH board to route all of the signal communications as shown below.

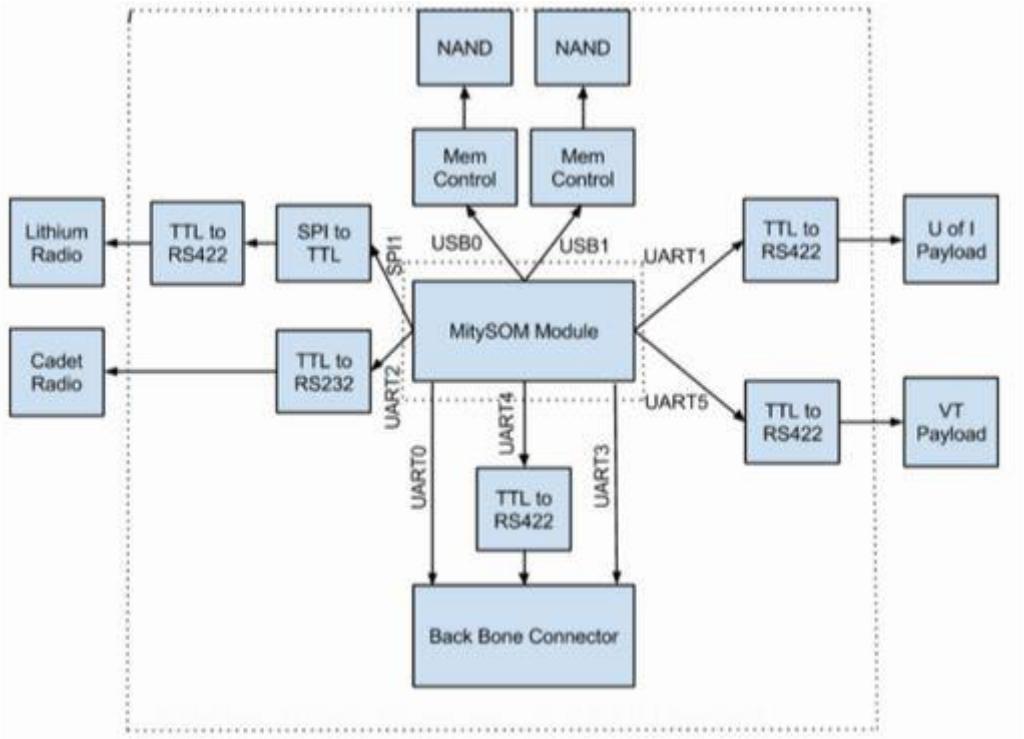

Figure 1: Block Diagram 1, Overall Block Diagram

Block Diagram 2[1]

Block Diagram 2 is the Power Flow diagram. The Backbone connector provides the connection between the Power Board on the CubeSat and the rest of the boards. The C&DH board uses a power delay circuit to allow the MitySOM to boot up first before the transceivers begin to draw power. This is to prevent any improper current draw from the MitySOM's pins that could potentially burn out the circuit.

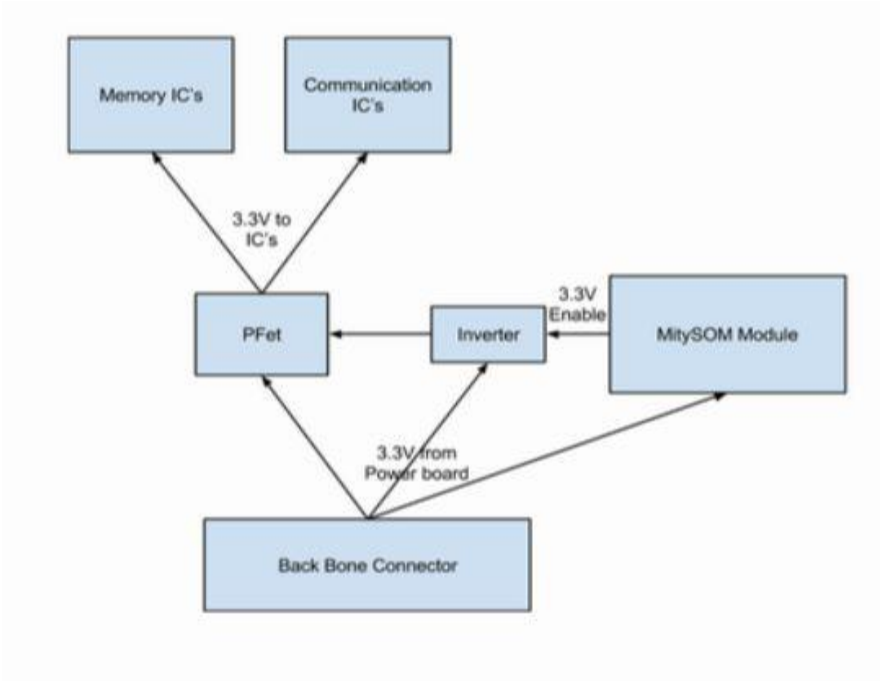

Figure 2: Block Diagram 2, Power Sequencing

[1] The block "PFET" is a misnomer; this is actually a more complicated IC, but it serves as a switch in this application, just like a PFET

Block Diagram 3

Block Diagram 3 is the flow control of the NAND Flash memory circuit. It utilizes both of the MitySOM's USB ports; the flow of data is through the two USB's via the Cypress memory controllers. The Micron chips are both 16 GB chips, one of which is used solely as a back-up memory unit in the event that one of the two circuits fails.

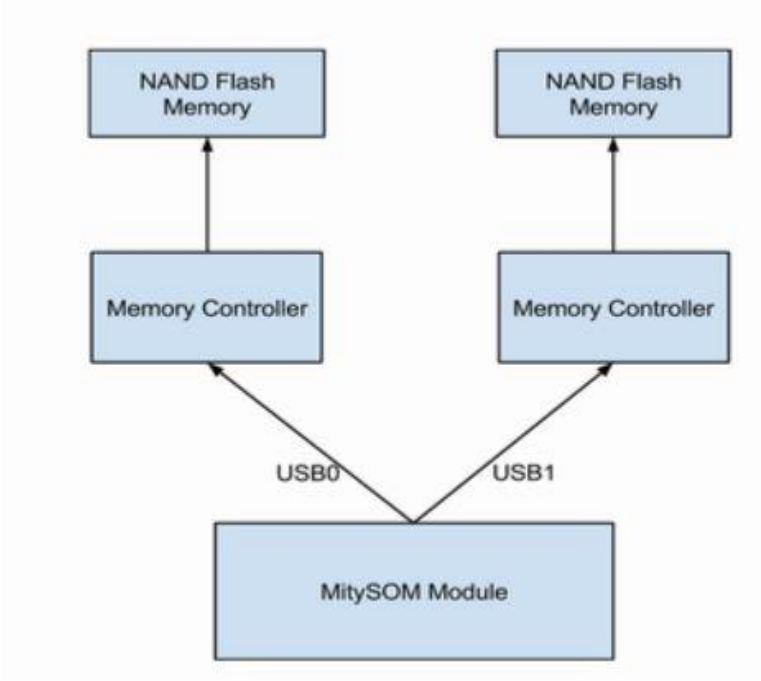

Figure 3: Block Diagram 3, Memory

1.3.2 Individual Block Description

TTL to RS422/RS232

Each one of these blocks represents a single UART to RS- transceiver. These transceivers provide the necessary two way communication that the MitySOM requires to communicate to peripherals.

SPI to UART Conversion

This block does the SPI to UART conversion; the reason for having this block is to add one more UART in the communication circuitry. The chip that does the SPI to UART conversion is a National Semiconductor SC16IS740.

NAND Flash

The NAND Flash blocks describe the Micron NAND Flash chips that will be used on the mission. Each of these chips are 16 GB TSOP chips that are controlled by a Cypress memory controller.

Memory Controller

The memory controllers take a USB differential as an input. These controllers follow a specific format and instruction set that is translated to reads and writes to the memory IC's.

Backbone Connector

This is the connector that connects the C&DH board to the other PCBs in the stack. It also provides the power for the C&DH board.

MitySOM Module

The daughter card that mates with the C&DH board. This card holds the processor as well as the NAND Flash that the ARM processor uses to boot up.

All other components or blocks not described are covered in greater detail in later sections and are not important for understanding the block diagrams. The blocks outside the outer dashed box are the Peripherals; for more information on them, see section 2.2.1.

2. DESIGN [2]

The design is largely implemented based on constraints from other parts of the satellite. Requirements such as size and location of tall components were major factors; other items to consider were the types of peripherals that connect to the C&DH board and how the MitySOM module communicates with the other boards in the PCB stack. These design factors can be rolled into four main categories: Space Operation, Communication, Memory, Peripherals, and Power Sequencing. A few other more minor design implementations are discussed in section 2.5, as well as other possible implementations of the design in section 2.6.

2.1 Space Operation

In order to operate in space, special considerations must be made for the design and implementation of the C&DH board. Due to the size constraint of the CubeSat, the C&DH board must meet very specific requirements on dimensions. In order to have enough room to slide a PCB over the top, the C&DH board must have a height that is no more than 8 mm. On the bottom of the C&DH, the location of any tall components is required to be in the center of the board; this is to accommodate the Power Board that sits beneath it.

Other space considerations include screwing down any component that could move free on the board. This includes the MitySOM daughter card and one of the oscillators on the board. During space launch, the vibrational forces are strong enough that the MitySOM module could shake loose from the SODIMM connector; therefore it is a requirement to provide screw holes that would lock the card to the C&DH board. For similar reasons, the oscillator that is located on the

[2] All schematics for the entire design are in Appendix B at the end of this report

top of the board has a wire that wraps over the top of it to prevent it from moving away from the board.

Most importantly, the climate of space must be considered. Due to the lack of air, heat sinking becomes an issue. The only way to draw heat away from the processor and other IC's is to use conduction through the board's screws and down towards the heat sinks located on another PCB in the stack. Another issue that arises in space is a phenomenon called solder whiskering. This is when the solder on the PCB begins to grow very tiny strands. These strands can sometimes grow large enough to the point that they short out circuitry [2]. One method of preventing this is to conformal coat that board, which is a requirement of the C&DH board (conformal coating also solves another problem known as outgassing) [3].

2.2 Communication[3]

This is the most critical part of the design; in order for the C&DH board to be of any use at all, it must provide communication capabilities to the MitySOM module. Because of this, careful considerations are made in the design of all communication systems. These systems include the peripherals, and the communications between the Power Board and the C&DH board.

2.2.1 Peripherals[4]

There are four peripherals on the Cubesat that connect with the C&DH board. These are the Lithium Radio, the Cadet Radio, the UIUC Payload, and the VT Payload. The Cadet radio is the main control radio that is used to communicate with the satellite from the ground station on Earth. The two payloads are the photometer and the ion detector, both of which are used to take scientific measurements. The Lithium Radio is a commercial amateur radio that people on the ground can use.

Each of these peripherals has their own specific communication protocols. The job of the C&DH board is to provide the correct transceiver for each of the peripherals; all of these involve a conversion of UART TTL signals to RS- protocols. Each of these conversions is done via a transceiver IC that is placed on the C&DH board. The only difference in each case is the type of RS- protocol used for each peripheral and the type of data flow control for each peripheral. An example of this is RS-232 with CTS and RTS control signals, which is the scheme for the Cadet Radio peripheral. The two university payloads and the Lithium Radio are simpler in their design. All that these payloads require are RS-422 TX+/- and RX+/- signals.

There are two main differences between the Lithium Radio and the two payloads. Due to the fact that the MitySOM module only has a maximum of six UART's, another step is taken in the conversion from TTL logic to the RS- protocol. In order to generate another UART connection, an SPI to UART IC[5] is used on the C&DH board. After this conversion, the UART goes to the same type of transceiver as the ones used for the university payloads, and functionally is the same as the payloads as well. The other smaller difference is the Lithium Radio uses an enable signal as well, so one of the pins is tied to a GPIO on the MitySOM module.

[3] See the schematics in Appendix B for the part numbers.
[4] In the appendix pages there is a chart listing the pinouts for all of the DF11 connectors.
[5] See footnote 3.

The peripherals connect to the C&DH board via a right angled connector. These connectors are a Hirose brand known as a DF11. Each connector has six pins for the RS-422 communication. For all the payloads except the Cadet Radio, four of these pins are RX+/- and TX+/- signals. In the case of the Cadet Radio, two of the pins are RX and TX, and two of the pins are CTS and RTS signals.

For all of the peripherals, the two remaining pins are tied to ground. The reason for this design choice is in practice the RS- communication only needs five pins for each of the transceivers; however a five pin connector does not exist. Therefore, six pins are used to fulfill the functionality. Since a floating pin can be dangerous, the remaining pin is tied to ground for safety reasons.

2.2.2 Backbone Connector[6]

The Backbone Connector is a 40 pin connector that attaches the C&DH board with the rest of the PCB stack in the CubeSat. It is through the Backbone Connector that the C&DH board communicates to the Power Board. This communication is used to provide the MitySOM module with data on the overall power remaining in the system, as well any health status information about the satellite. Once the MitySOM module receives this information, it can act accordingly in the best interest of the satellite, and relay the relevant information back to the ground station on Earth. It is also through this link that the MitySOM module can receive the signal that a power shutdown is about to go into effect for the CubeSat.

This communication is done in a similar way as the two payloads. A UART TX and RX signal comes from the MitySOM module which is then passed into the transceiver that converts the logic to the RS-422 protocol. This is then passed on through to the Power Board via the Backbone Connector.

There is one other set of communications that the MitySOM module sends through the Backbone Connector. There are three signals: a TX[7], a RX, and an enable. These TTL logic lines are directly connected to the Backbone Connector because the transceiver that does the conversion of these signals is located on the Power Board rather than the C&DH board. These lines are used for communicating to the Bus Hardware on the CubeSat.

[6] In the Appendix pages there is a table with the pinout of the Backbone Connector for reference.
[7] These TX and RX signals are from UART3; see the MitySOM pinout in Appendix C.

2.3 Memory Circuitry[8]

The Memory Circuitry provides the MitySOM module with an additional 16 GB of NAND Flash memory. There are two Micron 16 GB chips on the C&DH board; one of these is used as a back-up location for any data taken during the mission in the event that the main memory chip goes down at any time during the mission. This concept is known as 32 GB with 16 GB duplicate.

Each memory circuit has three components: a USB port from the MitySOM module, a Cypress memory controller, and a Micron 16 GB NAND Flash chip. If any one of these components goes down during the mission, all of the data is still maintained in the other memory chip. Originally the design implemented a USB hub to allow for two USB ports to be controlled by one USB; however in the event that the USB hub goes down, both memory circuits are lost, thus breaking the concept of duplicated memory. The memory controllers are two Cypress chips that follow the standard memory controller protocol. The USB connections write a command to the controllers. The controllers then translate the command into a read or write and send this information to the memory IC's on the C&DH board.

2.4 Power Sequencing

This part of the design involves booting up all of the IC's and the MitySOM module in the correct order. The reason for this is the MitySOM module could potentially damage itself or the transceivers if they were turned on before the processor on the MitySOM module is fully booted up [4]. The Power Sequencing circuit involves connecting the MitySOM's 3.3VOUT pin to the enable of a PFET. The PFET acts as a switch that closes and connects the power from the Backbone Connector to the rest of the IC's on the C&DH board. This switching motion acts as a delay for the powering on for the rest of the circuitry, thus allowing the MitySOM module to boot up first, then the rest of the components on the board.

2.5 Miscellaneous

2.5.1 Boot-up Pin Routing

The MitySOM module can boot up from a variety of different sources. For the purposes of the mission, the MitySOM module is hardwired on the C&DH board to boot up via the memory that is on the MitySOM module. This hardwiring scheme is implemented on the C&DH board by tying the boot up configuration pins to power or ground. The boot-up configuration pins are the LCD_DATA pins located on the MitySOM module.

[8] For the part numbers of the Micron and Cypress IC's, look in section 4.1 for "NAND Flash" and "Memory Controller" respectively

Boot Pin	Value
LCD_DATA0	1
LCD_DATA1	1
LCD_DATA2	0
LCD_DATA3	0
LCD_DATA4	1
LCD_DATA5	1
LCD_DATA6	0
LCD_DATA7	0
LCD_DATA8	0
LCD_DATA9	0
LCD_DATA10	0
LCD_DATA11	0

Table 1: Boot-up pins and their corresponding values; VCC is 1, GND is 0

This boot up configuration forces the MitySOM module to boot up from the NAND Flash memory on the daughter card, which is the desired boot up mode for the purposes of the CubeSat project.

2.5.2 Backup Battery

The backup battery is required in order to keep the Real Time Clock (RTC) running on the MitySOM in the event that it shuts down. This is so that the real time is never lost throughout the satellite's entire mission. Losing track of time can have a significant impact on data gathering and operational movements of the satellite, so it is vital that time is kept for the entirety of the mission.

2.5.3 Part Locations

One other design consideration is the placement of various components on the board. Due to the fact that the MitySOM module sits so low on the C&DH board, the entire area underneath the MitySOM module is a keep-out zone. This made placement of the other components more difficult since roughly 60% of the top part of the C&DH board is taken up by the MitySOM module.

The bottom of the board had a different set of constraints, most of which were mandated by the Power Board that rests beneath the C&DH board. The oscillators that are used for the memory controllers are about 4.5 mm tall; this meant that they could potentially interfere with the Power Board underneath if the placement was in the wrong location. Because of this limiting factor, the oscillators are located in the center of the board, where it is least likely to interfere with the Power Board.

2.6 Design Alternatives

Besides picking different IC's that achieved the same functionality, the only real part of the circuit that has a reasonable design alternative is the memory circuitry. At the onset of this project, the initial line of thinking always was to use SPI to control the memory chips. The reasons for leaving this idea and switching to a USB memory controlled circuits were twofold. First, finding a 16 GB NAND Flash chip that is controlled by SPI is simply impossible. Therefore, to achieve that type of memory capacity there would have to be several chips. This would take up too much space on the board, and therefore it was not a possibility. Secondly, there is only one set of SPI connections on the MitySOM module; thus it would be impossible to perform the necessary duplicated memory scheme described earlier. This would be a serious hindrance in the event that the SPI port or the memory chip failed.

3. REQUIREMENTS AND VERIFICATION

There were a specific set of requirements that this board had to meet. The Requirements and Verification table provided in the Appendix pages lists out all of these requirements, as well as steps for verifying them. This section will break down the Requirements and Verification steps into two main categories: tests that were performed and tests that were not performed.

3.1 Performed Tests

These were the set of tests that could be performed in a timely manner and could be demoed in about ten minutes.

3.1.1 Power Requirements

The steps for the Power Sequencing are performed as specified in the Requirements and Verification table in the Appendix A. The picture of the scope readings was taken that shows the delay in the voltage rise over the circuit. This picture is shown below, and as one can see, it starts out low when the power is first turned on, and then rises high after a short delay.

Figure 4: Proof of the Power Sequencing. Note the initial delay in spiking from 0V to 3.3V.

The Power Consumption test was performed, and once again the requirement was met. At the highest current draw, the reading was around 550 mA, which is well within the target max current draw of 700 mA. One should note that this test was performed without the memory circuitry in place; however the most current that those components will add is around 100 mA [5], so it should still meet the requirements.

3.1.2 Communication Tests[9]

Communication tests for the UART (Test 1) and the TTL to RS422 (Test 2) conversion were performed; the remaining circuit tests were not performed. Both Test 1 and Test 2 were performed in a similar manner. A simple loopback test was implemented in each instance. For Test 1, the TX and RX of UART3 are tied together, and then bytes are sent across and echoed on the screen for the user to see. This test passed with exceptionally good results; the image below is an echoed text file of several hundred bytes, without a single error.

[9] See Appendix D for detailed instructions on how to set up the communication testing. Source code is presented in Appendix E.

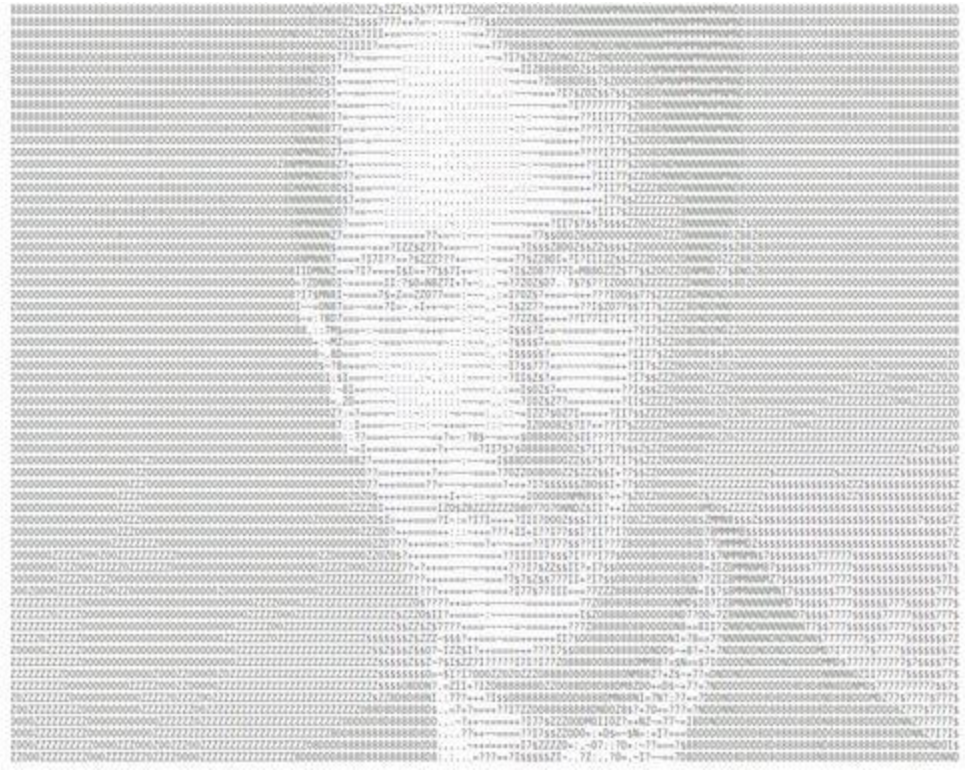

Figure 5: File that was echoed over UART3

Test 2 is a similar test, with the TX and RX lines tied together. Here again a loopback test is performed with bytes, however in this instance the bytes are sent but do not loop back. Therefore this test fails, and it fails on all of the transceivers. There are several possible reasons for failing this requirement:

- Pin MUXing issues on the MitySOM module
- Mis-routing the transceivers
- Code for the loopback test is incorrect

Of the three possible issues, the first one is most likely the main cause. The routing of the transceivers is straightforward, and it is therefore unlikely that the routing was done incorrectly. Since the same code that is used for the loopback test of Test 1, it is unlikely that the code is the problem. Therefore this leads one to believe that the pin MUXing is most likely not working correctly. The next step for testing is to scope the transceivers to verify that data is indeed being sent out of the UART's on the MitySOM module, and that something is going out of the transceivers.

To sum up, at this time, it is possible that the hardware that is present on the board is in fact correct; more testing is needed to verify that the level shifting logic implemented in hardware is incorrect.

3.1.3 Board Dimensions and Keep-outs

These are the easiest of all of the tests to verify if they are correct. The Keep-out is violated because the footprint made in Cadence is wrong for the MitySOM module. This error is due to the fact that there is not any clear documentation that shows how much the MitySOM module goes into the SODIMM connector. The footprint should have a keep-out area that is slightly longer than it is shown to be in Cadence. Currently the battery that sits on top of the C&DH board will hit the MitySOM module. Furthermore, the screw locations that secure the MitySOM module are not in the right location; this again has to do with the footprint being incorrect.

Board dimensions and specific locations of the connectors have all been met. There was not any user error in the positioning of the components, or the cutout of the board itself.

3.2 Non-Performed Tests

These tests were not performed for two main reasons. Some of the parts were difficult to track down, and because of that there was not enough time to both solder the components on and do the programming to ensure the components work. This applied to the memory and SPI interface testing (Test 3 and Test 4 in the Communications requirements section). Because of this, it is unknown whether or not the hardware for these components works as expected.

The other tests that have not been performed are all of the space tests. This is because the board itself is not going to be the finalized board for the space launch; it will instead be used as a testing board for the software group in the Cubesat team. Because of this the board was not fabricated with conformal coating, nor was tin free solder used in the fabrication (simply because the cost of doing this is extremely high). Therefore it would be almost a given that these tests would fail, so there is no point in performing them and destroying a fine test board in the process.

4. COST ANALYSIS

4.1 Labor

Name	**Hourly Rate**	**Total Hours Invested**	**Total = Hourly Rate x 2.5 x Total Hours Invested**
Mark Mahowald	$40.00	150	$15,000
Daniel Brackmann	$40.00	150	$15,000
Anuj Pasricha	$40.00	150	$15,000
Total	$120	450	$45,000

4.2 Parts

Item	**Quantity**	**Total Cost ($)**
Passive Devices (Capacitors, Resistors etc.)	100	50
MitySOM3359 (Processor Card)	1	153.00
JAE MM80-204B1-1 (SO-DIMM connector)	1	6.89
SC16IS750 (SPI bridge)	6	18.66
MAX3222 (RS-232 Transceiver)	6	3.76
AMD3488 (RS-422 Transceiver)	6	22.56
CY7C68023 (Memory Controller)	2	23.96
MT29F128G08AJAAAWP-ITZ (Mircon NAND Flash)	4	Samples (not delivered)
Hirose DF11_6DP Connector (for Peripherals)	4	50.24
FOXLF018S (Crystal Resonator)	6	6.84
USB to RS422 Cable	1	57.74
MCP2210 (USB to SPI converter)	1	2.10

Total	---	395.75

4.3 Grand Total

Section	Total
Labor	$45,000
Parts	$395.75
Total	**$45,396.75**

5. CONCLUSION

5.1 Accomplishments

The C&DH board built and designed in this project is a great first step towards the final product that will be launched into outer space. The board provides the ability to boot up the MitySOM module and run communication tests to verify that software works on the MitySOM. It also provides the ability to easily debug the software through the UART_0 ports. UART_3 communication is already working, so further testing can be performed on the UART communications.

The power sequencing performs as one would expect as well, adding the necessary delay for the booting up of the IC's on the board. Power draw is also within the constraints that were requested with this design, and the dimensions of the board as well as the locations of the various components on the board work with the Power Board that sits underneath the C&DH board.

5.2 Uncertainties

The transceivers that are on the board do not appear to be fully functional. Whether or not this is due to a hardware issue or software issue is still up for debate; since the wiring of these transceivers is fairly straightforward, it would seem to imply that there is an error with the configuration of the MitySOM. The test scripts do the echo test correctly since it works with a UART port on the MitySOM itself. Because of this, the most likely cause of the problem is the pin MUXing done in software on the MitySOM module.

The memory circuitry may or may not work; this testing could not be performed because components failed to be delivered on time for the project. The memory controllers came in but the actual NAND Flash IC's went missing. Since none of this could be tested, it is unknown whether or not there was a mistake in the routing of these chips.

5.3 Future Work

Future work mostly entails thorough testing of the C&DH board. Due to the fact that components came in late, there is still much to be determined on the functionality of the board. In particular, the transceivers have to be debugged to figure out why the communication circuitry appears to be failing during the loopback testing. This will most likely entail scoping the inputs and outputs to determine what (if anything) is being transmitted by the MitySOM.

Testing of the NAND Flash will also need to be performed. Right now it theoretically will work once the chips are soldered onto the board; however there needs to be rigorous testing to prove that this is actually the case.

All space requirements will also have to be met at some point in time, but since most of these are met by fabricating the board in a specific process, it should not be too difficult to verify that these requirements are being met and that the board can safely go into space.

It should be noted that the current board is not meant to go to space, and has not been fabricated to protect against the space environment.

5.4 Ethical Considerations

Despite the fact that the C&DH board will be operating in outer space and that there may not be any direct ethical considerations in relation to human use, certain aspects of the IEEE Code of Ethics must still be taken into account during the design process.

The following points from the IEEE Code of Ethics apply to this project:

Given that the C&DH board will be operating in outer space, the team must learn how materials and electronics behave in outer space. Outer space, unlike the Earth's environment, presents a lot more technical challenges that need to be overcome (some of which are stated in the Requirements & Verification section). Over the span of this project, team members will gain an understanding on technology from a different perspective, in accordance with point 5 of the IEEE Code of Ethics:

5. to improve the understanding of technology; its appropriate application, and potential consequences;

As a continuation of the previous point, team members will learn how to design a circuit board from scratch, especially one that takes an incredible amount of precision. The stakes of failing being very high in outer space force team members to adapt new skills very quickly and understand the implications of their work on other modules on board the satellite. Team members will thus gain immense technical competence over the course of the design process, as is codified by point 6 in the IEEE Code of Ethics.

6. to maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations;

While working on the project, we need to ensure that our work environment fosters professionalism, as required in engineering projects - this includes being open to new ideas, acknowledging one's own mistakes, assisting peers with their parts of the project, accepting and giving criticism in a healthy manner. Moreover, proper credit must be given to whose work we borrow from. These points are cited in the 7th code of the IEEE Code of Ethics.

7. to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others;

Knowing that the project is based in a multidisciplinary setting, which includes teams from various backgrounds, cultural and academic, respect must be given to all team members and honesty and fairness should be of utmost importance. Tying in with the previous code, individuals must not be taken undue advantage of, which will be in direct violation of code 8.

8. to treat fairly all persons and to not engage in acts of discrimination based on race, religion, gender, disability, age, national origin, sexual orientation, gender identity, or gender expression;

Team members have done their best to abide by the IEEE Code of Ethics, especially bearing in mind the particular points stated above.

6. REFERENCES

[1] *IlliniSat C&DH Carrier Board Document*, Wang, Shimeng, IL 2014.

[2] *Basic Information Regarding Tin Whiskers.* N.p.: nasa.gov, n.d. PDF.

[3] *Conformal Coatings for Printed Circuit Board Protection*. N.p. dymax.com, n.d. Web Oct. 10th, 2014.

[4] *MitySOM-335x Processor Card*. N.p. criticallink.com, n.d. PDF.

[5] *NAND Flash Memory*. N.p. micron.com, n.d. PDF.

7. APPENDICES

APPENDIX A: Requirements and Verification Table

Outer Space:

Requirements	Verification
1. Solder that is solder whiskering resistant	1. Verify no solder whiskering can occur a. Place board in a vacuum chamber b. Leave the board in for 24 hours c. Inspect board the next day d. Passes inspection if no shorts occurred i. Take a voltmeter ii. Set it to connectivity test iii. Check each trace that is near to each other for connectivity; should not be any of them
2. Board must not outgas	2. Verify that board cannot outgas in space a. Place board in a vacuum chamber b. Leave the board in for 24 hours c. Inspect board the next day, checking for outgassing issues (pockmarks in the traces, PCB itself, or the solder joints)
3. Board must conduct heat efficiently through the attachment screws	3. Verify that the board is conducting heat a. Place board in vacuum chamber b. Provide power to the board c. Verify the regulators do not overheat d. Run test scripts (see **Communications** section) and measure the heat of the IC's e. Verify that none of the components are overheating while communicating
4. MitySOM Module connection must be shake resistant	4. Verify that under extreme vibration, MitySOM module stays connected to the C&DH board a. Place the board on a shaker table b. Run the shaker test for 10 minutes c. Vary the severity of the vibration, and repeat step b d. Verify that the circuit still works by running Test Script C (see Appendix B for description of the scripts, code not available)
5. Board must be conformal coated	5. Verification of the conformal coat will follow similar steps as requirement 1 listed in this table since its main purpose is to prevent solder whiskering.

Board Dimensions:

Requirements	**Verification**
1. Height less than 8 mm but greater than 5 mm	1. Verify that the board fits within those limits a. Connect the MitySOM Module to the C&DH board b. Take calipers c. Measure the height from top of MitySOM Module to bottom of C&DH board; should be between 5 and 8 mm d. As a further test, assemble the C&DH board with boards that are on top and on bottom and make sure the boards connects together
2. 90x90 mm board dimensions	2. Verify that the board width and length are both 90 mm by measuring the fabricated board a. Acquire the fabricated board b. Measure the width of the board with calipers; should be 90 mm ± 0.01 mm c. Measure the length of the board with calipers; should be 90 mm ± 0.01 mm
3. Cutout on one side is 70x8 mm	3. Verify that the cutout is 70x8 mm by measuring the fabricated board a. Acquire the fabricated board b. Measure the length with calipers; should be 70 mm ± 0.01 mm c. Measure the width with calipers; should be 8 mm ± 0.01 mm
4. Screw center hole locations are 5.5x5.0 mm ± 0.01 mm on the board	4. Verify the top screw center hole locations are in the correct location by measuring the center holes on the fabricated board a. Acquire fabricated board b. measure the center hole top/down location; should be within 0.01 mm of 5.5 mm c. Measure the center hole right/left location; should be within 0.01 mm of 5.0 mm
5. Backbone Connector center location should be 33mmx11mm ±0.01 mm for each dimension	5. Verify that the Backbone Connector is in the right location by measuring the center location a. Acquire fabricated board b. Measure the center point top/down location; should be 11 mm ± 0.01 mm c. Measure the right/left position of the center point; should be 33 mm ± 0.01 mm

MitySOM Module Keep-Out Areas:

Requirements	Verification
1. Recommended that there is at least 2 mm of space between the bottom of the MitySOM module board and anything beneath it[10]	1. Verify bottom Keep-out is met by measuring the highest point on the C&DH board to the MitySOM Module a. Obtain the fabricated board b. Use calipers to measure the height between the MitySOM Module and the C&DH board c. Height should be no more than 2mm, preferably less than 2 mm

Communications:

Requirements	Verification
1. TTL to RS422 conversion works	1. Verify TTL to RS422 Level Conversion works by running Test Script A[11] a. Obtain the fabricated board b. Power on the board c. Boot up the MitySOM module d. Boot up a computer e. Connect the computer by using a USB to RS422 connector f. Run Test Script A
2. UART communication to the MitySOM works[12]	2. Verify UART communications to the MitySOM works by running Test Script A a. Obtain the fabricated board b. Power on the board c. Boot up the MitySOM module d. Boot up a computer e. Connect the computer by using a USB to UART connector f. Run Test Script A
3. SPI Communication to the MitySOM works	3. Verify SPI works for communicating to the MitySOM by sending data via Test Script A a. Obtain the fabricated board b. Power on the board c. Boot up the MitySOM module d. Boot up a computer e. Connect the computer using a USB to SPI connector f. Run Test Script A

[10] See Figures 15 and 16 in Appendix F.

[11] See Appendix D for more information on this test script.

[12] See Appendix E for test source code.

4. NAND Flash Communication works	4. Verify that the MitySOM can communicate with the NAND Flash by writing data and then readin data a. Obtain the fabricated board b. Power on the board c. Boot up the MitySOM module d. Boot up a computer e. Connect the computer to MitySOM UART_0 via a USB to UART connector f. Run Test Script B[13] on the MitySOM to verify that the NAND Flash is working

Power:

Requirements	**Verification**
1. Current draw is at most 700 milliamps	1. Verify the current draw by using a power generator, setting it to 3.3 volts, and measuring the current draw a. Acquire the fabricated board b. Acquire a power generator (something like a signal generator or any power supply in the lab will do) c. Plug in the positive terminal of the power supply to the 3.3 volt pin locations for the Backbone connector d. Plug in the negative terminal to the GND pin on the Backbone Connector e. Turn on the power generator; measure the current draw. Should be less than 700 milliamps
2. Power Sequencing works correctly (MitySOM powers up first before the other IC's)	2. Verify Power Sequencing a. Attach an oscilloscope to the output of the PFET on the C&DH Board b. Apply power to the C&DH board via the Backbone Connector c. Verify that the Oscilloscope reading has a delay in the voltage that the PFET outputs

[13] See Appendix D for more information on this test script.

APPENDIX B: Schematics and Mechanical Outline

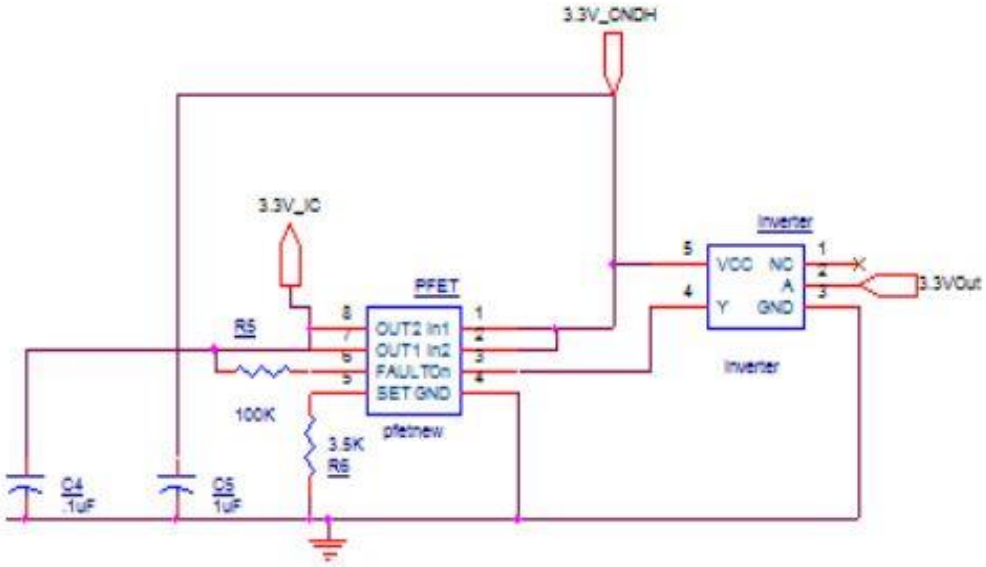

Figure 6: Power Sequencing schematic

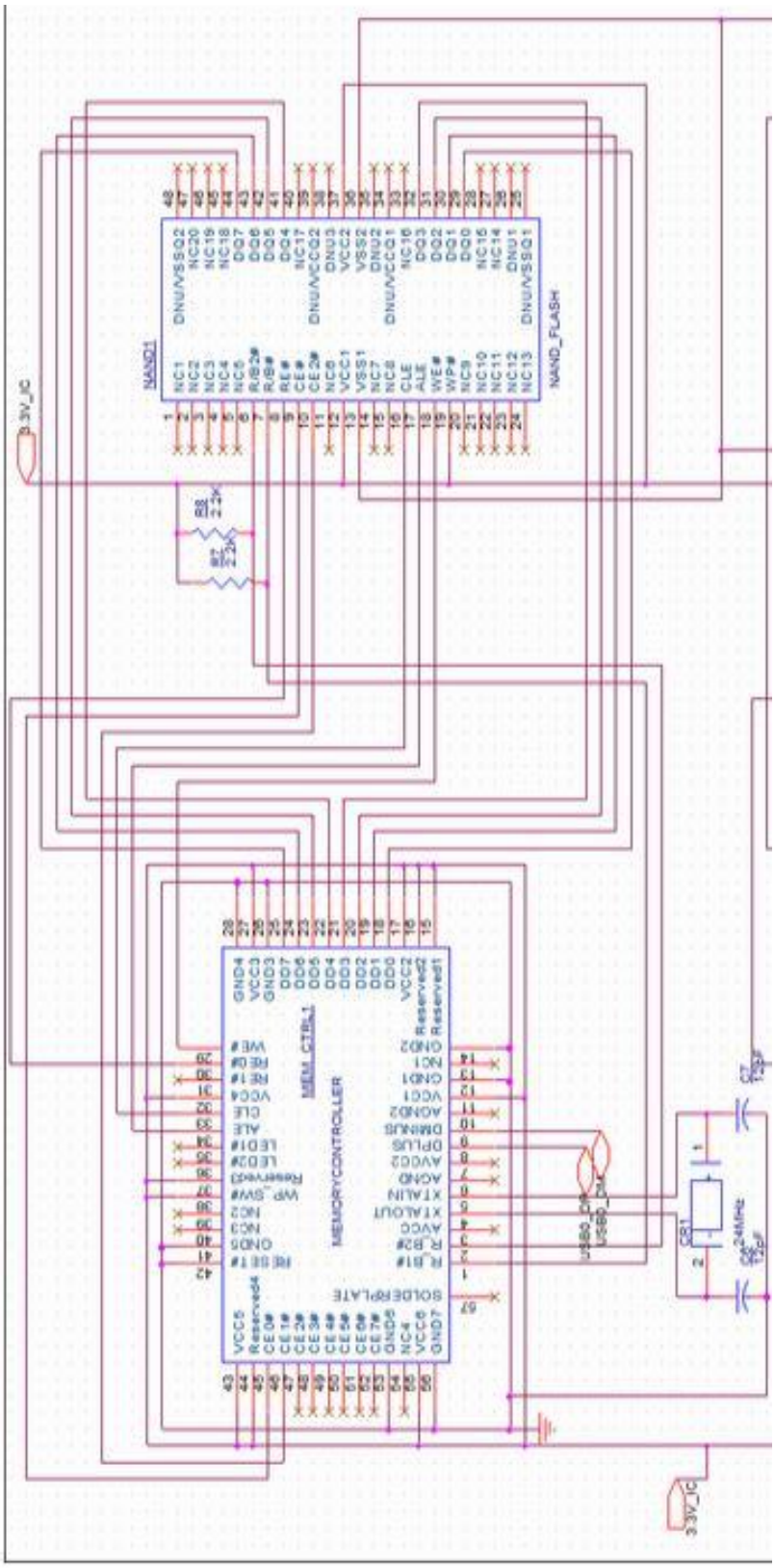

Figure 7: Memory Schematic. Duplicated circuit is cut out of this picture for clarity reasons

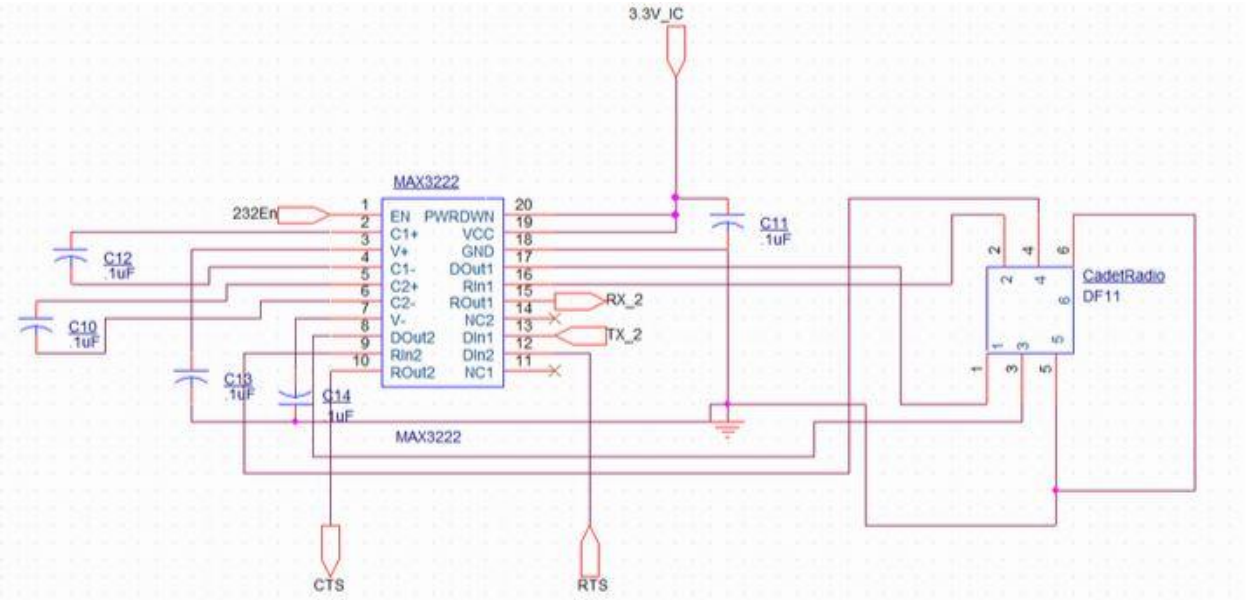

Figure 8: RS-232 schematic

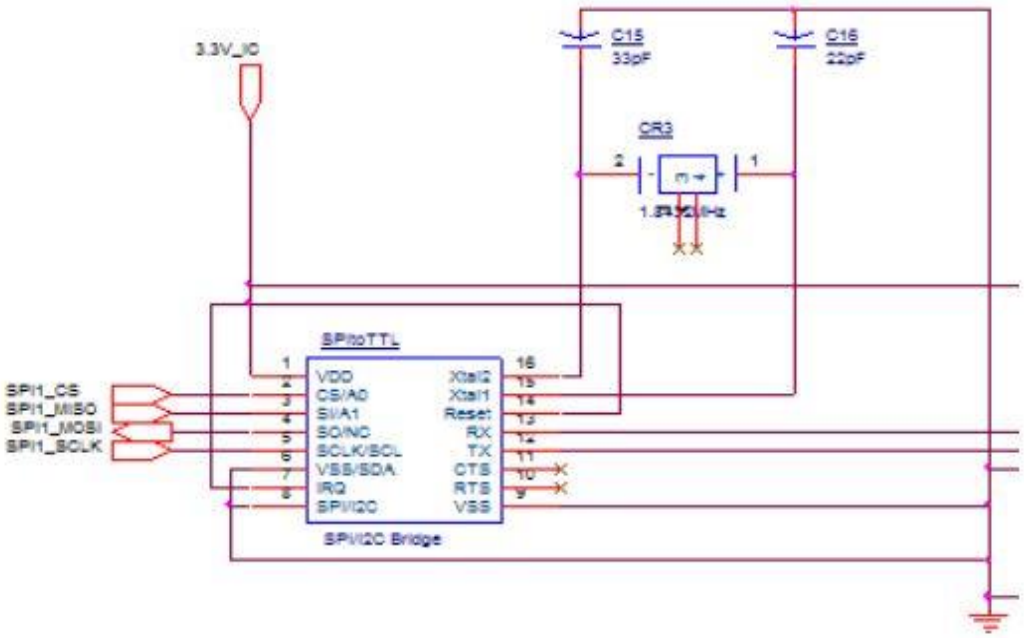

Figure 9: SPI to UART schematic. Schematic is cropped for additional focus on SPI.

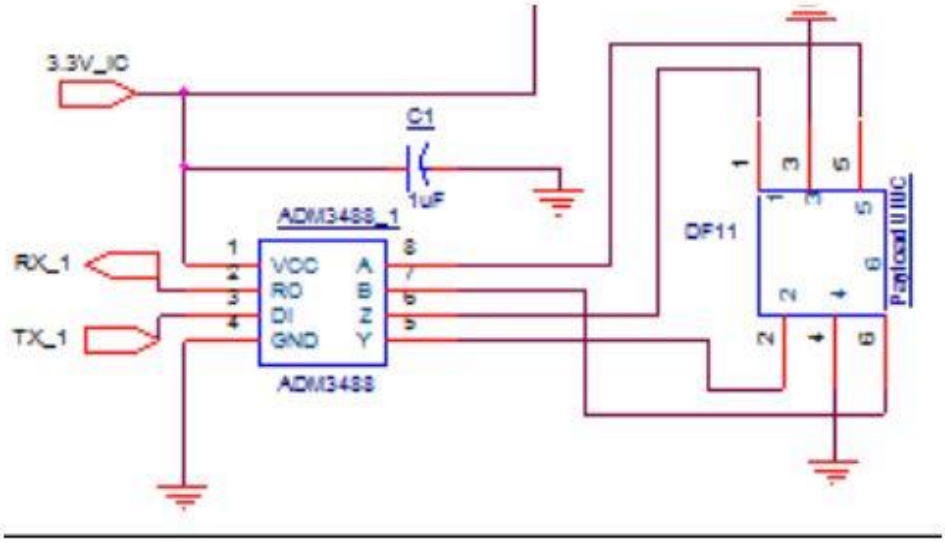

Figure 10: UART to RS-422 schematic; schematic is cropped for clarity purposes.

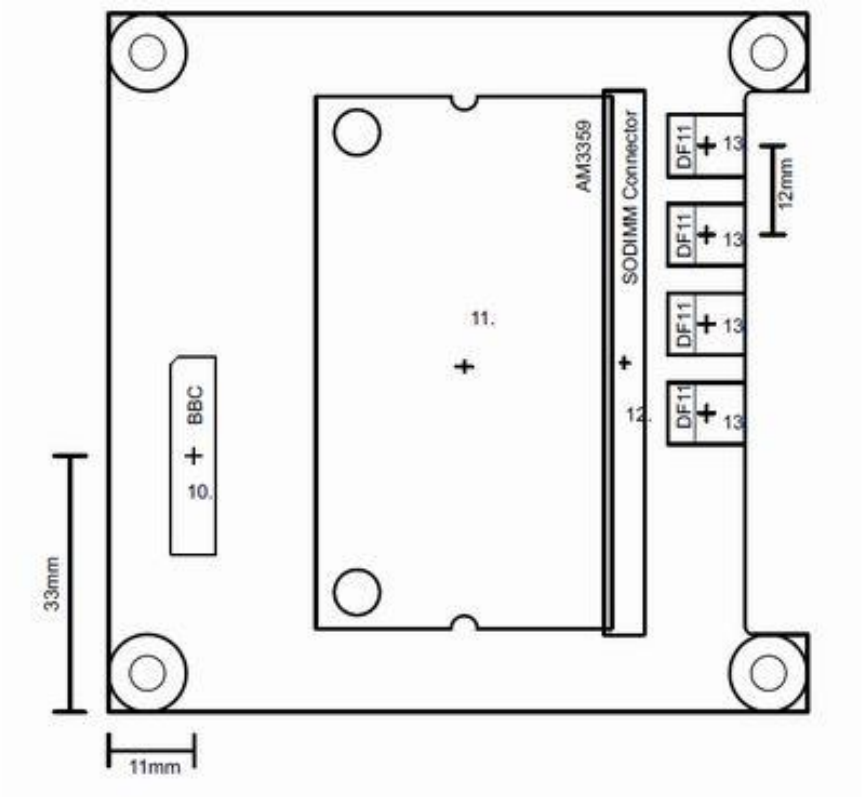

Figure 11: Mechanical Drawing showing the specific location of the Backbone Connector (BBC). Author: Dan Brackmann

APPENDIX C: Pinouts

DF11 Connector[14]:

UIUC and VT Payloads:

Pin	Function
1	TX-
2	TX+
3	GND
4	GND
5	RX+
6	RX-

Lithium Radio:

Pin	Function
1	TX-
2	TX+
3	RX-
4	Enable
5	RX+
6	GND

Cadet Radio:

Pin	Function
1	TX
2	RX
3	RTS
4	CTS
5	GND
6	GND

Notes: DF11's pin one is the located on the inner pins when looking downward at the board. It is the bottom and inmost pin. Odd pins are the inner pins, even are the outer ones.

Function refers to the signals coming from the transceiver on the C&DH board. See the schematics in Appendix B for clarification.

[14] See Appendix F for a mechanical diagram of this connector.

Backbone Connector:

Backbone Pin	Function
1, 3, 5, 7, 9, 11	3.3V C&DH
13, 15, 17, 19, 21, 23	Unregulated 7.7-9.6 Volts from Batteries
27	UART3_EN (GPIO pin on MitySOM module
29	UART3_RX on MitySOM module
31	UART3_TX on MitySOM module
33	TX_P on C&DH
35	TX_N on C&DH
37	RX_N on C&DH
38	UART0_TX on MitySOM module
39	RX_P on C&DH
40	UART0_RX on MitySOM module

Notes: Pins 33,35,37,39 are RS-422 connections on the transceiver that is on the C&DH board. Those pins connect to a transceiver on the Power Board. All other pins not listed are currently not being used for any power or communication circuitry

MitySOM module:

Connection	Thru	Protocol	Pin #	Signal
Debug port	Backbone connector	RS232	169	UART0_Tx
			171	UART0_Rx
UIUC payload	Harness thru DF11 connector	RS422	173	UART1_Tx
			175	UART1_Rx
CADET radio	Harness thru DF11 connector	RS232	183	UART2_Tx
			187	UART2_Rx
			177	UART2_RTS
			179	UART2_CTS
Bus hardware	Backbone connector	RS485	116	UART3_Tx
			118	UART3_Rx
			126	UART3_En
Powerboard	Backbone connector	RS422	132	UART4_Tx
			134	UART4_Rx
VT payload	Harness thru DF11 connector	RS422	122	UART5_Tx
			138	UART5_Rx
Lithium Radio	SPI to UART conversion	RS422	145	SPI1_CS
			193	SPI1_SCLK
			195	SPI1_MOSI
			197	SPI1_MISO
			114	Lithium_Enable
Memory	Traces	USB	131	USB0_DM
			133	USB0_DP
	Traces	USB	123	USB1_DM

Redundant memory			121	USB1_DP

Notes: 27 Pins total = 7 *data* signals thru backbone + 20 others. The SPI will need to be refigured because of the pin MUXing issue described earlier; there is also an enable pin to the Lithium Radio that is not connected as of right now.

APPENDIX D: Explanation of Testing Procedures

One script was implemented to verify that the communication from peripherals to the MitySOM Module is working correctly. These scripts shall be referred to as Test Script A and Test Script B.

Test Script A: This script is used for all communication tests except for the NAND Flash. That test will be done via an entirely separate script known as Test Script B. The basic concept is to use a USB port on a computer and send data through that port to the MitySOM Module, have the MitySOM Module echo that data back, and verify that it is the same data that was sent initially. This logic can be used for the USB, UART, and the RS422 transceivers. The only thing that changes is the type of converter that the computer uses to send the data. For example, testing the UART will require a small USB to UART adapter. We were able to transmit, but for receive, data for the RS422 and RS232 transceivers. However, we were successfully able to do a loopback test (what you send is what you receive) for the UART3 connection. Source code is provided in Appendix D. In addition, 24 hour testing can be used to verify the transmission error rates. The data analysis module can be used to come up with the relevant metrics.

Test Script B: This script is used for testing the NAND Flash circuitry. This script will be run on the MitySOM module itself. The idea with this script is it first writes data to the NAND Flash circuitry, then reads from that same location. After it accomplishes this, it verifies that the initial and final data is the same as the one that was initially sent. This test is done over the course of 24 hours to verify how many bytes were correctly stored and retrieved over all transactions. The data analysis module can be used to make the relevant comparisons. No source code is provided for this test because no memory tests were performed (the memory chip was lost in shipment).

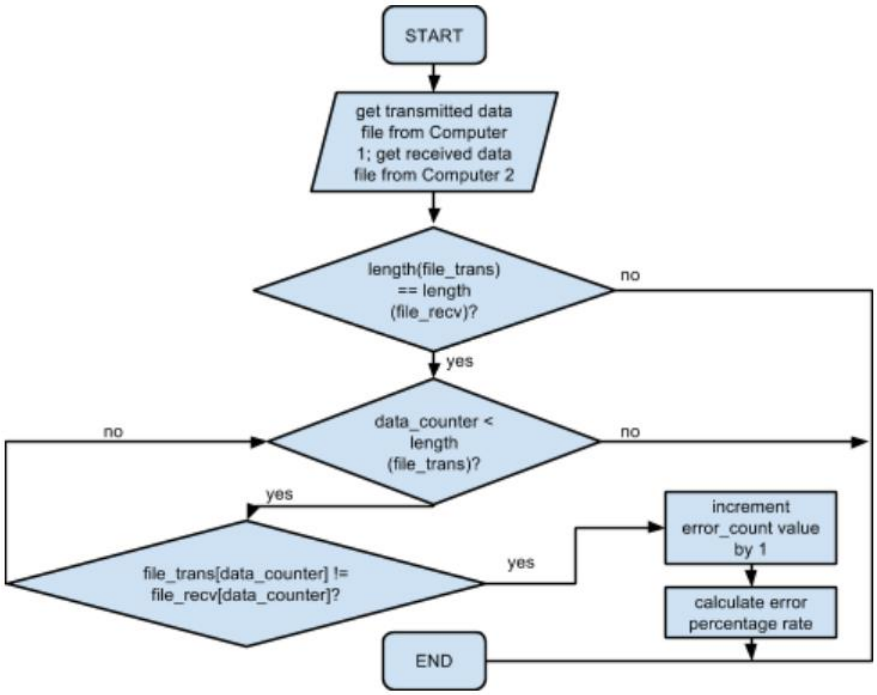

Figure 12: This flowchart depicts functionality for the data analysis module, as described above.

APPENDIX E: Source Code for Loopback Testing

```
// Written by C&DH board team on Dec 3, 2014 to make a UART3 verifier
// Latest version: Dec 2014, v1
// Sends text file across serial port for loopback testing

#include <stdio.h>
#include <stdint.h>
#include <stdlib.h>
#include <errno.h>
#include <termios.h>
#include <unistd.h>
#include <sys/ioctl.h>
#include <fcntl.h>
#include <errno.h>
#include <string.h>
#include <time.h>
#include <unistd.h>
#include "math.h"

// Global variables
int fd_port;
int ff_port;

int set_interface_attribs (int fd_port, int speed, int parity)
{
// Refer for explanation of options:
// www.cmrr.umn.edu/~strupp/serial.html#3_1

struct termios tty;

    memset (&tty, 0, sizeof tty);
    if (tcgetattr (fd_port, &tty) != 0)
    {
        printf ("error %d from tcgetattr\n", errno);
        return -1;
    }

    cfsetospeed (&tty, B115200);    // Output baud rate
    cfsetispeed (&tty, B115200);    // Input baud rate

    // Input options:
    tty.c_iflag &= ~(IGNBRK | BRKINT | PARMRK | ICRNL | INLCR | INPCK | ISTRIP | IXON);
    // Local options: select raw unprocessed input
    tty.c_lflag &= ~(ECHO | ECHONL | ICANON | IEXTEN | ISIG);

    // Output options:
    tty.c_oflag = 0;
    tty.c_oflag &= ~OPOST;  // Raw output

    // Control options:
    tty.c_cflag |= (CLOCAL | CREAD);    // Local line (don't change line owner) | Enable receiver
    tty.c_cflag &= ~PARENB;             // Disable parity bit
    tty.c_cflag &= ~CSTOPB;             // 1-stop bit (2 otherwise)
    tty.c_cflag &= ~CSIZE;              // Bit mask for data bits
    tty.c_cflag |= CS8;                 // 8-bit chars

    // Control characters:
    tty.c_cc[VMIN]  = 2;            // read blocks until atleast 1 byte received
    tty.c_cc[VTIME] = 0;            // 0.1 second timeout

    if (tcsetattr (fd_port, TCSANOW, &tty) != 0)
    {
```

```
        printf ("error %d from tcsetattr\n", errno);
        return -1;
    }
    return 0;
}

void pmtActions(void)
{
    int i, n_write, n_read;
    char TX[161];
    char RX[161];
    struct timeval timestamp;

    printf("Simulator started=======================================\n");

    char const* const fileName = "makela.txt"; /* should check that argc > 1 */
    FILE* file = fopen(fileName, "r"); /* should check the result */
    char line[161];
    while(1) {
        while (fgets(line, sizeof(line), file)) {
            /* note that fgets don't strip the terminating \n, checking its
               presence would allow to handle lines longer that sizeof(line) */
            n_write = write(fd_port, line, strlen(line));
            n_read = read(fd_port, RX, n_write);
           printf("%s", line);
       }
    }
    return;
}

int main(void)
{
    char *portname = "/dev/ttyO3";

    fd_port = open (portname, O_RDWR | O_NOCTTY | O_SYNC);
    if (fd_port < 0)
    {
            printf ("Error %d opening %s: %s", errno, portname, strerror(errno));
            return;
    }
    else printf ("Serial port opened successfully\n");

    set_interface_attribs (fd_port, B115200, 0);  // set speed to 115,200 bps, 8n1 (no parity)

    while(1) pmtActions();

    return 0;
}
```

APPENDIX F: Additional Diagrams

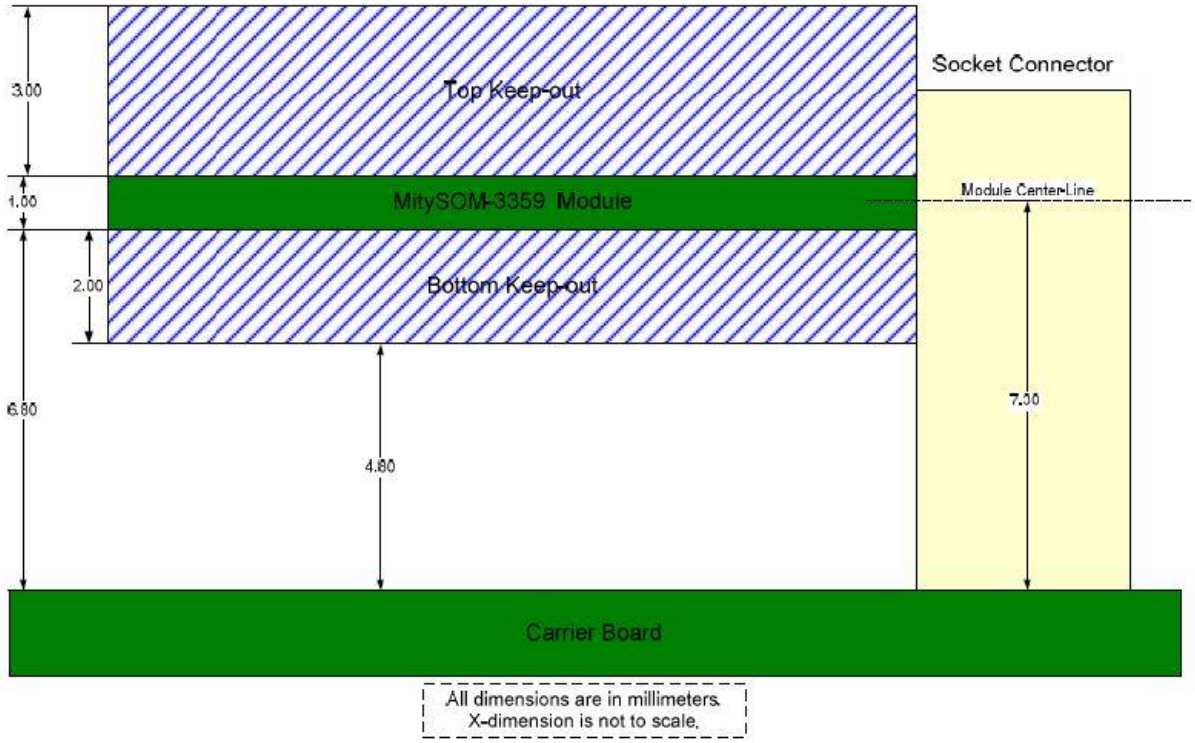

Figure 13: Diagram outlining the Keep-out areas for the MitySOM Module. Note that the connector shown is not the one is used; a smaller height (5.2 mm) connector is used instead. This image was taken from the *MitySOM-335x Carrier Board Design Guide*, a pdf on the Critical Link website. (www.criticallink.com)

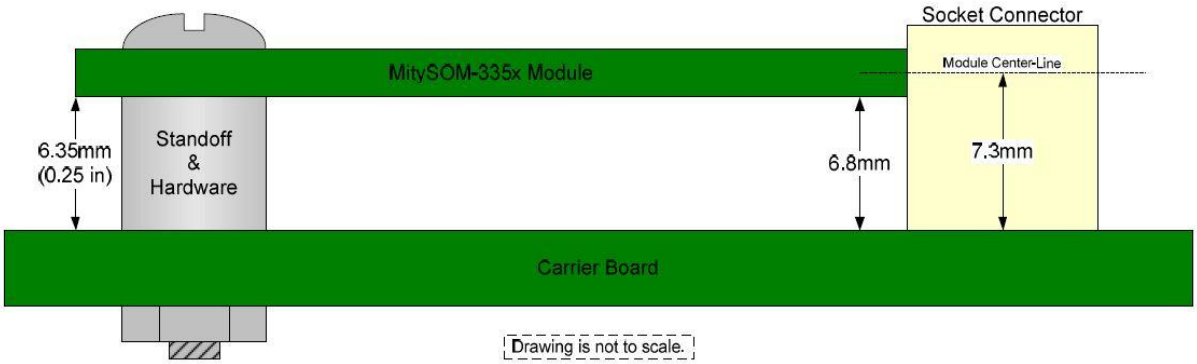

Figure 14: Diagram of how the MitySOM Module will be secured to the C&DH board. Note that the socket connector used is not 9.2 mm high; instead it is 5.2 mm. This image was taken from the *MitySOM-335x Carrier Board Design Guide*, a pdf on the Critical Link website. (www.criticallink.com)