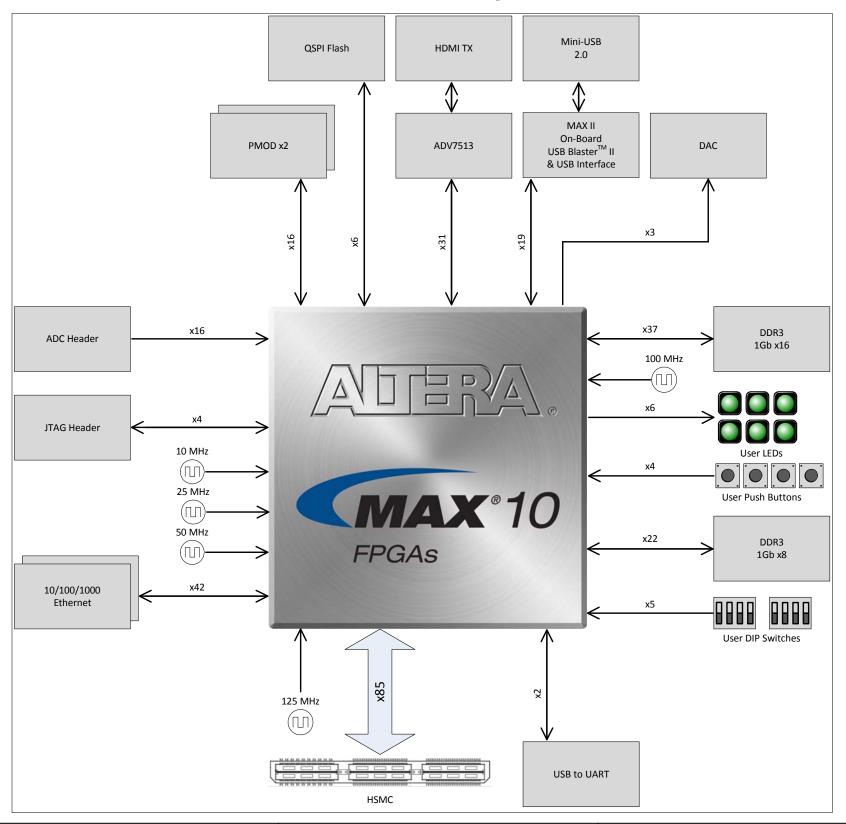
#### NOTES:

1. Project Drawing Numbers: Raw PCB Gerber Files PCB Design Files Assembly Drawing Fab Drawing

100-0321401- C1 110-0321401- C1 120-0321401- C1 130-0321401- C1 140-0321401- C1 Schematic Drawing PCB Film 150-0321401- C1 160-0321401- C1 Bill of Materials 170-0321401- C1 180-0321401- C1 Schematic Design Files Functional Specification 210-0321401- C1 PCB Layout Guidelines 220-0321401- C1 Assembly Rework

# **Pre-Release Schematic** DO NOT COPY

## **MAX 10 Development Kit Board**

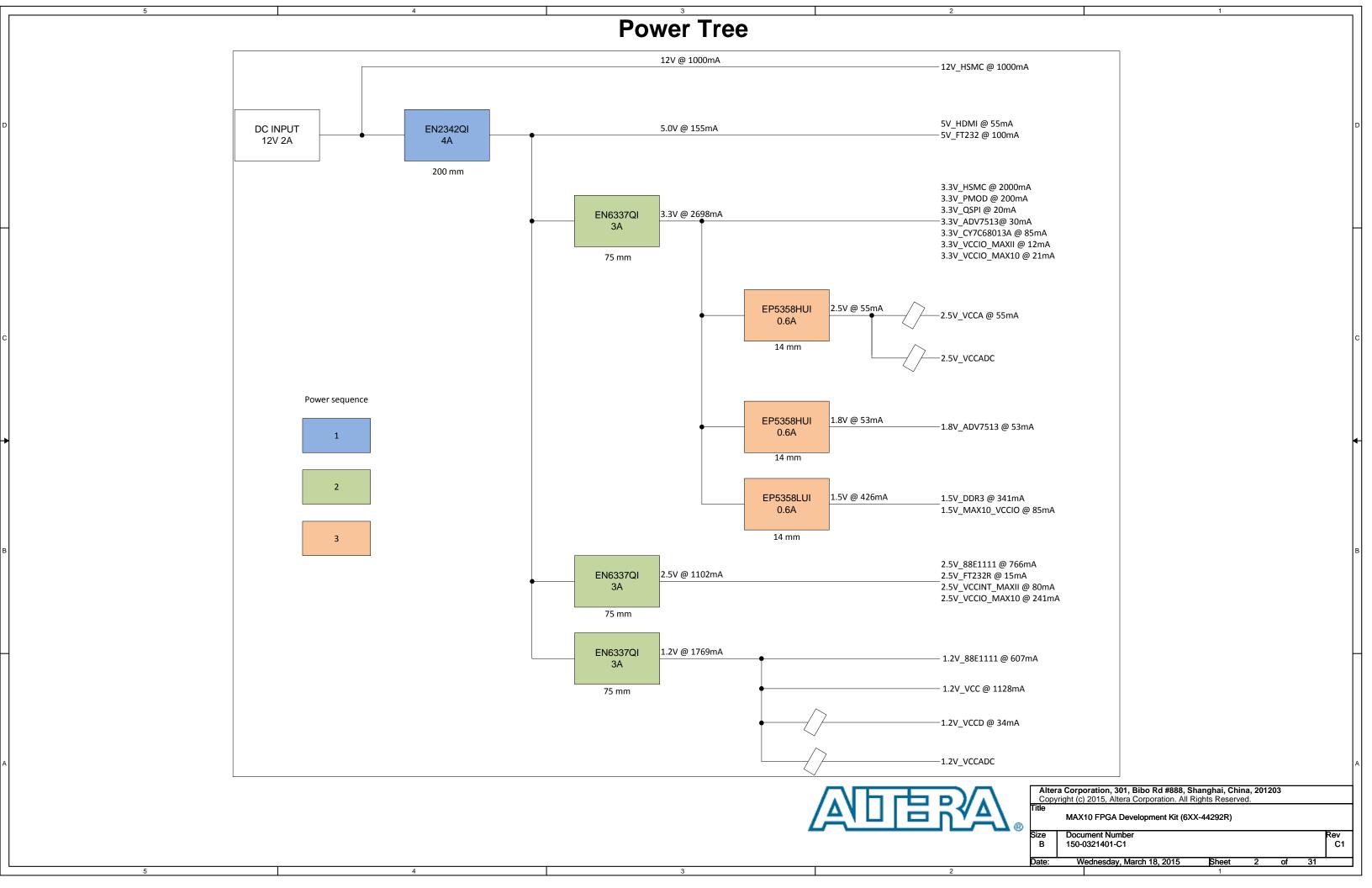


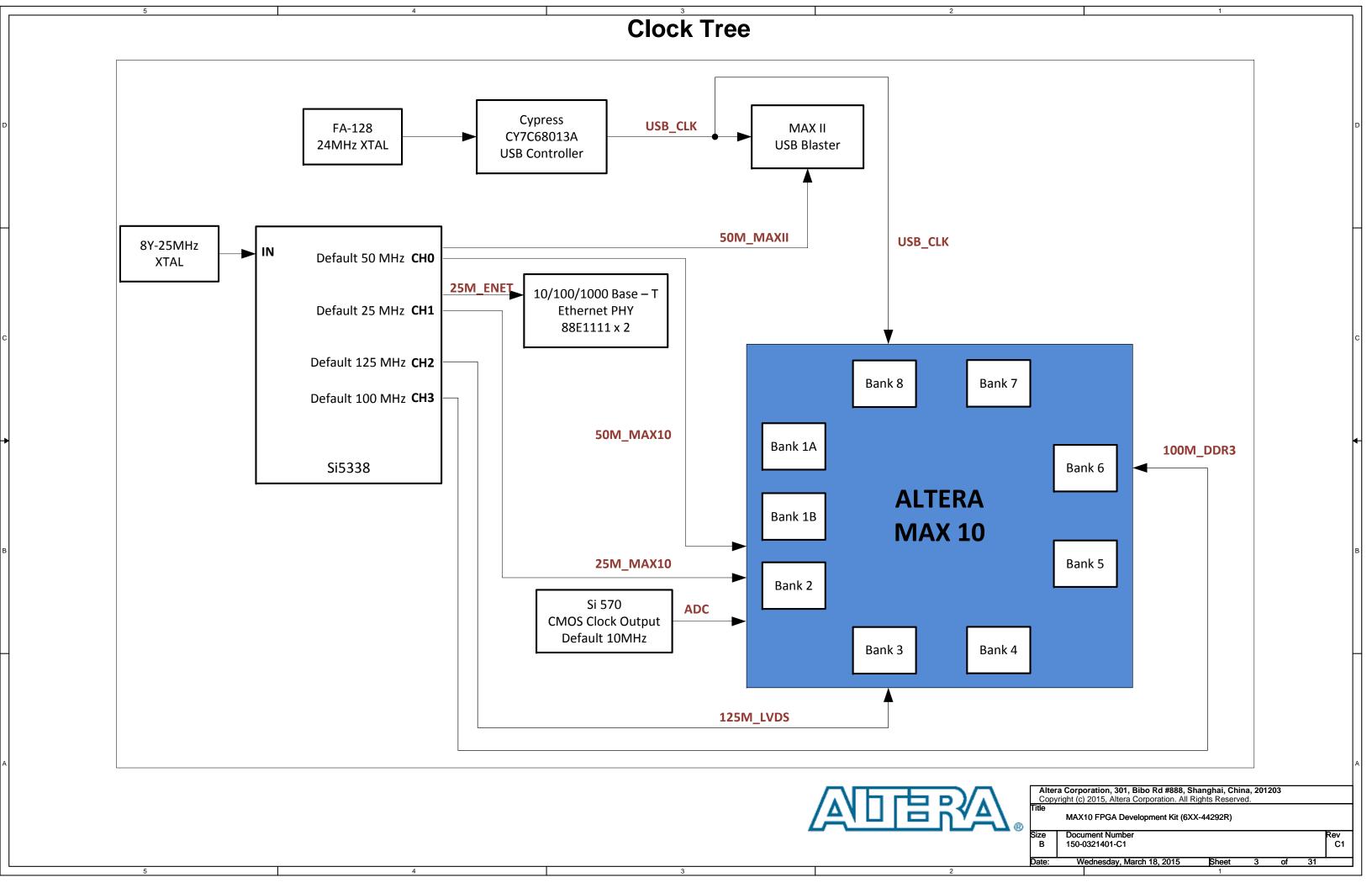
REV	DATE	PAGES	DESCRIPTION
Α	20 May 2014	All	INITIAL REVISION A RELEASE
В	2 Sep 2014	6	Swap pin AA21 with AA22
	•	7	Swap pin D5 with C3, and E8 with C6
		23	Change resistor value, R44 to 10K, R106 to 1K, R99 to 2K, R100 to 1K, R104 to 1K
		24	SW3 pin number change
		26 27	Add DNI capacitor, C70 and C166
	24 Sep 2014	1	Add functional diagram
	•	24	Change resistor value, R169 to 10K
	26 Jan 2015	All	Update notes for release version
C	17 Mar 2015	6	Swap pin F20 with D19, F21 with C20, F18 with A21, and E19 with B20
		10	Add resistors R303, R304, R305, R306, R80, R81, C355
		13	Add resistors R307
		9 & 23	Update the net name from BOOT SEL to CONFIG SEL
		22 & 23	Update the net name from MAX10 BYPASSn to VTAP BYPASSn

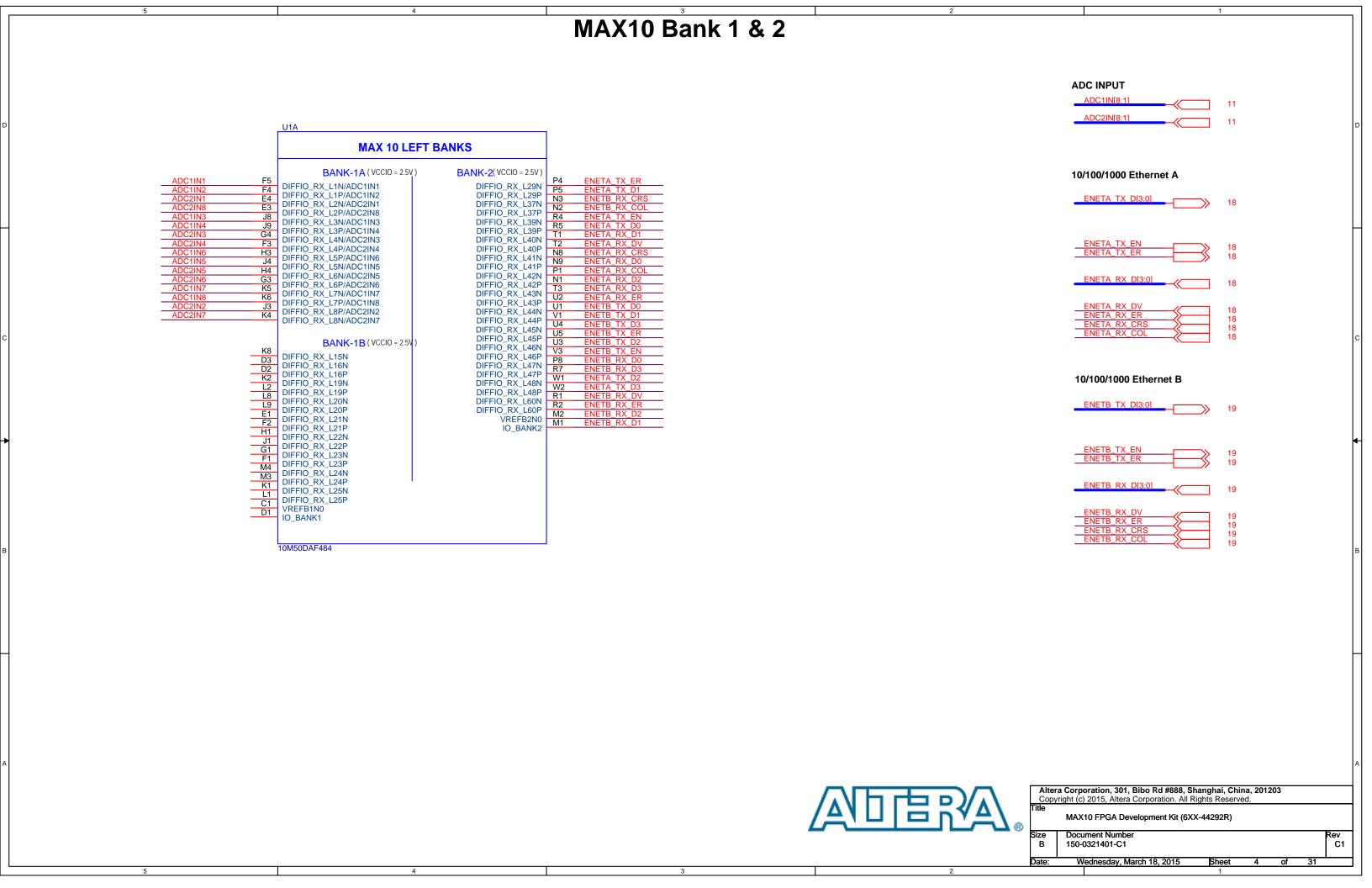
PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History	/ 30	MAX10 Ground
2	Power Tree	31	Decoupling
3	Clock Tree		
4	MAX10 Bank 1 & 2		
5	MAX10 Bank 3 & 4		
6	MAX10 Bank 5 & 6		
7	MAX10 Bank 7 & 8		
8	MAX10 Configuration		
9	MAX10 Clocks		
10	PLL		
11	ADC Filter		
12	DAC		
13	DDR3 SDRAM		
14	QSPI FLASH		
15	HSMC Port		
16	GPIO, PMOD		
17	HDMI		
18	10/100/1000 Ethernet A		
19	10/100/1000 Ethernet B		
20	USB to UART		
21	On-Board USB Blaster II-1		
22	On-Board USB Blaster II-2		
23	LED, User IO, Connector		
24	Power1		
25	Power2		
26	Power3		
27	Power4		
28	Power5		
29	MAX10 Power		



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## **MAX10 Bank 3 & 4**

		MAX 10 BOTTOM BANKS			
		<b>BANK-3</b> ( VCCIO = 2.5V )	<b>BANK-4</b> ( VCCIO = 2.5V )		
HSMC D0	Y7			W11	HSMC_RX_D_N13
HSMC D1	Y8	DIFFIO_RX_B10N	DIFFIO_RX_B25N	Y11	HSMC RX D P13
HSMC D2	AB2	DIFFIO_RX_B10P	DIFFIO_RX_B25P	AB10	HSMC_RX_D_N14
HSMC D3	AB3	DIFFIO_RX_B12N	DIFFIO_RX_B27N	AB11	HSMC_RX_D_P14
HSMC RX D N6	Y3	DIFFIO_RX_B12P	DIFFIO_RX_B27P	AB12	HSMC RX D N15
HSMC RX D P6	Y4	DIFFIO_RX_B14N	DIFFIO_RX_B29N	AB13	HSMC RX D P15
HSMC_RX_D_N7	AA5	DIFFIO_RX_B14P	DIFFIO_RX_B29P	W12	HSMC_RX_D_N8
HSMC_RX_D_P7	AB5	DIFFIO_RX_B17N	DIFFIO_RX_B35N	W13	HSMC_RX_D_P8
HSMC_RX_D_N5	AB6	DIFFIO_RX_B17P	DIFFIO_RX_B35P	AA14	HSMC_RX_D_N9
HSMC_RX_D_P5	AB7	DIFFIO_RX_B19N	DIFFIO_RX_B38N	AB15	HSMC_RX_D_P9
HSMC_RX_D_N3	AA8	DIFFIO_RX_B19P	DIFFIO_RX_B38P	AA15	HSMC_RX_D_N10
HSMC_RX_D_P3	AB8	DIFFIO_RX_B21N	DIFFIO_RX_B40N	Y16	HSMC_RX_D_P10
HSMC_RX_D_N4	AA9	DIFFIO_RX_B21P DIFFIO_RX_B23N	DIFFIO_RX_B40P DIFFIO_RX_B42N	AB16	HSMC_RX_D_N11
HSMC_RX_D_P4	AB9			AA16	HSMC_RX_D_P11
HSMC_RX_D_N0	V4	DIFFIO_RX_B23P DIFFIO_RX_B2N	DIFFIO_RX_B42P DIFFIO_RX_B44N	AB19	HSMC_RX_D_N16
HSMC_RX_D_P0	V5	DIFFIO_RX_B2N DIFFIO RX B2P	DIFFIO_RX_B44N DIFFIO_RX_B44P	AB20	HSMC_RX_D_P16
HSMC_RX_D_N1	Y1	DIFFIO_RX_B4N	DIFFIO RX B46N	AA19	HSMC_SDA
HSMC_RX_D_P1	Y2	DIFFIO_RX_B4N	DIFFIO_RX_B46N DIFFIO_RX_B46P	Y18	HSMC_SCL
HSMC_RX_D_N2	AA1	DIFFIO_RX_B6N	DIFFIO RX B50N	AB21	HSMC_CLK_IN_N1
HSMC_RX_D_P2	AA2	DIFFIO RX B6P	DIFFIO RX B50P	AA20	HSMC_CLK_IN_P1
ENET_MDIO	Y5	DIFFIO_RX_B8N	DIFFIO RX B58N	AB17	HSMC_RX_D_N12
ENET_MDC	Y6	DIFFIO RX B8P	DIFFIO RX B58P	AB18	HSMC_RX_D_P12
HSMC_TX_D_N7	W9	DIFFIO TX RX B11N	DIFFIO TX RX B24N	V11	HSMC_TX_D_N13
HSMC_TX_D_P7	W10	DIFFIO_TX_RX_B11P	DIFFIO_TX_RX_B24P	V12	HSMC_TX_D_P13
HSMC_TX_D_N3	W7 W8	DIFFIO TX RX B13N	DIFFIO TX RX B26N	R12	HSMC_TX_D_N14
HSMC_TX_D_P3		DIFFIO TX RX B13P	DIFFIO TX RX B26P	P12	HSMC_TX_D_P14
HSMC_TX_D_N6	R10	DIFFIO TX RX B15N	DIFFIO TX RX B28N	AA11	HSMC_TX_D_N15 HSMC_TX_D_P15
HSMC_TX_D_P6 HSMC_TX_D_N5	P10 AA6	DIFFIO_TX_RX_B15P	DIFFIO TX RX B28P	AA12 V13	HSMC_TX_D_P15  HSMC_TX_D_N8
HSMC_TX_D_NS	AA7	DIFFIO_TX_RX_B16N	DIFFIO_TX_RX_B34N	W14	HSMC TX D P8
HSMC_TX_D_P3	W5	DIFFIO TX RX B16P	DIFFIO TX RX B34P	R13	HSMC CLK OUT N1
HSMC_TX_D_N2	W6	DIFFIO_TX_RX_B1N	DIFFIO_TX_RX_B36N	P13	HSMC_CLK_OUT_P1
HSMC_TX_D_F2	Y10	DIFFIO_TX_RX_B1P	DIFFIO_TX_RX_B36P	Y13	HSMC_CLK_COT_FT
HSMC_TX_D_P4	AA10	DIFFIO_TX_RX_B22N	DIFFIO_TX_RX_B37N	Y14	HSMC_TX_D_P9
HSMC TX D N1	U6	DIFFIO_TX_RX_B22P	DIFFIO_TX_RX_B37P	V14	HSMC CLK OUT N2
HSMC TX D P1	U7	DIFFIO_TX_RX_B3N	DIFFIO_TX_RX_B39N	W15	HSMC CLK OUT P2
HSMC TX D N0	W4	DIFFIO_TX_RX_B3P	DIFFIO_TX_RX_B39P	U15	HSMC_TX_D_N10
HSMC TX D P0	W3	DIFFIO_TX_RX_B5N	DIFFIO_TX_RX_B41N	V16	HSMC TX D P10
ENETA INTn	V7	DIFFIO_TX_RX_B5P	DIFFIO_TX_RX_B41P	AA17	HSMC TX D N16
ENETA RESETn	V8	DIFFIO_TX_RX_B7N	DIFFIO_TX_RX_B43N	Y17	HSMC TX D P16
ENETA_LED_LINK100	R9	DIFFIO_TX_RX_B7P	DIFFIO_TX_RX_B43P	V15	HSMC_TX_D_N11
ENETB_LED_LINK100	P9	DIFFIO_TX_RX_B9N	DIFFIO_TX_RX_B45N	W16	HSMC_TX_D_P11
ENETB_INTn	AA3	DIFFIO_TX_RX_B9P	DIFFIO_TX_RX_B45P	Y19	UART_RX
ENETB_RESETn	AB4	VREFB3N0	DIFFIO_TX_RX_B49N	W18	UART_TX
		IO_BANK3	DIFFIO_TX_RX_B49P	AA13	HSMC_CLK_OUT0
			VREFB4N0	AB14	HSMC_PRSNTn
			IO_BANK4		

HSMC_RX_D_P0 HSMC_RX_D_N0	R249 DNI
HSMC_RX_D_P1 HSMC_RX_D_N1	R250 DNI
HSMC_RX_D_P2 HSMC_RX_D_N2	R251 DNI
HSMC_RX_D_P3 HSMC_RX_D_P3	R252, DNI
HSMC_RX_D_P4 HSMC_RX_D_P4	R253 DNI
HSMC_RX_D_N4  HSMC_RX_D_P5 HSMC_RX_D_N5	R254 DNI
HSMC_RX_D_P6	R255 DNI
HSMC_RX_D_N6 HSMC_RX_D_P7	R256, _ DNI
HSMC_RX_D_N7 HSMC_RX_D_P8	R257
HSMC_RX_D_P8 HSMC_RX_D_N8 HSMC_RX_D_P9	R258 A ADNI
HSMC_RX_D_N9	
HSMC_RX_D_P10 HSMC_RX_D_N10	R259 DNI
HSMC_RX_D_P11 HSMC_RX_D_N11	R260 DNI
HSMC_RX_D_P12 HSMC_RX_D_N12	R261 DNI
HSMC_RX_D_P13 HSMC_RX_D_N13	R262 DNI
HSMC_RX_D_P14 HSMC_RX_D_N14	R263 DNI
HSMC_RX_D_P15 HSMC_RX_D_N15	R264 DNI
HSMC_RX_D_P16 HSMC_RX_D_N16	R265 DNI

Notes: R249-R265 are 100 ohm termination resistors for LVDS RX.

#### **HSMC** Interface

•	HSMC_D[3:0]	<b>≪</b> >>>	15
	HSMC RX D P[16:0]	-«——	15
	HSMC_RX_D_N[16:0]	~	15
	HSMC_TX_D_P[16:0]		8,15
	HSMC_TX_D_N[16:0]		8,15
	HSMC_CLK_IN_P[2:1]		8,15
	HSMC CLK IN N[2:1]	<u> </u>	8,15
	HSMC_CLK_OUT_P[2:1]		15
	HSMC CLK OUT N[2:1]		15
	HSMC_CLK_IN0		8,15
	HSMC_CLK_OUT0		15
	HSMC_PRSNTn		15,22
	HSMC_SDA		15
	HSMC_SCL		15
		//	10

#### Ethernet

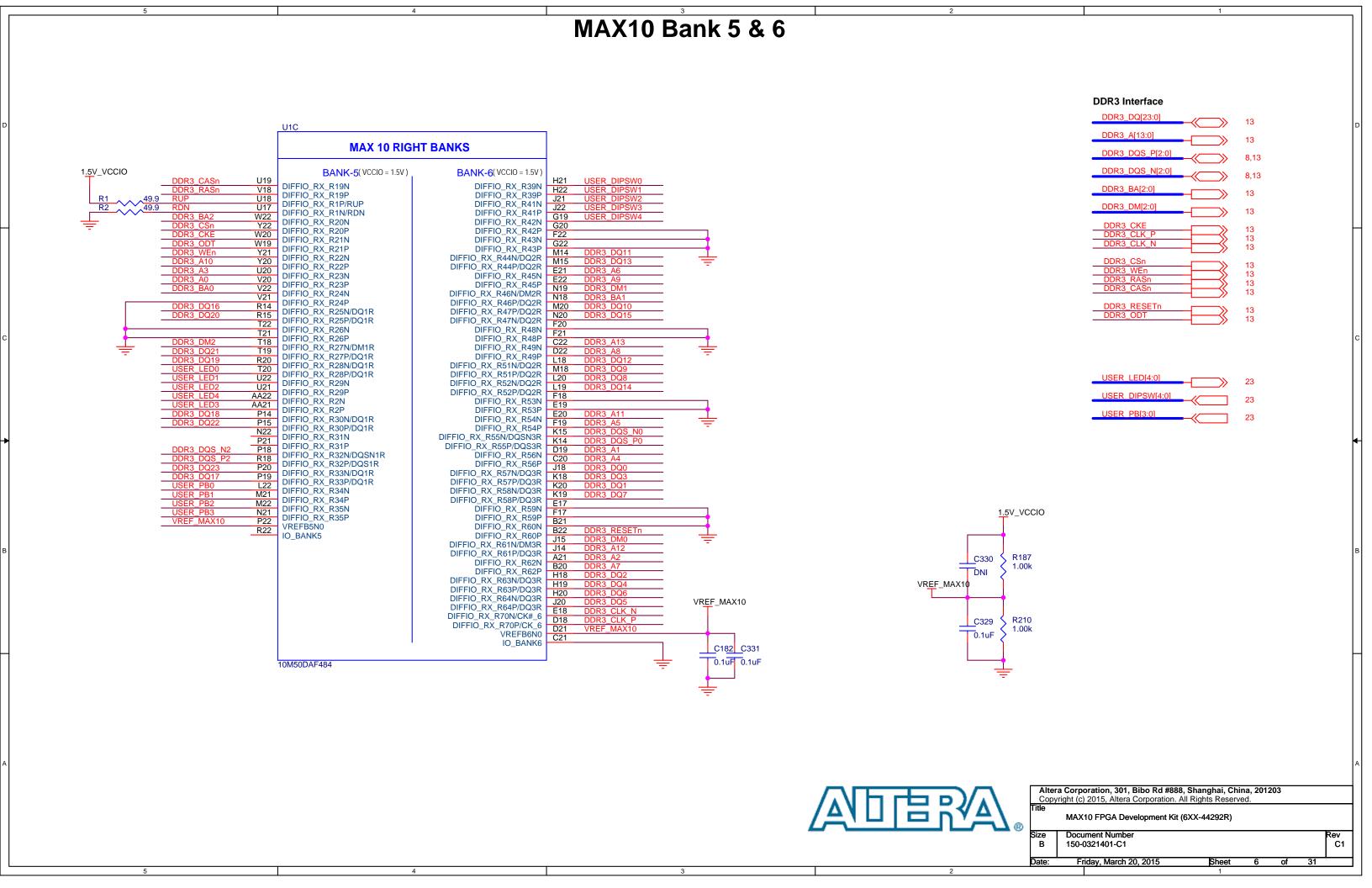
ENET_MDC	18,19 18,19
ENETA_INTn ENETA_RESETn	18 18
ENETB_INTn ENETB_RESETn	19 19
ENETA_LED_LINK100 ENETB_LED_LINK100	18 19

#### UART

UART_RX	//	20
UART_TX		20



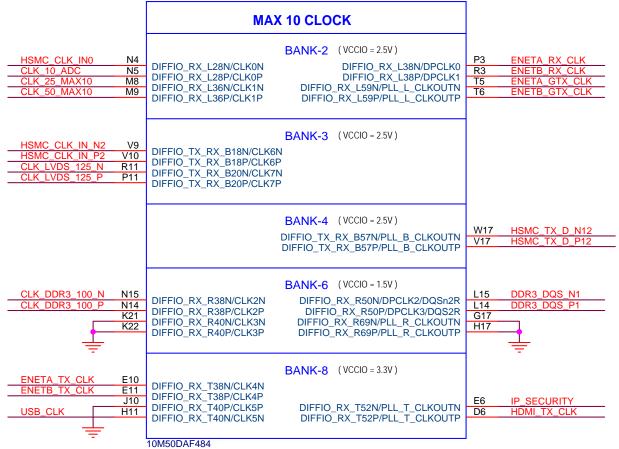
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Title	MAX10 FPGA Development Kit (6)	(X-44292R)				
Size B	Document Number 150-0321401-C1					Rev C1
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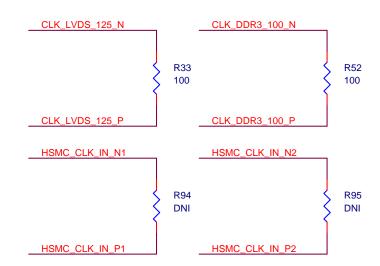


#### **MAX10 Bank 7 & 8 HDMI TX** HDMI\_TX\_D[23:0] HDMI\_TX\_HS HDMI\_TX\_VS **MAX 10 TOP BANKS** HDMI\_TX\_DE \_\_HDMI\_TX\_INT **BANK-7**( VCCIO = 3.3V ) **BANK-8**( VCCIO = 3.3V ) PMODA\_IO0 DIFFIO\_RX\_T10N DIFFIO\_RX\_T39N HDMI\_SDA DIFFIO\_RX\_T10P DIFFIO\_RX\_T39P PMODA IO: DIFFIO\_RX\_T41N B7 DIFFIO\_RX\_T15N PMODA IC HDMI\_SCL 17 DIFFIO\_RX\_T15P DIFFIO\_RX\_T41P A16 DIFFIO\_RX\_T16N DIFFIO\_RX\_T42P DIFFIO\_RX\_T43N A5 DIFFIO\_RX\_T16P DIFFIO\_RX\_T17N DIFFIO\_RX\_T43P **PMOD** DIFFIO\_RX\_T44N A2 DIFFIO RX T17P DIFFIO\_RX\_T45P DIFFIO\_RX\_T45N B3 B4 DIFFIO\_RX\_T18N DIFFIO\_RX\_T18P B14 DIFFIO RX T19N PMODB\_IO[7:0] A14 DIFFIO\_RX\_T46N B5 DIFFIO\_RX\_T19P E15 DIFFIO\_RX\_14/r DIFFIO\_RX\_T47N E8 D5 DIFFIO RX T1N DIFFIO RX T1P E13 **MAX10 USB INTERFACE** DIFFIO RX T20N DIFFIO\_RX\_T49N C5 DIFFIO RX T20P 22 DIFFIO RX T21P DIFFIO RX T49P DIFFIO\_RX\_T51N B2 DIFFIO RX T21N USB\_ADDR[1:0] DIFFIO\_RX\_151F DIFFIO\_RX\_T53N C3 D7 22 DIFFIO\_RX\_T22N DIFFIO\_RX\_T22P USB FULL A12 DIFFIO RX T23N VREFB8N0 C6 22 22 DIFFIO\_RX\_T23P DIFFIO\_RX\_T24N IO\_BANK8 22 DIFFIO\_RX\_T24P DIFFIO\_RX\_T25N USB\_RESETn USB\_OEn DIFFIO\_RX\_T25P C10 22 22 DIFFIO\_RX\_T26N DIFFIO\_RX\_T26P DIFFIO\_RX\_T27N DIFFIO\_RX\_T27P H12 DIFFIO\_RX\_T28N B8 DIFFIO\_RX\_T28P **QSPI FLASH** DIFFIO\_RX\_T31N DIFFIO\_RX\_T31P D17 DIFFIO\_RX\_T2N DIFFIO\_RX\_T2P \_\_QSPI\_CLk 14 DAC\_SYNC DAC\_SCLK DAC\_DIN HDMI\_TX\_D6 HDMI\_TX\_D3 DIFFIO\_RX\_T30N DIFFIO\_RX\_T30P QSPI\_CSn DIFFIO\_RX\_T29P A8 DIFFIO\_RX\_T29N DIFFIO\_RX\_T5N HDMI\_TX\_D19 HDMI\_TX\_D19 HDMI\_TX\_D20 HDMI\_TX\_D18 HDMI\_TX\_D18 HDMI\_TX\_D12 HDMI\_TX\_D12 HDMI\_TX\_D14 HDMI\_TX\_INT HDMI\_SDA DIFFIO\_RX\_T5P DAC DIFFIO\_RX\_T6N DIFFIO\_RX\_T6P \_\_DAC\_SYNC 12 DIFFIO\_RX\_T7N C18 DIFFIO RX T7P DAC\_SCLK 12 DIFFIO\_RX\_T8N A20 DIFFIO RX T8P DAC\_DIN DIFFIO\_RX\_T9N 12 D15 DIFFIO\_RX\_T9P VREFB7N0 \_\_JTAG\_SAFE HDMI\_TX\_D23 A15 IO\_BANK7 22 10M50DAF484 Altera Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2015, Altera Corporation. All Rights Reserved MAX10 FPGA Development Kit (6XX-44292R)

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HDMI TX HDMI_TX_CLK	> 17
HSMC_TX_D_N12 HSMC_TX_D_P12	> 15 > 15
HSMC CLK IN P[2:1]  HSMC CLK IN N[2:1]	] 15 ] 5,15 ] 5,15
Ethernet  ENETA_RX_CLK  ENETB_RX_CLK  ENETA_TX_CLK  ENETB_TX_CLK  ENETB_GTX_CLK  ENETB_GTX_CLK	18 19 18 19 19 18
DDR3 DDR3_DQS_N1 DDR3_DQS_P1	> 13 > 13
Prom PLL CLK_10_ADC CLK_50_MAX10	
DDR3_DQS_N1 DDR3_DQS_P1  From PLL CLK_10_ADC	13
From PLL CLK_10_ADC CLK_50_MAX10 CLK_25_MAX10 CLK_LVDS_125_P	13 10 10 10 10 10 10 10 10 10 10 10 10 10



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Size	Document Number					Rev
В	150-0321401-C1					C1
Date:	Thursday, March 19, 2015	Sheet	8	of	31	

