Aarav Vidhawan

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EDUCATION

University Of California San Diego — **San Diego, CA**
Bachelor of Science, Computer Engineering **| GPA: 3.85 | Provost Honors** — **2022-Present**
Relevant Coursework: Computer Architecture**,** Digital Systems, Advanced Digital Design Project, Digital Circuits, Linear Algebra, Intro to Machine Learning, Computer Organization, Data Structures & Algorithms, Operating Systems.

University Of California San Diego — **San Diego, CA**
Master of Science, Computer Engineering - Accepted for BS/MS — **Starting 2026**

La Martiniere For Boys — **Kolkata, India**
- **Completed Grade 12, June 2022 ; ISC Result: 97.25%** — **2012-2022**
- **Completed Grade 10, June 2020; ICSE Result: 94.80%**

SKILLS

Hardware Design & Verification: SystemVerilog, Verilog, Quartus, Modelsim, Vivado, PSpice/LTSpice, Virtuoso
Embedded/Firmware: C, C++, Arduino, FreeRTOS, ESP32, STM32, CH32V, SPI, I2C, USART.
Software: Python, Java, JavaScript, HTML, CSS
Tools: GitHub, VSCode, KiCAD, JIRA/Confluence, Lab Gear (Multimeter, Oscilloscope, Soldering Iron)

EXPERIENCE

CSE Department Tutor | Problem Solving, Communication, ARM, C — **San Diego, CA**
CSE 141/L Tutor - Computer Architecture — **June, 2025 – Present**
- Led weekly sections and office hours for **~50** undergrads. Prepared targeted problem sets on **ARMv8** pipelines, hazards, caches and memory models. Responded to **~40** forum questions, with avg **<2** hrs response time.
- Co-designed and proctored midterms and final. Graded **~80** submissions with a designed rubric.
- 1 on 1 discussion in Office Hours led to an average of **~15** point increase on Midterm 2 and **~10%** on the Final.
- Guided **100+ students** in **CSE 141L** through designing custom ISAs and single-cycle CPUs in SystemVerilog. Debugged datapath and control logic, improving synthesis success and comprehension of microarchitecture.

VLSI System Design | CH32V, Arduino, Assembly, C++ — **Bangalore, India**
Research Intern — **October, 2024 – November, 2024**
- Profiled **CH32V RISC-V** instruction execution and branch/memory latencies; analyzed **50+ traces** and found **~12% stall overhead** from load dependencies and mispredictions. All simulation and debugging performed on **VirtualBox** on Win 11.
- Optimized assembly loops, removing redundant loads/stores, cutting execution cycles by **~10%** - preserving functionality.
- Built a **MacroPad proof-of-concept** using the VSDSquadron Mini, integrating display and dual-button firmware on CH32V

UCSD ITS - Information Technology Services | JavaScript, REACT, HTML, CSS, ServiceNow — **San Diego, CA**
Document And Case Management - Student Developer — **October, 2023 - June, 2024**
- Shipped **10+** production forms/workflows (Messaging Colab, Laptop Borrow Request, etc) used by **~3,000+** students and faculty, automation improvements cut manual handling from ~**30** min to ~**15** min per request(**-50%**).
- Built **3+** Analysis dashboards using ServiceNow's experience builder. Required **25+** hours of coursework.
- Built QA scripts, and performed over **100+** E2E tests of other developer's work.

TRITONS RCSC - RoboCup Soccer | PSpice, LTSpice, Circuit Design, Arduino — **San Diego, CA**
Embedded Team Member — **October, 2023 - June, 2024**
- Designed and simulated linear and chip kick circuits for solenoid actuation, validating charge timing and energy delivery.
- Built **STM32**-based activation circuitry for the solenoid system, ensuring reliable **<20 ms** trigger response during tests.

TRITON SolarCar | — **San Diego, CA**
Battery Team Member — **October, 2023 - June, 2024**
- Configured and tuned a 3-phase BLDC motor controller, calibrating pedal and throttle mapping for smooth torque control.
- Integrated and tested pedal feedback with the drive system, ensuring stable current draw and responsive motor behavior.

PROJECTS

MacroPad - Project Lead | C++, KiCAD, LTSpice, Team Management
- Designed a modular ESP32 MacroPad with **9**, **64x64 RGB OLEDs**, mechanical keys, and **2** rotary encoders.
- Seamless desktop activation via custom, cross-platform Qt companion application. Written in C++ and Objective C.
- Implemented using serial protocol supporting profile switch < **50 ms**, and activation latency <**40 ms.**
- Designed driver circuit for the **SSD1357z** controller, integrated into custom PCB for the keyboard.
- Led a **9-person** team, sprint cadence, code review and integration.

Sora v1.0 - Self Designed ISA and CPU | SystemVerilog, Python, Quartus, ModelSim
- Authored a 9-bit ISA (16 instr, 2 addressing modes, load-store) with an 8-bit datapath. Wrote assembler in Python.
- Achieved Hamming Distance Calculation and **double precision** multiplication using only **9 bits**. Fastest execute in the class.
- Single-cycle, with RTL in SystemVerilog, simulated in ModelSim, and resource mapped on Cyclone-V using QuartusPrime.

Nachos Operating System | Java, C,
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Viterbi Encoder/Decoder | SystemVerilog, ModelSim, Quartus

- Implemented a convolutional encoder (rate 1/2, K=7) and a pipelined Viterbi decoder (ACS + traceback depth 35). Passed the end-to-end tx/rx testbench and verified min branch metric = 0 in a no-error channel.
- Built deterministic + random error-injection. Evaluated uncorrected errors across periodic/burst patterns up to a 1/16 rate.
- Synthesized on Cyclone V. Exported RTL-viewer/netlist and wrote state-transition/branch-metric notes for reproducibility.

Nixie Tube Clock | PSpice, LTSpice, Circuit Design, CH32V

- Designed a "Nixie Clock" using 1900s vacuum tubes. used **IN-14** tubes with **11-pin** cathode/anode interface.
- Built using VSDSquadron Mini, C++ on **CH32V** platform. Built in Alarm as well, standard alarm clock layout for setting.
- Added Time Zone changing functionality, 4 buttons for 4 pre-set Time Zones.

Ultrasonic Smart Clock | PSpice, LTSpice, Circuit Design, Arduino

- Designed a "Smart Clock" that used an ultrasonic sensor to detect if the user was still sleeping or not, and decided accordingly whether or not it should ring the alarm. Used a Metro M0 Express and CircuitPython to program it.
- Added "Stop" and "Snooze" functionality. Hope to add "Time Setting" functionality in the future.
- Used Onshape to construct 3D models of the Prototype, and EagleCAD to make the circuit diagrams for the clock.

LEADERSHIP/ EXTRACURRICULAR

HKN (Eta Kappa Nu) - CSE Department Chair (Events)

- Designed and hosted **10+** technical workshops, such as the Macro Key and I2C Workshop, and also ECE Depths Seminar.
- Communicated with **15+** professors and alumni for events, technical guidance, and project support.
- Participated in weekly meetings to facilitate the creation and execution of HKN events, ranging from professional to social.

Early Learning and Cognition Lab (UCSD) - Volunteer Engineer

- Designed a child-proof "blicket" machine used to study probabilistic vs deterministic learning in children under age 5.
- Built using an Arduino, 5 hall sensors, a rotary mode switch and an RGB LED. 3D designed enclosure as well.

HOBBIES

Vinyls, Gaming, Pool, Golf, Football(Soccer), Badminton, Coffee, Food, Music, Cars, Travel