GStreamer-integrated HLS-based JPEG Encoder for Edge FPGA SoCs

Yuri Guimaraes Pereira Primo da Silva[1], Shinya Honda[1], Sugako Otani[12], Masato Edahiro[1], Abraham Monrroy Cano[3]

[1]Nagoya University, [2]Renesas Electronics, [3]Map IV Inc.

Motivation

1. Lack of freely available image encoder designed for edge use case.
2.

Approach

Architecture

Results & Comparisons

Future Work

GStreamer-integrated HLS-based JPEG Encoder for Edge FPGA SoCs

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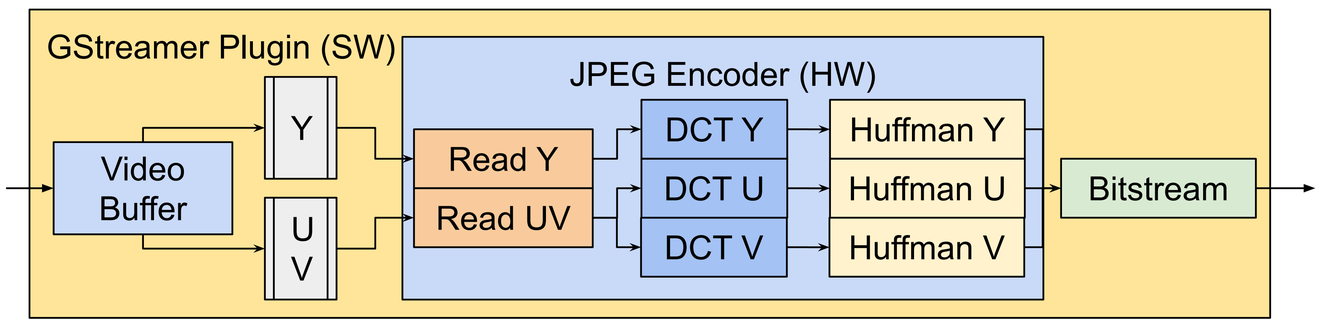
Approach

JPEG HLS Encoder

GStreamer Plugin Integration

Architecture



Experiments

Future Work

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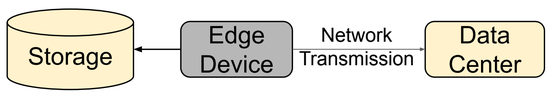
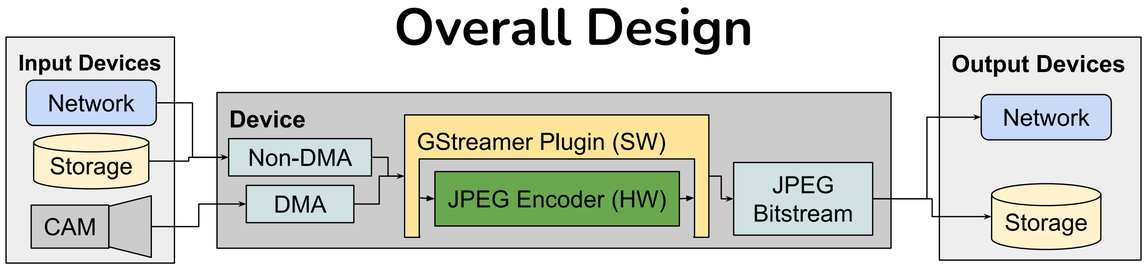


- Increasing importance of image encoding at the edge.
- **Image encoding** efforts have been mostly concentrated on accelerator cards.
- This research focuses on the implementation and integration aspect of an **HLS-based JPEG encoder** on Kria KV260 SoC [1] integrated with **GStreamer**.

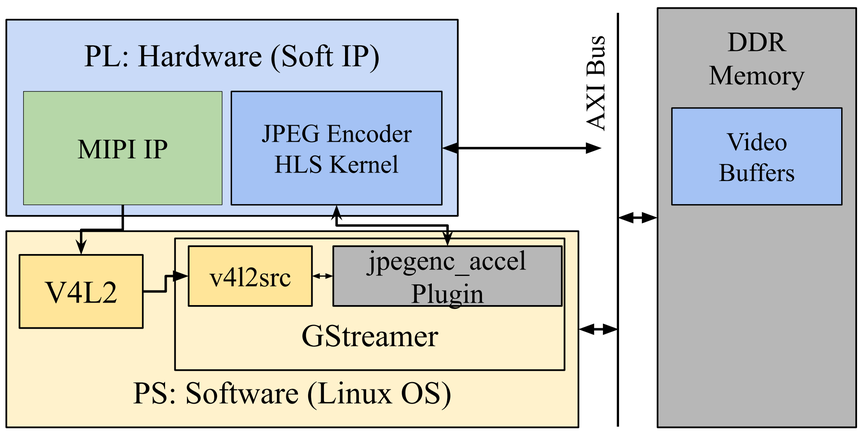
Approach

Overall Design



- HW JPEG Encoder implemented in *High-level Synthesis* [2].
- *GStreamer* plugin interfaces with encoder.
  - Allows for mix and matching of pipeline elements for arbitrary media processing.
  - Easy usage of DMA capabilities.

Top-level Block Design



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- Conventional JPEG algorithm design implemented C++ HLS.
- Streaming design:
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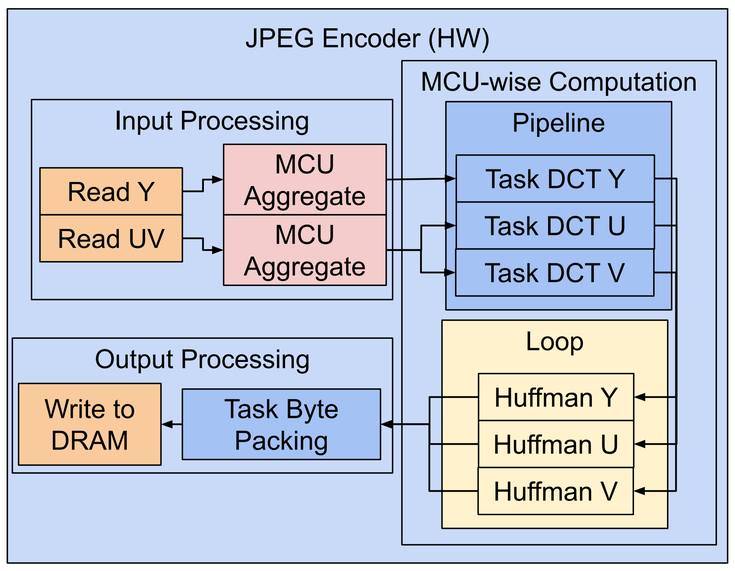
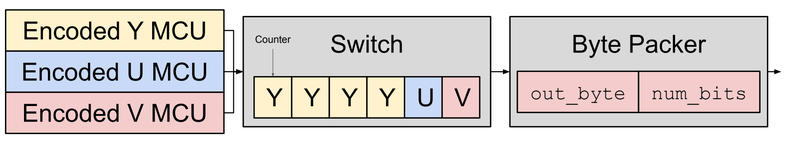
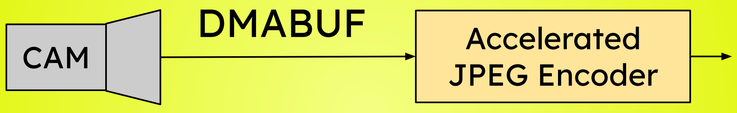




Pipelines

cam: From Camera Device (DMA-able)



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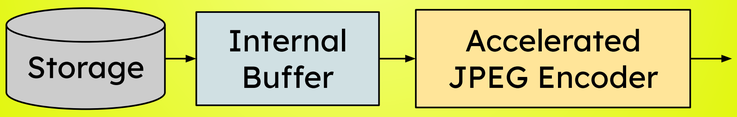

Performance Evaluation

FPGA vs. CPU (jpegenc)

		CPU	FPGA
cam	FPS	2.6	**19.5**
	CPU %	93	**5**
file	FPS	**22.6**	21.7
	CPU %	107	**14**

Resource Utilization

Generally, *Vitis Libraries* [4] codec kernels **exceed resource limitations** for edge boards, such as the **KV260**. Thus, employing these kernels on such boards often requires **lowering the target frequency**.
Our encoder is able to achieve **7~25%** of the resource usage of even the smallest Vitis encoding kernel (Webp at 100MHz), as shown below.
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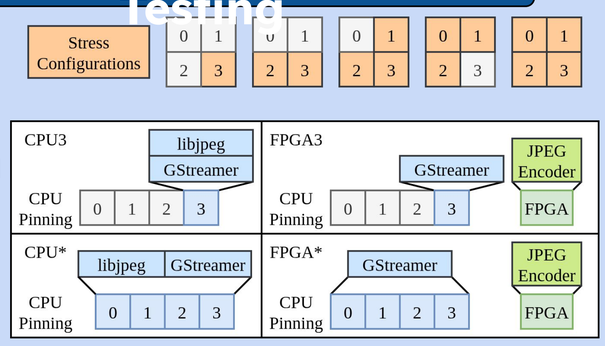
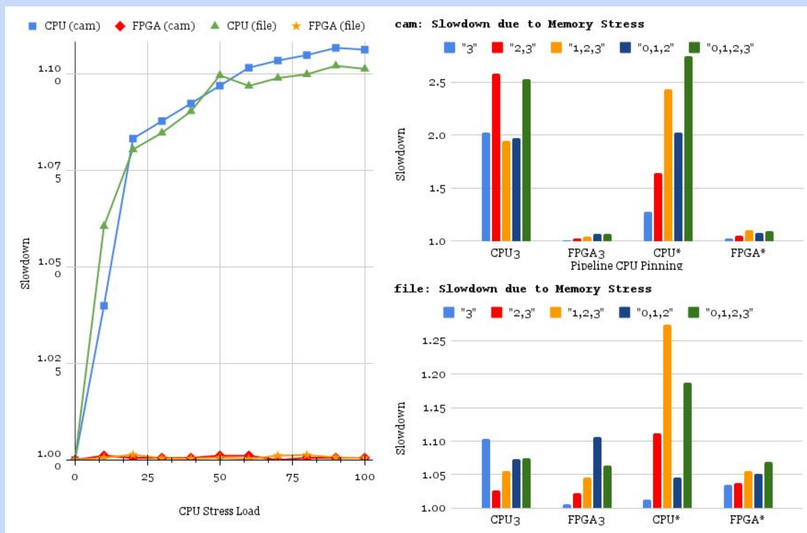
Objective: Test the **slowdown** behavior of both the **jpegenc-based CPU encoder** and our **FPGA encoder** when the system is under load.





Discussion and Conclusions

1. Suitability for Edge
2.
3. Increased Predictability

References

[1] AMD. "Kria KV260 Vision AI Starter Kit". https://www.amd.com/en/products/system-on-modules/kria/k26/kv260-vision-starter-kit.html. Accessed 2025-08-20.
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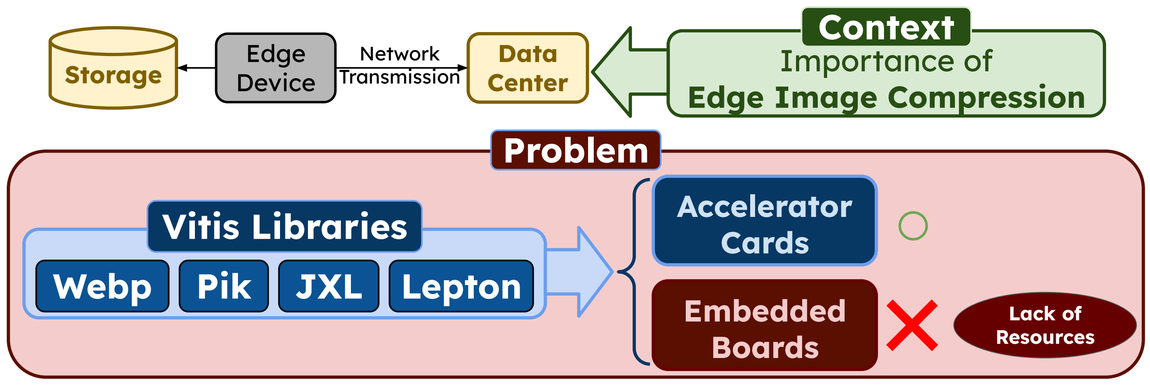

Approach

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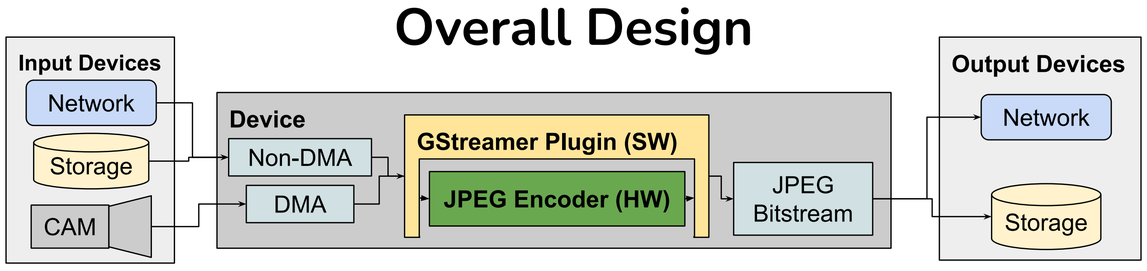

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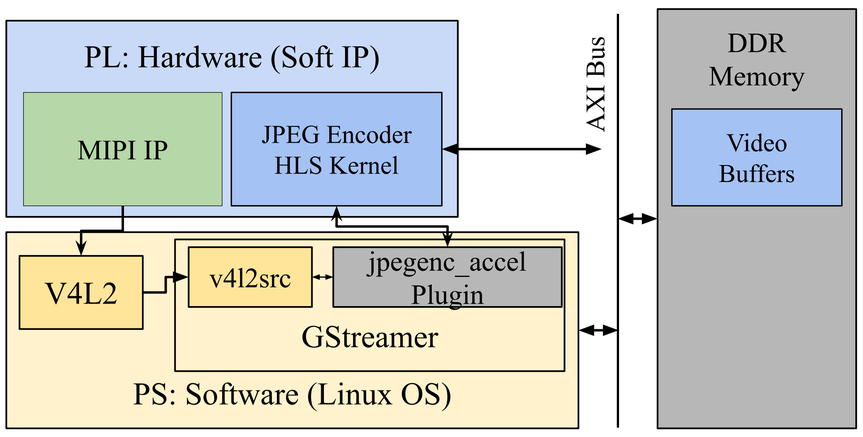

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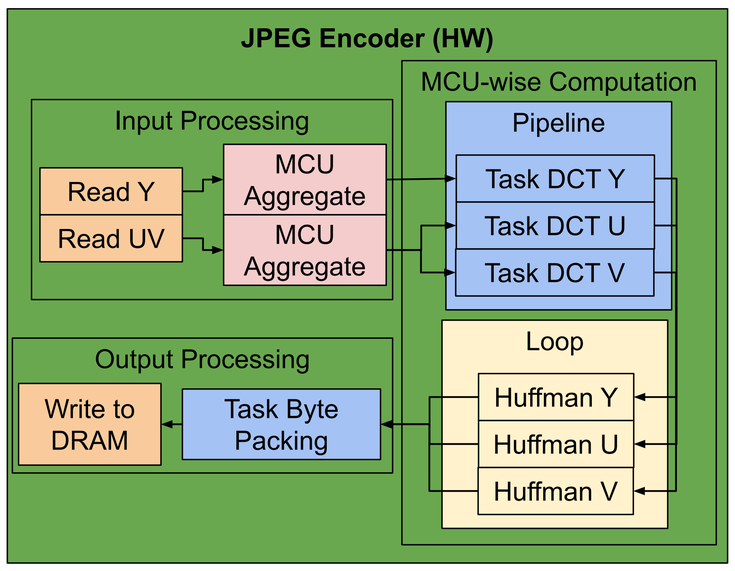
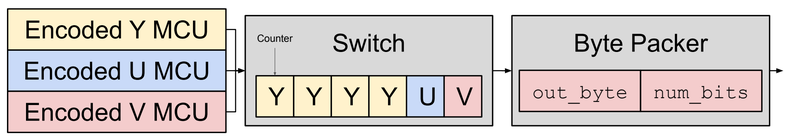
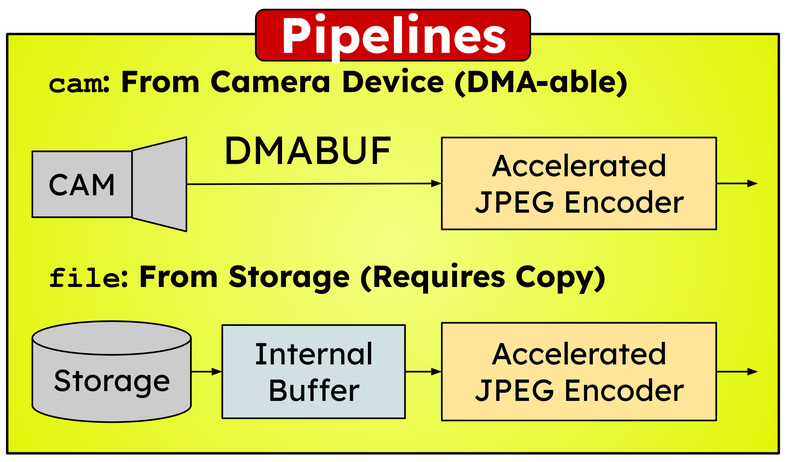




Pipelines



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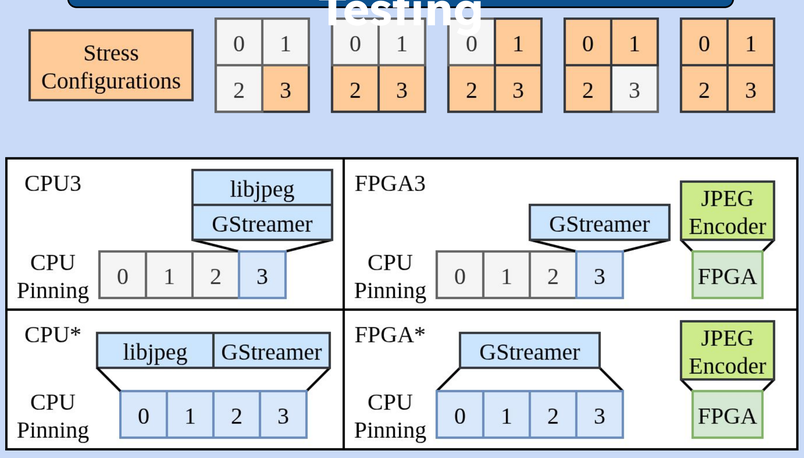
Experiments

CPU/Memory Stress Testing



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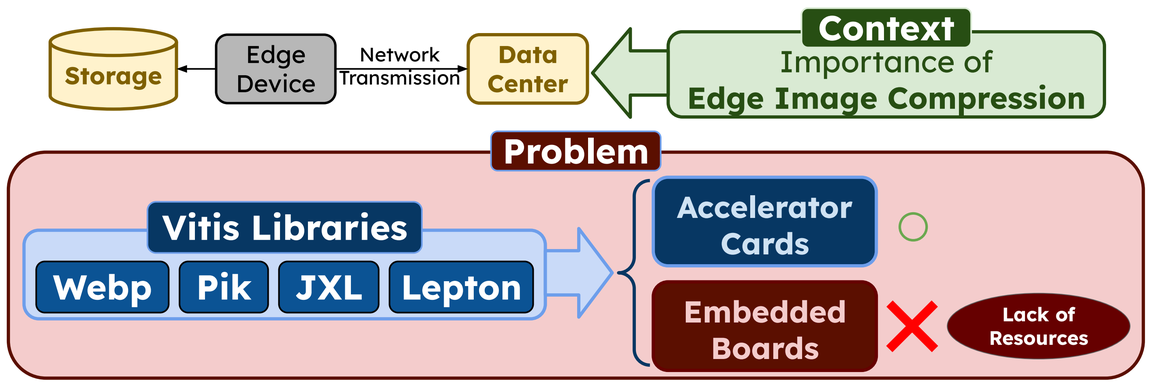
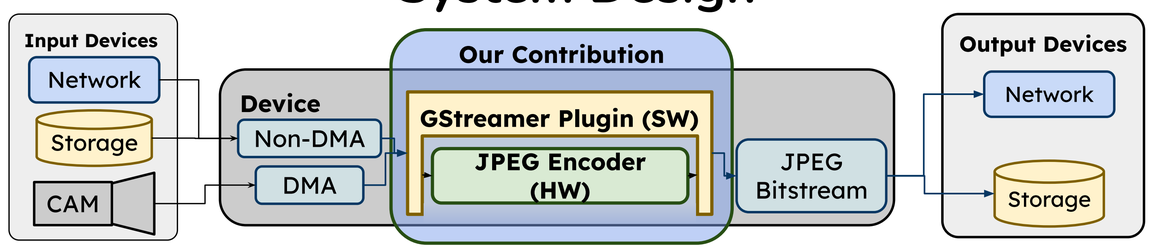


Approach

System Design



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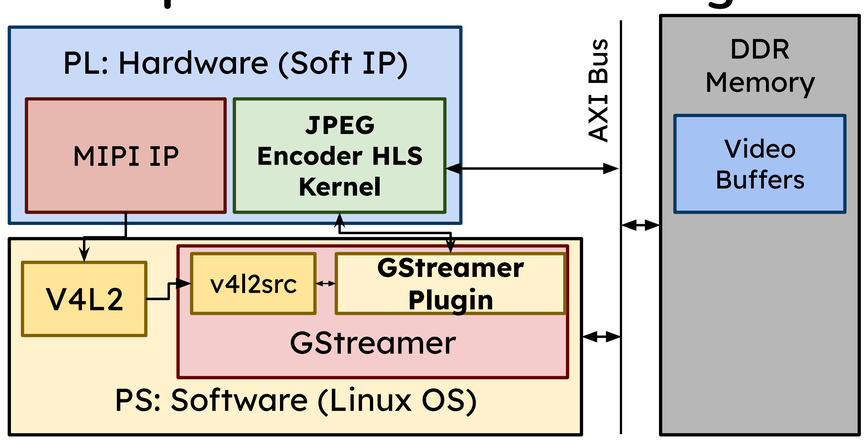
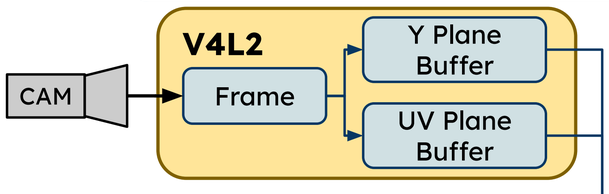


Hardware Architecture



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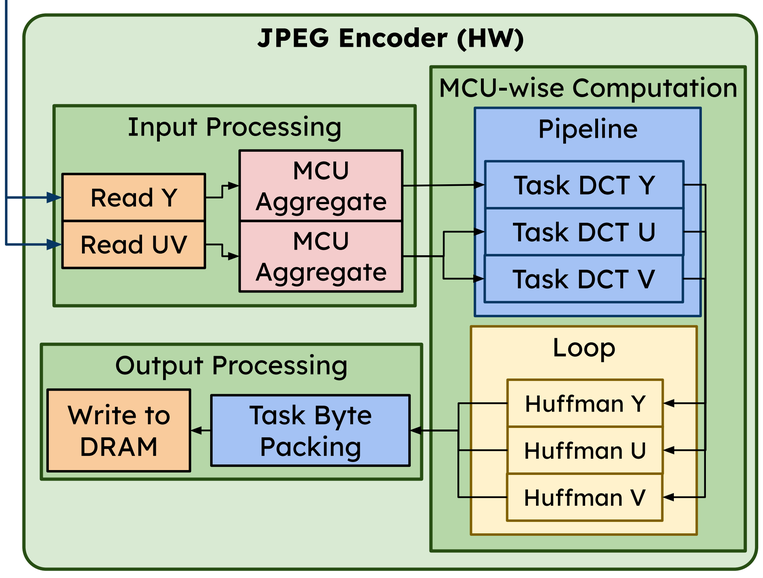
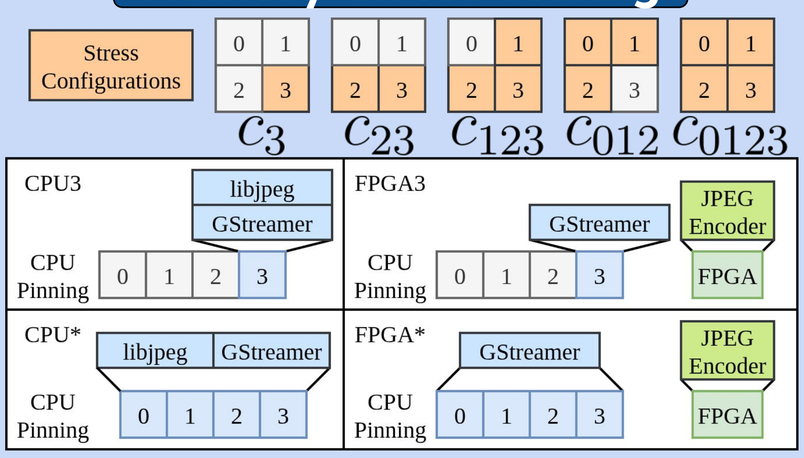
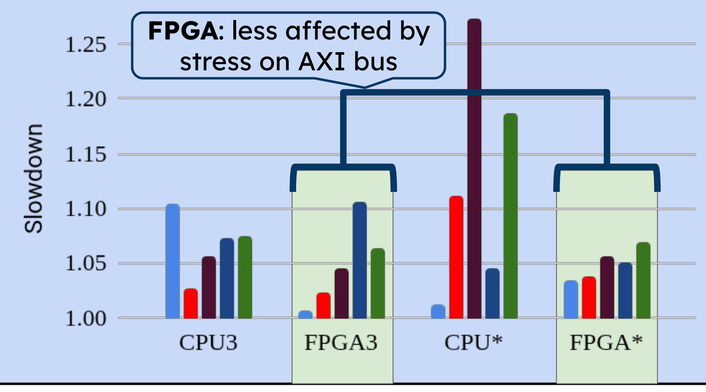


Experiments

Memory Stress Testing

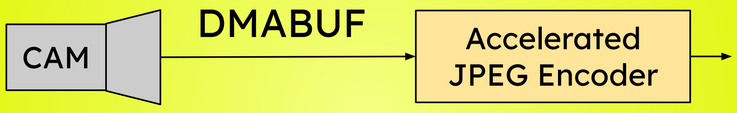


`file`: **Slowdown Comparison under Memory Stress**



Definition: Pipelines

`cam`: From Camera Device (DMA-able)



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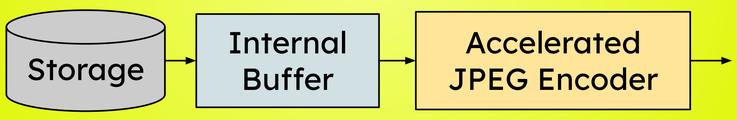

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Webp Encoder[2]

- **High Resource Usage**
  - Requires lowering **target frequency** to 100Hz

JPEG Encoder[1]

- **7~25%** of Webp Resources
  - Can fit **four** JPEG encoders in place of a **single** Webp Encoder

[1]Our work [2]Vitis Codec Libraries

Discussion and Conclusions

1. Suitability for Edge
   - Low resource usage
   - Realtime performance
2. Usability
   - GStreamer integration
     - Easy composition of media pipelines
3. Increased Predictability
   - Resilience against memory stress

Future Work

- Streamlined flow for GStreamer integration with arbitrary HLS kernels

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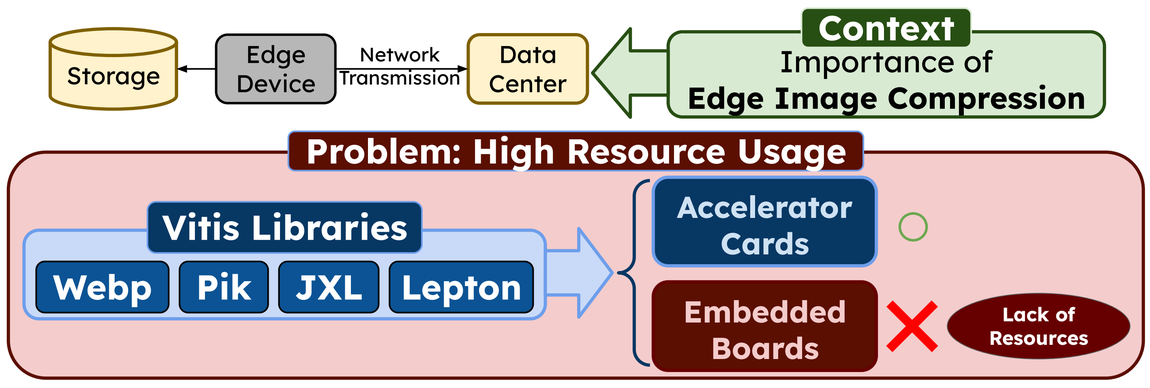
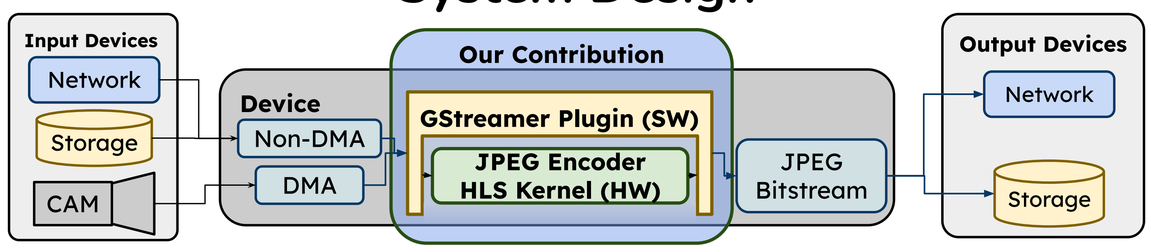


Lack of low-resource HLS solutions for real-time FullHD image compression

Approach

System Design



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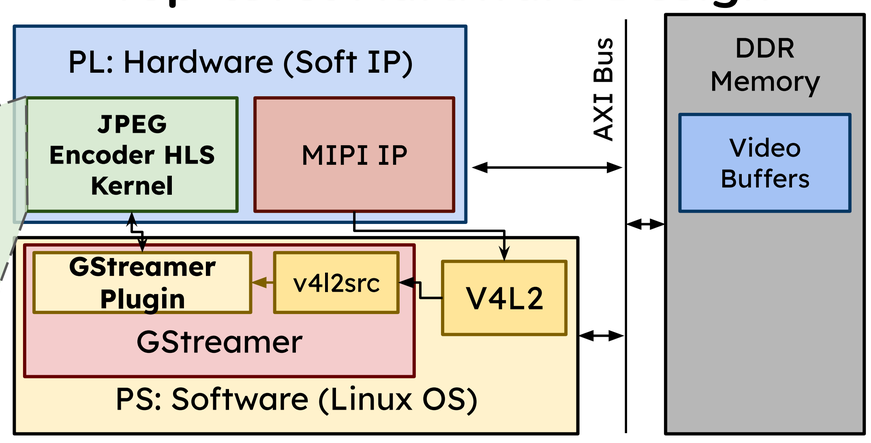
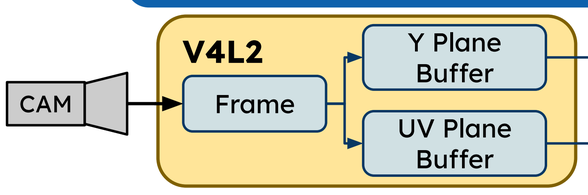


- Camera accessed through V4L2
  - Accesses must go through AXI bus

Hardware Architecture



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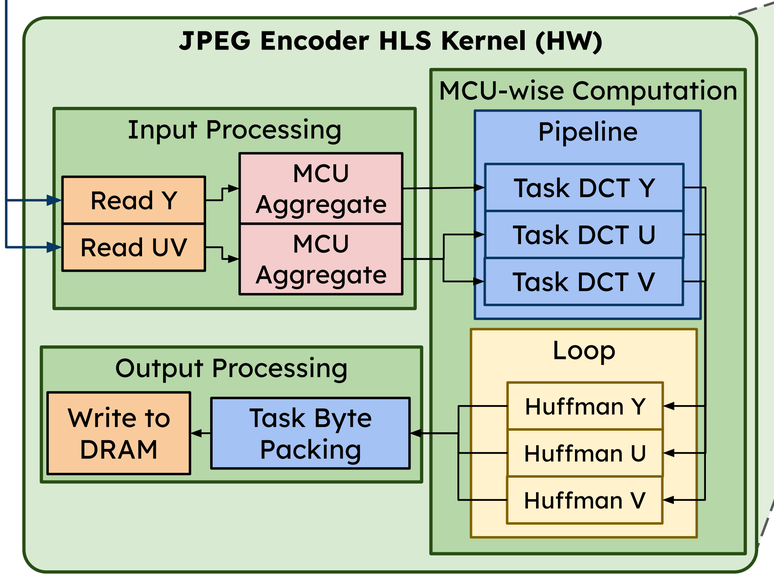

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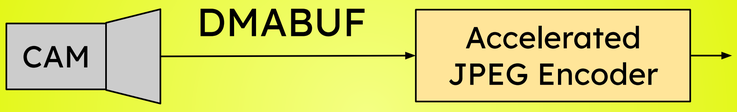

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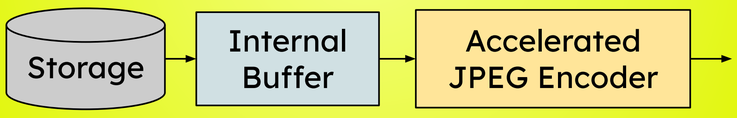

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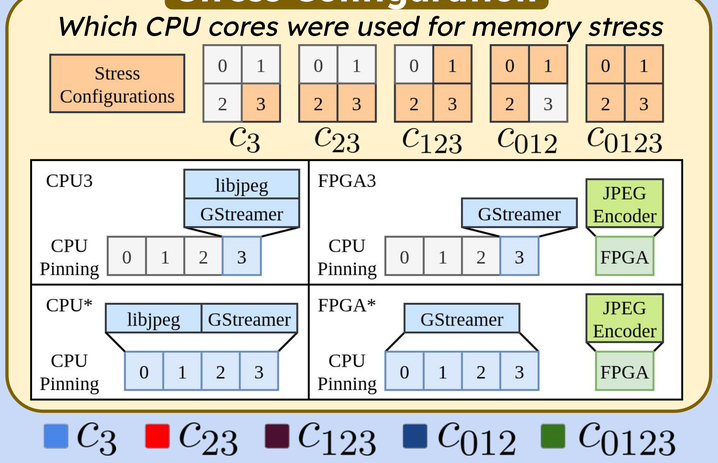
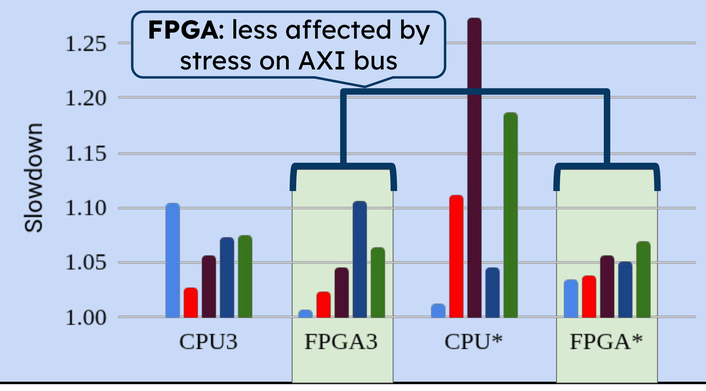
Slowdown Comparison under Memory Stress

Stress Configuration

Which CPU cores were used for memory stress





Discussion and Conclusions

1. Suitability for Edge
   - Low resource usage
   - Realtime performance
2. Usability
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     - Easy composition of media pipelines
3. Increased Predictability
   - Resilience against memory stress

Future Work

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GStreamer-integrated HLS-based JPEG Encoder for Edge FPGA SoCs

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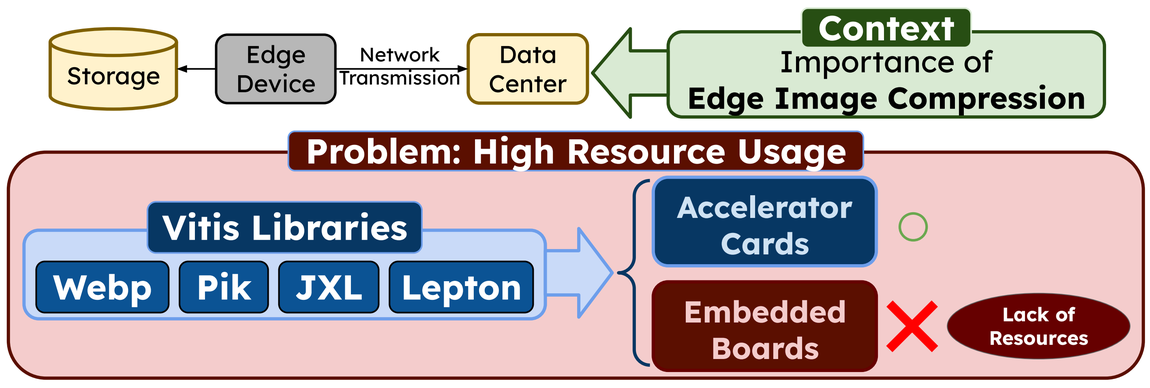
[1]Nagoya University, [2]Renesas Electronics, [3]Map IV Inc.

E-mail: yuri_gpps1@ertl.jp

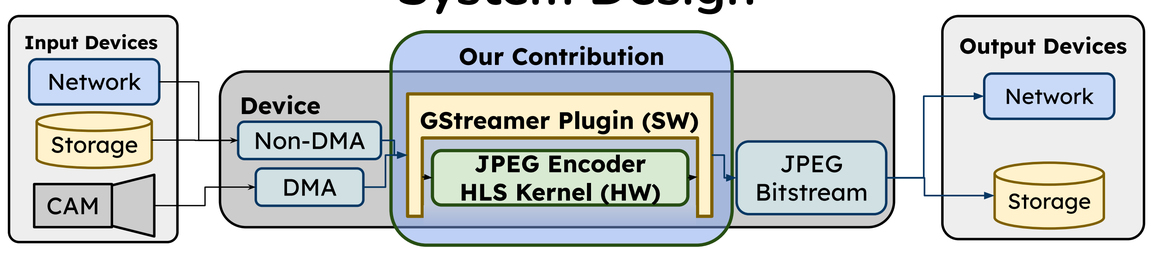
Motivation



Lack of low-resource HLS solutions for real-time FullHD image compression

Approach

System Design



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- ***GStreamer* plugin** interfaces with encoder.
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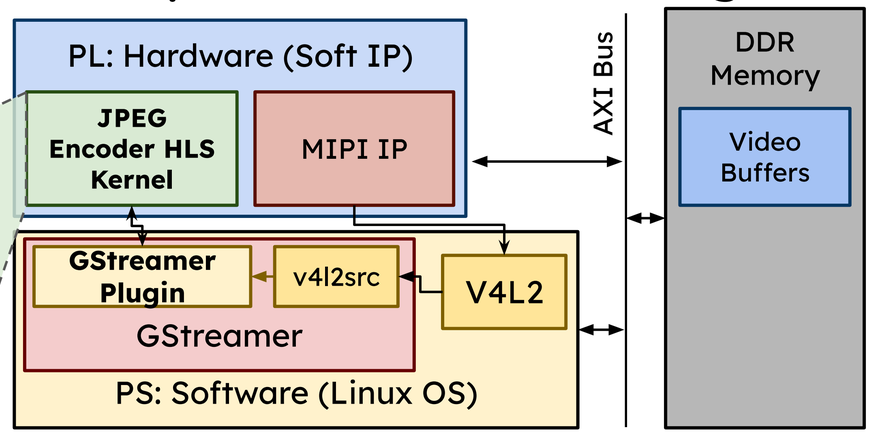
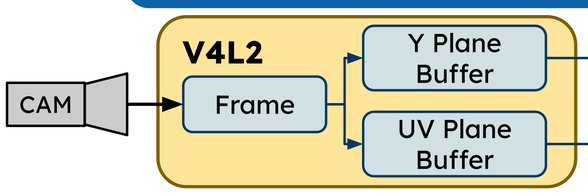
  - Easy usage of DMA capabilities.

Top-level Hardware Design



- Camera accessed through V4L2
  - Accesses must go through AXI bus

Hardware Architecture



- Send each plane to the encoder via AXI
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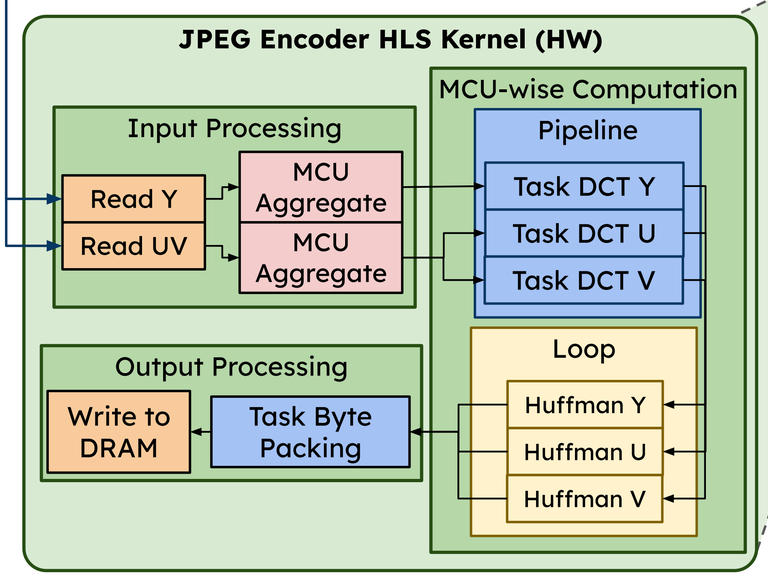

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Experiments

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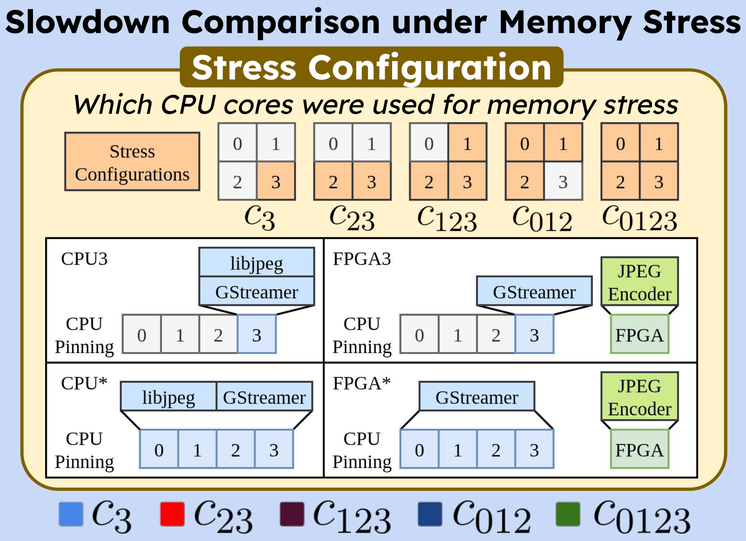
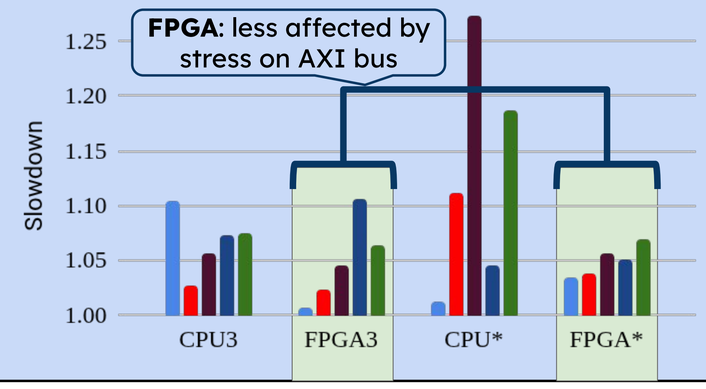
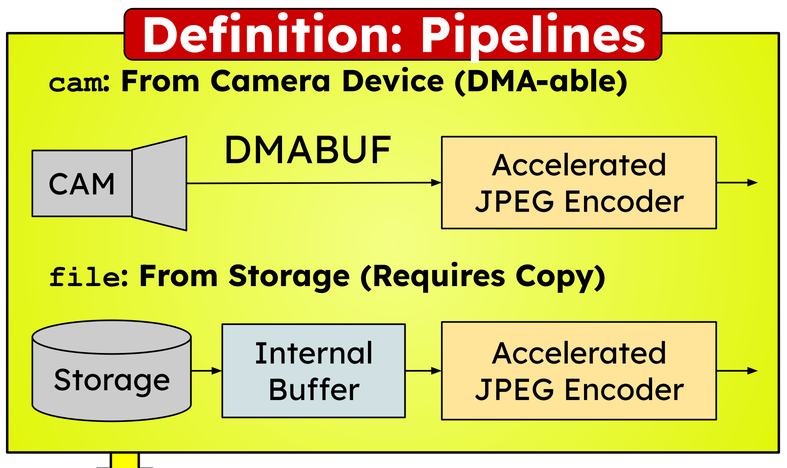
Slowdown Comparison under Memory Stress





Definition: Pipelines



Performance

FPGA vs. CPU (jpegenc)

		CPU	FPGA	FPGA/CPU
cam	FPS	2.6	**19.5**	**7.5**
	CPU %	93	**5**	**0.054**
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- **High Resource Usage**
  - Requires lowering **target frequency** to 100Hz

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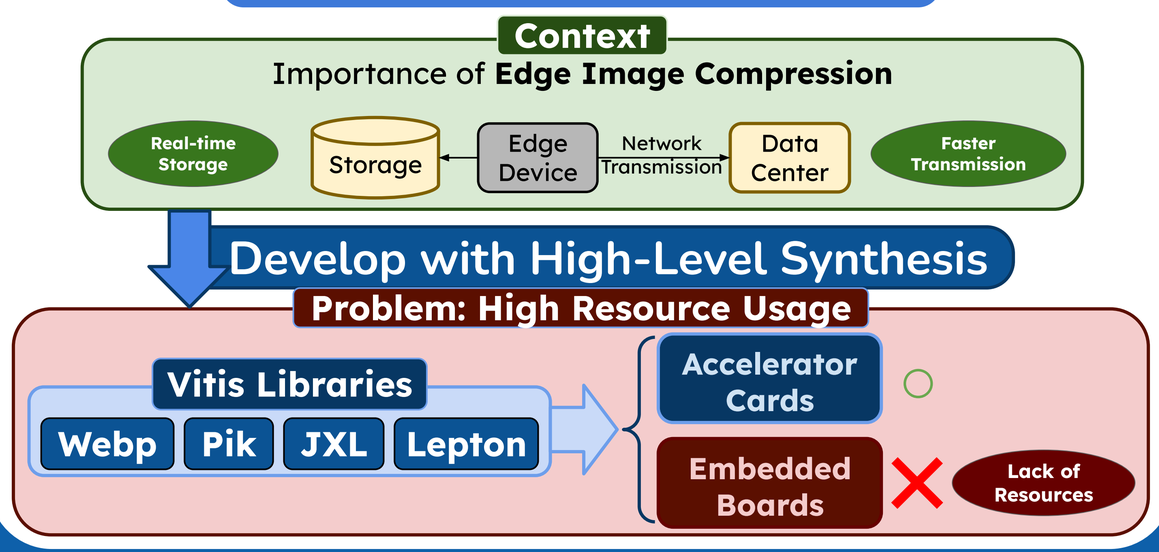

Approach

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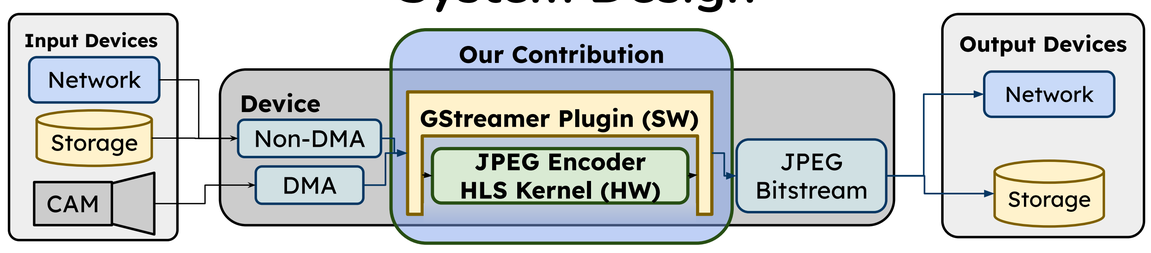

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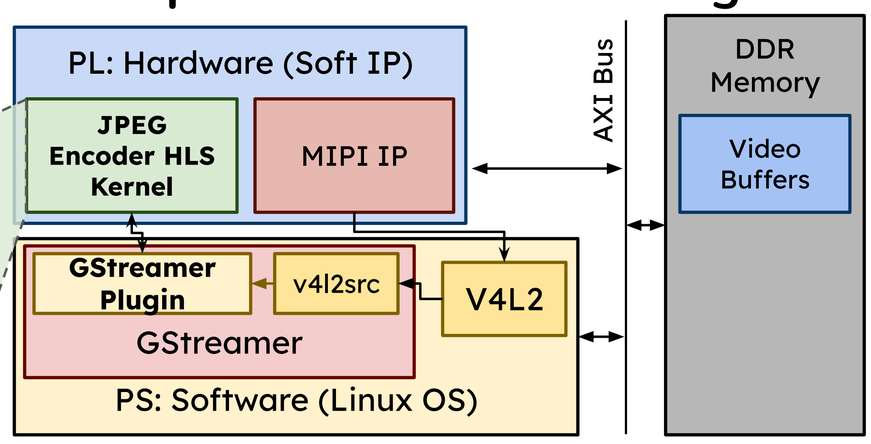

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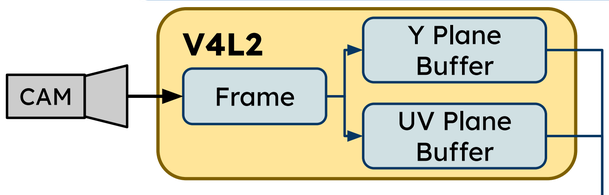

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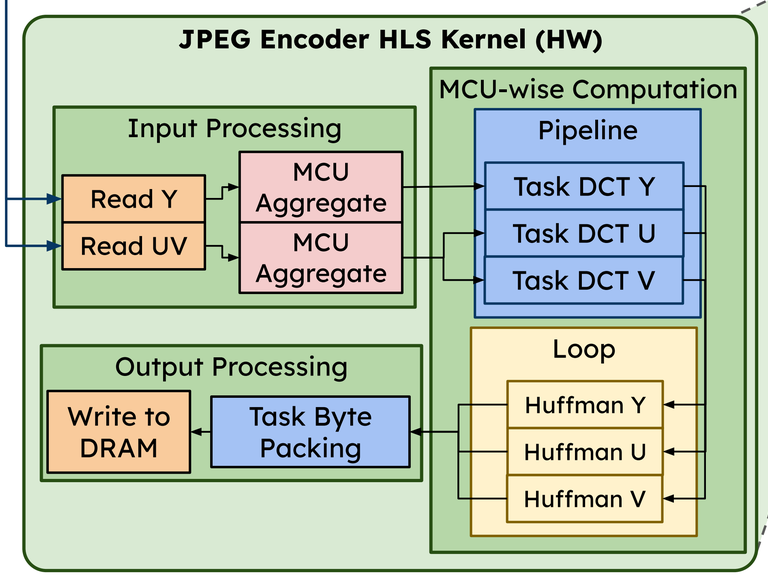

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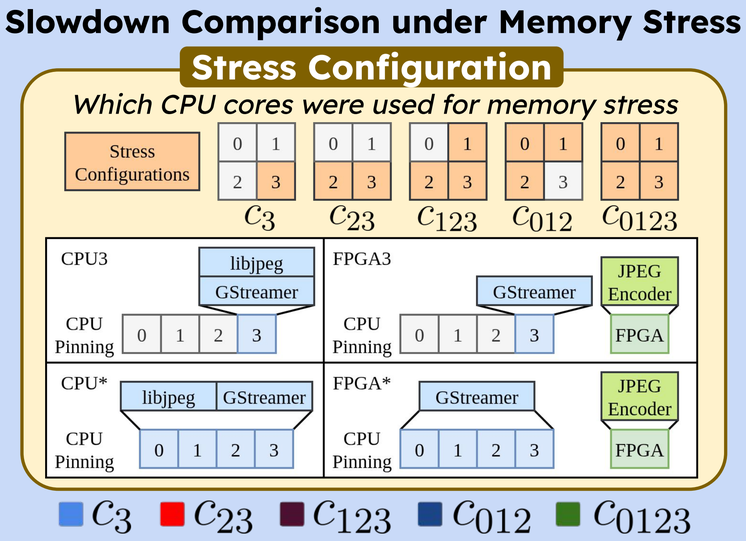

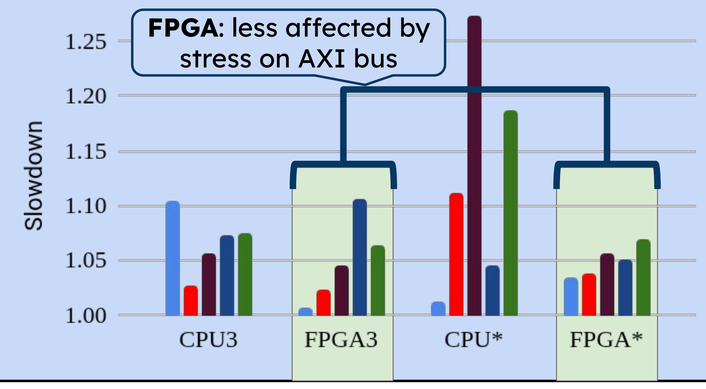

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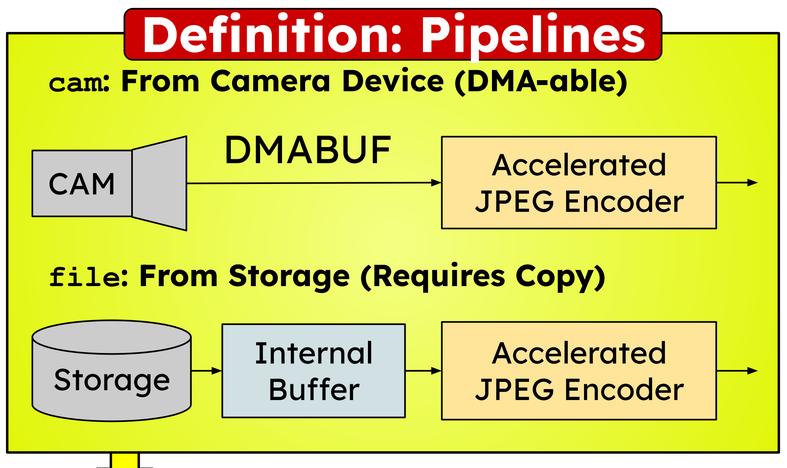

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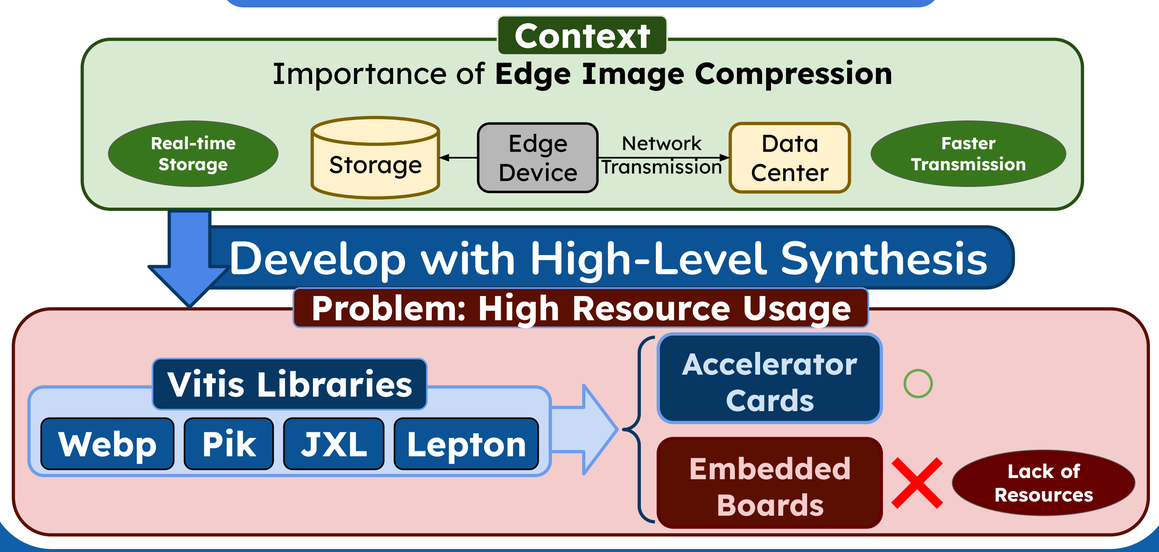

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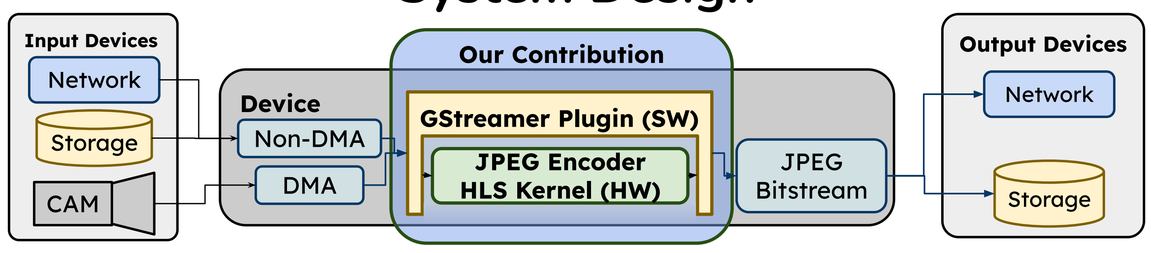

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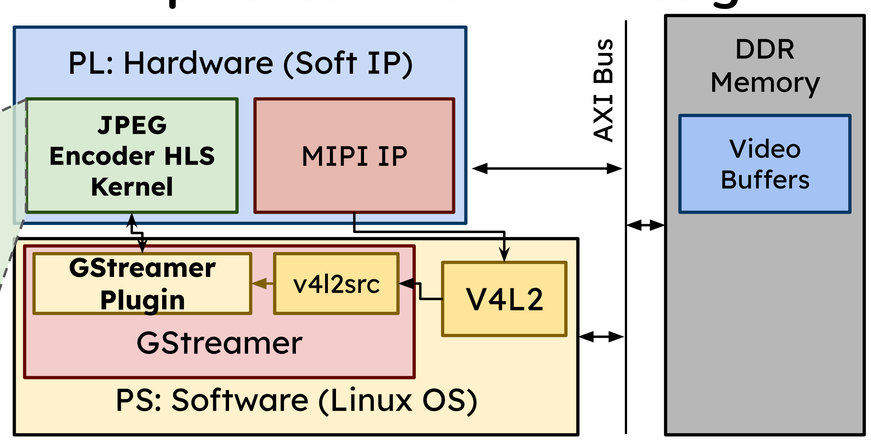

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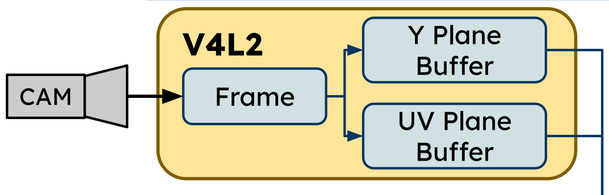

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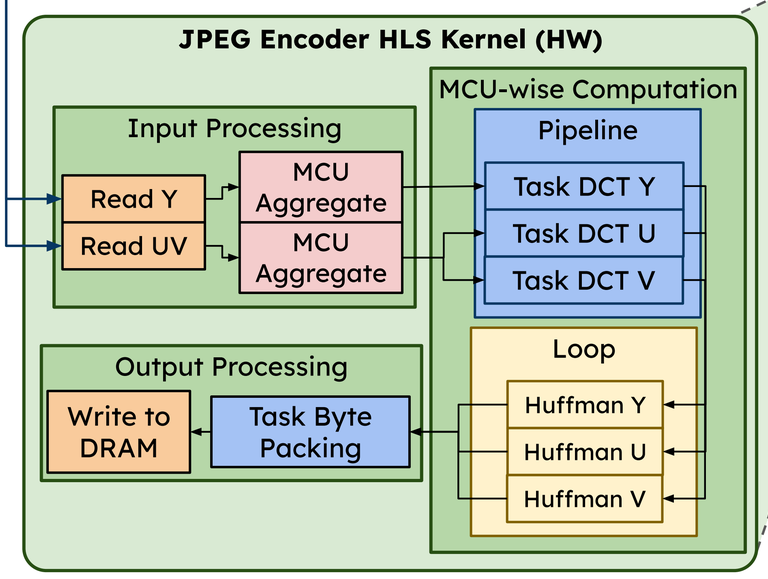

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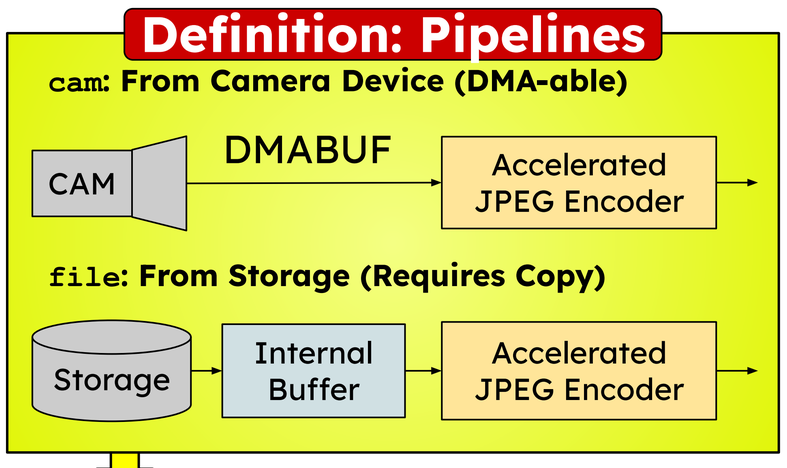

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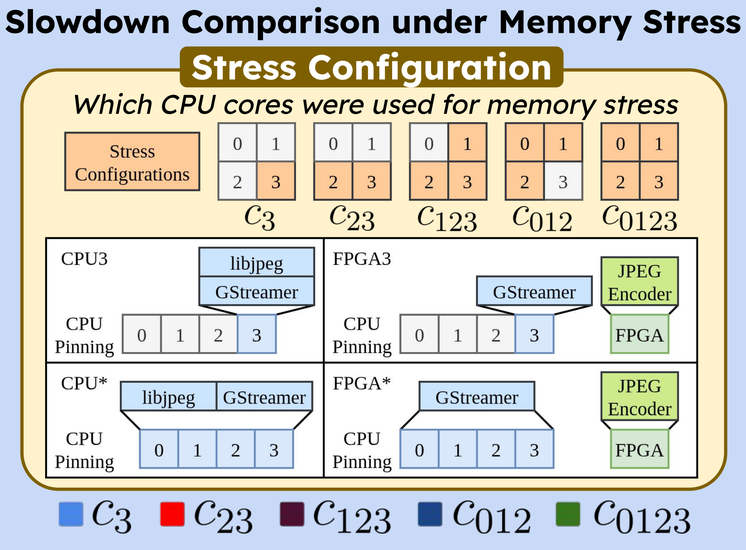

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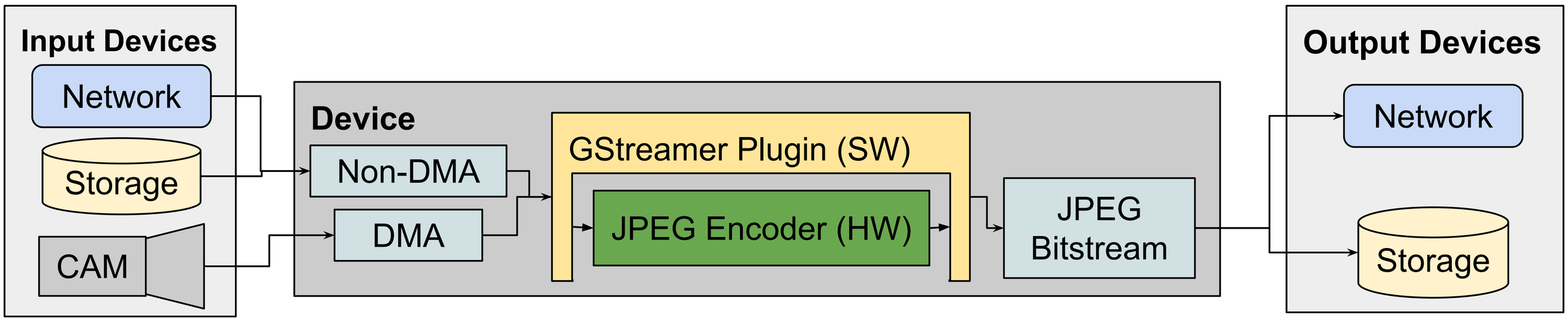
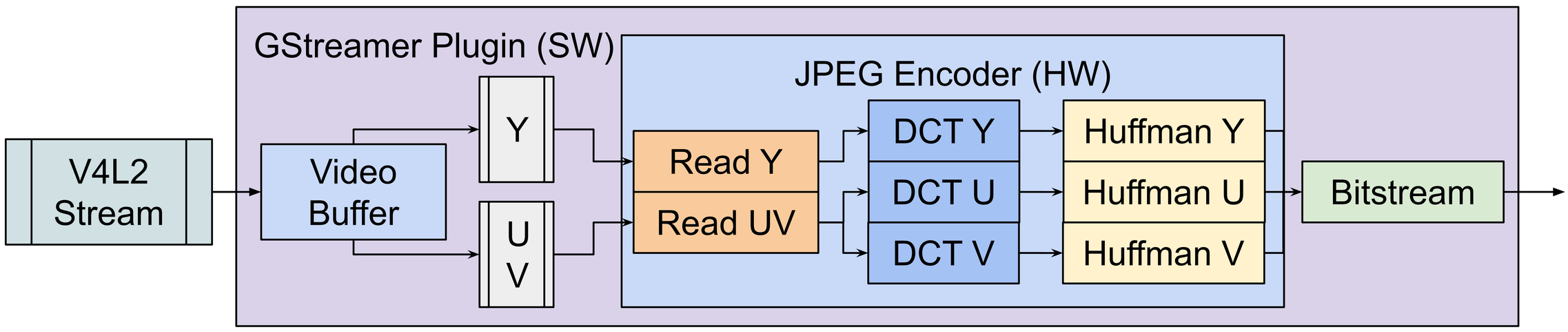
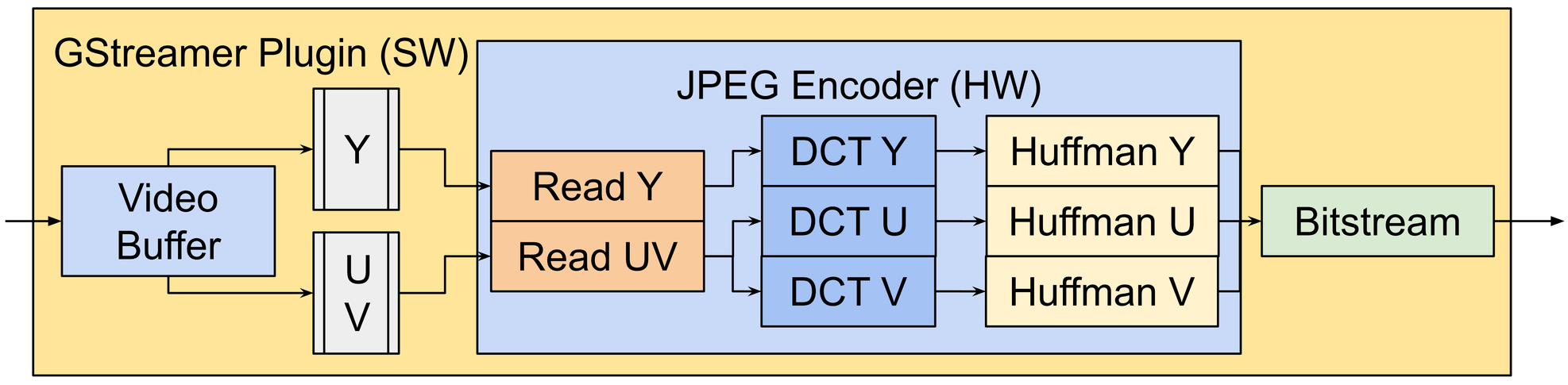
Download this Poster!


Input Devices
Network
Storage
CAM
Device
Non-DMA
DMA
GStreamer Plugin (SW)
JPEG Encoder (HW)
JPEG
Bitstream
Output Devices
Network
Storage


V4L2
Stream
GStreamer Plugin (SW)
Video
Buffer
Y
U
V
JPEG Encoder (HW)
Read Y
Read UV
DCT Y
DCT U
DCT V
Huffman Y
Huffman U
Huffman V
Bitstream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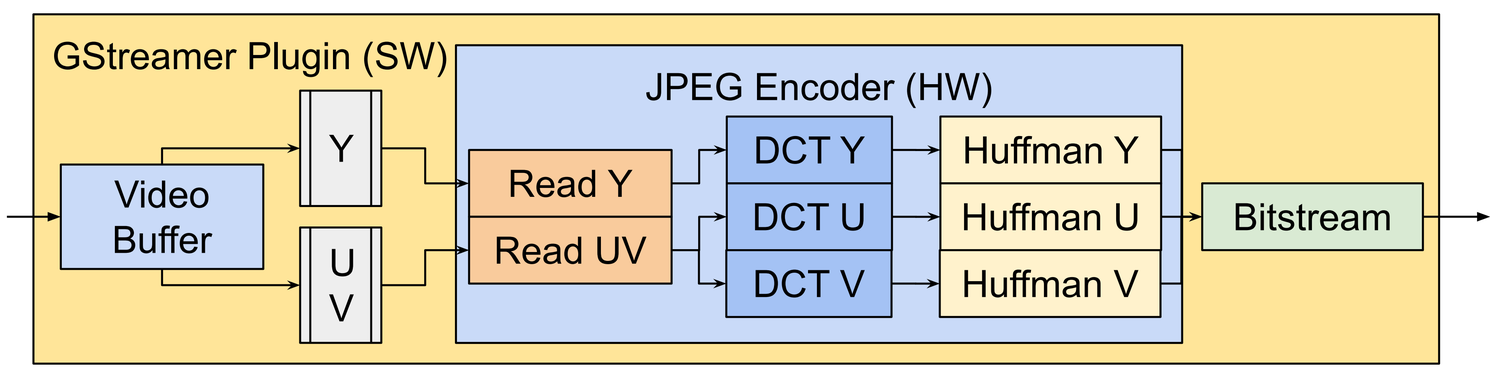
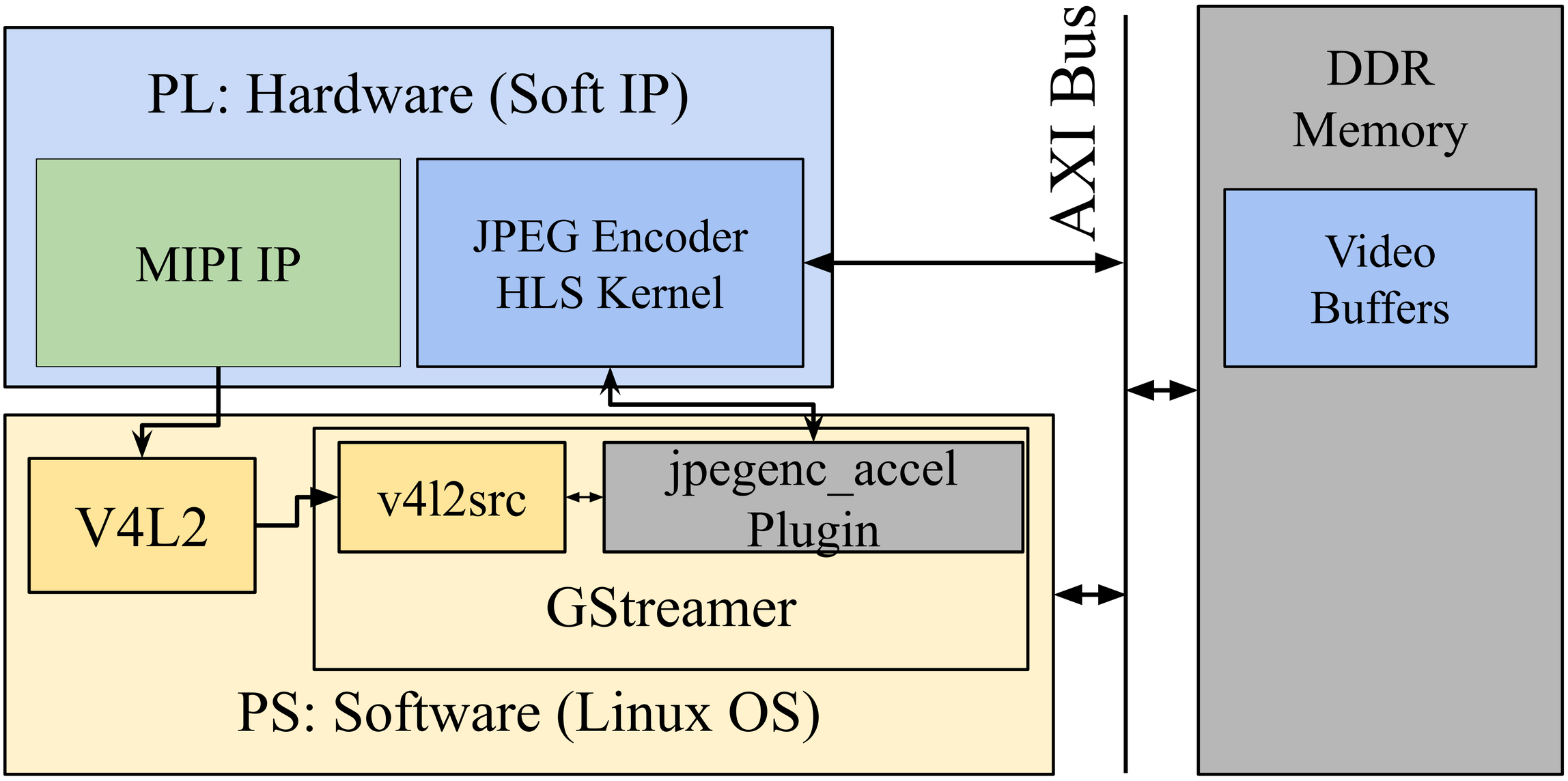
Overall Architecture

The design consists of a HW component integrated with a *GStreamer* plugin.



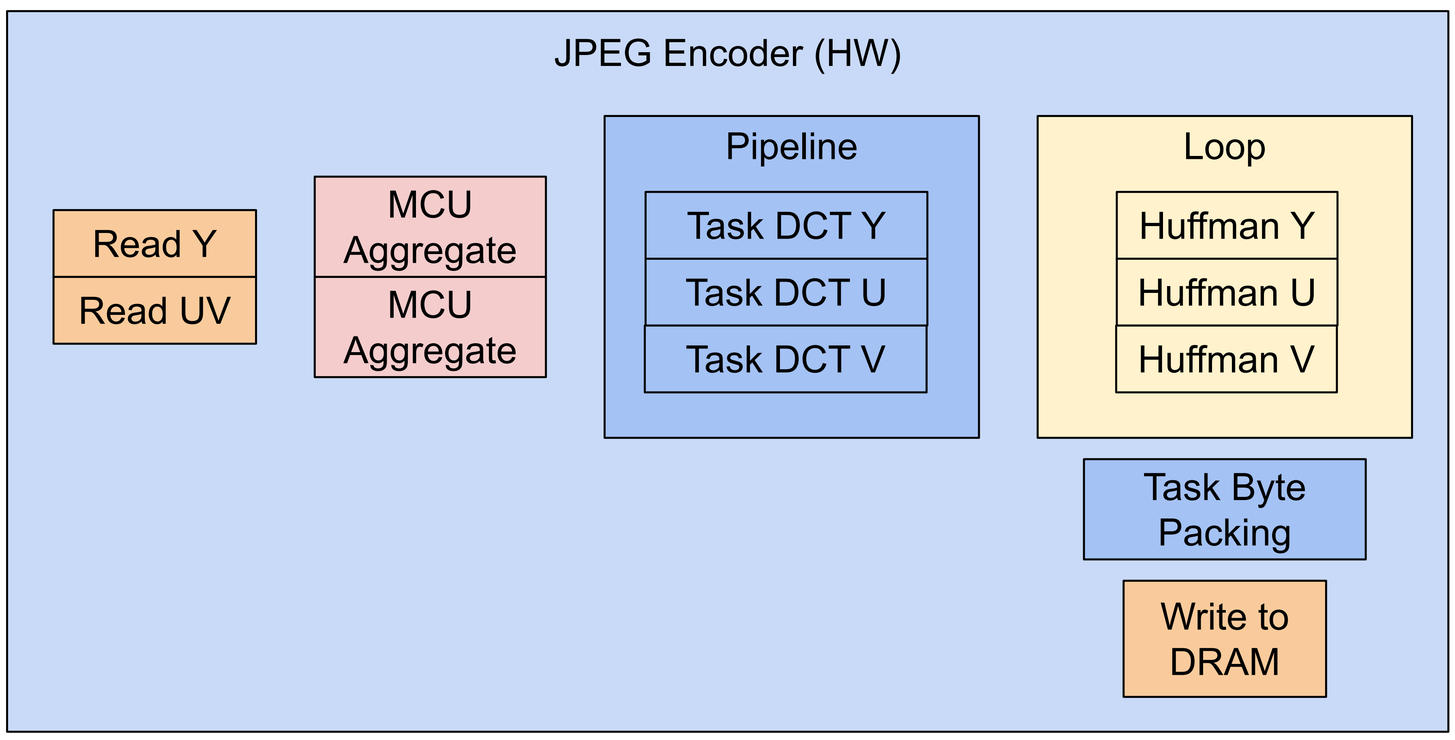
GStreamer allows for easy and quick composition of media pipelines, making the design easily testable in a wide range of scenarios.

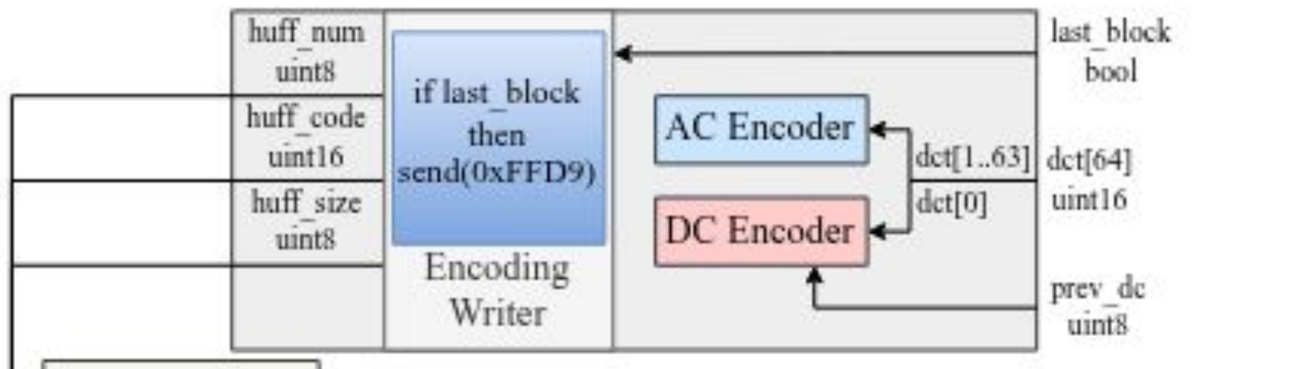


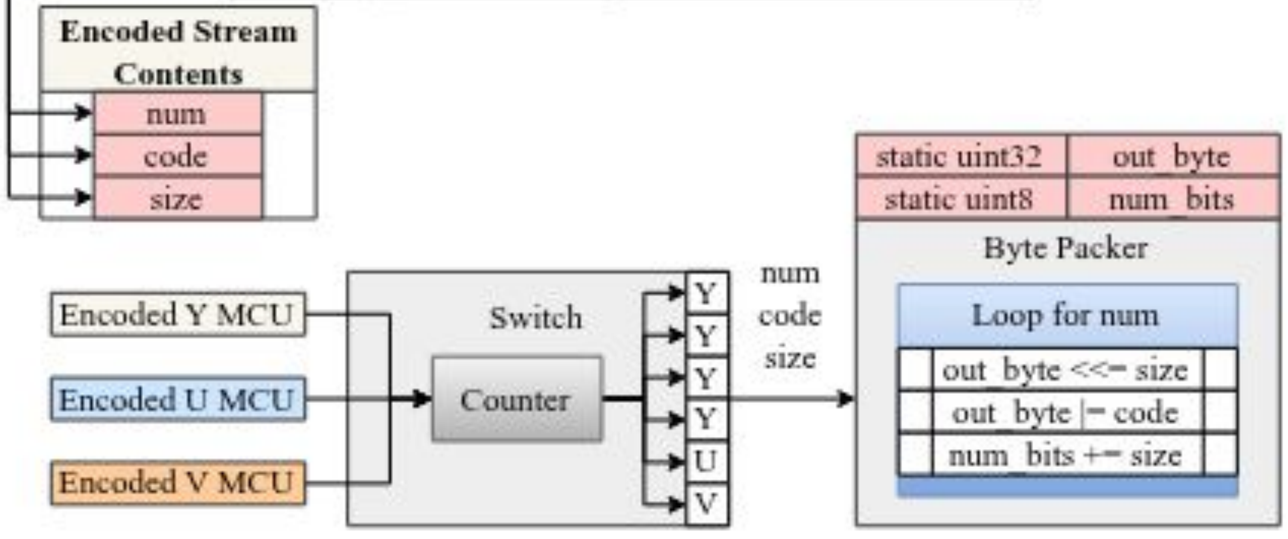
The camera-based pipeline consists of an AMD MIPI IP accessed through the v4l2src GStreamer plugin node. Separate buffer planes can be accessed directly and processed as individual channels on the JPEG IP, improving throughput.

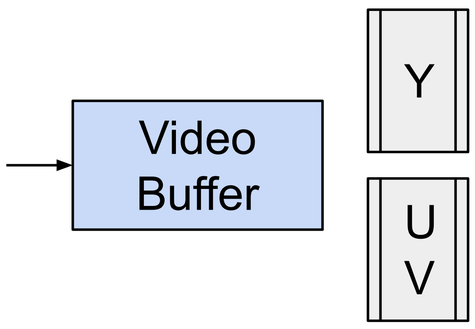
Hardware Components

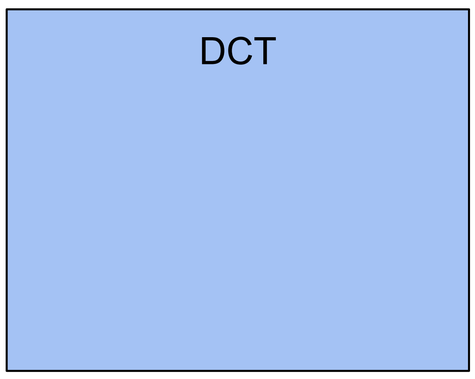
Y and UV channels are processed separately in order to aggregate MCUs into streams.
Afterwards, each MCU goes through DCT, RLE, Huffman encoding.
Finally, all MCU channels are merged together acording to the YYYYUV order for YUV420.

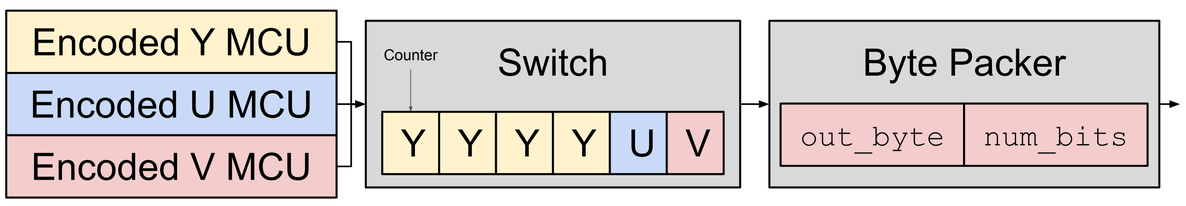


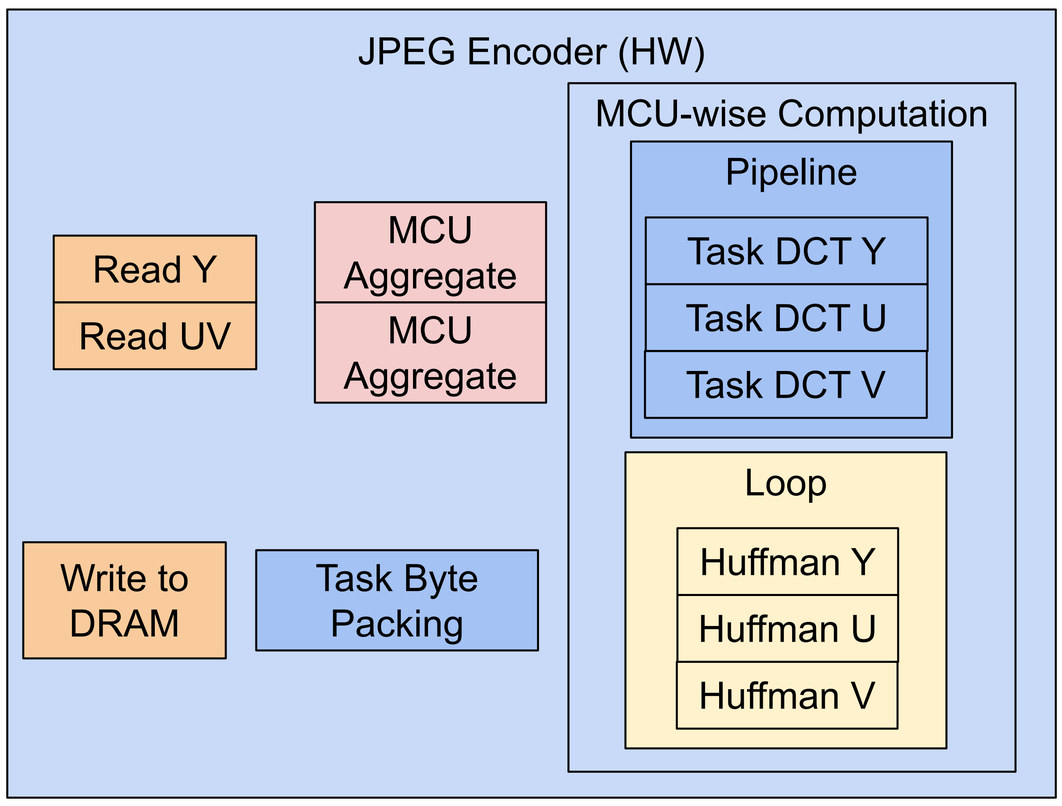












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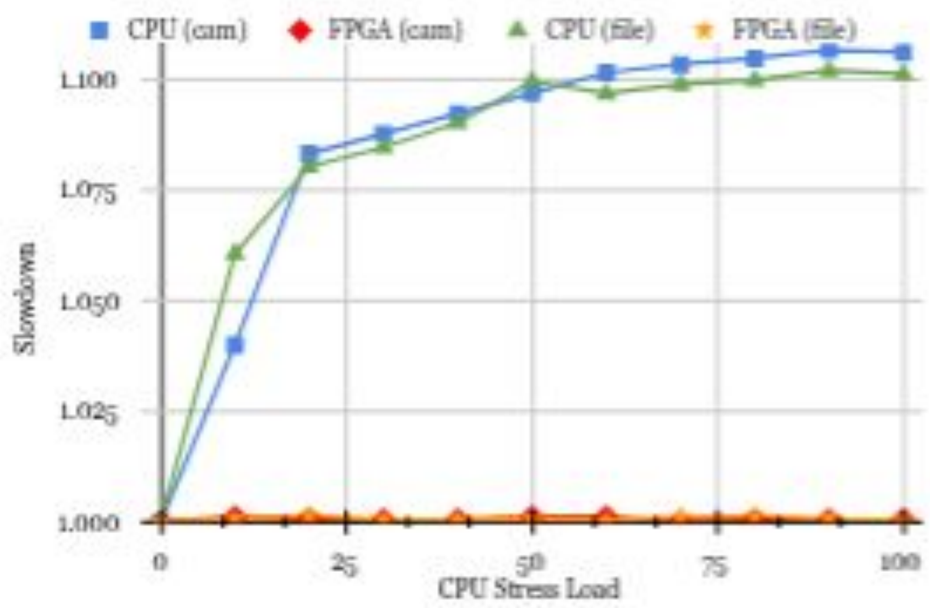

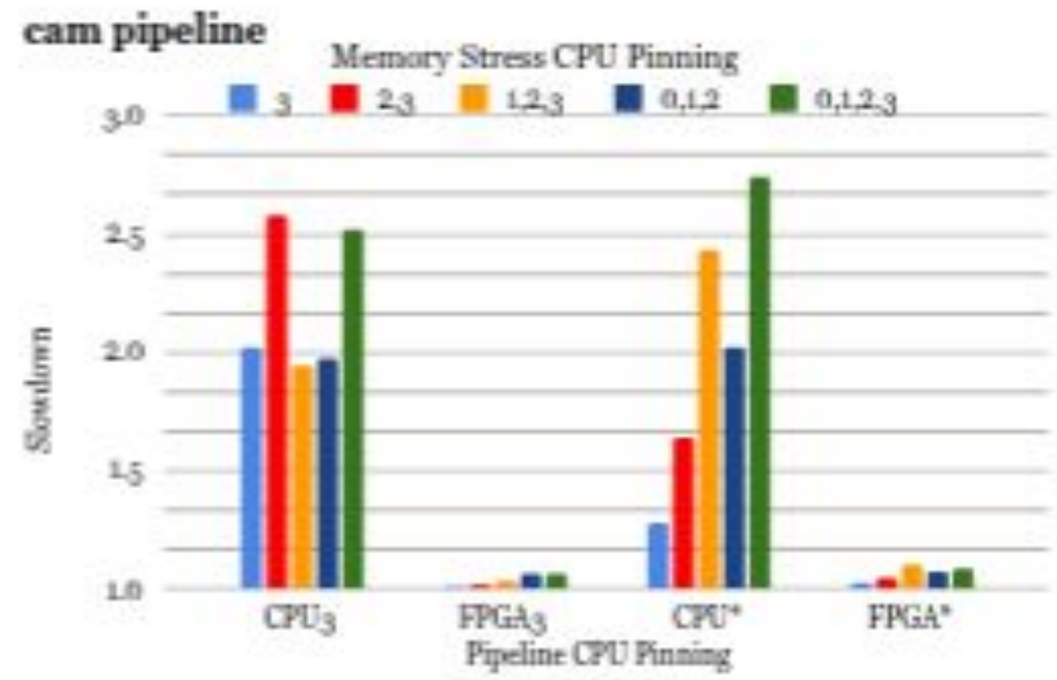

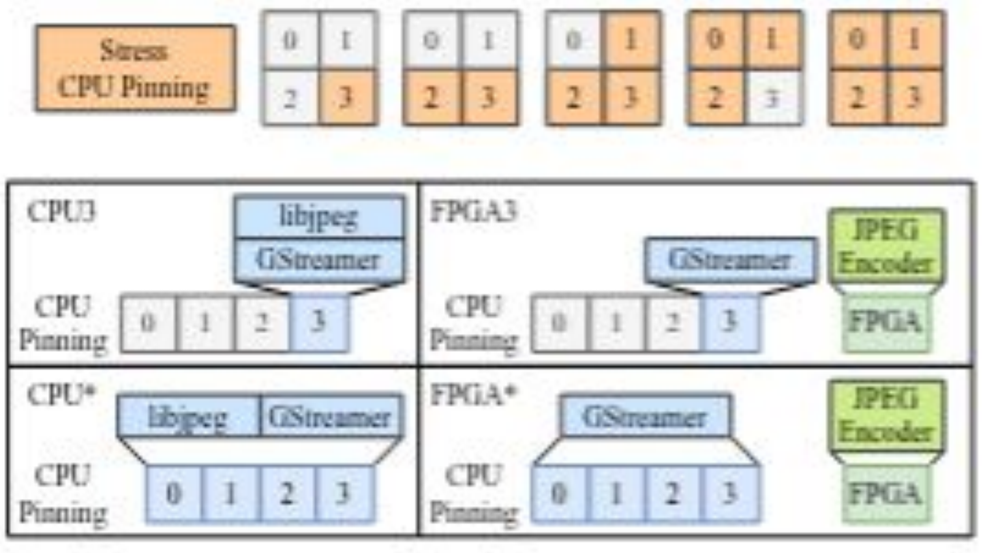

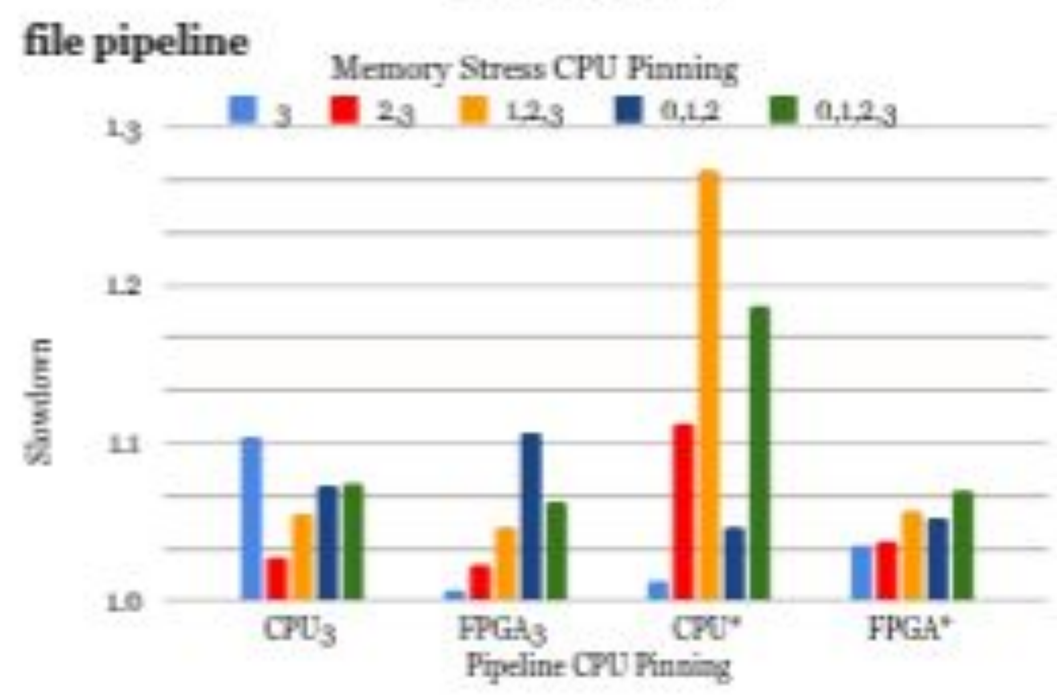

Fig. 6. **Memory Stress Configuration**: Four configurations for single-core or multi-core affinity of the pipeline (CPU3, CPU*, FPGA3, FPGA*), as well as five CPU affinity configurations for the memory stress.

TABLE II
RESOURCE UTILIZATION COMPARISON OF JPEG AND WEBP ENCODERS ON KV260

	JPEG (our work)	WebP [3]	Total Available
Frequency	250 MHz	100 MHz	
Throughput	4.49 MPps	1.88 MPps	
LUT	**11,513**	62,296	92,832
LUTAsMem	**2,355**	6,610	55,336
REG	**18,150**	71,227	191,197
BRAM	**6**	81	106
URAM	**12**	46	56
DSP	**85**	834	1248

TABLE III
PERFORMANCE EVALUATION OF THE JPEG ENCODER

		CPU	FPGA (Our)
`cam`	Throughput (fps)	2.6	**19.5**
	CPU Usage (%)	93	**5**
`file`	Throughput (fps)	**22.6**	21.7
	CPU Usage (%)	107	**14**
	Compression Ratio	3.202%	**3.219%**
	PSNR (dB)	**27.72**	27.45