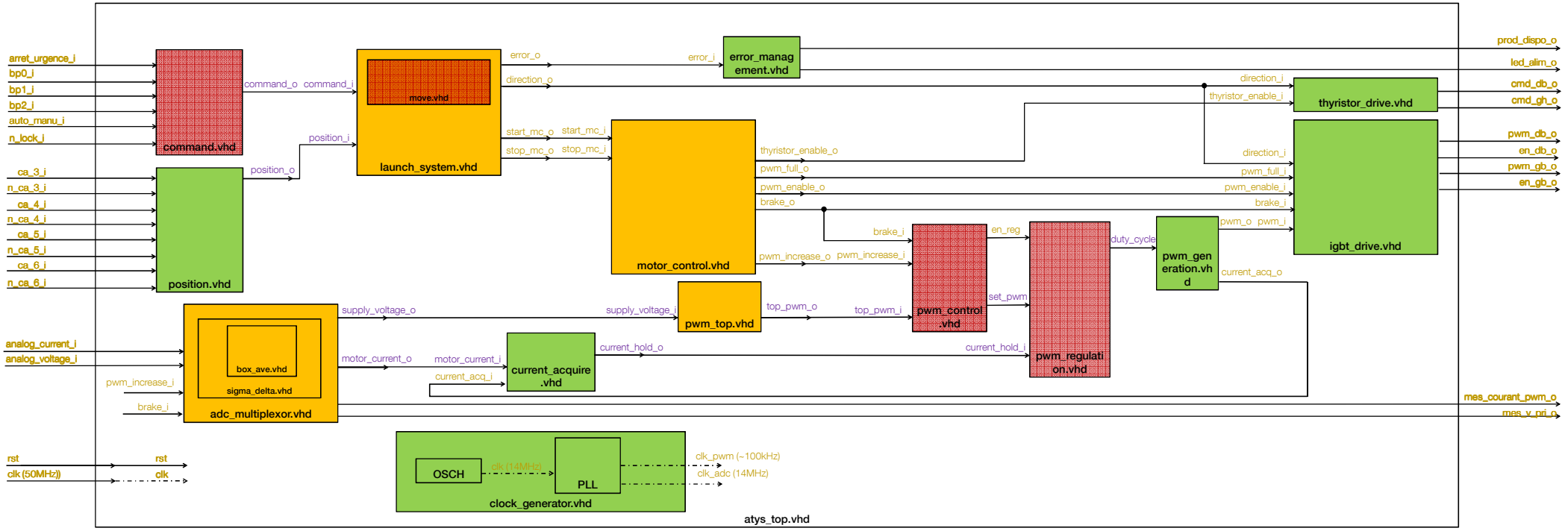
VHDL Modules



std_logic
std_logic_vector

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