1 Introduction

This application note explains the influences external circuitry and component selection can have on cell measurement accuracy using the bq76PL455 and provides a calibration procedure using the features provided in the bq76PL455 to correct for these errors.

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2 Reasons to Calibrate

The bq76PL455 is factory calibrated to provide the highest possible accuracy in input measurement. However, both internal settings and external circuitry implemented in the user's application can affect cell measurement accuracy. For these reasons, it is strongly recommended to always perform a final calibration on the bq76PL455.

Some examples of required circuits that can have an influence are:

- Input filters
- Input protection devices (Zener diodes)
- Battery connection harness and connectors
- Connection point of TOP pin to highest cell
- Connection point of system ground to lowest negative terminal
- OUT cap value

System configuration of the bq76PL455 can also have an influence:

- ADC sample period
- Oversample configuration
- Type of oversampling (stay on channel or cycle through channels)

It is strongly recommended to start with a 390pF OUT capacitor, 60uS ADC conversion period and 8x oversampling (on the same channel before changing channels – CMD_OVS_CYCLE = 0) to achieve the best accuracy results.

Additionally, to prevent further inaccuracies due to moisture incursion, thermal and physical stress on the device and other related factors, it is recommended that the moisture free bq76PL455 be mounted according to the recommended IPC/JEDEC soldering/relow profile, conformal coated once mounted and baked at 125°C for at least 1 hour prior to the application circuit being calibrated and placed into regular service.

2.1 Zener Diode Leakage

The leakage should be as low as possible. If you look at the curves provided in the datasheet for leakage current over voltage, of course the Zener voltage can have an impact.

2.1.1 Effects from Input Filter

The selection of the input filter cap value can have a significant impact on cell measurement accuracy, and will drive the requirement of calibration. The ADC has an internal ~1MΩ resistor applied during sampling, which acts to drain the input filter cap for the duration of sampling. With the recommended sample settings of 60µs sample period, 8x oversampling, and staying on channel for oversampling, the total sample duration is ~150µs (see note below). The simulation results in Figure 1 below with a 470Ω input resistor and 500nF input filter cap show the amount the input voltage will drop during this period (between cursors ≈150µs) is ≈1.13mV.

NOTE: The total sample duration is the ADC sample period + n-1 oversamples at the configured oversample period. The recommended settings are ADC sample period = 60µs, 8x oversamples, 12.6µs

oversample ADC sample period and staying on channel to oversample. This would result in 60.04µs (for the first sample) + 7 * (12.6µs for each of the next 7 samples) = 60.04µs + 88.24µs = 148.24µs = ~150µs.

If different ADC sample settings are used, then the 150µs value should be changed to the new value.

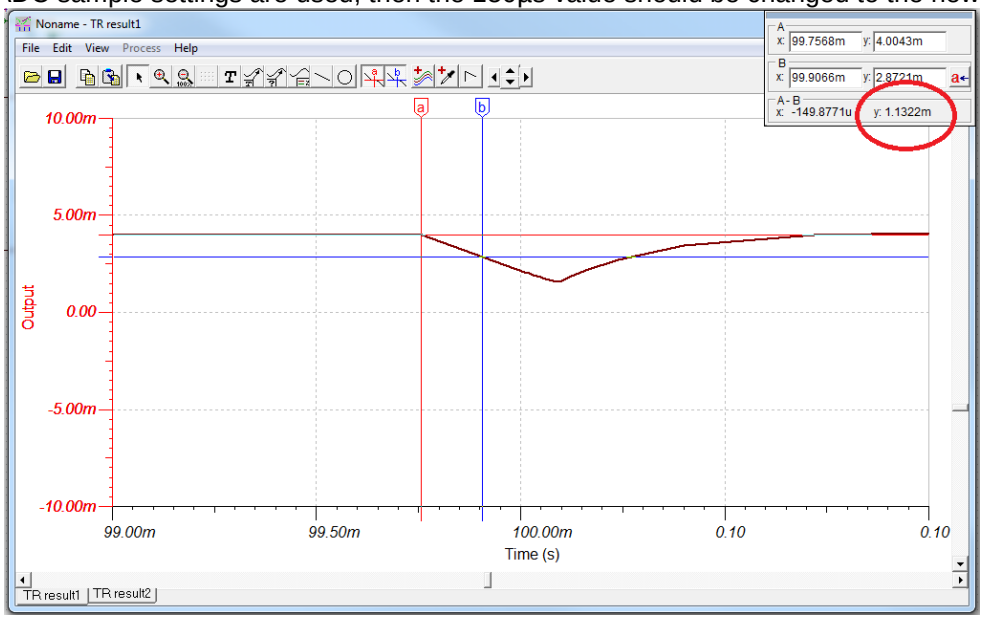

Figure 1 - Input offset during sampling (470ohm and 500nF)

The simulation results in Figure 2 below with a 1kΩ input resistor and 1µF input filter cap show the amount the input voltage will drop during this period (between cursors ≈150µs) is ≈377µV. A significant difference in input offset error.

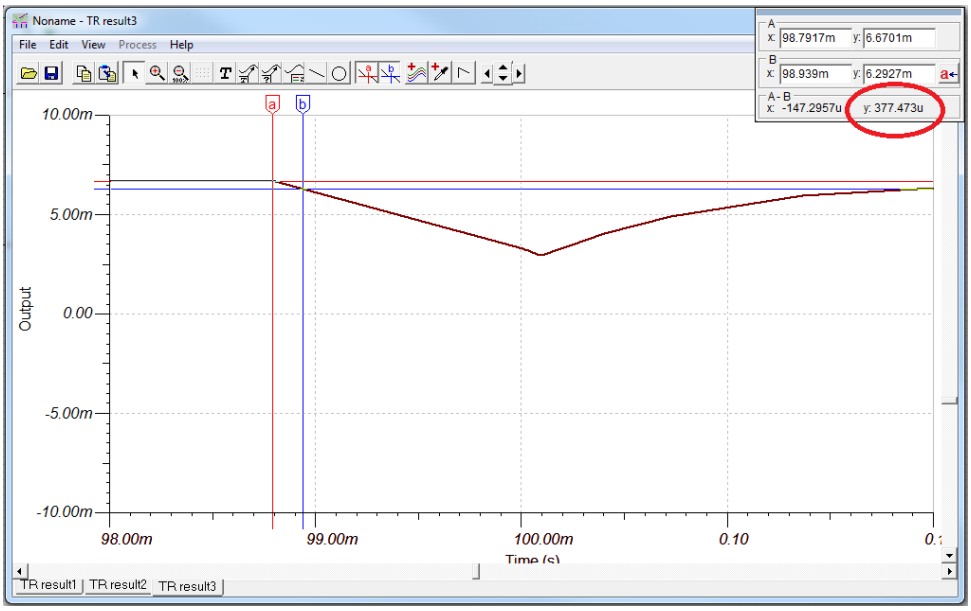

Figure 2 - Input offset during sampling (1kohm and 1uF)

2.2 Temperature Derating

Zener diode leakage can also be derated over temperature, as in Figure 3 from the DDZ9690Q-7 datasheet. This is an AEC-Q100 qualified 5.6V Zener diode with 200nA @4V leakage rating. A similar derating curve will be found with most Zener diodes, but the manufacturer should provide this information.

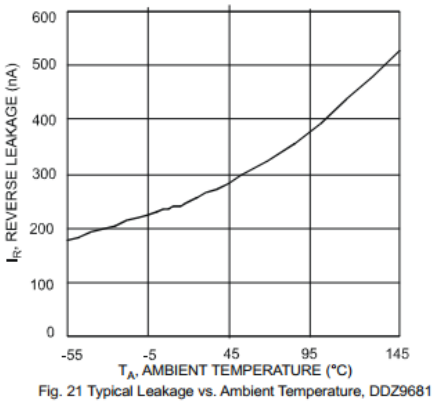

Figure 3 - Zener Leakage Temperature Derating Curve

For these reasons, the Zener diode should be selected for the lowest possible leakage current parameter. Careful analysis of Zener diode specs are required to select an appropriate device for attaching to a cell measurement input.

2.3 Zener Diode Breakdown Voltage

A Zener diode does not start conducting exactly at its breakdown voltage, so careful analysis of the breakdown curves for the potential voltages that could be applied to the Zener diode in normal operation should be done. The typical voltages seen by a Zener diode in this application will be ~2 to 4.5V, accommodating for different cell chemistries and load transients in normal operation. A 5.1V Zener diode will start to partially conduct at 4.5V, which will be a current load on the input filter cap, drawing down the input and producing a significant offset error. Choosing a Zener diode with a higher breakdown voltage raises it above the level where partial breakdown will have a significant effect.

The curve in Figure 4 shows the Zener voltage vs Zener current for the MMSZ5232BT1G. You can see that for a 5.1V device (5.6V not shown for some reason) that at 4.5V, it will be conducting ~10mA. The curve doesn't extend low enough to see, but it can be assumed that a higher Zener voltage will have much lower current at typical cell voltages.

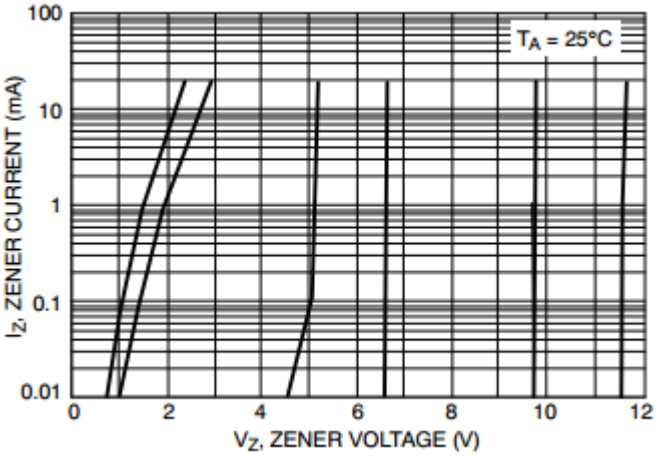

Figure 4 - MMSZ5232BT1G Zener Diode Breakdown Voltage Curve

2.4 Calibration Procedures (Vsense)

The correction procedures in this section apply to the Vsense inputs (including affects contributed by external components between the cells and the Vsense input pins). A separate but similar calibration procedure is available for the AUX inputs.

Two registers are used in this calibration procedure. One affects the gain and is called VSGAIN[], and the other affects the offset and is called VSOFFSET[]. Please refer to the bq76PL455 data manual for additional information about how to address these registers. It is important to understand, the values in these regsiters apply globally to all Vsense inputs.

Because the effects apply globally to all Vsense channels, it is important to decide which channels or sub-set of channels will be used to determine the offset and gain values. Several methods are available from which to choose, however testing has shown the best performance is generally to either include all channels or all channels except the lowest and highest channels. However, any of the following sources can be used:

1. Measure and average all used Vsense inputs (channels 1 to 16 for a fully utilized device)
2. Measure and average all Vsense inputs except channel 1 and the top-most channel (channels 2 to 15 for a fully utilized device)
3. Measure and average only the lowest and highest channel (channel 1 and 16 in a fully utilized device)
4. Measure and use the middle channel (channel 8 for a device which measures 16 inputs)

Although the correction procedures can be performed at any temperature, it is typically performed at room temperature (RT) using a stable, high-accuracy DC source and / or precision voltmeter. The VSGAIN[] and VSOFFSET[] registers contain signed 2's complement values, thus correction values are 0x00 to 0x7f for positive corrections, or 0xff to 0x80 for negative corrections. A zero value in either register indicates no correction. To make corrections, two voltage points are measured. The user's expected minimum and maximum values for the cells can be used, however the lowest VIN_{MIN} value should be greater than or equal to 2.0V, and the highest VIN_{MAX} should be less than or equal to 4.5V.

2.4.1 Gain Correction

Gain Error Correction: -9.77mV to +9.69mV in 255 steps (8 bits) in register VSGAIN[] (for full scale input).

NOTE: It is mandatory that the correction/calibration procedures which follow be performed with both the VSGAIN[] and VSOFFSET[] registers set to an intial value of zero.

*NOTE: For details on how to interpret the ADC conversion values (i.e. ADC VOUTx in the procedures which follow), please refer to the bq76PL455 data manual. Bit weight for the ADC conversion result and the gain and offset values are the same and essentially equate to (2 * VREF)/2^{16}, where VREF is ideally 2.500V. For record keeping purposes it is advisable to record the actual value of VREF measured at the VREF pin of the bq76PL455 along with the calibration measurements and calculated gain and offset data.*

Gain Adjustment Procedure:

1. For each channel, apply voltage VIN1, read back from ADC VOUT1 and record both values.
2. For each channel, apply voltage VIN2, read back from ADC VOUT2 and record both values.
3. Depending on the calculation method chosen for the input (i.e. all channels, channels 2-15, etc.) , calculate the averages of the two sets of values measured in step 1 above. This will result in $VIN1_{AVG}$ and $VOUT1_{AVG.}$
4. Depending on the calculation method chosen for the input (i.e. all channels, channels 2-15, etc.) , calculate the averages of the two sets of values measured in step 2 above. This will result in $VIN2_{AVG}$ and $VOUT2_{AVG.}$
5. Calculate slope m = ($VOUT2_{AVG}$-$VOUT1_{AVG}$) / ($VIN2_{AVG}$-$VIN1_{AVG}$).
6. Find the gain error correction (GEC) in 16 bit format (*5V is used regardless of VINx value*):

$$GEC = \left(\frac{1}{m} - 1\right) * \frac{5}{\left(\frac{5}{2^{16}}\right)} = \left(\left(\frac{1}{m}\right) - 1\right) * 2^{16}$$

Note: The final GEC should be an 8-bit twos-complement value in the range -128 to +127 after discarding the upper 8-bits of the 16-bit value.

*Values exceeding this are suspect and **probably indicate an error**. If such a value must be used, the resulting 8-bit value should be saturated (-128 or +127) and sign corrected as necessary.*
This gain adjustment is input dependent – a correction of 9mV at full scale input, results in a correction of 4.5mV at half scale input.

7. Write the 8-bit value to the VSGAIN[] register
8. Perform the Offset Error Correction step below.

2.4.2 Offset Correction

Offset Error Correction: -9.77mV to +9.69mV in 255 steps (8 bits) in register VSOFFSET[]

Procedure: *(use m, VIN1 (i.e. $VIN1_{AVG}$) and VOUT1 (i.e. $VOUT1_{AVG}$) from the GAIN correction procedure above)*

1. Find the offset error correction (OEC) in 16 bit format

$$OEC = \frac{VIN1 - \left(\frac{1}{m}\right) * VOUT1}{\frac{5}{2^{16}}} = \left(VIN1 - \left(\frac{1}{m}\right) * VOUT1\right) * \frac{2^{16}}{5}$$

*Note: The final OEC should be an 8-bit twos-complement value in the range -128 to +127 after discarding the upper 8-bits of the 16-bit value. Values exceeding this are suspect and **probably indicate an error**. If such a value must be used, the resulting 8-bit value should be saturated (-128 or +127) and sign corrected as necessary.*

2. Write the 8-bit value to the VSOFFSET[] register

NOTE: Although is is recommended to perform both the gain and offset correction, it is also possible to program only an offset correction into VSOFFSET[]. If the VSGAIN[] will not be adjusted, steps 1 and 3 from the gain correction procedure should still be performed to obtain the VINx and VOUTx values, and a gain/slope of m = 1 can be used in the preceding offset correction procedure.

At this point, the gain and offset values are stored only in the RAM registers. If the device is power cycled before these values are tested and confirmed, then these values will be lost. The new values should therefore be tested without power cycling the device by repeating steps 1 through 5 of the gain correction procedure and verifying that the intial errors between VIN and VOUT have been minimized.

If the results are acceptable, the new values in the VSGAIN[] and VSOFFSET[] registers should be committed to EERPOM so they are applied henceforth after a device power cycle. The following steps can be followed to perform this action:

1. Since register values have been changed, the checksum will also require re-calculation and saving due to this (or any) change. The most efficient way to do this is to copy the value from CSUM_RSLT[] to CSUM[].
2. Save the new VSGAIN[], VSOFFSET[] and CSUM[] values to EEPROM by writing 0x8C2DB194 to MAGIC1, 0xA375E60F to MAGIC2, then setting DEV_CTRL[WRITE_EEPROM].

2.4.3 Command Examples

Following are examples of commands which can be used to write and read registers associated with the calibration procedure. These commands assume calibration of a bq76PL455 with ADDR[] (Device

Address) = 0. If ADDR[] is not zero, then the example commands would need to be adjusted accordingly. Refer to the data manual and SLVA617 - Communication Examples application note for further examples of other related commands.

NOTE: In the following examples, all data values are in hexadecimal, but register addresses are given in decimal. If a bq76PL455EVM and GUI are available, the command examples below can be used to implement a rudimentary test of the procedures outlined above.

```
# Read the current OVERSMPL[] value (Oversampling Register at address 7)
81 00 07 00 2A 0C

# Read the current CELL_SPR[] value (Cell and Temperature Sampling Period
Register at address 62)
81 00 3E 00 38 5C

# Read the current CHANNEL[] value (Channel Select Register at address 3-6)
81 00 03 03 68 CD

# Read the current VSOFFSET[] value (User Offset Register at address 210)
81 00 D2 00 74 9C

# Sample at the currently configured settings using CMD[] (Command register
at address 2)
E1 02 00 51 56

# Set VSOFFSET[] to max positive offset (7Fh -> +9.7mV)
# {Substitute the desired value to make a positive offset}
91 00 D2 7F 31 BC

# Read VSOFFSET[] to make sure it was set to desired value
81 00 D2 00 74 9C
```

…OR…

```
# Sample at the above settings with the revised User Offset
E1 02 00 51 56

# Set VSOFFSET[] to max negative offset (80h -> -9.7mV)
# {Substitute the desired value to make a negative offset}
91 00 D2 80 71 FC

# Read VSOFFSET[] to make sure it was set to desired value
81 00 D2 00 74 9C
```

3 Revision History

This section records a brief summary of changes to each revision of this document. For a complete change history, please see the checked in versions in Galileo and view each version in the "Final Showing Markup" mode inside Microsoft Word.

Revision	Date	Author	Description of Changes from Previous Revision
0.1	03/06/2014	Stephen Holland	First release
0.2	03/07/2014	Thomas Schumann	Modified wording in first two sections. Added more detail to save to EEPROM section at end of offset correction procedure in Section 2.4.
0.3	03/07/2014	Thomas Schumann	Changed copyright year to 2014. Changed restriction to TI Confidential – NDA Restrictions.
0.4	03/21/2014	Thomas Schumann	Modified the text describing how to save values to EEPROM and update the checksum (Section 2.4). Added text to the "Reasons to Calibrate" section to include internal reasons and a strong recommendation to always perform final calibration.
0.5	03/24/2014	Stephen Holland	Added note to section 2.1.1 explaining the 150µs sample duration
0.6	8/28/2014	Thomas Schumann	Updated the Calibration Procedures section with additional information and procedural steps. Added text to the introduction regarding bake, conformal coating, etc. Incorporated documented review feedback.