bq76PL455-Q1 16-Cell Battery Monitor with Passive Cell Balancing

1 Features

- Monitors and Balances Up to 16 Cells per Device
- AEC Q-100 Grade 2 with ESD CDM Classification of C3; T_A = –40°C to 105°C
- 8-to-16 Cells per Device, Up to 256-Series Cells
- Designed for Robust Hot-Plug Performance
- High Performance 14-bit 250 kS/s Analog-to-Digital Converter (ADC)
  - All Cells Converted in ≈2.4 ms (nominal)
  - Eight AUX Inputs for Temperature, etc.
  - Internal Precision Band Gap Reference
- Efficient Communications Performance
  - Up to 1-Mbaud Communications
  - Differential Daisy-Chain Without Isolators
- Excellent Electromagnetic Compatibility (EMC) with Low Component Count
  - Bulk Current Injection Test Report Available
- Passive Balancing Control with External N-FETs
- Built-in Self-Tests to Validate Internal Functions
  - Support for Open Wire Detection
  - Monitoring of Internal Voltage Sources
- Automatic Thermal Shutdown
- Built-in Secondary Monitors/Comparators
  - Programmable V_{CELL} Overvoltage (OV) and Undervoltage (UV) Set Points
  - Separate V_{REF} for Comparators
- Configurable Automatic Power Down

2 Applications

- Electric and Hybrid Electric Vehicles
- 48-VDC Systems (Single-Chip Solution)
- Uninterruptible Power Supplies (UPS)
- E-Bikes, E-Scooters

3 Description

The bq76PL455-Q1 is an integrated 16-cell monitor, protector, and cell balancer designed for high-reliability automotive applications with many built-in functional verification features.

A high-speed differential capacitor-isolated communications interface allows up to 16 bq76PL455-Q1 devices to be stacked. The bq76PL455-Q1 communicates with the host via high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, provides up to six general-purpose programmable digital I/O ports, and eight analog AUX ADC inputs.

The device will detect overvoltage, undervoltage, overtemperature, communication, and many other fault conditions. Secondary fault detection circuitry for overvoltage and undervoltage detection is also provided. The device automatically shuts down when a pre-programmed thermal shutdown threshold is reached.

The bq76PL455-Q1 should be powered from the same cells it monitors. The device generates all other required voltages with its internal control loop circuitry.

The bq76PL455-Q1 drives external n-channel field-effect transistors (N-FETs) and power resistors for passive cell balancing.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq76PL455-Q1	TQFP (80)	12.00 mm × 12.00 mm

Simplified Schematic

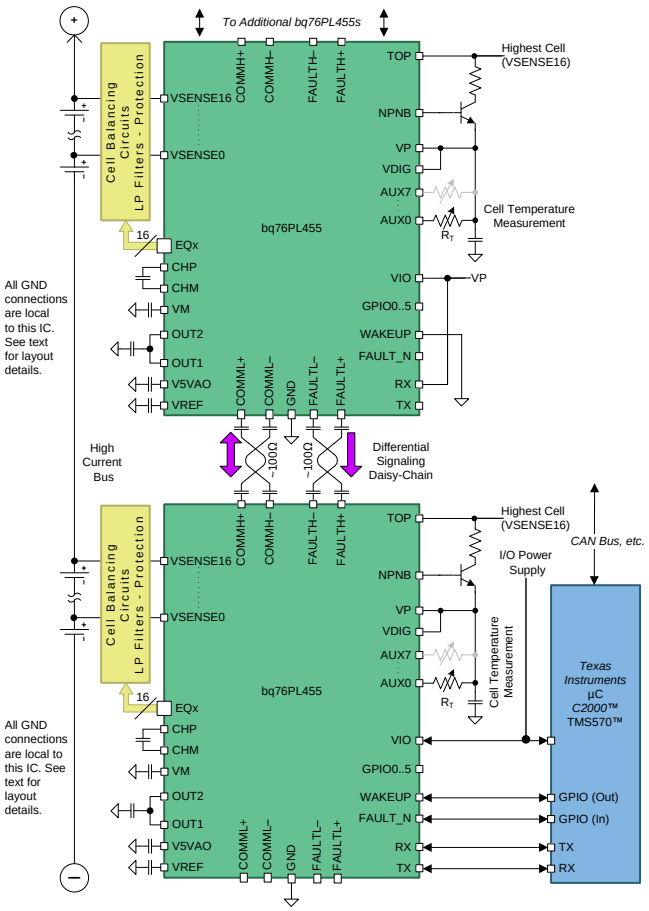


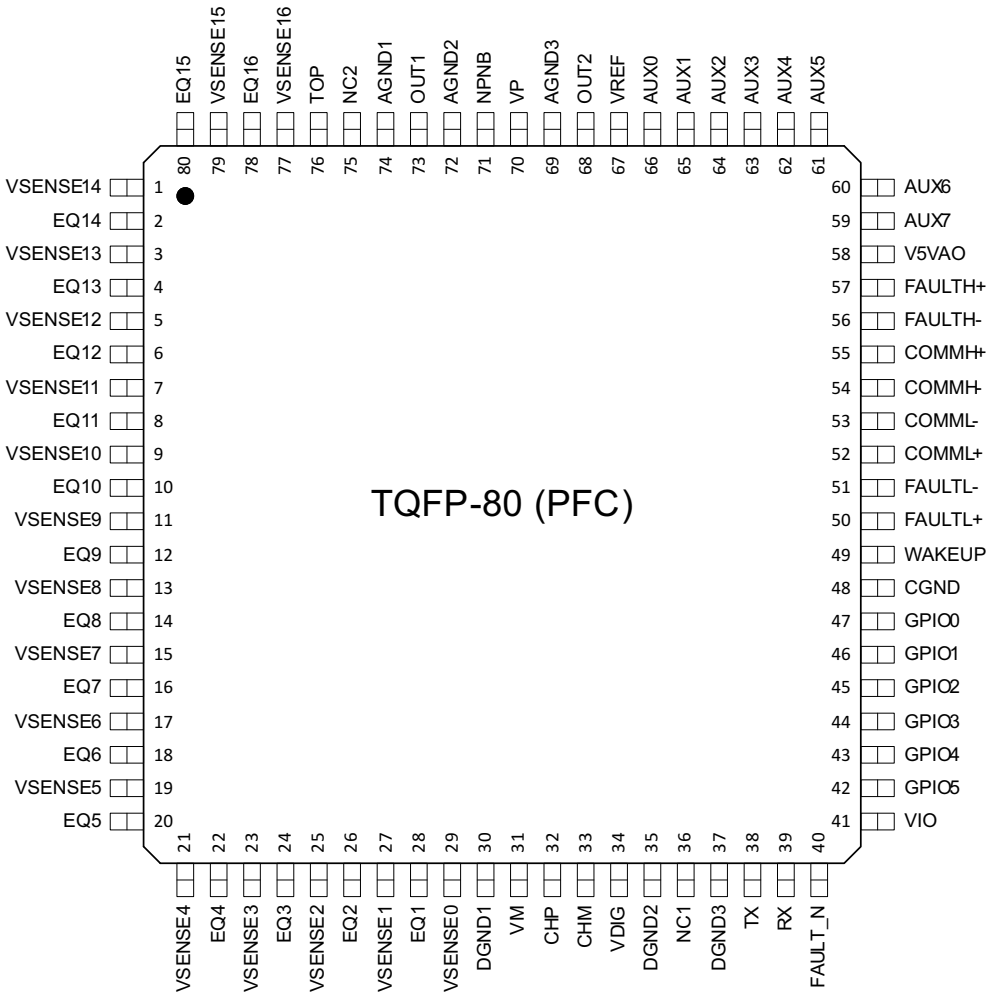
Table of Contents

4 Revision History

DATE	REVISION	NOTES
November 2014	*	Initial Release

5 Pin Configuration and Functions

Top View



Pin Functions

PIN	NO.	TYPE[1]	DESCRIPTION
AGND1	74	P	Analog Ground[2]. Connect to ground plane.
AGND2	72	P	Analog Ground[2] for VREF. Internally shorted to AGND3, this connection should also be made externally in the printed-circuit board (PCB) layout. Connect to ground plane.
AGND3	69	P	Analog Ground[2] for VREF. Internally shorted to AGND2, this connection should also be made externally in the PCB layout. Connect to ground plane.
AUX0	66	AI	Ground referenced general-purpose analog measurement input.
AUX1	65	AI	Ground referenced general-purpose analog measurement input.
AUX2	64	AI	Ground referenced general-purpose analog measurement input.
AUX3	63	AI	Ground referenced general-purpose analog measurement input.
AUX4	62	AI	Ground referenced general-purpose analog measurement input.
AUX5	61	AI	Ground referenced general-purpose analog measurement input.
AUX6	60	AI	Ground referenced general-purpose analog measurement input.
AUX7	59	AI	Ground referenced general-purpose analog measurement input.
CGND	48	P	Communication ground[2]. Connect to ground plane.

Pin Functions (continued)

PIN	NO.	TYPE[1]	DESCRIPTION
CHM	33	P	Charge pump *flying* capacitor connection. Connect a 22-nF ceramic capacitor[3] between this pin and CHP.
CHP	32	P	Charge pump *flying* capacitor connection. Connect a 22-nF ceramic capacitor[3] between this pin and CHM.
COMMH–	54	DIO	Inverting, high-side differential connection to the COMML– pin of the higher adjacent module in a daisy chain. This pin should be left unconnected if not used.
COMMH+	55	DIO	Non-inverting, high-side differential connection to the COMML+ pin of the higher adjacent module in a daisy chain. This pin should be left unconnected if not used.
COMML–	53	DIO	Inverting, low-side differential connection to the COMMH– pin of the lower adjacent module in a daisy chain. This pin should be left unconnected if not used.
COMML+	52	DIO	Non-inverting, low-side differential connection to the COMMH+ pin of the lower adjacent module in a daisy chain. This pin should be left unconnected if not used.
DGND1	30	P	Digital Ground[2]. Connect to ground plane.
DGND2	35	P	Digital Ground[2]. Connect to ground plane.
DGND3	37	P	Digital Ground[2]. Connect to ground plane.
EQ1	28	DO	Cell Equalization control output used to drive an external N-FET balancing cell 1. This pin may be left unconnected if not used.
EQ2	26	DO	Cell Equalization control output used to drive an external N-FET balancing cell 2. This pin may be left unconnected if not used.
EQ3	24	DO	Cell Equalization control output used to drive an external N-FET balancing cell 3. This pin may be left unconnected if not used.
EQ4	22	DO	Cell Equalization control output used to drive an external N-FET balancing cell 4. This pin may be left unconnected if not used.
EQ5	20	DO	Cell Equalization control output used to drive an external N-FET balancing cell 5. This pin may be left unconnected if not used.
EQ6	18	DO	Cell Equalization control output used to drive an external N-FET balancing cell 6. This pin may be left unconnected if not used.
EQ7	16	DO	Cell Equalization control output used to drive an external N-FET balancing cell 7. This pin may be left unconnected if not used.
EQ8	14	DO	Cell Equalization control output used to drive an external N-FET balancing cell 8. This pin may be left unconnected if not used.
EQ9	12	DO	Cell Equalization control output used to drive an external N-FET balancing cell 9. This pin may be left unconnected if not used.
EQ10	10	DO	Cell Equalization control output used to drive an external N-FET balancing cell 10. This pin may be left unconnected if not used.
EQ11	8	DO	Cell Equalization control output used to drive an external N-FET balancing cell 11. This pin may be left unconnected if not used.
EQ12	6	DO	Cell Equalization control output used to drive an external N-FET balancing cell 12. This pin may be left unconnected if not used.
EQ13	4	DO	Cell Equalization control output used to drive an external N-FET balancing cell 13. This pin may be left unconnected if not used.
EQ14	2	DO	Cell Equalization control output used to drive an external N-FET balancing cell 14. This pin may be left unconnected if not used.
EQ15	80	DO	Cell Equalization control output used to drive an external N-FET balancing cell 15. This pin may be left unconnected if not used.
EQ16	78	DO	Cell Equalization control output used to drive an external N-FET balancing cell 16. This pin may be left unconnected if not used.
FAULT_N	40	DO	Single-ended active-low fault output. This pin should be left unconnected if not used.
FAULTH–	56	DI	Inverting, high-side differential connection to the FAULTL– pin of the higher adjacent module in a daisy chain. This pin should be left unconnected if not used.
FAULTH+	57	DI	Non-inverting, high-side differential connection to the FAULTL+ pin of the higher adjacent module in a daisy chain. This pin should be left unconnected if not used.

Pin Functions (continued)

PIN	NO.	TYPE[1]	DESCRIPTION
FAULTL–	51	DO	Inverting, low-side differential connection to the FAULTH– pin of the lower adjacent module in a daisy chain. This pin should be left unconnected if not used.must either
FAULTL+	50	DO	Non-inverting, low-side differential connection to the FAULTH+ pin of the lower adjacent module in a daisy chain. This pin should be left unconnected if not used.
GPIO0	47	DIO	General Purpose I/O. This pin may optionally be used as an external FAULT input or address assignment. *The GPIO pins should not be allowed to float when configured as inputs.*
GPIO1	46	DIO	General Purpose I/O This pin may optionally be used as an external FAULT input or address assignment. *The GPIO pins should not be allowed to float when configured as inputs.*
GPIO2	45	DIO	General Purpose I/O. This pin may optionally be used as an external FAULT input or address assignment. *The GPIO pins should not be allowed to float when configured as inputs.*
GPIO3	44	DIO	General Purpose I/O This pin may optionally be used as an external FAULT input or address assignment. *The GPIO pins should not be allowed to float when configured as inputs.*
GPIO4	43	DIO	General Purpose I/O This pin may optionally be used as an external FAULT input or address assignment. *The GPIO pins should not be allowed to float when configured as inputs.*
GPIO5	42	DIO	General Purpose I/O. This pin may optionally be used as an external FAULT input. *The GPIO pins should not be allowed to float when configured as inputs.*
NC1	36	NC	Do not connect to this pin. *This pin must remain floating for correct operation.*
NC2	75	NC	Do not connect to this pin. *This pin must remain floating for correct operation.*
NPNB	71	AO	Internal voltage regulator controller output pin. Connect to the base of the external NPN transistor. Leave unconnected if not used.
OUT1	73	AO	Analog mux output. Connect a 390-pF filter capacitor type C0G or NP0 between this pin and AGND. Connect externally to pin OUT2. Internally tied to pin OUT2.
OUT2	68	AI	ADC input pin. Connect externally to pin OUT1. Internally tied to pin OUT1.
RX	39	DI	Single-ended UART receive input. This pin must be either: • Driven from a UART signal OR • Pulled up to VIO This pin should not be allowed to float at any time.
TOP	76	P	Power supply input and module voltage-measurement pin. Connect to the top cell of the module through a series resistor. A decoupling capacitor[3] from TOP to the ground plane is required. See *TOP Pin Connection* for details. Locate decoupling capacitor as close to pin as possible. The low-pass filter created by the RC should have a tau similar to the low-pass filter used in the VSENSE circuits. See *VP Regulated Output* or *bq76PL455-Q1 Design Reference Manual* (TIDU245) for component selection details.
TX	38	DO	Single-ended UART transmit output. This pin should be left unconnected if not used.
V5VAO	58	P	Connection to internal 5-V always-on supply. Decouple with a 4.7-µF capacitor[3] connected to the ground plane. Locate decoupling capacitor as close to pin as possible. This pin should not be used to supply external circuitry.
VDIG	34	P	5.3-V Digital Supply input. Always connect VDIG to VP with 1-Ω resistor. Decouple with 4.7-µF and 0.1-µF capacitors[3] in parallel to the ground plane. Locate decoupling capacitors as close to the VDIG pin as possible.
VIO	41	P	3-V to 5-V power input for IO supply. This pin should be connected to the same power supply that is used to drive the source/receiver for the GPIO, FAULT_N, RX, and TX pins. Typically, this pin is connected to VP/VDIG for all devices except the base device in the stack. In the base (or single) device, this pin is typically driven from the same supply as the microcontroller I/O pins. If VP/VDIG is connected as the power source, this pin should be decoupled with a 0.1-µF capacitor[3] to the digital ground plane. Place a 1-Ω resistor in series from VP to VIO. Locate the decoupling capacitor as close to the VIO pin as possible. If another supply is used, decouple with parallel 10-µF and 0.1-µF capacitors[3].
VM	31	P	Internal –5V charge pump output. Decouple with 4.7-µF and 0.1-µF capacitors[3] in parallel to the ground plane. Locate decoupling capacitor as close to pin as possible.
VP	70	P	5.3-V regulated analog power supply input/sense pin. Connect to external NPN transistor's emitter and decouple with a 0.1-µF capacitor[3] to AGND and a 4.7-µF capacitor[3] in series with a 0.390-Ω resistor to GND. Locate decoupling capacitors as close to the VP pin as possible. Always connect VDIG to VP with 1-Ω resistor.

Pin Functions (continued)

PIN	NO.	TYPE(1)	DESCRIPTION
VREF	67	P	VREF output filter pin. Decouple with parallel 0.1-µF and 1.8-µF (25 V+) capacitors(3) to the ground plane. Locate decoupling capacitors as close to the pin as possible. To maintain measurement fidelity, no external loads should be placed on this pin.
VSENSE0	29	AI	To be connected to the negative pin of the 1st cell.
VSENSE1	27	AI	Channel 1. To be connected to the positive pin of the 1st cell.
VSENSE2	25	AI	Channel 2. To be connected to the positive pin of the 2nd cell.
VSENSE3	23	AI	Channel 3. To be connected to the positive pin of the 3rd cell.
VSENSE4	21	AI	Channel 4. To be connected to the positive pin of the 4th cell.
VSENSE5	19	AI	Channel 5. To be connected to the positive pin of the 5th cell.
VSENSE6	17	AI	Channel 6. To be connected to the positive pin of the 6th cell.
VSENSE7	15	AI	Channel 7. To be connected to the positive pin of the 7th cell.
VSENSE8	13	AI	Channel 8. To be connected to the positive pin of the 8th cell.
VSENSE9	11	AI	Channel 9. To be connected to the positive pin of the 9th cell.
VSENSE10	9	AI	Channel 10. To be connected to the positive pin of the 10th cell.
VSENSE11	7	AI	Channel 11. To be connected to the positive pin of the 11th cell.
VSENSE12	5	AI	Channel 12. To be connected to the positive pin of the 12th cell.
VSENSE13	3	AI	Channel 13. To be connected to the positive pin of the 13th cell.
VSENSE14	1	AI	Channel 14. To be connected to the positive pin of the 14th cell.
VSENSE15	79	AI	Channel 15. To be connected to the positive pin of the 15th cell.
VSENSE16	77	AI	Channel 16. To be connected to the positive pin of the 16th cell.
WAKEUP	49	DI	Wakeup input. This pin should be pulled low or tied to ground if not used. *This pin should not be allowed to float at any time.*

(1) Key: AI = analog input; AO=analog output; DI = digital input; DO= digital output; DIO= digital I/O; P= Power; NC= no connect.

(2) These pins are externally connected as common ground or GND in the design. See *Grounding* for details.

(3) All capacitors are type X7R or better, unless otherwise noted.

6 Specifications

6.1 Absolute Maximum Ratings

Over specified Ambient Temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
AUX0–7	Lesser of two MAX values	–0.3	6 or (VP + 0.3)	V
COMMH+, COMMH–, COMML+, COMMH–, FAULTH+, FAULTH–, FAULTL+, FAULTL–	Lesser of two MAX values	–0.3	6 or (V5VAO + 0.3)	V
	AC pulse specification(3) for these eight pins only: V_{pk} maximum ≤ 6.5 V for 100 ns or less, 100 kHz ≤ f ≤ 400 MHz	–0.3	6.5	V_{pk}
GPIO0–5	Lesser of two MAX values	–0.3	6 or (VIO + 0.3)	V
RX	Lesser of two MAX values	–0.3	6 or (VIO + 0.3)	V
TOP (4)		–0.3	88	V
TOP to VSENSE16 delta(4)(5)	(VSENSE16 + 5.5 V) ≥ TOP ≥ (VSENSE16 – 1 V)	(VSENSE16 – 1 V)	(VSENSE16 + 5.5 V)	V
VDIG		–0.3	6	V
VIO		–0.3	6	V
VP		–0.3	6	V
VSENSE0		–0.3	0.3	V
VSENSEn – VSENSEn–1; n=1 to 16		–0.3	5.5	V
WAKEUP		–0.3	6	V
Ambient free-air temperature range (T_A)		–40	105	ºC
Junction temperature range (T_J)		–40	125	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Unless otherwise noted, voltages are given with respect to device commons (AGND1–3, DGND1–3, CGND) tied together (device VSS or GND).
(3) Specified by design, not tested in production.
(4) All stated conditions for the TOP pin must be met at all times.
(5) The highest-connected cell must be shorted to the unused VSENSEn inputs above it in configurations that use < 16 cells. For example, a 14-cell configuration must short pins VSENSE14, VSENSE15, VSENSE16.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{STG}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM, per Automotive Electronics Council (AEC) Q100-002(1)		–2	2	kV
		Charged device model (CDM) ESD stress voltage, per AEC Q100-011	Corner pins (1, 20, 21, 40, 41, 60, 61, 80)	–750	750	V
			Pin 76	-450	450	
			Other pins	–500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and TOP = 57.6 V; Min/Max values stated where T_A = –40°C to 105ºC and TOP = 16 V to 79.2 V, unless otherwise noted.

			MIN	NOM	MAX	UNIT
V_{TOP}	Supply voltage	TOP – GND (VSENSE16 = TOP)	16	—	79.2	V
V_{IO}	Digital interface voltage		2.7	—	5.5	V
V_{TOP_DELTA}	Max delta, TOP to highest cell (1)(2)	TOP – VSENSE16	—	0	–300	mV
$I_{I/O}$	Output current, any one pin	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, TX, FAULT_N	—	—	5	mA
I_{I/O_T}	Output current, sum of	GPIO0 + GPIO1 + GPIO2 + GPIO3 + GPIO4 + GPIO5 + TX + FAULT_N	—	—	20	mA

(1) V_{SENSE} input measurement accuracy is degraded when V_{TOP_DELTA} is exceeded, but the delta is less than the limit in the *Absolute Maximum Ratings* table.
(2) The highest-connected cell must be shorted to the unused VSENSEn inputs above it in configurations that use < 16 cells. For example, a 14-cell configuration must short pins VSENSE14, VSENSE15, and VSENSE16.

6.4 Thermal Information

THERMAL METRIC(1)		TQFP (PFC) 80 PINS	UNIT
$R_{\theta JA,\ High\ K}$	Junction-to-ambient thermal resistance(2)	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	6.4	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	21.5	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	21	
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance(7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics: Supply Current(1)

The following applies to all Electrical Characteristics in the tables below, unless otherwise noted: TYP values are stated in each table where VP = VDIG = 5.3 V, VIO = 5 V, T_A = 25°C and V_{CELL} = 3.6 V (V_{CELL}= VSENSEn – VSENSEn–1; n=1 to 16), TOP = 57.6 V. MIN/MAX values are stated where VP = VDIG = 5.3 V, VIO = 5 V, –40°C ≤ T_A ≤ 105ºC, 1 V < V_{CELL} < 4.95 V, 16 V ≤ TOP < 79.2 V and GND = 0 V. All measurements requiring the use of the ADC were taken with VREF = 2.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IDLE}	Total input current from the monitored cells.	Power state: IDLE(2)	4	5	7	mA
I_{TOP_IDLE}	Input current into TOP pin, IDLE mode	Power state: IDLE(2)	250	350	450	µA
I_{SLEEP}	Total input current from the monitored cells into TOP pin, 0°C to 65°C	Power state: SHUTDOWN(3) VP = VDIG = VIO = 0 V, TOP = 57.6	—	22	75	µA
	Total input current from the monitored cells into TOP pin, –40°C to 105°C	Power state: SHUTDOWN(3) VP = VDIG = VIO = 0 V, TOP = 57.6	—	22	3600	µA
I_{ACTIVE}(4)	Total input current from the monitored cells while communicating.	Power state: IDLE plus comms(5), differential comm capacitance 70 pF, no load on GPIO.	—	8	—	mA
I_{VIO_IDLE}	VIO input current	Power state: IDLE(2)	—	40	—	µA
I_{SLP_DELTA}	Delta $I_{SHUTDOWN}$ between ICs in a stack	T_A = 25°C ± 5°C for all ICs	—	4	3600	µA

(1) All internal pull-up and pull-down resistors are disabled and their current is not included in parameters listed in this table.
(2) IDLE mode defined as: device awake, ready for communications, and not communicating.
(3) SHUTDOWN mode defined as: test conditions, no communications, no wakeup tone activity, and no FAULT heartbeat.
(4) Specified from characterization.
(5) ACTIVE mode defined as: UART, differential communications link, and FAULT heartbeat active.

6.6 VP 5.3-V Supply Regulation Voltage

Pins VP, NPNB

Characteristics stated using NPN transistor in circuit rated at BV_{CEO} > 100V, β ≥ 100 at 5 mA, Base-Collector C ≤ 35 pF, $I_{COLLECTOR}$ > 100 mA, $R_{COLLECTOR}$ = 400 Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP_{VR}	Regulated Voltage		5.1	5.3	5.5	V
I_{NPNB}	External NPN base drive current		0.5	—	—	mA
VP_{SD_DLY}	VP/VDIG delay before SHUTDOWN(1)		30	75	160	ms

(1) Time measured from VP falling below threshold until the part enters SHUTDOWN, or from the part attempting to exit SHUTDOWN (wakeup) until re-entering SHUTDOWN.

6.7 VDD18 1.8-V Internal Digital Supply(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VDD18_{VO}$	VDD18 Output voltage(1)	As measured by internal ADC	1.7	1.8	1.9	V

(1) Internal node only, no external access. This parameter is supplied for internal measurement and verification purposes only.

6.8 V5VAO Analog Supply

Pin V5VAO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V5VAO_{SD}$	Output Voltage	Power state: SHUTDOWN, VP = VDIG = VIO = 0 V	4.0	4.7	5.3	V
$V5VAO_{IDLE}$	Output Voltage	Power state: IDLE(1), unloaded	VDIG – 0.500	—	VDIG	V

(1) VDIG internally connected to V5VAO in IDLE mode.

6.9 VM –5V Integrated Charge Pump

Pin VM

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VM_{VM_ON}	VM Output Voltage		–5.5	–5	–4.5	V
f_{CP}	Charge pump switching frequency		—	375	—	kHz
VM_{TRIP}	VM low-voltage monitor trip point		—	–3.8	—	V
VM_{VO}	Measured value read back from ADC VM monitor		–5.56	–5	–4.54	V

6.10 Analog-to-Digital Converter (ADC): Analog Front End

All ADC specifications are stated for the sampling intervals and register settings shown in Table 3. A 390-pF capacitor is used on pin OUT1. The low-pass filter components consist of a 100-Ω resistor in series with the cell input (VSENSEn; n=1 to 16) and 0.1-µF capacitor connected to ground.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$OUT1_{RANGE}$	Pin OUT1 Analog Front End / Level Shifter output voltage range		0	—	VP	V
R_{OUT_PIN}	OUT1 pin internal series resistance		1.10	1.20	1.35	kΩ

6.11 ADC: VSENSEn Cell Measurement Inputs

Pins VSENSE0… VSENSE16

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CELL_VR}	Input voltage range	V_{CELL}= VSENSEn – VSENSEn–1, n=1 to 16	1	—	4.95	V
$V_{CHANERR65}$	Total Channel Measurement Accuracy(1)(2) (3)	VSENSE = 3.6 V, 0°C ≤ T_A ≤ 65°C	–20.0	2.6	20.0	mV
		VSENSE = 4.5 V, 0°C ≤ T_A ≤ 65°C	–24.3	3.9	24.3	mV
$V_{CHANERR105}$	Total Channel Measurement Accuracy(1)(2) (3)	VSENSE = 3.6 V, –40°C ≤ T_A ≤ 105°C	–20.4	2.8	20.4	mV
		VSENSE = 4.5 V, –40°C ≤ T_A ≤ 105°C	–24.7	3.9	24.7	mV
I_{SENSE_SEL}(4)(5)	VSENSEn input current n = 1 to 16	VSENSEn–1 pin; on selected channel	—	2	5	µA
I_{SENSE_NSEL}		Channel not selected	—	< ±100	—	nA
I_{SENSE_SD}		VSENSEn input current in SHUTDOWN Mode	—	< ±100		nA
R_{SENSE_SEL} (5)	VSENSE input resistance	Channel selected for conversion, measured differentially [VSENSEn – VSENSE(n – 1)]	—	1	—	MΩ
OWD_{SR}	Open-wire detection shunt resistance	Open-wire test mode, TSTCONFIG[4] = 1 all odd (CBENBL = 0xAA); or all even (CBENBL = 0x55) cell "squeeze" resistors on (alternate resistors only)	4	5	6	kΩ
LT_Drift_{VCHAN}(6)(7)	Long-term drift (total channel path)	VSENSE = 3.6 V, T_A = 30°C	—	35.7	—	ppm/ 1000 hours

(1) User adjustable Gain and Offset registers are provided for further error trim at VSGAIN and VSOFFSET, respectively.
(2) Calculated and statistically projected worst case from characterization data. Not tested in production.
(3) Error measured with Averaging enabled.
(4) When the bq76PL455 is in IDLE power mode, but not converting any ADC input channel, the part idles the multiplexer on the highest channel enabled for conversions in the CHAN register.
(5) The current into VSENSEn = ISENSE_SEL + VCELL/RSENSE_SEL.
(6) Typical based on characterization data, not tested in production.
(7) Based on 408-hours HTOL at stress temperature of 125 °C and operating temperature of 55 °C. Equivalent to 31,637 hours of operation (3.6 years).

6.12 ADC: V_{MODULE} Input

Pin Top

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{MODULE_VR}	Input voltage range	Measured from TOP to GND (AGND1)	V_{TOP} MIN	—	V_{TOP} MAX	V
V_{MODULE_ERR65}	Total error from all internal sources	T_A = 0°C to 65°C	–1	±0.1	1	V
V_{MODULE_ERR105}		T_A = –40°C to 105°C	–1	±0.1	1	V

6.13 ADC: AUXn General Purpose Inputs

Pins AUX0… AUX7

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AUX_VR}	Input voltage range(1)	VP/VDIG = 5.3 V	0	—	5	V
$V_{AUXERR65}$	Total AUX Channel Measurement Accuracy(2)	VAUX = 0.05 V, 0°C ≤ T_A ≤ 65°C	–4.6	0.1	4.9	mV
		VAUX = 4.95 V, 0°C ≤ T_A ≤ 65°C	–21.6	0.1	24.5	mV
$V_{AUXERR105}$	Total AUX Channel Measurement Accuracy(2)	VAUX = 0.05 V, –40°C ≤ T_A ≤ 105°C	–7.1	0.1	7.4	mV
		VAUX = 4.95 V, –40°C ≤ T_A ≤ 105°C	–24.1	0.1	27.0	mV
I_{DCL_AUX}	DC Leakage Current	Channel not selected for conversion, TESTAUXPU = 0	—	< ±0.1	—	µA
R_{IN_AUX}(1)	Equivalent input resistance	Channel selected In Acquisition Mode	—	>3	—	MΩ
C_{AUX}(1)	Input capacitance	Channel selected	—	30	—	pF
R_{AUX_PU}	Internal switched pull-up resistor per AUXn input, supplied from VP pin	TESTAUXPU[n] = 1; n = 0 to 7	18	26	40	kΩ

(1) Specified by design, not tested in production.
(2) Calculated and statistically projected worst case from characterization data. Not tested in production.

6.14 ADC: Internal Temperature Measurement and Thermal Shutdown (TSD)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{INT_AD}(1)	Internal temperature accuracy of analog die		–7	3	13	°C
T_{INT_DD}(1)	Internal temperature accuracy of digital die		–34	8	54	°C
TSD_T(2)	Thermal shutdown, junction temperature both analog and digital dies	Increasing temperature	115	140	—	°C

(1) Specified from characterization data, not tested in production.
(2) Specified by design, not tested in production.

6.15 Passive Balancing Control Outputs

Pins EQ1...EQ16

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EQ_{SR_OFF}	Output resistance, internally in series with driver	EQn = 0 (OFF)	1.2	1.5	1.8	kΩ
EQ_{SR_ON}		EQn = 1 (ON)	1.9	2.3	2.9	kΩ
EQ_{VMIN}(1)	Cell voltage required for balancing		1.8	—	—	V
$VS1_{MIN}$	VSENSE1 minimum voltage for balancing(2)		1.8	—	—	V

(1) In the event of an open wire condition, if TSTCONFIG[EQ_SQUEEZE_EN] = 1 and this causes EQVMIN to be violated, it may be necessary to power down the device to disable the squeeze resistor.
(2) VSENSE1 minimum voltage required for correct operation of any or all EQn outputs. If VSENSE1 falls below this value, any or all other EQ outputs may fail to assert when requested. The opposite is not true; outputs will not unintentionally assert when set to the OFF state.

6.16 Digital Input/Output: VIO-Based Single-Ended I/O

Pins VIO, TX, RX, FAULT_N, GPIO0…GPIO5

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Logic-level output-voltage high FAULT_N, TX, GPIO	I_{LOAD} = 5 mA	VIO – 0.7	—	VIO	V
V_{OL}	Logic-level output-voltage low FAULT_N, TX, GPIO	I_{LOAD} = 5 mA	DGND	—	0.7	V
V_{IH}	Logic-level input-voltage high RX, GPIO		VIO – 0.7	—	—	V
V_{IL}	Logic-level input-voltage low RX, GPIO		—	—	0.7	V
C_{DIG_IN}	Input Capacitance(1) RX, GPIO		—	5	—	pF
R_{PU}	GPIO0..5 pull-up resistor		13	17	23	kΩ
R_{PD}	GPIO0..5 pull-down resistor		16	22	31	kΩ
I_{LKG}	Input leakage source/sink current RX, GPIOx		—	< ±1	—	µA
$RXTX_{BAUD}$	RX/TX signaling rate(2)(3)		125	—	1000	kbaud
ERR_{BAUD_RX}	Input Baud rate error(1)		–3%	—	3%	
ERR_{BAUD_TX}	Output Baud rate error(1)		–1.5%	—	1.5%	
t_{COMM_BREAK}	Communications Clear (Break)(1)		10	—	15	bit periods
t_{COMM_RESET}	Communications Reset(1)		200	—	—	µs

(1) Specified by design, not tested in production.
(2) Defaults: RX = TX = 250 kBd at communications RESET or (factory set) EEPROM setting at POR.
(3) Discrete rates only, not continuously variable.

6.17 Digital Input/Output: Daisy Chain Vertical Bus

Pins COMML+, COMML–, COMMH+, COMMH–, FAULTL+, FAULTL–, FAULTH+, FAULTH–

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH\_DCC\_TX}$	Logic level output voltage high	Single driver loaded, I_{LOAD} = 5mA	VDIG – 1	—	VDIG	V
$V_{OL\_DCC\_TX}$	Logic level output voltage low	Single driver loaded, I_{LOAD} = 5mA	GND	—	1	V
T_{PD}	Internal propagation delay, COMML to COMMH(1)		—	< 60	—	ns
$T_{DCC\_BIT\_TIME}$	Diff. Comms. Bit Time(1)		—	250	—	ns
f_{WAKE_TONE}	WAKE TONE frequency(1)	50% duty-cycle WAKE TONE transmitted on differential pins COMMH+/COMMH–	—	100	—	kHz
$t_{WAKE\ TONE}$	WAKE TONE duration(1)	WAKE TONE transmitted on differential pins COMMH+/COMMH–	—	1	—	ms

(1) Specified by design, not tested in production.

6.18 Digital Input/Output: Wakeup

Pin WAKEUP

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_WAKEUP}	WAKEUP high-input voltage		2.3	—	—	V
V_{IL_WAKEUP}	WAKEUP low-input voltage		—	—	0.7	V
t_{WAKEUP_HOLD} (1)	WAKEUP hold time (high-pulse width)	Pulse driven 0-1-0	100	—	—	µs
t_{WAKEUP_DLY}	Delay(2) between WAKEUP pin assertion and WAKETONE transmission	After POR exit conditions are met.	—	—	0.5	ms
$t_{WAKE\ TONE\ DELAY\_DC}$	Delay(2)(3) between start of WAKETONE received and WAKETONE transmission	After POR exit conditions are met.	——	—	1	ms
$t_{WAKEUP\_TO\_DCOMM}$	Required delay from WAKETONE transmission to ready for differential communications (4)		—	—	1.1	ms
$t_{WAKEUP\_TO\_UART}$	Required delay from WAKETONE transmission to ready for UART communications(4)		—	—	200	µs

(1) Pulses shorter than 100 µs may wake the device, but 100 µs must be maintained to assure start up.
(2) Internal IC delay only, after VP/VDIG/VIO/VREF are above POR thresholds.
(3) Environmental noise may affect tone detection.
(4) Specified by design, not tested in production.

6.19 EEPROM

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EE_{PGM} (1)	EEPROM total program time(2)	No writes to the device are allowed during the programming cycle	—	210	500	ms
EE_{CYCLES}	Erase / Program cycles(2)		—	—	5	cycles
EE_{RETN}	Data retention(2)		10	—	—	years

(1) EEPROM should be programmed at temperatures less than 30°C.
(2) Specified by design, not tested in production.

6.20 Secondary Protector – Window Comparators

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OV_{RANGE}	Over-voltage comparator register set-point limits(1)		2	—	5.175	V
UV_{RANGE}	Under-voltage comparator register set-point limits(1)		0.7	—	3.875	V
$OVUV_{STEP}$	Threshold step resolution		—	25	–	mV
ERR_{CMP_UV}	Total UV threshold error (includes $ERR_{VCOMP\_REF\_45}$)	Vin = 0.7 to 3.875 V	–80	—	80	mV
$ERR_{CMP\_UV\_EXT}$	UV threshold error when range-extend bit is set	COMP_UV[CMP_TST_SHF_UV] = 1	–130	—	130	mV
ERR_{COMP_OV}	Total OV threshold error (includes ERRVCOMP_REF_45)	Vin = 2 to 5.175 V	–50	—	50	mV
$ERR_{COMP\_OV\_EXT}$	OV threshold error when range-extend bit is set	COMP_UV[CMP_TST_SHF_OV] = 1	–60	—	60	mV
V_{COMP_HYST}	Threshold hysteresis	Hysteresis enabled; DEVCONFIG[COMP_HYST_EN] = 1	50	85	130	mV
T_{COMP_UV}	UVP Response time	Overdrive = 100 mV	—	20	—	µs
T_{COMP_OV}	OVP Response time	Overdrive = 100 mV	—	20	—	µs
$V_{COMP\_REF\_45}$	Comparator reference	Measured by ADC	—	4.5	—	V
$ERR_{VCOMP\_REF\_45}$	Comparator reference error	0°C ≤ T_A ≤ 65°C, measured by ADC	–22	–7	9.5	mV
		–40°C ≤ T_A ≤ 105°C, measured by ADC	–27	–7	15	mV

(1) Normal range specification. Ranges can be extended by using the COMP_UV[CMP_TST_SHF_UV] and COMP_OV[CMP_TST_SHF_OV] bits. See register bit description in *Table 5* for additional details.

6.21 Power-On-Reset (POR) and FAULT Flag Thresholds

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP_{FLT_TRIP}	VP_FAULT voltage threshold, analog die	Falling VP	4.3	4.5	4.7	V
		Rising VP	4.3	4.5	4.7	
VM_{FLT_TRIP}	VM_FAULT voltage threshold, analog die	Falling VM (more negative)	–4.2	–4	–3.8	V
		Rising VM (more positive)	–3.9	–3.8	–3.7	
$DDIE_{POR}$	VP/VDIG POR voltage threshold, digital die	Falling voltage, VP connected to VDIG	3.9	4.15	4.4	V
		Rising voltage, VP connected to VDIG	4.1	4.5	4.7	
$V5VAO_{SD}$	V5VAO SHUTDOWN voltage threshold, digital die	Falling V5VAO	1.8	2.3	2.8	V
		Rising V5VAO	—	2.5	—	V
VIO_{POR}	VIO POR voltage threshold, digital die	Falling VIO	2.1	2.3	2.5	V
		Rising VIO	2.3	2.5	2.7	
VIO_{SD_DLY}	VIO delay before SHUTDOWN	VIO ≤ VIO_{POR}	35	57	100	ms

6.22 Miscellaneous

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Main oscillator frequency (±1.5%)		47.28	48	48.72	MHz
f_{HBEAT}	Fault tone (heartbeat) frequency at pins FAULTL±	No fault condition present, heartbeat enabled	—	10	—	kHz
HB_{PULSE}	Fault heartbeat pulse width at pins FAULTL±	No fault condition present, heartbeat enabled	—	125	—	ns
t_{CKSUM_USER}	Time to complete User-space checksum test(1)		—	—	5	ms
t_{CKSUM_TI}	Time to complete TI-space checksum test(1)		—	—	5	ms

(1) Specified by design, not tested in production.

6.23 Typical Characteristics

This section contains plots of typical data taken from characterization testing. For Figures 2 and 3, VREF is trimmed to 2.500 V at each temperature shown. For Figures 2, 3, 5, and 6, data for temperature 115°C are shown for reference only; normal operating range is –40°C to 105°C.

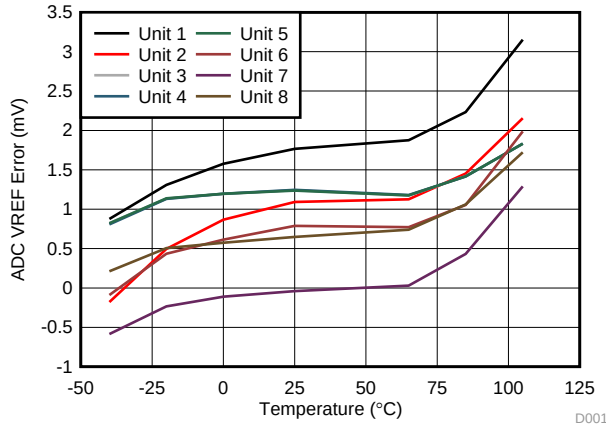


Figure 1. ADC VREF Error (mV)

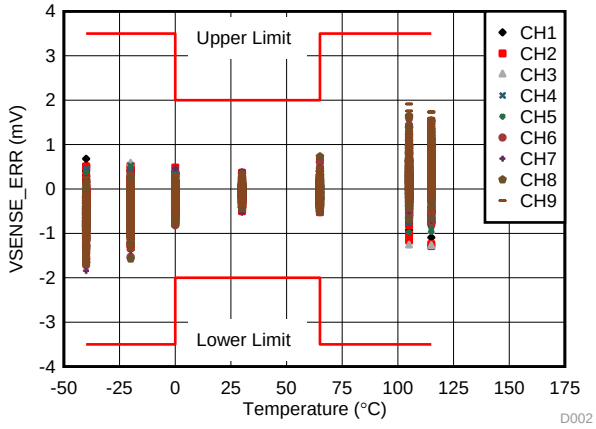


Figure 2. VSENSE Error at 3.6 V Across Temperature

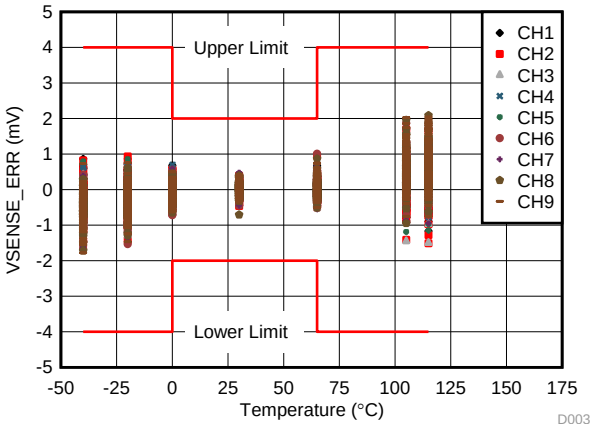


Figure 3. VSENSE Error at 4.5 V Across Temperature

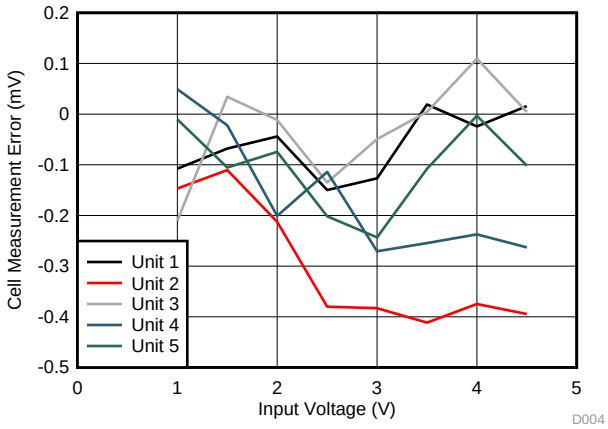


Figure 4. Typical Cell Measurement Error at 25°C

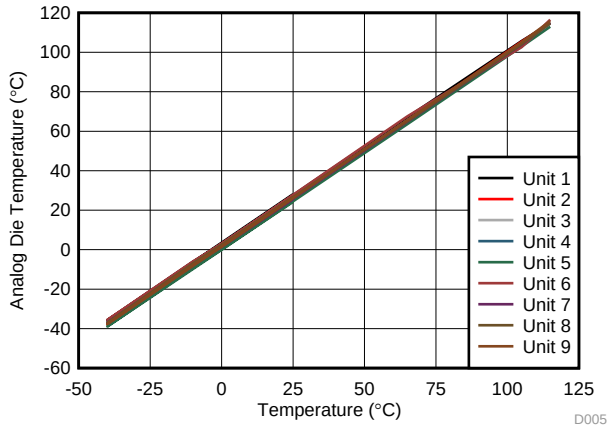


Figure 5. Analog Die Temperature Versus Temperature

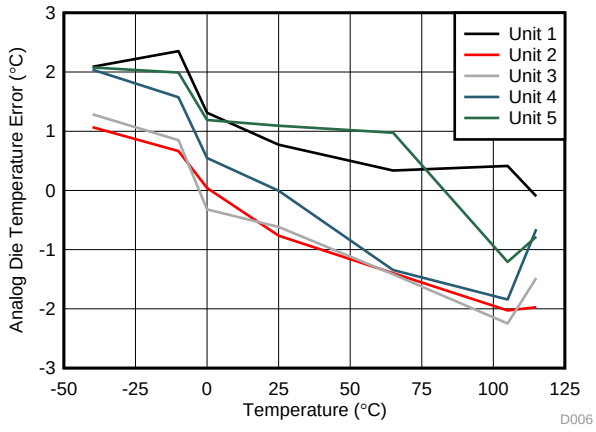


Figure 6. Analog Die Temperature Error Versus Temperature

7 Detailed Description

7.1 Overview

The bq76PL455-Q1 is an integrated 16-cell monitor, protector, and cell balancer designed for high-reliability automotive applications with many built-in functional verification features.

Up to 16 bq76PL455-Q1 devices can be connected in series using the high-speed differential communications interface, which has been evaluated for compliance with Bulk Current Injection (BCI) standards. This capacitor-isolated communications link provides effective common-mode noise rejection. The bq76PL455-Q1 communicates with the host via high-speed UART interface. The bq76PL455-Q1 provides up to six general-purpose, programmable, digital I/O ports, as well as eight AUX ADC inputs, typically used to monitor externally supplied temperature sensors. The digital I/O ports can be configured to generate faults based on conditions set in register GP_FLT_IN. These faults can be further configured to indicate a fault on the FAULT_N output pin.

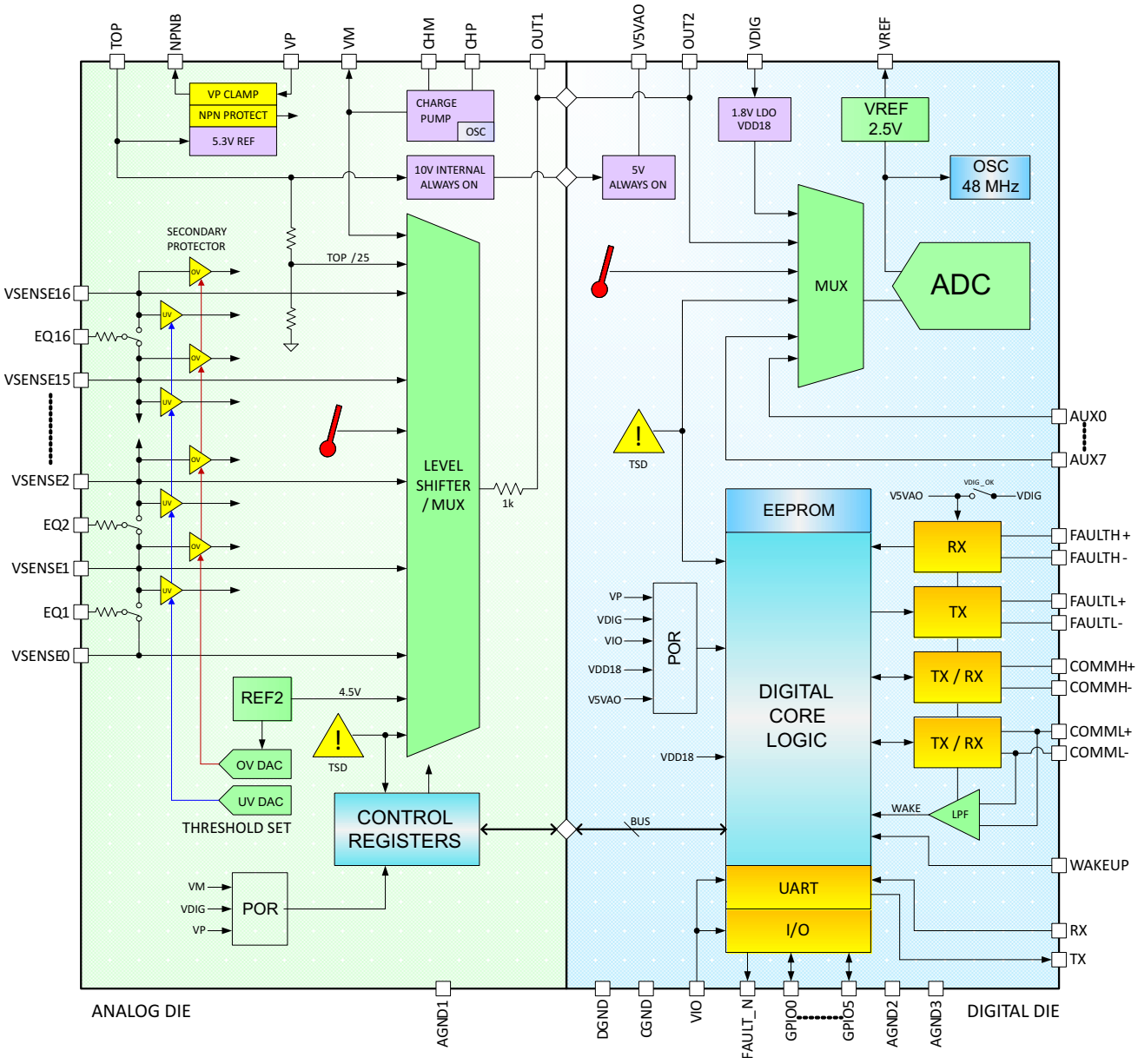
Designed for high-reliability automotive applications, the bq76PL455 includes many functional blocks and self-diagnostic test features covering defined single fault conditions in the analog and digital blocks. The host microcontroller is notified of faults via a separate communications path. The device contains user-selectable self-test features to diagnose functional blocks within the device, such as automatic shutdown in the event of over temperature, calibration integrity, and so forth. A Safety Manual is available upon request for reference to aid the user in the evaluation of the bq76PL455's built-in test features.

A built-in secondary protection block, with two dedicated programmable comparators per cell input, is provided for independently sensing and reporting over-voltage and under-voltage conditions. The comparators utilize a second independent testable internal band gap reference.

The bq76PL455-Q1 provides pins for direct drive of external N-FETs for passive cell balancing with power resistors. The balancing function can be configured to respond to on or off commands or specified to run for a specific time.

The device is typically powered from the stack of cells to which it is connected and all required voltages are generated internally.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Block Descriptions

7.3.1.1 Power

The bq76PL455-Q1 is designed to operate from internally generated or externally supplied regulated voltages. The group of cells the device is monitoring is the source for the internal regulators. Power is taken from the most-positive and most-negative pins of the series-connected cells to minimize the likelihood of cell unbalancing. In most applications, the bq76PL455-Q1 is operated using its internal supplies.

Feature Description (continued)

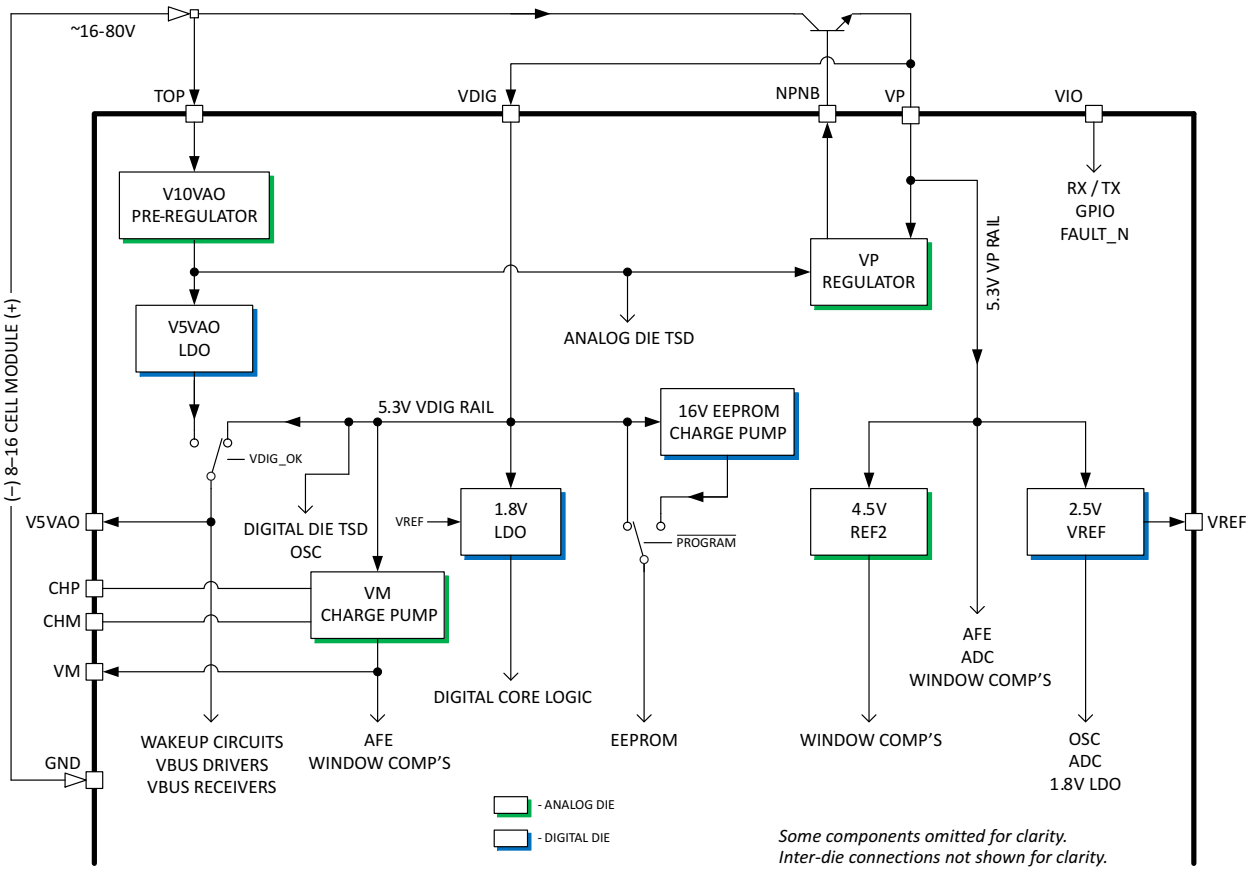


Figure 7. Power Flow Diagram

Feature Description (continued)

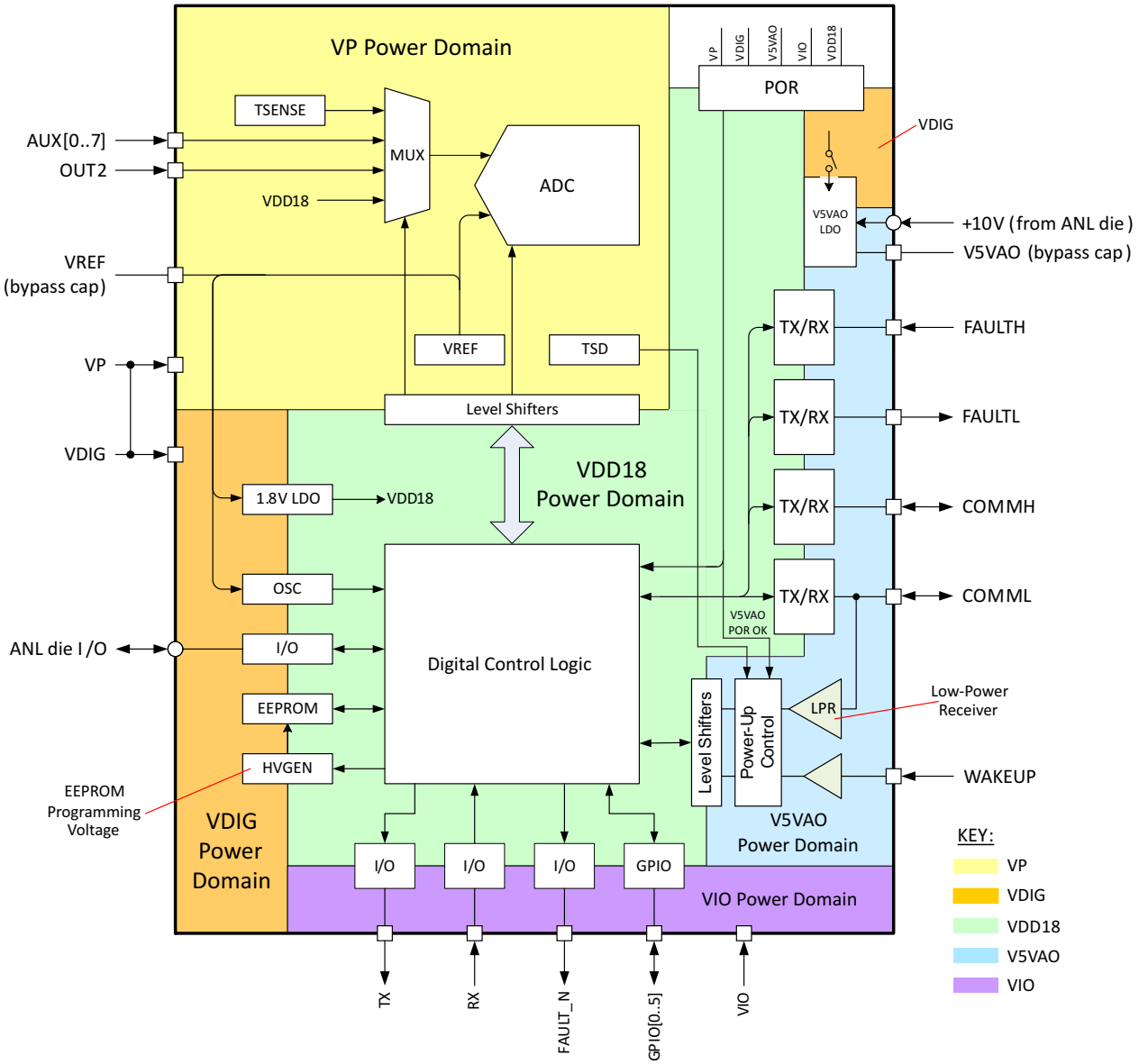


Figure 8. Digital Die Power Domains

Feature Description (continued)

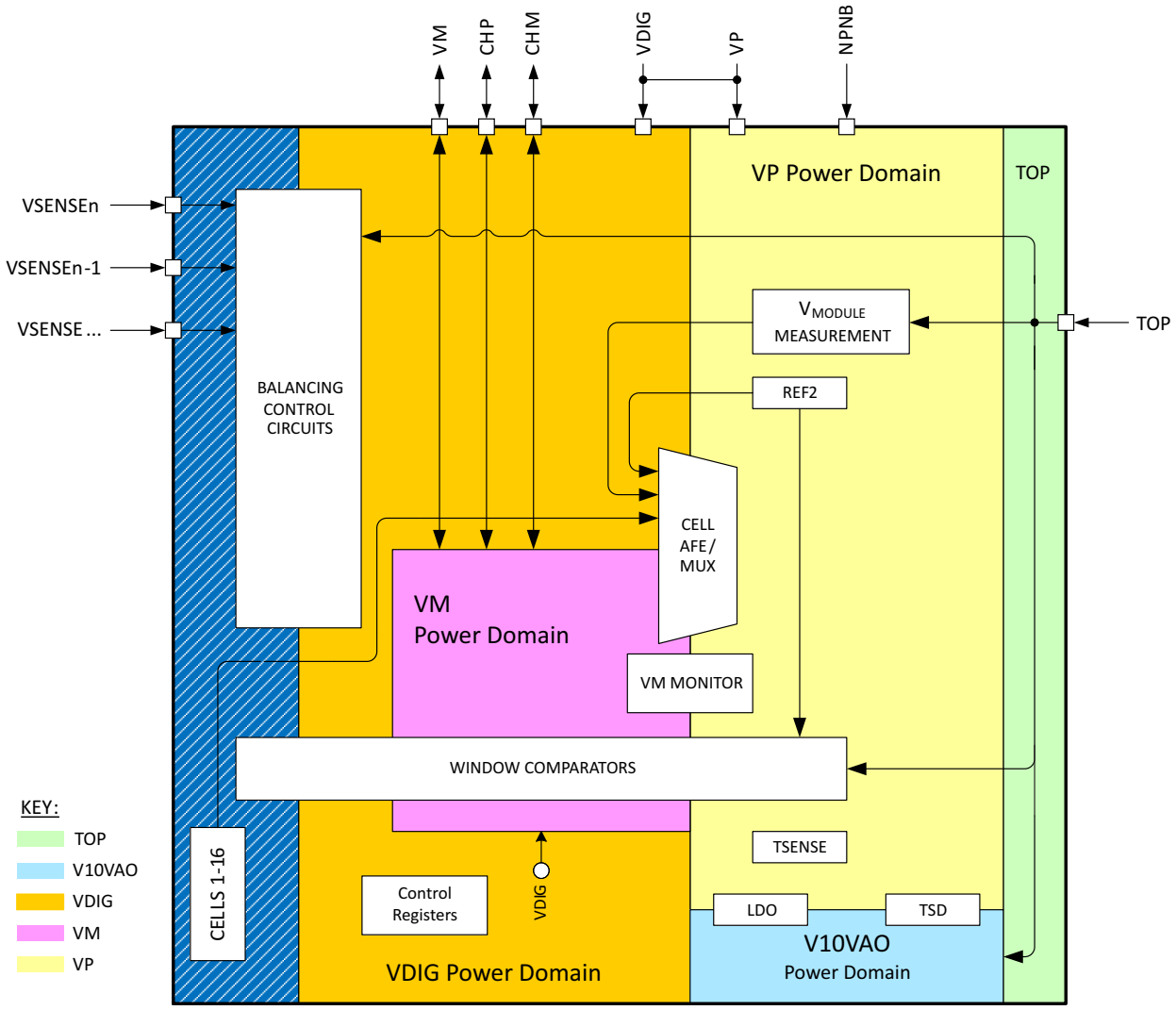


Figure 9. Analog Die Power Domains

7.3.1.1.1 TOP Pin Connection

The bq76PL455-Q1 has a connection from the top of the cell-module battery stack to the TOP pin, typically through an external-series resistor and capacitor to GND forming a low-pass filter. The low-pass filter typically is designed to have a similar time constant to the VSENSE input pins. The minimum recommended values are 100 Ω and 0.1 µF. See the *bq76PL455-Q1 Design Reference Manual* (TIDU245).

7.3.1.1.2 V10VAO

V10VAO is an internal-only, always on, pre-regulator supplied from the TOP pin. It supplies the power to the V5VAO block, Analog Die TSD block, and VP control and regulator circuits. It is not externally accessible.

7.3.1.1.3 V5VAO

V5VAO is the always-on power supply. It supplies the power to the differential communications circuits (COMML+/–) and the WAKEUP pin at all times. This allows the IC to detect the WAKEUP signal and the differential communications block to receive the WAKE tone. An internal regulator drives V5VAO when VDIG is below its normal operating voltage and by VDIG when VDIG is at its normal operating voltage. Once the bq76PL455-Q1 is awake and VDIG is up, V5VAO will be supplied by (essentially shorted to) VDIG.

Feature Description (continued)

NOTE

V5VAO can only supply enough power to meet internal IC requirements; it should not be connected to external circuitry.

7.3.1.1.4 VP Regulated Output

The bq76PL455-Q1 is powered directly from the cells to which it is connected. Current is drawn at the top and bottom of the n-cell battery assembly so that current through each cell is the same. An integrated linear regulator utilizes an external NPN transistor (Zetex ZXTN4004K or similar) to generate a nominal 5.3 V rail on pin VP. VP is both a power input and the sense node for this supply. The NPNB pin controls the external NPN transistor of the regulator. A capacitor or resistor-capacitor combination must be connected externally from VP to GND, see *Pin Configuration and Functions* for details. VP must be connected externally to VDIG and can optionally be connected to VIO. Both of these connections are made through series 1-Ω resistors and independently decoupled. This regulator is OFF in SHUTDOWN mode.

Table 1. Recommended NPN Transistor Characteristics

PARAMETER	DESCRIPTION	TEST CONDITION	TYPICAL VALUE	UNIT
BV_{CEO}	Collector-Emitter voltage(1)		100	V
Beta β	Gain	at 5 mA	> 100	
C_{CB}	Collector-Base capacitance		≤ 35	pF
P	Power handling(2)	See the following text for collector resistor details.	500	mW
IC	Collector current rating		> 100	mA

(1) This value should be chosen with respect to the locally supplied maximum cell voltage and derated appropriately for operating conditions and temperature.
(2) This value should be derated appropriately for operating conditions and temperature.

A collector resistor is added between the NPN collector and the TOP pin to reduce power dissipation in the NPN under normal and system fault conditions. The value of this resistor is chosen based on the minimum battery-stack voltage, the bq76PL455-Q1 VP/VDIG total load current, and the load current of any external I/O circuitry powered directly or indirectly by VP/VDIG. It is also recommended to add a 1-µF decoupling capacitor directly from the collector to AGND.

The maximum resistor value is calculated as follows, the exact value is not critical:

$$R_{COL} = (VMODULE_{MIN} - (VP_{MAX} + V_{CE\_SAT})) / Q_{I\_MAX}$$

where

- $VMODULE_{MIN}$ is the minimum expected voltage of the cells connected to the IC (minus headroom)
- VP_{MAX} is the maximum regulated voltage produced by VP under control of the IC
- V_{CE_SAT} is obtained from the NPN transistor data sheet
- Q_{I_MAX} is the maximum expected total load current for VP/VDIG, the sum of internal and external load currents

Example:

$VMODULE_{MIN}$=16 V, VP_{MAX}=5.3 V, V_{CE_SAT}=0.3 V, Q_{I_MAX}=15 mA

R = [16 – (5.3 + 0.3)] / 0.015

where

- R = 693, a 680-Ω 5% resistor is chosen
- VP will fall out of regulation if either VMODULE < 16 V, or Q_{I_MAX} > 14.7 mA
- Additional headroom compensation for VCE_SAT and R drift over temperature may be required.

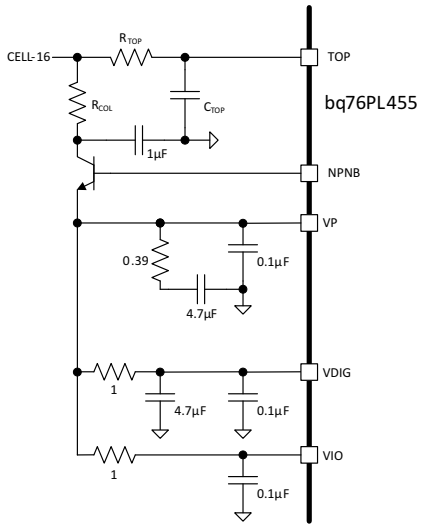


Figure 10. VP / VDIG / VIO Recommended Circuit

7.3.1.1.5 VDIG Power Input

VDIG is the digital voltage supply input. It is always connected to the VP pin, which normally receives power from the NPN. It may optionally be driven from an external supply, but still must be connected to VP. This applies in all operating modes. VDIG is sourced from VP through a 1-Ω resistor. VDIG is decoupled with a separate capacitor at the pin.

7.3.1.1.6 VDD18 Regulator

An internal regulator is provided to generate a 1.8-V digital supply for internal device use only. The 1.8-V supply does not require an external capacitor, and there is no pin or external connection.

7.3.1.1.7 VIO Power Input

VIO is the voltage supply input used to power the digital I/O pins TX, RX, FAULT_N, and GPIOn. VIO may be connected to an externally regulated supply rail, which is common to an I/O device such as a microcontroller. VIO may alternately be sourced from VP through a 1-Ω resistor. VIO is decoupled with a separate capacitor at the pin.

If VIO is not powered, the part will be held in reset and will enter shutdown after a short delay. This gives a very good reset mechanism for non-stacked systems. Upon power up from a SHUTDOWN, the SHDN_STS[GTSD_PD_STAT] bit will be set. This flag bit is the logical <OR> of this condition or triggering the thermal shutdown of the digital die in a die overtemperature situation.

7.3.1.1.8 VM Charge Pump

An internal charge pump is included for biasing the Analog Front End (AFE) and other analog circuits. It requires an external flying capacitor connected between the CHP and CHM pins plus a storage capacitor on pin VM to generate a –5 rail for internal use. The charge pump (VM) is always on in IDLE and off in SHUTDOWN. VM requires the oscillator to be running and stable and does not start until the other supplies are above their POR thresholds. The VM charge pump will start ramping at the start of the WAKEUP tone on COMH.

7.3.2 Analog Front End (AFE) / Level Shifter

The bq76PL455-Q1 AFE allows up to 16 cells to be monitored. Seventeen VSENSE inputs, labeled VSENSE0 through VSENSE16, are provided for this purpose. The bq76PL455-Q1 can be programmed to sample all, or a subset, of the connected cells. Sampling always begins at the highest-selected cell and finishes with the lowest-selected cell. During measurement, the AFE will select the cell addressed by the logic block and level-shift the sensed cell voltage with a gain of 1 down to the ground-referred OUT1 pin.

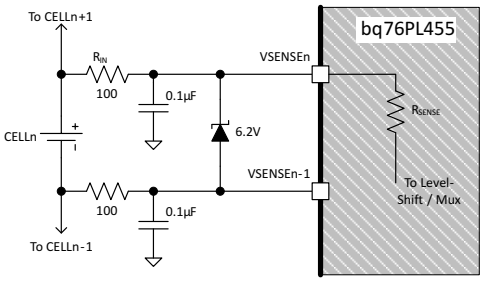


Figure 11. VSENSE External Low-Pass Filter Components, Typical Values Shown (Some Parts Omitted for Clarity)

External 100-Ω resistors in series with each VSENSE input and 0.1-µF capacitors between VSENSE inputs and VSS are recommended for low-pass filtering for the input as shown in Figure 11. These values can be changed to suit application needs, but it is recommended the series resistor value not be increased above approximately 1 kΩ as this may cause voltage measurement errors. The worst-case error can be approximated by Error = V_{CELL} × [R_{IN} / (R_{SENSE} + R_{IN})]. Any external, input protection, Zener diodes used should generally be connected on the IC side of the series low-pass filter resistors. Very low leakage diodes are selected to prevent the Zener leakage current flowing through the input resistors and causing additional input voltage errors during measurement. The Zener diode is principally in the circuit to help protect the device during the initial cell connection event (hot-plug).

The analog output of the AFE connects to OUT1 via an internal 1-kΩ series resistor. OUT1 should be externally connected to OUT2. At this external connection between the AFE and the ADC, it is required to place an external filter capacitor to form an RC filter to reduce the noise bandwidth. A filter capacitor will increase the settling time of the signal presented to the ADC input. A trade-off can be made between ADC sample time, filtering, and accuracy. More information is available from the *bq76PL455-Q1 Design Reference Manual* (TIDU245).

7.3.3 ADC

The ADC in the bq76PL455-Q1 is a 14-bit Successive Approximation Register (SAR) ADC. It has a fixed conversion (hold) time of 3.44 µs, with a user-selectable sample interval or period between conversions. The user-selectable sample interval determines the acquisition (tracking) settling time between conversions, used mostly to allow the input capacitor on OUT1 to settle between conversions, and to allow for internal settling.

The ADC input mux on the digital die allows it to connect to the following:

- The AFE (analog die) mux output on OUT1 which measures:
  - Up to 16 cell voltage channels
  - The V_{MODULE} voltage
  - The internal temperature of the analog die
  - The REF2 analog die reference
  - The VM (–5V) charge pump generated voltage supply on the analog die
- Measurement channels on the digital die:
  - The 8 AUX input channels
  - The VDD18 1.8-V voltage supply on the digital die
  - The internal temperature of the digital die

The ADC can be set up to take single samples or multiple samples in one of two averaging modes. This selection is made using OVERSMPL[CMD_OVS_CYCLE].

7.3.3.1 Channel Selection Registers

Channels to be measured are programmed by setting bits in the CHANNELS and NCHAN registers. Each channel can be set up for measurement individually. User programmable correction factors are available for cell and AUX channels. Conversion times are individually programmable for different types of inputs (that is, cells, AUX, internal).

The NCHAN register sets the number of VSENSE channels (cell inputs) that will be used by the device. Unused channels are dropped consecutively starting from channel 16. Set this register for the number of cells used, that is, for 14 cells, program 0x0E. This register also setting masks cell over-voltage and under-voltage faults for unused channels, and turns off the UV and OV comparators associated with the channel. The idle channel (the channel the mux "rests" on between sample intervals) is set to the value in this register. This allows the OUT1 pin to hold the filter capacitor at the voltage, which will be sampled first on the next cycle.

7.3.3.2 Averaging

The ADC can be programmed to average results by sample/oversampling 1, 2, 4, 8, 16, or 32 times. Individual samples are arithmetically averaged by the bq76PL455-Q1, which then outputs a single 16-bit (14 bits + 2 additional bits created by the averaging process) average measurement. The individual samples used to create the average value are not available.

As shown in Figure 12, the ADC averages any selected cell voltages first, then any selected AUX input channels, and then any remaining channels selected in the CHANNELS register in the order listed. Depending on the state of the CMD_OVS_CYCLE bit in the OVERSMPL register, the Voltage and AUX channels will be oversampled by either:

- Sampling each channel once and cycling through all channels before oversampling again in the case of CMD_OVS_CYCLE = 1 (cycled averaging) OR
- Sampling multiple times on a single channel before changing channel in the case of CMD_OVS_CYCLE = 0 (non-cycled averaging).

Figure 12 shows these on the left and right, respectively.

When oversampling, the oversample periods for each channel after the first sample are shown in Table 2. The first sample can have a different period programmed (see Table 2), followed by all subsequent samples at different period shown in Table 3. The first sample and subsequent sample periods are independent of each other.

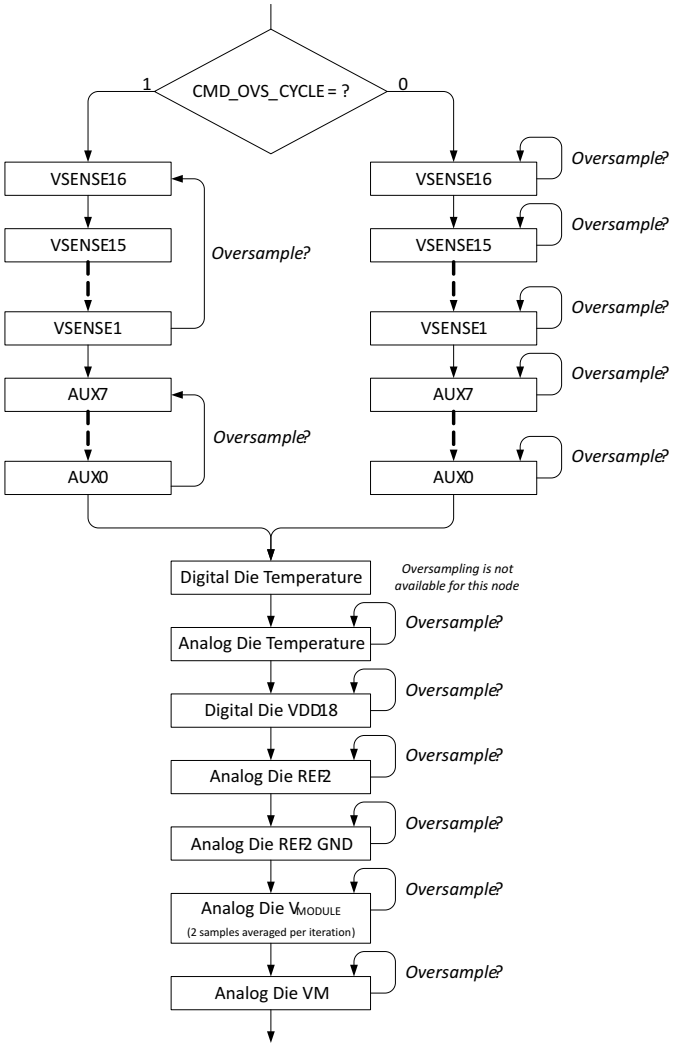


Figure 12. Sampling/Oversampling (Averaging) Sequence

Table 2. Channel Sample Period Settings

CHANNEL	FIRST SAMPLE	OTHER SAMPLES (AVERAGING)	
		CMD_OVS_CYCLE=0	CMD_OVS_CYCLE=1
VSENSEn (n=1..16)	ADC_PERIOD_VOL	CMD_OVS_HPER	ADC_PERIOD_VOL
AUXn (n=0..7)	ADC_PERIOD_AUXn	CMD_OVS_GPER	ADC_PERIOD_AUXn
DIGITAL DIE TEMP (1)	Approximately 50 µs	n/a	n/a
ANALOG DIE TEMP	ADC_PERIOD_TEMP	CMD_OVS_HPER	CMD_OVS_HPER
VDD18	CMD_OVS_GPER	CMD_OVS_GPER	CMD_OVS_GPER
ANALOG DIE VREF	ADC_PERIOD_REF	CMD_OVS_HPER	CMD_OVS_HPER
MODULE MONITOR	ADC_PERIOD_STK	CMD_OVS_HPER	CMD_OVS_HPER
VM	ADC_PERIOD_VM	CMD_OVS_HPER	CMD_OVS_HPER

(1) Oversampling (averaging) is not available for this measurement.

The ADC_PERIOD_VOL bits set the period between ADC samples for the indicated channels whether oversampling or not. When CMD_OVS_CYCLE = 1, the oversampling period of the Cell and AUX channels remains fixed at the single sample period of CELL_SPER[ADC_PERIOD_VOL] and AUX_SPER[ADC_PERIOD_AUX], respectively. Otherwise, if CMD_OVS_CYCLE = 0 then the oversample period for the Cell channels is set by bits CMD_OVS_HPER and for the AUX channels is CMD_OVS_GPER.

CMD_OVS_HPER must be programmed to 12.6 µs and CMD_OVS_GPER can be programmed between 4.13 µs and 12.6 µs in the OVERSMPL register.

After the initial sample period performed per a single sample, oversamples on all the other channels are at the CMD_OVS_GPER and CMD_OVS_HPER period settings as indicated in Table 2.

Writing to the CMD register is used to start the voltage sampling process. This is usually done with a BROADCAST Write_With_Response_Command sent to the CMD register. Using the BROADCAST version of the synchronously sample channels command will result in all devices in the stack sampling at the same time. That is, all devices begin sampling their respective cells, then AUX, and so on, simultaneously.

7.3.3.3 Recommended Sample Periods

Refer to Table 3 for initial recommended settings. Other settings are possible; consult *bq76PL455-Q1 Design Reference Manual* (TIDU245) for further information.

Table 3. ADC Recommended Sample Periods and Setup

MEASURED PARAMETER	PERIOD (1)		PERIOD REGISTER (2)	
	1st SAMPLE	SAMPLES 2–8	NAME	AS SHIPPED
VCELL	60 µs	12.6 µs	CELL_SPER	0xBC
VAUX	12.6 µs	12.6 µs	AUX_SPER	0x44444444
VMODULE	1000 µs	12.6 µs	TEST_SPER	0xF999
Die Temp (ANL)	100 µs	12.6 µs	CELL_SPER	0xBC
Die Temp (DIG)	50 µs	N/A	N/A	N/A
TSD (DIG) (3)	30 µs	12.6 µs	N/A	N/A
VM	30 µs	12.6 µs	TEST_SPER	0xF999
VDD18	30 µs	12.6 µs	N/A	N/A
REF2	30 µs	12.6 µs	TEST_SPER	0xF999

(1) Sampling periods and averaging mode will affect device accuracy. Device accuracy and register settings (including the sampling period) used to achieve stated device accuracy are specified under "Electrical Characteristics, ADC" in *Analog-to-Digital Converter (ADC): Analog Front End*. Other settings are possible. Consult the *bq76PL455-Q1 Design Reference Manual* (TIDU245) for further information. Device accuracy is not assured at settings other than those specified in the Electrical Characteristics tables.
(2) Other register settings used: OVERSMPL = 0x7B; PWRCONFIG = 0x80
(3) Thermal ShutDown

7.3.3.4 OUT1 Capacitor Selection

The value of the OUT1 capacitor is determined by the averaging mode, the sampling period, and the averaging sample interval.

7.3.3.4.1 For OVERSMPL[CMD_OVS_CYCLE] = 0

When OVERSMPL[CMD_OVS_CYCLE] = 0, each channel is sampled n times before proceeding to the next channel. This bit only affects the VSENSE, and AUX channels. The typical recommended OUT1 capacitor value is 390 pF, type C0G/NP0 or better.

7.3.3.4.2 For OVERSMPL[CMD_OVS_CYCLE] = 1

When OVERSMPL[CMD_OVS_CYCLE] = 1, all channels are sampled in order, then the cycle is repeated until the number of additional oversamples has been taken. This bit only affects the VSENSE and AUX channels. For a brief discussion of proper OUT1 capacitor selection and the default configuration, please see *Out Filter Selection* section in *bq76PL455 EVM and GUI User's Guide* (SLUUAT2).

7.3.3.5 VSENSE Input Channels

The VSENSE input channels are used to measure the voltages of individual cells in the approximate range of 1 V–5 V. Each input should be connected to an external low-pass filter (LPF) to reduce noise at the input, and a Zener diode to provide protection to the IC during random hot-plug cell connection. Typical values for the LPF range from 100 Ω to 1 kΩ, and 0.1 µF to 1 µF. Values outside this range may degrade accuracy from noise, or from excessive IR loss in the series resistor.

Unused inputs should be tied up to the highest connected cell. For example, in a 14-cell system, unused inputs VSENSE15 and VSENSE16 are tied to VSENSE14. Channels are used from lowest to highest, with VSENSE0 connected to the (–) terminal of the bottom cell.

The values returned from an ADC conversion for these channels are converted to volts by:

$$V_{CELL} = [(2 \times VREF) / 65535] \times READ\_ADC\_VALUE$$

Total channel measurement accuracy is affected by a number of factors, including but not limited to the VREF accuracy, any shift in VREF accuracy over temperature, gain inaccuracies over temperature, any current leakage in external components, and the method of sampling. Total channel measurement accuracy can be approximated by considering these inaccuracy sources. The following generalized formula can be used to approximate total channel measurement accuracy:

$$V_{CHANNEL\_ACCURACY\_TOTAL} = V_{SENSE\_ERR} + [2 \times (V_{ADC\_IN} / 5) \times VREF_{ERR\_TOTAL}]$$

where

- V_{SENSE_ERR} is the error of VSENSE input voltage over temperature
- V_{ADC_IN} is the error in the input voltage seen by the ADC
- $VREF_{ERR\_TOTAL}$ is the total error in VREF over temperature, which includes any inaccuracy in calibration of VREF and any induced VREF shift over temperature.

For more detail regarding the total channel accuracy calculation, refer to the application note(s) covering accuracy and calibration. Application notes also provide additional information regarding best practices for system calibration, which includes calibrating out inaccuracies in VREF and V_{SENSE}.

7.3.3.6 AUXn Input Channels

The AUXn input channels are used to measure external analog voltages from approximately 0 V–5 V. A typical use for these channels is to measure temperature using thermistors. These channels require a simple external low-pass filter to reduce high frequency noise for best operation. The RC values are chosen for the user's application requirements.

The values returned from an ADC conversion for these channels are converted to volts by:

$$V_{AUX} = [(2 \times VREF) / 65535] \times READ\_ADC\_VALUE$$

7.3.3.7 V_{MODULE} Measurement Result Conversion to Voltage

V_{MODULE} is the voltage measured from the TOP pin to GND. The value is scaled by 25 by an internal resistor voltage divider. Measuring VMODULE voltage is enabled by setting TSTCONFIG[MODULE_MON_EN]. The measurement is enabled or disabled to aid with self-testing. When set to 0, the channel should measure close to 0 V.

The values returned from an ADC conversion for this channel is converted to volts by:

$$V_{MODULE} = ([(2 \times VREF) / 65535] \times READ\_ADC\_VALUE) \times 25$$

7.3.3.8 Digital Die Temperature Measurement

The temperature of the digital die may be measured as a part of the normal ADC measurement sequence by setting bit CHANNEL[CMD_TSEL]. The result reported here is the voltage from the temperature sensor, not the actual temperature.

No averaging is ever performed on this channel, but the timing will appear as if the requested oversampling was performed.

FAULT_SYS[INT_TEMP_FAULT] is continuously updated based on the currently stored measurement result and threshold. The temperature must be sampled within a normal operating range to allow the fault to be cleared.

Conversion formula:

Internal Digital Die Temperature °C = (V_{ADC} – 2.287) × 131.944

7.3.3.8.1 Automatic Temperature Sampling

After initialization is complete, an internal timer will cause the digital die temperature sensor to be sampled once per second. No oversampling is performed. If a command cycle occurs that samples the digital die temperature sensor, the timer will be reset. A command will interrupt an automatic temperature sample, but if the digital die temperature is not sampled by the command, the automatic temperature sample will occur as soon as the command completes. This can cause sample values to appear to change without a sample request.

7.3.3.9 Analog Die Temperature Measurement

The temperature of the analog die may be measured as a part of the normal ADC measurement sequence by setting bit CHANNEL[CMD_HTSEL]. The result reported here is the voltage from the temperature sensor, not the actual temperature.

There is no internal threshold checking for this value. For self-testing purposes, the microcontroller is expected to compare this value with the converted temperature from the digital die and decide if they are reporting the same temperature. The temperatures should match within T_{INT_DELTA}.

Conversion formula:

Internal Analog Die Temperature °C = (V_{ADC} – 1.8078) × 147.514

7.3.3.10 VM Measurement Result Conversion to Voltage

There is no internal threshold checking of this value. The microcontroller is expected to check that the value is within the appropriate range.

The value returned from an ADC conversion for this channel is converted to volts by:

VVM = –2 × [(2 × VREF) / 65535] × READ_ADC_VALUE

7.3.3.11 V5VAO, VDIG, VDD18 Measurement Result Conversion to Voltage

The value returned from an ADC conversion for these channels is converted to volts by:

V_{ADC} = [(2 × VREF) / 65535] × READ_ADC_VALUE

There is no internal threshold checking of these values. The microcontroller is expected to check that the values are within the appropriate ranges.

7.3.4 Thermal Shutdown

Thermal shutdown occurs when one or both of the Thermal Shutdown (TSD) sensors, on either, die sense an overtemperature condition. The sensors operate independently without interaction, and are independent from the analog and digital die sensors. Each has a separate register-status indicator flag. When a TSD fault occurs, the part immediately enters the SHUTDOWN state. The part can be awakened by following the normal WAKEUP procedure. It does not exit SHUTDOWN automatically. It cannot be awakened until the temperature falls below the TSD threshold. Upon waking up, either SHDN_STS[GTSD_PD_STAT] or (SHDN_STS[ANALOG_PD_STAT]&& SHDN_STS[HTSD_PD_STAT]) bits will be set.

7.3.5 Voltage Reference (ADC)

A precise internal voltage reference for the ADC is brought out to VREF pin. Two parallel X7R or better filter capacitors between pins VREF and AGND are required for the reference; see *bq76PL455-Q1 Design Reference Manual* (TIDU245) for recommended values and PCB layout considerations.

7.3.6 Voltage Reference (REF2)

A 4.5-V internal voltage reference is provided for the window comparators. It is not brought out to an external pin. The reference may be checked by selecting it with the CHANNELS[CMD_REFSEL] bit.

7.3.7 Passive Balancing

Sixteen internal drivers are provided to control individual cell balancing through the pins labeled EQ1…EQ16. Figure 13 shows the external circuitry to turn on an external NMOS FET Q_{BAL} to discharge Cell N through resistor RBAL When a balance command is issued via register CBENBL, the EQ(N) output is asserted, switching to the VSENSE(N) rail and turning Q_{BAL} on. When the register bit is de-asserted, the EQn bit is switched to the VSENSEn–1 rail, turning Q_{BAL} off and reducing the balancing current to zero. The squeeze (OWD) function must be disabled for correct balancing operation by setting TSTCONFIG[EQ_SQUEEZE_EN] = 0.

If CBCONFIG[BAL_CONTINUE] is set to '0', then when there is a FAULT, balancing is disabled. The CBENBL register bits are cleared to indicate this event. However, there is one exception. The USER checksum fault indicated by FALUT_DEV[USER_CKSUM_FLT] does not disable balancing.

BAL_CONTINUE = 0: CBENBL is set to 0 and balancing is disabled until the fault and fault status bits are cleared. Information about what was being balanced is discarded. No change is made to the BAL_TIME bits in CBCONFIG. The CBENBL register must then be re-written with the desired balancing action.

BAL_CONTINUE = 1: CBENBL and CBCONFIG are unaffected, any balancing in progress is continued.

Changing the CBENBL register will create a checksum fault and cause FAULT_DEV[USER_CKSUM_ERR] to be set. This may be a result of setting bits to enable balancing for cells, or the register being reset because of a fault or CBTIME expiring.

The internal balancing control circuitry is only powered up when any bit in CBENBL is set.

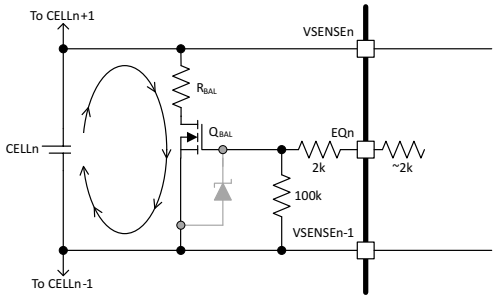


Figure 13. EQ Circuit Operation (Some Components Omitted for Clarity)

7.3.8 General Purpose Input-Outputs (GPIO)

There are six GPIO pins available in the bq76PL455-Q1. GPIO behavior is controlled by registers GPIO_xxx located at addresses 0x78–7D. Each can be programmed to be an input or output pin.

Each GPIO pin can have an internal pull-up or pull-down resistor enabled to keep the pin in a known state when external circuitry is not powered. Pull-up or pull-down resistors are configured in the GPIO_PU and GPIO_PD registers. The pull-up/down resistors are internally connected to supply VIO. The resistor values are shown in the *Digital Input/Output: Wakeup* section of the Electrical Characteristics tables.

The GPIOs can also be used to trigger a FAULT condition. GPIOs are programmed to trigger a FAULT indication by setting bits in register GPIO_FLT_IN.

The behavior of the IC in response to a FAULT triggered by an enabled GPIO pin is controlled by the FAULT_GPI register and the DEVCONFIG[UNLATCHED_FAULT] bit. The pin is usually configured to be an input in the GPIO_DIR register when used to trigger faults.

7.3.9 UART Interface to Host Microcontroller

The UART follows the standard serial protocol of 8-N-1, where information is sent as a START bit, followed by eight data bits, and then followed by one STOP bit. In all, 10 bits comprise a character time. Received data bits are oversampled by 16 times to improve communication reliability.

The UART sends data on the TX pin, and receives data on the RX pin. When the transmitter is idling (not sending data), TX = 1. The RX input pin idles in the same state, RX = 1. The RX line should be held high using a pull-up to VIO if not used (that is, non-base device in the daisy chain). The RX pin should not be allowed to float when VIO is present.

7.3.9.1 UART Transmitter

The transmitter can be configured to wait a specified amount of time after the last bit reception and start of transmission using the TX_HOLDOFF register. The TX_HOLDOFF register specifies the number of bit periods that the bq76PL455-Q1 will wait to allow time for the microcontroller to switch the bus direction at the end of its transmission.

7.3.9.2 UART Receiver

The UART interface is designed to work half-duplex. As a result, RX is ignored while the device is transmitting data on the TX pin. To avoid collisions when sending data up the daisy-chain interface, the host microcontroller should wait until all bytes of a transmission from the IC to the microcontroller have been received before attempting to send data or commands up the daisy-chain interface. In the event, the microcontroller starts a transaction without waiting to receive the preceding transaction's response, then communication might hang up and the microcontroller may need to send Communication Clear (see *Communication Clear (Break) Detection*) or Communication Reset (see *Communication Reset Detection*) to restore normal communications.

7.3.9.3 Baud Rate Selection

The baud rate of the communications channel to the microcontroller is set in the COMCONFIG[BAUD] register for 125k-250k-500k-1M baud. The default rate after a communications reset is 250k. The default rate after a POR is the rate selected by the value stored in EEPROM for the COMCONFIG[BAUD] register.

When the value in this register is changed, the new rate takes effect after the complete reception of a valid packet containing the new setting including the CRC. The next packet should be sent at the new baud rate, and all packets transmitted by the IC will be at the new rate. The baud rate can be changed at any time and optionally stored in the EEPROM as a new POR default. After changing baud rate, a minimum wait period of 10 µs should be observed before sending the first packet at the new baud rate.

The value in the COMCONFIG[BAUD] register only affects the baud rate used in microcontroller communications on the TX and RX pins, the daisy-chain vertical communication bus rate is fixed at a higher rate and not user modifiable. All devices in the stack must have the same baud rate setting as the base device to read data from stacked devices.

7.3.9.4 Communication Clear (Break) Detection

Communications clear is used to reset the receiver to resynchronize looking for the start of frame.

The receiver continuously monitors the RX line for a break (<BRK>) condition. A <BRK> is detected when the RX line is held low for at least $t_{COMM\_BREAKmin}$ bit periods (approximately 1 character times). Sending for more than $t_{COMM\_BREAKmax}$ bit periods may result in recognition of a communication reset instead of the intended communication clear. When detected, a <BRK> will set the STATUS[COMM_CLEAR] flag.

7.3.9.5 Communication Reset Detection

A communication reset is detected if the RX line is held low for more than approximately $t_{COMM\_RESETmin}$. The primary purpose of sending a communications reset is to recover the IC in the event the baud rate is inadvertently changed or unknown. The baud rate is unconditionally reset to the FACTORY default value of 250 kb/s, REGARDLESS of the value stored in the EEPROM COMCONFIG register. This sets the baud rate to a known, fixed rate (250k baud), and the STATUS[COMM_RESET] flag.

7.3.9.6 Communication Timeouts

Two timeouts can be programmed based on the absence of a valid packet from either UART or differential stack communications. The times are set in the two-bit fields of the Communications Timeout (CTO) register. A valid packet is defined as any packet with a valid CRC.

7.3.9.6.1 Communications Timeout Fault

Register CTO[COMM_TMOUT_PER] sets the period with no valid communications from either communications interface before a COMM_TIMEOUT fault is sensed.

CTO[COMM_TMOUT_PER] should always be set less than the CTO[COMM_PD_PER] to get a communications timeout fault before SHUTDOWN occurs.

7.3.9.6.2 Communications Timeout Power-Down (SHUTDOWN)

CTO[COMM_PD_PER] forces the part to shut down when this time is exceeded without a valid communication from either the UART or the differential stack communications.

7.3.10 Stacked Daisy-Chain Communications

In the stacked configuration, the main microcontroller first communicates through a bq76PL455-Q1 device using the UART communications interface as shown in Figure 14. Communication is then relayed up the chain of connected slave bq76PL455-Q1 devices using a proprietary differential communications protocol over AC-coupled differential links interconnect by the COMMH+/– and COMML+/– pins.

Each device in the daisy chain buffers the signal drive levels. The signal is not re-clocked or filtered; it passes through the device without change and the entire stack sees all data sequencing regardless of the target device. The packet is not validated before being transmitted to the next device in the daisy chain. The uniquely addressed or group addressed device acts on the command (that is, begins an ADC conversion of the inputs) as soon as the packet is received and validated for correct address, message contents, and CRC.

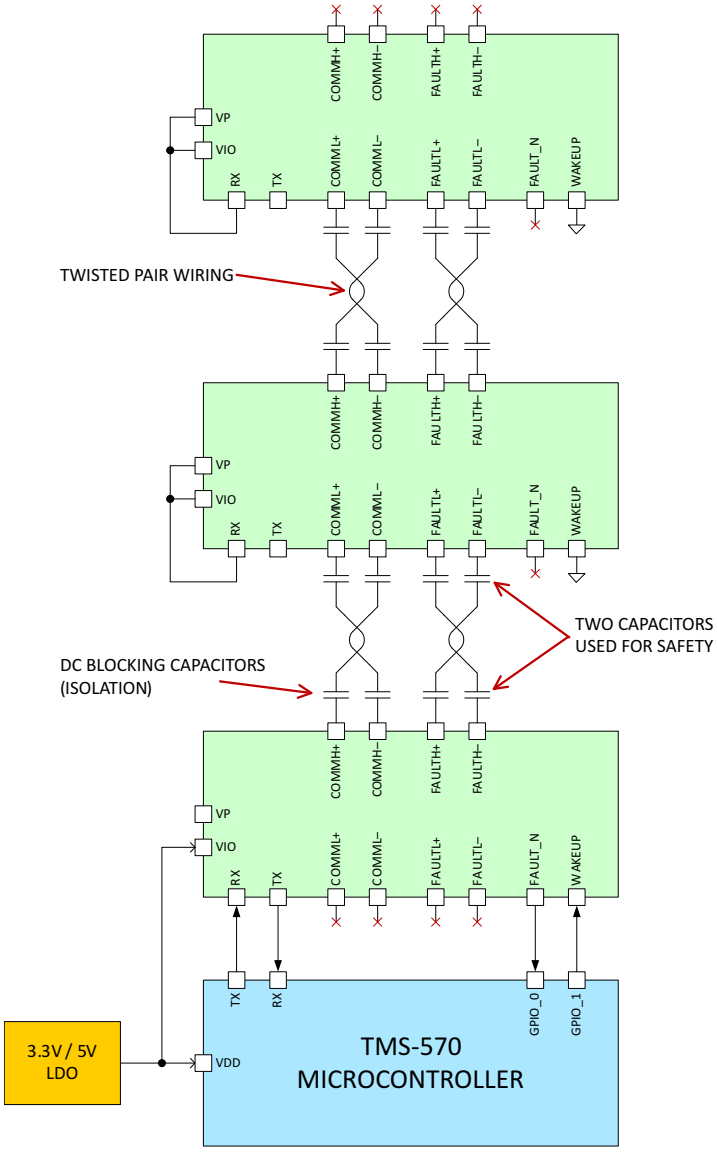


Figure 14. Simplified Stack Communications Connectivity

7.3.10.1 Differential Communications

The bq76PL455-Q1 uses two differential communications links, which perform different tasks. The hardware used for the transmitters and receivers are similar. The communications link used for data and commands (the vertical bus or VBUS) on the COMML+/– and COMMH+/– pairs is bidirectional, while the FAULTH+/– pins are receivers only, and the FAULTL+/– are transmitters only. See Figure 15 for additional information.

NOTE

The UART receiver (RX), COMMH+/– transmitters, and COMML+/– receivers cannot be disabled.

Data are sent and received by the base IC via UART at variable baud rates from 125 kb/s to 1 Mb/s. The VBUS daisy chain operates at a fixed nominal data rate of 4 Mb/s using a proprietary asynchronous protocol. Each byte is sent as 10 bits at 250 ns/bit or 2.5 µs/byte. The IC buffers differences between the UART and VBUS rates and automatic-variable spacing between bytes is provided on the VBUS.

The VBUS interface uses a modified version of the UART protocol so it can easily be translated to/from the UART protocol. Transmission of a bit requires 250 ns, including both half-bits. It is effectively a 4-MHz signal that is phase shift keyed, so the resulting transmission will have both 4-MHz and 2-MHz components.

7.3.10.2 Protocol Description

The differential VBUS uses an asynchronous byte transfer protocol with one start bit, eight data bits, and an optional framing bit. The start bit is always a zero. The LSB-first data are duplicated so that the transmission has no DC content. A zero is transmitted as one half-bit period low followed by one half-bit period high. A one is transmitted as one half-bit period high followed by one half-bit period low. The framing bit will be zero for the first byte of a protocol frame. Subsequent bytes will not normally contain a framing bit. The framing bit will be zero for the first byte of a protocol frame. Subsequent bytes will not normally contain a framing bit. A framing bit of one will cause the byte to be discarded and the byte abort flag (FAULT_COM[ABORT_H or ABORT_L]) will be set. Since the data are transmitted on the differential interface as it is being received from the single-ended UART interface, this is used to indicate that an erroneous stop bit was detected.

Each time a byte with a framing bit of zero is detected, it will be interpreted as a frame initialization byte. If the prior frame was not completed, FAULT_COM[FRAM_ERR] will be set. If a byte without the framing bit set is detected when a frame initialization byte is expected, FRAM_ERR will be set and the byte will be discarded.

If the start bit is detected, the receiver will sample the input on the fourth clock edge to produce the bit. Since a bit is always immediately followed by its complement, the two will be compared and the complement error flag (FAULT_COM[COMP_ERR_H or COMP_ERR_L]) will be set if they are not opposites. The first time such an error occurs during a frame, the first sampling of the bit (not the complement) will be assumed to be the correct one. (If this choice is incorrect, it should be detected as a CRC failure.) If such an error occurs more than once during a frame, the fatal-complement error flag (FAULT_COM[COMP_FLT_H or COMP_FLT_L]) will be set and the frame will be ignored. Because the remainder of the frame is ignored, this will generally also cause a FRAM_ERR when the next frame arrives.

While receiving a byte, the receiver will resynchronize on every falling edge. A falling edge is expected at least once every 3 bits. If the expected sampling point of the fourth bit does not detect a falling edge, the edge error flag (FAULT_COM[EDGE_ERR_H or EDGE_ERR_L]) will be set and the receiver will return to idle, discarding the frame.

If eight consecutive edge errors are detected on the low-side interface (COMM_L+/–) with no valid bytes being received, the block will be reset in the same manner as SOFT_RESET. This allows a wakeup tone from the chip below in the stack to cause the part to be reset.

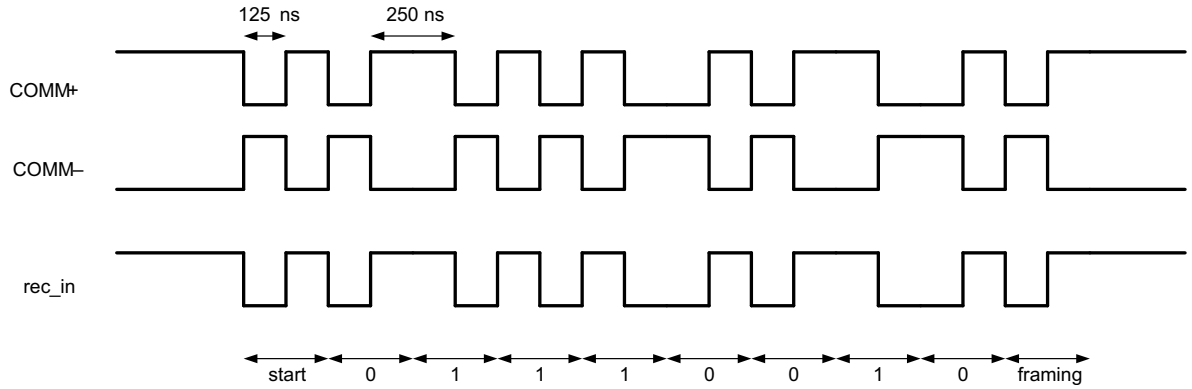


Figure 15. VBUS Data Example, 0x4E Sent

7.3.11 Register and EEPROM

7.3.11.1 Error Check and Correct (ECC) EEPROM

Register values for selected registers are permanently stored in EEPROM. All registers also exist as volatile storage locations at the same addresses, referred to as "shadow" registers. The volatile registers are used for reads, writes, and IC control. For a list of registers included in the EEPROM, see Table 5.

At wakeup, the bq76PL455-Q1 first loads all shadow registers with default values as shown in *Register Summary*. The results of the Error Check and Correct (ECC) evaluation of the EEPROM contents are then used to load the registers conditionally with EEPROM contents.

The EEPROM is loaded to shadow registers in 64-bit blocks; each block has its own Error Check and Correct (ECC) value stored. The ECC bits can be used to detect a single bit (Single-Error-Correction) or double (Double-Error-Detection) bit changes in the data stored in the EEPROM.

Each block and its ECC values are individually evaluated. Single bit errors are corrected, double or more bit errors are only detected, not corrected. A block with good ECC is loaded. A block with a single bit error is corrected, and either the FAULT_DEV[USER_ECC_COR] or FAULT_DEV[FACT_ECC_COR] bit is set to flag the corrected error event. The block is loaded to shadow registers after the single bit error is corrected. Since the evaluation is on a block-by-block basis, it is possible for multiple blocks to have a single correctable error per block and still be loaded correctly. Multiple bit errors can exist and be fully corrected, as long as they are limited to a single error per block.

A block with a bad ECC comparison (two or more bit errors in one block) is not loaded and the FAULT_DEV[USER_ECC_ERR] or FAULT_DEV[FACT_ECC_ERR] bit is set to flag the failed bit error event. The default value remains in the register. This allows some blocks to be loaded correctly (no fail or single bit corrected value) and some blocks to not load. Any time either of the FAULT_DEV[*_ECC_ERR] is set, and the condition is not cleared by a soft reset, the device has failed and should not be used.

7.3.12 FAULT Sensing and Signaling

A dedicated differential FAULT link allows each bq76PL455-Q1 in a stack of devices to signal the presence of any monitored and active/latched fault condition to the main microcontroller independently from the UART link when a fault occurs. The FAULTH+/– and FAULTL+/– pins implement an AC-coupled differential signaling scheme similar to the communications but using only a simple heartbeat pulse signal to indicate normal or fault conditions by the presence or absence of a repetitive pulse respectively. The low duty cycle heartbeat is stopped anytime a fault is sensed and the condition sets a bit in one of the FAULT_* registers. Masked faults have no effect on the heartbeat generation.

7.3.12.1 Fault Flow Schematics

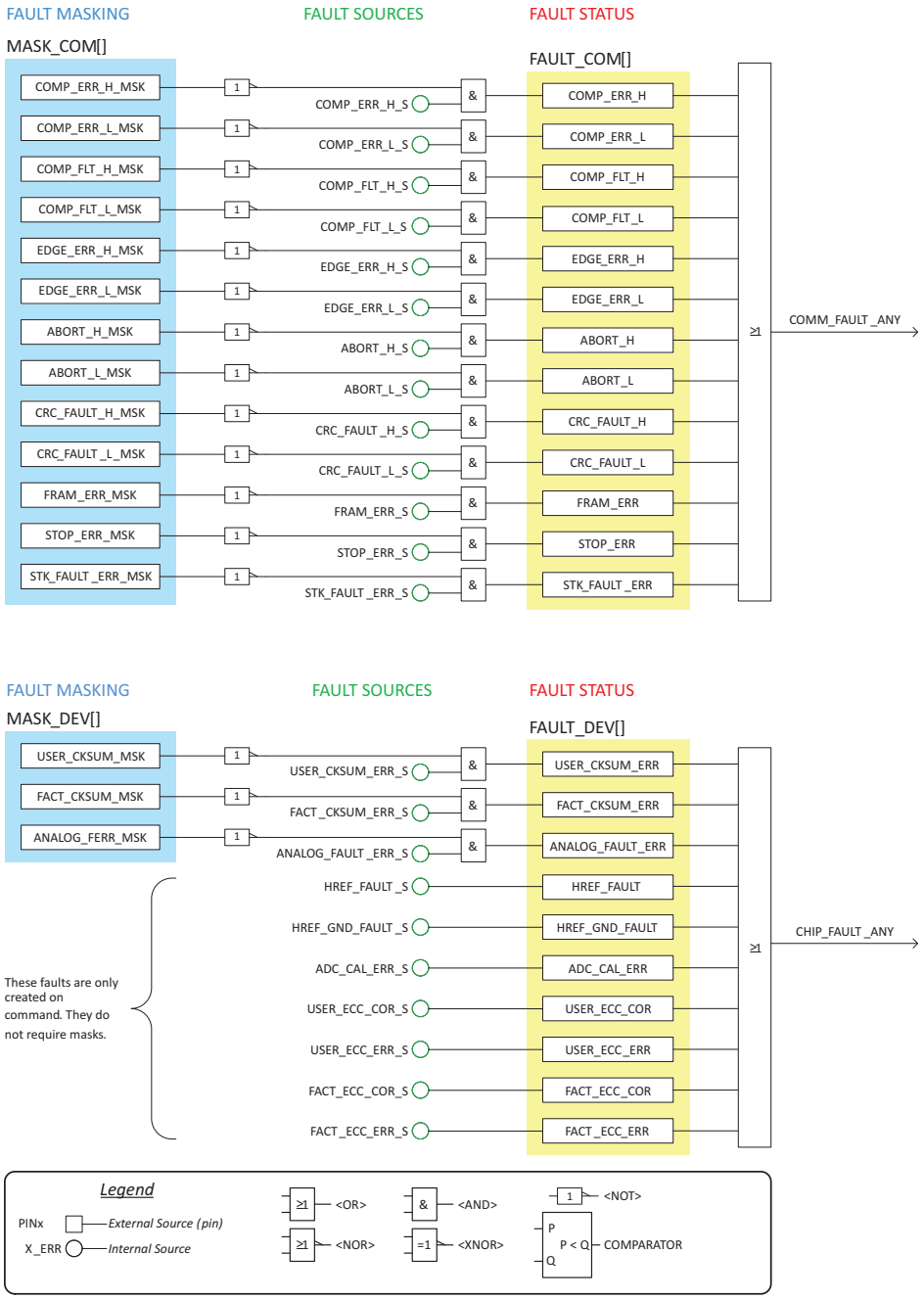


Figure 16. Digital Faults

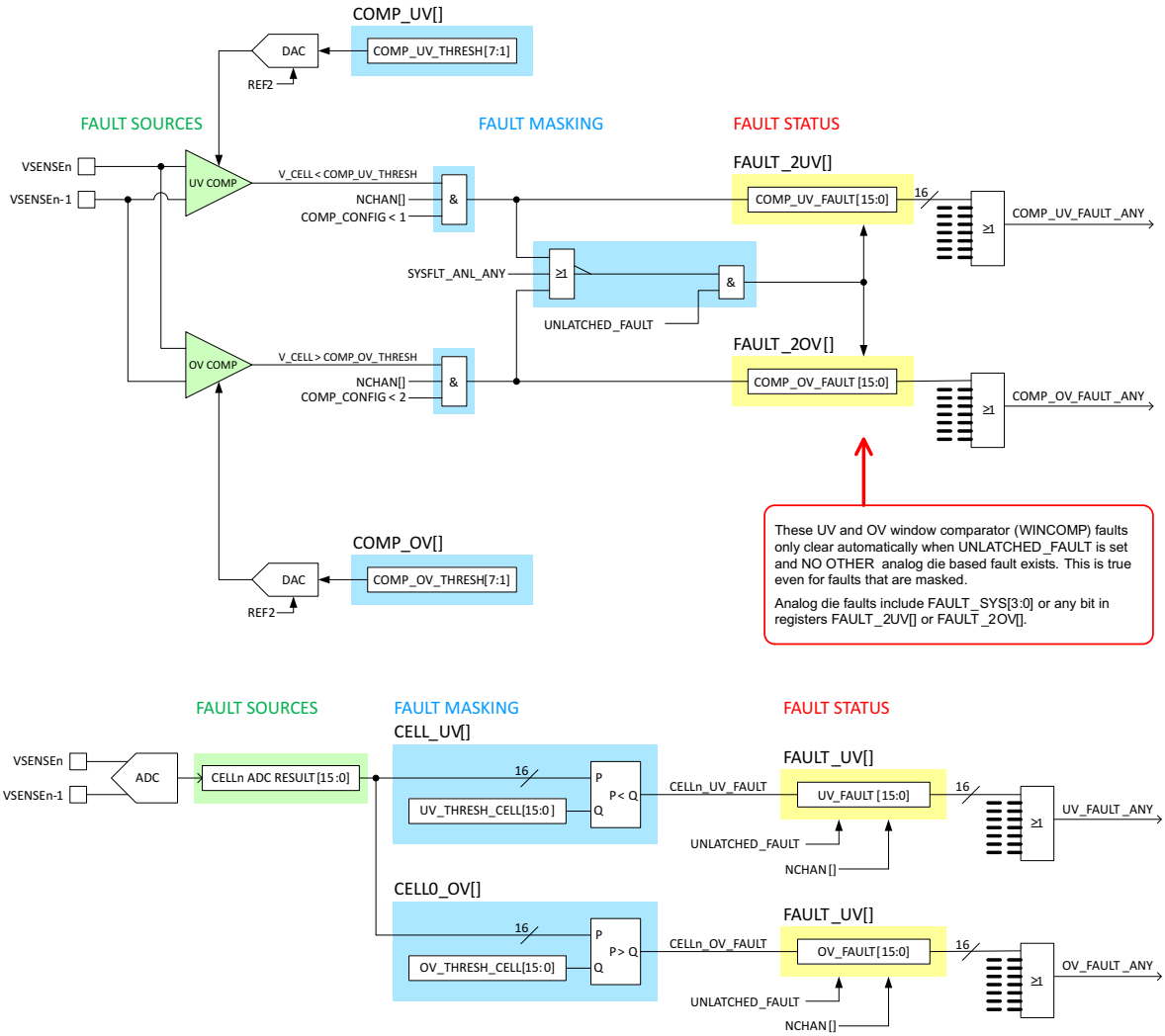


Figure 17. Analog Faults

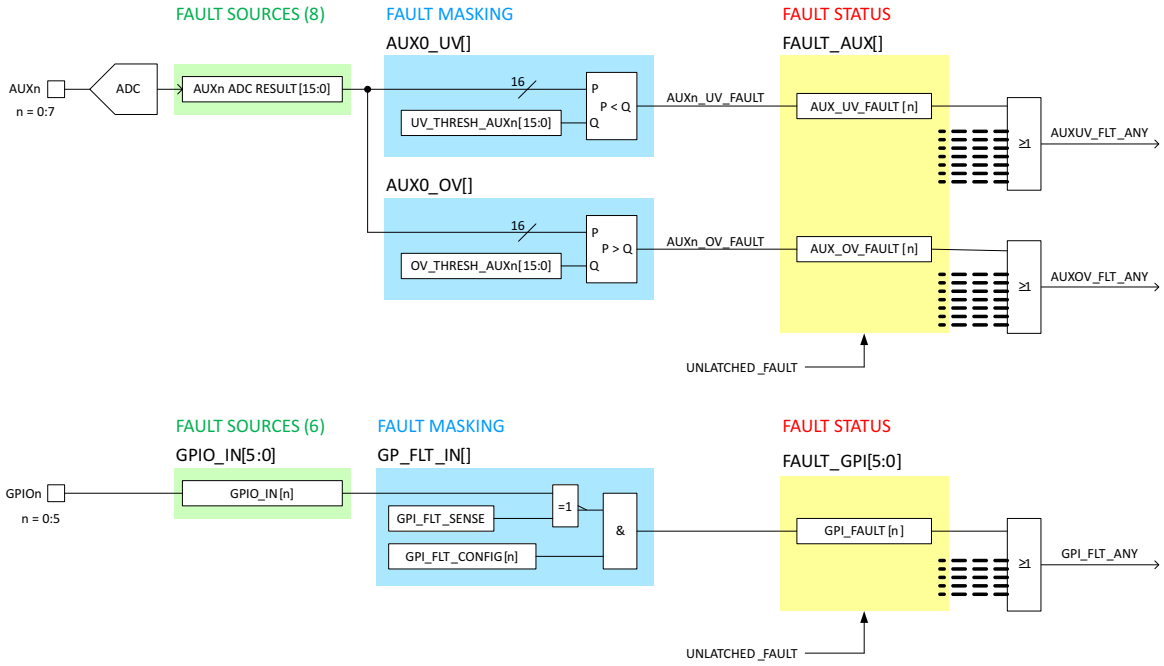


Figure 18. AUX and GPIO Pin Faults

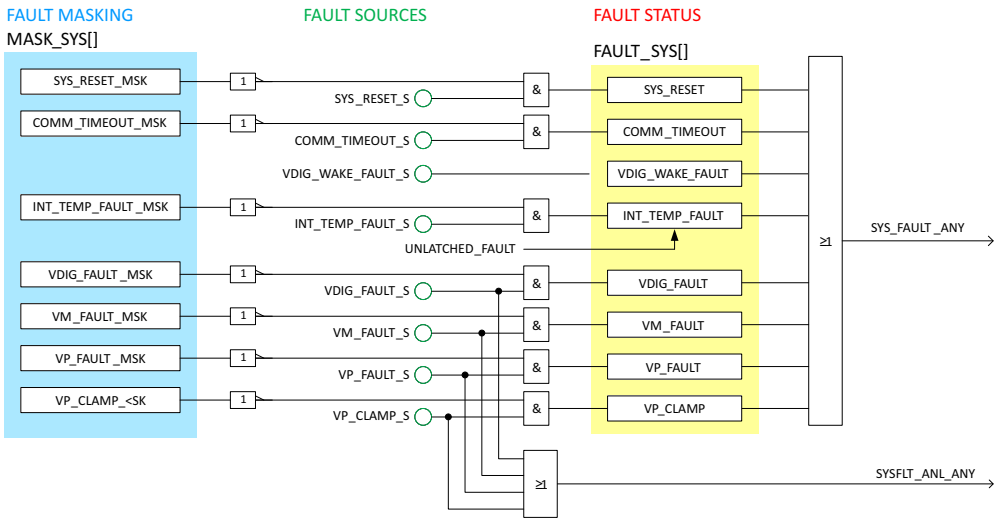


Figure 19. System Faults

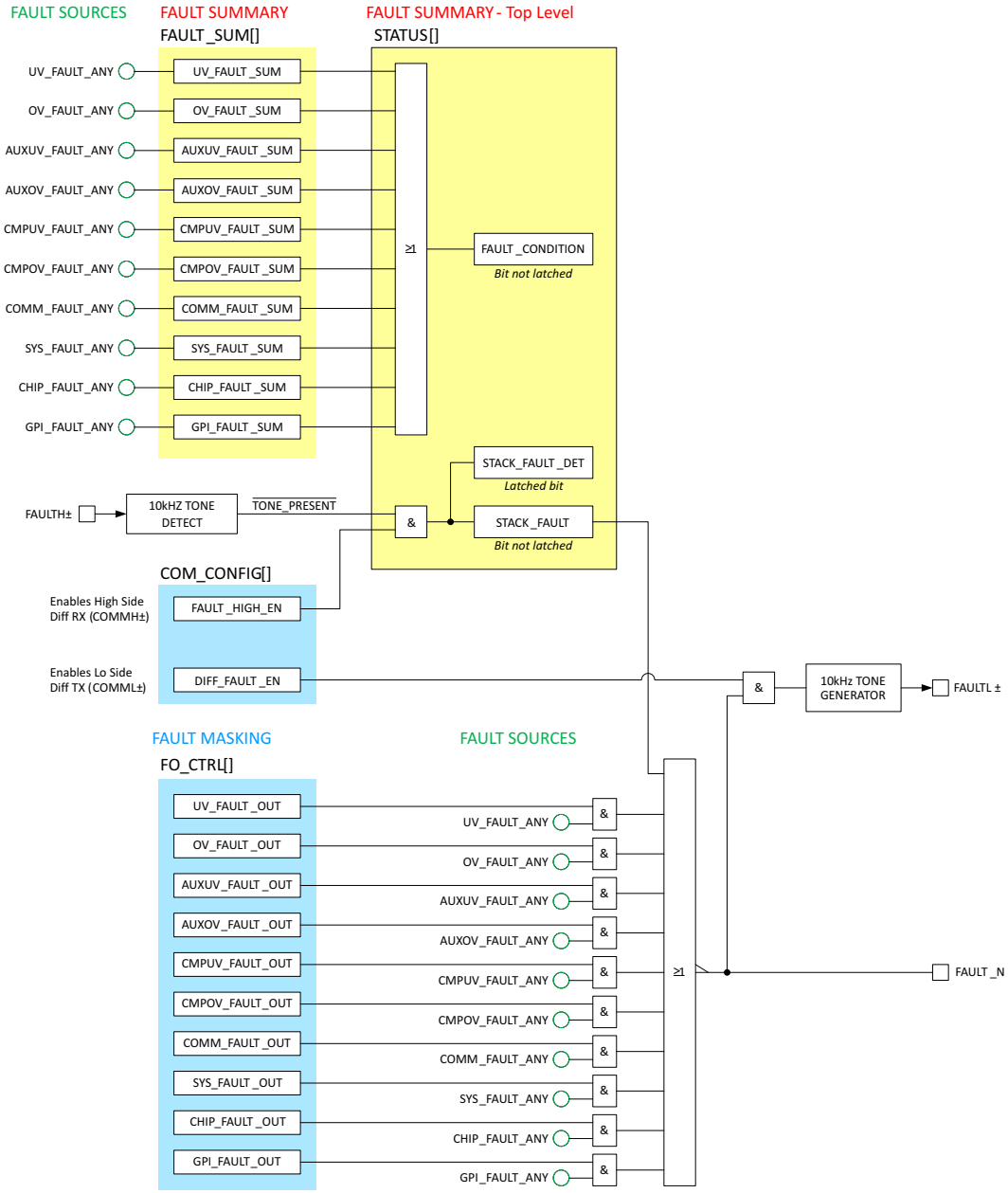


Figure 20. Fault Hierarchy Top-Level

7.3.12.2 FAULT Signaling

The FAULT bus transmits a simple heartbeat pulse at a fixed frequency when enabled and unmasked faults are not present. An IC sensing a fault condition will stop transmitting the heartbeat to the ICs in the chain below. This condition is then sensed by the ICs in the stack below, which then assert their FAULT_N pins if configured to sense the lack of tone in COMCONFIG.

The differential signal lines are isolated between ICs by a DC blocking capacitor in the same manner as the differential communications VBUS daisy chain. The capacitor is typically rated at a minimum of two times the stack voltage to provide plenty of standoff margins in the event of a fault in the system, which may expose the IC to a local hazardous voltage. One capacitor is sufficient for the normal operation of the IC. The system designer may elect to use two capacitors, one at each end of the cable or PCB wiring, for an additional safety factor. In this case, the capacitor value is doubled from the normal requirement such that the two capacitors in series result in the same value in the signal path.

The heartbeat is derived from the IC main oscillator and is generated independently out of each device in the stack. It is not copied or re-transmitted from the device above. There can be a slight variation of the frequency from device to device, but always within specification. The FAULT_COM[STK_FAULT_ERR] that indicates a problem with the fault heartbeat is sensed individually by each IC in the stack, and may be tripped in some devices and not in others under some fault conditions.

The FAULT_N pin signals faults from both internal sources and from ICs in the stack above if enabled to do so. Internal faults are signaled on FAULT_N depending on the enabled sources in the FO_CTRL register. Faults from stacked devices above are signaled on the FAULT_N pin when enabled by COMCONFIG[FAULT_HIGH_EN]. The FAULT_N pin always outputs a low signal in reset or shutdown.

7.3.12.3 Fault Sensing

Fault sources may be masked in registers MASK_COMM, MASK_SYS, and MASK_DEV. Masking a fault will prevent the flag from being set at a future time, but it will not clear a fault flag that is already set.

Any time an unmasked fault condition is triggered, it sets a bit in the appropriate FAULT_* register at addresses 0x52–63.

When an IC senses an unmasked fault, or when the fault communications are enabled and the heartbeat from the IC above stops, the FAULT_N pin is asserted low to signal the fault to a user circuit or microcontroller. Each IC in the stack, which sees one of these conditions, will assert its FAULT_N pin. The heartbeat stop and FAULT_N pin assertions occur simultaneously.

Normally after RESET, POR, or normal wakeup, user firmware must clear FAULT_SYS[SYS_RESET] to start the heartbeat. If the stack communications interface is enabled, the heartbeat will start after clearing SYS_RESET and receiving about four cycles of the heartbeat on the north-interface FAULTH pins. This typically requires a little more than 400 µs and results in clearing the STATUS[STACK_FAULT] flag.

Faults are propagated down the stack by the FAULTL pins. The bq76PL455-Q1 monitors the FAULTH pins for valid state transitions.

When COMCONFIG[FAULT_HIGH_EN] = 1, the logic will monitor the receiver for falling edges. Under-frequency conditions will set the STATUS[STACK_FAULT_DET] and STATUS[STACK_FAULT] flags. Note that this allows every other pulse to be lost without reporting an error.

Over-frequency conditions will set the FAULT_COM[STK_FAULT_ERR] flag.

The fault heartbeat stops and FAULT_N is asserted when:

- The fault heartbeat stops on the high-side fault interface FAULTH pins (if it is not configured to ignore it)
- Some automatic feature in the device detected a fault; that is, the secondary protector VSENSE comparators, checksum failure, automatic internal temperature sampling, etc.
- A command to sample, sampled a value that was out of range and caused a fault
- An internal self-test command fails

NOTE

The STK_FAULT_ERR may not be clearable under some conditions.

1. If a STK_FAULT_ERR is detected, and then no more edges appear on the high-side fault pins (as would be the case if the chip above had a fault condition), it may be impossible to clear the STK_FAULT_ERR flag. Once proper signaling resumes on the high-side fault pin, it will again be possible to clear this fault.
2. A masked STK_FAULT_ERR is not cleared during initialization. As a result, there is an approximately 4.5-µs window at startup. Such as, if the high-side fault receiver detects more than four falling edges, STK_FAULT_ERR will be set even though it is masked.

7.3.12.3.1 Fault Output Control

FO_CTRL allows groups of unmasked and enabled faults to drive the pin when the appropriate bit is set. When the register bit is set, any fault of the indicated type will cause the assertion of the fault outputs (FAULTL, FAULT_N) if they are enabled—that is, FAULT_N will be driven low and the tone on FAULTL pins will be stopped.

The following groups of faults are enabled in this register (see *FO_CTRL 0x6E–6F (110–111) Fault Output Control* for bit position details).

- Any UV fault (VSENSE inputs)
- Any OV fault (VSENSE inputs)
- Any UV fault (AUX inputs)
- Any OV fault (AUX inputs)
- Any UV fault (window comparators)
- Any OV fault (window comparators)
- Any communications fault
- Any system fault (see FAULT_SYS)
- Any device fault (see FAULT_DEV)
- Any GPIO fault (see FAULT_GPI)

7.3.12.3.2 Fault Masking

Fault sources can be enabled or masked individually or in groups in these registers. Masking the fault prevents it from being set, but does not clear an existing fault bit.

- MASK_COMM—Communications related faults
- MASK_SYS—System faults in power supplies, over temperature, and so on
- MASK_DEV—Internal register checksum faults, and so on
- GP_FLT_IN—GPIO input level faults

7.3.12.4 Fault Latching

When UNLATCHED_FAULT is set, the bits in some of the fault registers (see the following text and *Register Details* for included registers) will automatically clear when the fault condition goes away. Faults that are set continuously will clear when the condition goes away. Faults that are set by an event (such as when a channel is sampled) will clear when that channel is sampled. In this mode, writing to the included fault registers will have no effect. Unlatched faults when detected and cleared can result in creating transient behavior for the associated flag bits, the FAULT_N, and FAULTL pins.

The DEVCONFIG[UNLATCHED_FAULT] bit should only be changed while no fault bits are set. The latched/unlatched status of fault bits is undefined when the UNLATCHED_FAULT bit is changed while a fault bit = 1.

Fault bits in these registers are unaffected by the DEVCONFIG[UNLATCHED_FAULT] bit and are always latched:

- FAULT_COM—All bits
- FAULT_SYS—All bits except INT_TEMP_FAULT
- FAULT_DEV—All bits

The DEVCONFIG[UNLATCHED_FAULT] bit when set prevents the latching of fault bits in the following registers:

- FAULT_UV—Undervoltage VSENSE ADC limit exceeded
- FAULT_OV—Overvoltage VSENSE ADC limit exceeded
- FAULT_AUX—Programmable AUX threshold in AUXn_UV or AUXn_OV exceeded
- FAULT_2UV—Undervoltage VSENSE secondary protection comparator limit exceeded
- FAULT_2OV—Overvoltage VSENSE secondary protection comparator limit exceeded
- FAULT_SYS—System level faults; power supplies, over temperature, communications timeout, reset
- FAULT_SYS—INT_TEMP_FAULT bit only
- FAULT_GPI—GPIO (programmable) logic input level triggered a fault

7.3.12.5 OV, UV FAULT Application Notes

In unlatched mode, when secondary protector (window comparator) faults are sensed and recorded in the FAULT_2UV and FAULT_2OV registers, and one or more other analog die faults (that is, VP_FAULT, VDIG_FAULT, and VM_FAULT) are present, none of the mentioned faults will clear until all have been cleared, even if the cause of the fault has gone away. That is, they may appear to act as though they are latched until all have been cleared.

If these faults (FAULT_SYS[VP_FAULT, VP_CLAMP, VM_FAULT, or VDIG_FAULT]) are present, it is reasonable to assume that the comparators may not be functioning properly and/or may have stopped reporting a fault because they stopped functioning rather than the fault condition having gone away.

7.3.12.6 Fault Status and Fault Reset

Fault status can be read or reset individually or in groups in the following registers:

STATUS—The sum of all faults plus stack fault conditions are in this register, some faults are reset here. This register is at the top of the fault hierarchy.

FAULT_SUM—Groups of faults are summarized by single flags in this register and may be simultaneously read or reset here, level 2 of the hierarchy.

FAULT_UV—Undervoltage VSENSE ADC limit exceeded, level 3 of the fault hierarchy

FAULT_OV—Overvoltage VSENSE ADC limit exceeded, level 3 of the fault hierarchy

FAULT_AUX—Programmable AUX threshold in AUXn_UV or AUXn_OV exceeded, level 3 of the fault hierarchy

FAULT_2UV—Undervoltage VSENSE secondary protection comparator limit exceeded, level 3 of the fault hierarchy

FAULT_2OV—Overvoltage VSENSE secondary protection comparator limit exceeded, level 3 of the fault hierarchy

FAULT_SYS—System level faults; power supplies, over temperature, communications timeout, reset, level 3 of the fault hierarchy

FAULT_GPI—GPIO (programmable) logic input level triggered a fault, level 3 of the fault hierarchy

7.3.12.7 Checksum Faults

To discover changes to registers, the bq76PL455-Q1 constantly runs a background check on the contents by computing a checksum and comparing it to a stored value. Changes are detected approximately every two microseconds. The changes can be intentional (that is, a change written by the microcontroller), unintentional (due to an unexpected device or system fault), or in some cases the result of an automated operation (expiration of the balancing timer). The test is run against the registers in both TI space and USER space. Most registers, which might be changed by the microcontroller, are included; consult *Register Summary* for an exact list of included locations.

The currently computed checksum value is held in the CSUM_RSLT register. It is compared against the stored checksum value held in register CSUM. The value stored is updated by reading the current value in CSUM_RSLT and writing it back to the CSUM register. It is then usually saved to EEPROM by setting MAGIC1, MAGIC2, and DEV_CTRL[WRITE_EEPROM].

When CSUM and CSUM_RSLT do not match, the FAULT_DEV[USER_CKSUM_ERR] flag will be set until the condition is corrected. This fault flag is unlatched and will self-clear when the mismatch is corrected.

The TI EEPROM space is also continuously monitored in a similar fashion concurrently with the monitoring of the USER space. If a register change is detected, the FAULT_DEV[FACT_CKSUM_ERR] flag is set. If this ever occurs, the user firmware should perform a soft RESET of the part. This fault flag is not self-clearing and must be cleared by writing a '1' to the bit. If this does not correct the issue, the part should not be used.

7.3.12.7.1 Checksum Testing

Each of the checksums (TI, USER spaces) has a test mode that causes each input bit to the checksum calculation (that is, the register bits which are part of the checksum calculation) to flip twice (once per clock) and the number of toggles on the checksums fault output are counted in the TEST_CSUM register. This helps to ensure that the background checksum testing described previously correctly discovers any bit, which might be in the wrong state.

The tests are initiated by the user's firmware usually as a part of self-testing and validation. The TESTCTRL[CKSUM_TEST_RUN] bits are set to begin the test on either the TI or USER space registers. See Section 13.4.16 for details of the bit settings.

NOTE

Other faults may be set in the process of running this procedure and should be ignored.

7.3.12.8 AUXn OV/UV Threshold Faults

The AUXn input pins can be used to trigger a fault indication. The OV and UV thresholds for each AUXn input can be set independently in the AUXn_OV and AUXn_UV registers. The result of each AUXn channel conversion is compared to these values. When the threshold is exceeded (less-than AUXn_UV, greater-than AUXn[OV]), the FAULT_N and FAULTL pins are asserted if enabled. To stop unwanted FAULT pin assertions from one or more channels (but other channels are desired), the threshold voltage settings for the undesired channels can be set to their minimum and maximum values, or only convert the desired channels.

FAULT_AUX[AUX_UV_FAULT, AUX_OV_FAULT] will be continually set based the currently stored ADC result and threshold. This allows the threshold and fault to be tested by changing the threshold without having to sample the channel.

Example:

The design requires AUX0 and AUX1 UV triggers at 1V, and AUX0 and AUX1 OV triggers at 3V. The design requires that no FAULT pin activation result from AUX UV or OV conditions on AUX2…AUX7. Set the following conditions:

AUX0_UV = 1 V, AUX0_OV = 3 V
AUX1_UV = 1 V, AUX1_OV = 3 V
AUX2_UV = 0 V, AUX2_OV = 5 V
AUX3_UV = 0 V, AUX3_OV = 5 V
AUX4_UV = 0 V, AUX4_OV = 5 V
AUX5_UV = 0 V, AUX5_OV = 5 V
AUX6_UV = 0 V, AUX6_OV = 5 V
AUX7_UV = 0 V, AUX7_OV = 5 V

7.3.12.9 Secondary Protectors: Analog Window Comparators for Cell UV/OV

Thirty-two analog comparators, connected in pairs as window comparators for the 16 channels provide cell voltage monitoring independently from the main acquisition path and work in parallel with the main ADC route. In case of malfunction of the AFE or ADC, the analog comparators will still be able to flag the crossing of the (register selectable) undervoltage and overvoltage comparator thresholds.

The faults sensed by the analog window comparators are configured by the number of channels enabled in the NCHAN register. To avoid undesired comparator faults, two internal DACs set the independent overvoltage (COMP_OV) and undervoltage (COMP_UV) thresholds. The DACs use the REF2 (4.5 V) reference which is an independent circuit from the 2.5 V (VREF) ADC reference. The OV threshold can range from 2 V to 5.175 V in steps of 25 mV. The UV threshold can range from 0.7 V to 3.875 V in steps of 25 mV.

OV and UV faults, OV-only faults, or no faults are enabled in the DEVCONFIG[COMP_CONFIG] register. Enabling UV-only fault is not possible.

7.3.12.9.1 Window Comparator Special Considerations

As shown in Figure 21, internally there are approximately 100-Ω resistors in series with each VSENSE pin that isolate the connections to the AFE from the secondary protector circuits (window comparators). This is provided to help prevent some common-cause failure from affecting both the AFE and secondary-protector circuits.

A "Squeeze" function is provided in the device to help detect open-sense wire (to the monitored cell) conditions. When the Squeeze function turns on, it places an approximately 5-kΩ resistance across adjacent VSENSE inputs, and creates an additional voltage drop through the approximately 100-Ω series resistors. This causes the apparent increase in the voltage applied to the window-comparator blocks immediately above, and below, the inputs that have the Squeeze resistor applied. The increased voltage is only seen by the comparators and not by the AFE. This in turn may cause the OV comparator fault to trip even if the external sense-pin voltage measurement says otherwise, depending on the user's setting of the OV threshold.

CAUTION

If the squeeze function is used under open wire conditions and the connection to the required external Zener is broken, internal IC damage may occur.

If the squeeze function is used under open wire conditions and the connection to the required external Zener is broken, internal IC damage may occur. It is highly recommended to run all diagnostic tests on the bq76PL455 once the open wire condition has been corrected. Special attention should be placed on the validation of the window comparator accuracy against the AFE accuracy to ensure parametric compliance. In the event of non-compliance, the affected bq76PL455 should be removed from service immediately.

In example, the Squeeze resistor is enabled for (across) VSENSE2 to VSENSE3. This will cause the apparent voltage seen by the comparators for cell 2, and cell 4 to increase. For the cell voltage for cell 3, in this case is approximately 3.6 V, there will be an additional drop on the internal lines going to the window-comparator block (but not the AFE) of approximately (3.6 V / 5K × 100 × 2) = approximately 144 mV. This will also show up as an increase of approximately 72 mV on the cells above and below the cell that is being squeezed. Larger input resistors, such as 1 kΩ, will dominate this error source and may result in unexpected trips of the window comparators, depending on the threshold settings used.

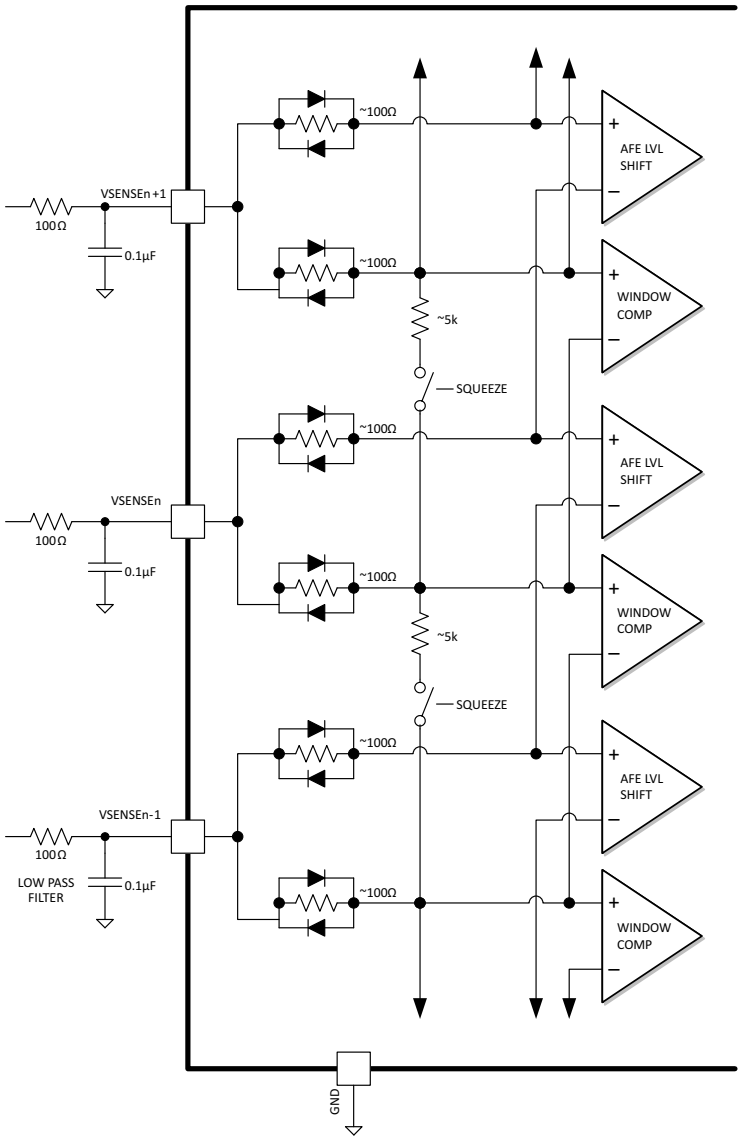


Figure 21. Window Comparator Input Configuration Overview

7.3.12.10 Communications Faults

During the course of normal data communications, noise may induce errors in the bit stream. The errors may assert faults depending on the mask settings in the MASK_COMM and MASK_SYS registers.

- UART communications faults are discussed in *UART Interface to Host Microcontroller*.
- Differential (VBUS) communications faults are discussed as part of the protocol description in *Protocol Description*.

7.3.12.11 Communications Timeout Counters

The communication timeout counters can be checked by setting and reading the 24 most-significant bits of the timeout counter using COMM_TIM_CNT. The timeout counter is driven by a 4-kHz clock source. To aid this testing, CCNT_RST_OFF may be set so the communication sent to set or monitor the counter does not reset the counter. The counter value may be set using COMM_TIM_CNT to enable faster testing of long periods. The bits that are not accessible are set to '1' by writing this register so counter rollovers can be quickly tested.

7.3.13 Built-in-Test Functions

Test functions may be accessed by setting bits in various registers. These bits are identified in the descriptions of the appropriate registers and their bits in *Register Details*.

7.3.13.1 Safety Manual and FMEDA

These documents are available separately from Texas Instruments. Please contact your TI Sales Associate or Applications Engineer for further information.

7.4 Device Functional Modes

The device has three power states (modes):

- SHUTDOWN (sleep)—The lowest power state used for long periods of inactivity to extend battery life.
- IDLE—The default state when awake and ready to receive and execute commands.
- ACTIVE—The highest power state while communicating; that is, IDLE + communications activity.

7.4.1 SHUTDOWN

SHUTDOWN is the lowest power state available in the part. In this state, most internal blocks are powered off and monitoring is disabled. SHUTDOWN is typically used for long periods of inactivity when the battery is not being charged or discharged. The part must receive a high signal on the WAKE pin, or WAKEUP tone via the vertical communications bus to transition to the IDLE state.

To enter SHUTDOWN, external sources of VP, VDIG, VIO and all I/O pin voltage sources (communication, fault, GPIO or AUX inputs) must be removed or disabled. While in SHUTDOWN mode, these must remain off or disabled to avoid back powering the bq76PL455-Q1 via internal ESD structures. The bq76PL455-Q1 will immediately go into reset when VIO is lowered. If VIO is held low for longer than VIO_{SD_DLY} MAX, then the device will enter SHUTDOWN mode.

If VIO is held low for approximately 5 seconds, the device will enter shutdown mode. The WAKEUP pin must be held in the low state to allow the device to enter and remain in the SHUTDOWN state (setting the pin low does not place the device in SHUTDOWN). If the WAKEUP pin is allowed to remain in the high state, the device will cycle off and immediately back on. Operation is unpredictable if the pin is allowed to float. This is not harmful to the device, but may not provide the expected behavior in the designers system.

If the NPN circuit is not used (external supply), VP and VDIG should be turned off immediately after entering shutdown mode. Lowering VP and VDIG will also put the device in shutdown mode.

Device Functional Modes (continued)

The part will enter SHUTDOWN when the following occurs:

- The user requested SHUTDOWN via a command by asserting DEV_CTRL[PWRDN]. This is usually done with a broadcast form of the command. The WAKEUP pin on the base bq76PL455-Q1 must be held in the low state.
- There was a communications timeout caused by the timer set in register CTO[COMM_PD_PER] expired due to:
  - No valid frames (packets) were received in the set period, <OR>
  - TSTCONFIG[CCNT_RST_OFF] is set and the timer expired whether valid frames were received or not, usually as a part of BIST.
- TSTCONFIG[VDIG_TEST] was set at some time since the last SHUTDOWN <AND> VDIG dropped below its SHUTDOWN threshold ($DDIE_{POR}$). Once set, subsequently clearing TSTCONFIG[VDIG_TEST] will not disable this control even though the bit will read 0. It will not be disabled until the device enters shutdown.
- One of the two thermal shutdown (TSD) circuits sensed an overtemperature condition (there is one sensor on each die that operates independently, with separate register flag indicators).
- VIO was below its VIOPOR threshold for longer than VIO_{SD_DLY}.
- V5VAO was below the $V5VAO_{SD}$ threshold.
- Internal VP regulator is on and attempting to drive the NPNB signal, but VP remained below the VP_{SD_POR} threshold for longer than VP_{SD_DLY}.

NOTE

Once in the SHUTDOWN state, the part must be re-awakened as below to continue normal operations.

7.4.2 Wakeup

The bq76PL455-Q1 device will wake up and enter the IDLE state when either or both of the following conditions occur.

1. The WAKEUP pin is high.
2. The WAKE tone is received on the COMML pins.

7.4.3 Wakeup Behavior from SHUTDOWN

The WAKEUP pin is used to bring the part from the SHUTDOWN state to the IDLE state. It can do this in any stack position. However, it is typically only used by the base device when driven from a microcontroller. The pin is level sensitive and is normally kept at a low (logic zero) level. When the part is in SHUTDOWN, and the WAKEUP pin is brought high, the part will transition from SHUTDOWN to IDLE. After applying the high signal, the WAKEUP pin must be de-asserted and returned to the low state to allow the part to enter SHUTDOWN again. Upon changing state, the bq76PL455-Q1 will briefly transmit a differential wakeup tone on its COMMH+ and COMMH– pins to the next higher bq76PL455-Q1, where it is received on that device's COMML+ and COMML– pins.

NOTE

The WAKEUP pin is usually kept in the de-+asserted (low) state. If the pin is asserted (high) and then the device is commanded to SHUTDOWN, it will immediately reawaken and become IDLE. This pin must not be allowed to float to prevent unexpected state transitions. Use caution that the pin does not float if the device driving the pin is not powered.

The wakeup tone is sent by the bottommost ("south" most) device in the stack out the COMMH pins in response to the WAKEUP pin assertion. The next device to the north receives the WAKEUP tone on its COMML pins. It awakens, which in turn sends the WAKEUP tone to the next device above it. The WAKEUP tone propagates up the stack in this way to wake all devices in the stack. While the part is in SHUTDOWN, the COMML pins are in receive mode, and any transmission is aborted.

Device Functional Modes (continued)

7.4.4 Power-On Reset (POR) or Wakeup

The IC's state machine is fully reset at wakeup. Wakeup causes the VP/VDIG output to come up, which in turn brings up VDD18, providing power to portions of the analog circuits and all of the core logic including the registers and the EEPROM. This is effectively a POR of the part. All registers are loaded with values stored in EEPROM. Registers, which are not loaded from EEPROM, are reset to their default values indicated in Table 5.

NOTE

Immediately following a reset for any reason, some faults are not valid (=0) until a sample is taken. All fault bits in registers FAULT_UV, FAULT_OV, and FAULT_AUX are invalid. In addition, the following bits are also invalid: FAULT_DEV[HREF_FAULT, HREF_GND_FAULT]. Reading a fault register will not cause a sample to be taken or the bits to be updated. A command must be sent to the device to sample all channels to update the above listed fault bits, making them valid.

Note that this sequence is the same regardless of the reset source—POR, soft reset, wake tone received from part below.

1. External NPN regulator circuit turns on. VP, VDIG, (and VIO if connected to VP) begin to ramp up. If VIO is supplied by an external source (such as, the microcontroller I/O power supply), then VIO must be stable and greater than its POR threshold.
2. Once VDIG reaches its POR threshold, the internal 1.8 V (internal digital supply VDD) regulator begins to ramp up. Once VP reaches its POR threshold, VREF begins to ramp. The reference for the VDD (1.8 V) supply is VREF, so it will not reach its final operating voltage until VREF reaches its final voltage.
3. Once VP, VDIG, VIO, and VDD all reach their POR thresholds, the oscillator starts up.
4. Once the oscillator is running, the Finite State Machine (FSM) starts up and begins sending the wake tone the wake tone out of the high-side interface (COMMH±).
5. The FSM in turn waits approximately 10 µs for the EEPROM to be ready.
6. All system registers will be loaded from EEPROM.
7. Relevant information will be propagated to the Analog die registers, except regulator power down.
8. If GPIO addressing is enabled (DEVCONFIG[ADDR_SEL] = 0), the GPIO[4:0] pins are sampled to determine the device's communication address and recorded in ADDR.
9. Sample the internal Digital-die temperature channel. This pre-loads the value, so temperature-based calibration will function properly. No other channels will be sampled during initialization and faults will not be generated from them until *after* they are sampled.
10. Clear any masked faults that could have occurred. This includes clearing threshold-based faults that are masked by their threshold.
11. Begin monitoring for UART communications.
12. Initialize Analog die faults. (Continue sequencing in parallel; do not wait for the following sub-sequence to complete.)
    (a) Wait until no VM fault is reported from Analog die or the user writes '1' to STATUS[SYS_INIT].
    (b) Enable all Analog die fault registers.
    (c) Set STATUS[SYS_INIT] = 0.
13. Wait for wakeup tone to complete.
14. Begin monitoring for differential communications.
15. Once the FAULT_SYS[SYS_RESET] fault is cleared by the host microcontroller, turn off the external NPN-regulator circuit if the regulator is disabled (that is, DEVCONFIG[REG_DISABLE] = 1).

Many faults will not be properly reported and sampling commands may not function properly while the system initialization sequence above is in progress (while SYS_INIT reads '1'). Also, note that aborting the initialization sequence (by writing '1' to SYS_INIT) may cause erroneous faults to be reported and sampling of Analog channels to report invalid results until the VM voltage is up and stable.

Device Functional Modes (continued)

Upon application of power or device wakeup, communications are ignored during the startup process for a minimum time of 1 ms plus one sample period as set in the EEPROM. It is possible to shorten the required wait by setting the initial sample period stored in EEPROM to a very fast value. Because the "fast" sample period is not usually matched to the external capacitor on the OUT1 pin, the initial sample may have a large error, causing false detection and activation of fault indicators. After the part is up and running, the user firmware will need to update the sample period and averaging registers to work at the slower speed correct for the chosen OUT1 capacitor.

Additionally, it normally requires a maximum of approximately 200 µs to enable UART communications and approximately 40 µs to complete initialization after the VM fault clears (or the user aborts the initialization sequence).

7.4.5 Calculating Wakeup Timing

The following sequences assume that the microcontroller power circuit provides the VIO supply. The host microcontroller initiates the sequence and the VIO is up and stable. (The sequence does not change if VIO is tied to the regulator. However, if some other source is providing WAKEUP, but the VIO supply is provided by the microcontroller, the VIO supply needs to clear the POR threshold within a few microseconds of WAKEUP or the part will go back into shutdown.)

1. The user asserts the WAKEUP pin on the bottom board's base device.
2. At this point, the VP regulator will turn on and ramp the VP/VDIG supplies. The time required to reach the POR thresholds for VP/VDIG varies and is dependent on the designer's component selection. (Note that VP/VDIG/VIO must all reach their respective POR thresholds).
3. The time from reaching the POR thresholds to the start of the wakeup tone being transmitted from the high-side interface is specified as t_{WAKEUP_DLY}.
4. The time from the start of the wakeup tone being transmitted until communications are allowed to this part is specified as $t_{WAKEUP\_TO\_UART}$.

NOTE

It is acceptable to begin communicating with this part at this point if it is the only part in the stack. If there are additional parts in the stack, you can still begin communicating with the bottom part at this point. However, this may cause communications error flags to get set in bq76PL455-Q1 parts positioned higher in the stack.

5. The time from the wakeup tone being transmitted from the high side of the device below (end of step 3), until the regulator turns on the current board, is specified as ($t_{WAKE\_TONE\_DLY\_DC} - t_{WAKEUP\_DLY}$).
6. The regulator turns on and ramps the VP/VDIG/VIO supplies. As with the bottom board, this time is board dependent.
7. The time from reaching the POR thresholds to the start of the wakeup tone being transmitted from the high-side interface to the next IC up the stack is specified as t_{WAKEUP_DLY}. Note that for calculation purposes to group #5 and #7 together as $t_{WAKE\_TONE\_DLY\_DC}$.
8. The time from the wakeup tone being transmitted from the high-side interface until you are allowed to communicate with this part is specified as tWAKEUP_TO_DCOMM.

If there are additional parts in the stack, steps 5–8 are applied accordingly.

To compute the total time from assertion of WAKEUP to the stack being ready for communications, we will define:

- t_{BOT_RAMP} as the time needed for the supply ramp on the bottom board
- t_{STACK_RAMP} as the time needed for the supply ramp on all stacked boards
- n_{STACK_BOARDS} as the number of stacked boards (not including the bottom board)
- n_{ABOVE_BOARDS} as the number of boards above the current board in the stack

Device Functional Modes (continued)

If we have only one device, then the required delay from WAKEUP until it is acceptable to begin communicating will be:

$t_{BOT\_RAMP} + t_{WAKEUP\_DLY} + t_{WAKEUP\_TO\_UART}$

Else, if we have more than one board in the stack, the delay from WAKEUP until it is acceptable to begin communicating will be:

$t_{BOT\_RAMP} + t_{WAKEUP\_DLY} + n_{STACK\_BOARDS} * (t_{STACK\_RAMP} + t_{WAKE\_TONE\_DLY\_DC}) + t_{WAKEUP\_TO\_DCOMM}$

NOTE

The reason for doing this would be that the board above is not responding for some reason and you are attempting to recover it. Depending on the state of the boards above, this calculation could be rather pessimistic. However, without knowing anything else, this is the safest timing.

It is generally acceptable to begin communicating with the stack once the bottom UART interface is ready for communications. However, parts above in the stack may not respond until their above mentioned times. It is also possible to cause communications error flags to be set in the parts above by doing this. However, the fastest way to get the stack talking (assuming all parts have the EEPROM burned for their stack location and configuration) may be to continuously send a read request to the top device until it responds and then clear all communications errors that have been caused.

If you try to send communications to the bottom device before the UART interface is ready, it can get out of sync. To fix this, send a comm_clear. This is not necessary for parts on the differential interface, since they will re-synchronize to the bottom chip on every frame. Therefore, only the bottom chip can lose synchronization.

7.4.6 Soft Reset

Setting the SOFT_RESET bit in the DEV_CTRL register will not power down the device, but it will fully reset/restart the state machine per the sequence above in *Power-On Reset (POR) or Wakeup*. All ICs in the stack above the reset part will wake up if in SHUTDOWN and reset if awake.

7.4.7 Wakeup Behavior in IDLE Mode

When the part receives a WAKEUP tone while it is already awake, it performs a reset. The IC requires 10 pulses of the received WAKEUP tone to begin the reset process. Sending the tone will wake it if asleep, or reset it if idle. The result is that sending the wakeup tone to parts in the stack can be used to reset them and cause all to enter the IDLE state whether they were previously in SHUTDOWN or IDLE. This is another method to reset the state of all devices in the stack.

The device will generate a wakeup tone to the other devices "north" in the chain as a part of the reset sequence. As a result, each IC above the device receiving the wake tone will in turn be reset.

7.5 Command and Response Protocol

This protocol enables a single host, such as a microcontroller, to communicate with one or more bq76PL455-Q1 devices. The host initiates every transaction between the host and one or more bq76PL455-Q1 devices. The bq76PL455-Q1 will never send data to the host without first receiving a command from the host.

NOTE

After each command is transmitted, the initiator should *always* wait for all expected responses to be returned (or a timeout in case of error) before initiating a new command.

The phrases "Write without Response" and "Write" or "write" are equivalent and synonymous.

The phrases "Write with Response" and "Read" or "read" are equivalent and synonymous, unless otherwise noted.

Command and Response Protocol (continued)

7.5.1 Transaction Frame Description

The transaction frame format includes both Command Frames and Response Frames. There are five field types used within a transaction frame:

1. Frame Initialization
2. Device Address or Group ID
3. Register Address
4. Data
5. Cyclic Redundancy Check (CRC)

Note that not all byte types are part of every transaction frame.

7.5.1.1 Frame Initialization Byte

The Frame Initialization Byte is always the first byte of the frame. In all cases, the length of the frame can be determined from this initial byte. Note that bit 7 identifies each frame as either a command frame or a response frame. The initialization byte is defined as follows for each of the two Frame Init types:

	7	6	5	4	3	2	1	0
Command Frame Init	FRM_TYPE = 1	REQ_TYPE			ADDR_SIZE	DATA_SIZE		
Response Frame Init	FRM_TYPE = 0	RESP_BYTES-1						

The fields shown in the frame initialization bytes above are described in Table 4.

Table 4. Frame Initialization Byte Fields

	VALUE (BINARY)	DESCRIPTION
FRM_TYPE	0	Response Frame
	1	Command Frame
REQ_TYPE	000	Single Device Write with Response
	001	Single Device Write without Response
	010	Group Write with Response
	011	Group Write without Response
	100	Reserved
	101	Reserved
	110	Broadcast Write with Response
	111	Broadcast Write without Response
ADDR_SIZE(1)	0	8-bit Register Address
	1	16-bit Register Address
DATA_SIZE(2)	000	0 bytes
	001	1 byte
	010	2 bytes
	011	3 bytes
	100	4 bytes
	101	5 bytes
	110	6 bytes
	111	8 bytes
RESP_BYTES-1		Number of data bytes contained in response frame minus 1

(1) ADDR_SIZE = 0 is recommended. All USER registers are addressable using an 8-bit register address.
(2) Data size of 7 bytes is not supported.

7.5.1.2 Device Address/Group ID Byte

The Device Address or Group ID Byte identifies the device or group of devices targeted by the command. Only those devices that contain a matching value in their Device Address Register (register address 10) or Group ID Register (register address 11) will respond to the command. The REQ_TYPE field in the command frame will determine how this byte is interpreted.

NOTE

Device Address/Group ID Byte is not present in a Broadcast command frame.

	7	6	5	4	3	2	1	0
Device Address or Group ID	Identifier of device(s) receiving communication (always one byte)							

7.5.1.3 Register Address Byte(s)

Register addresses can be one or two bytes in length. For single byte addresses (ADDR_SIZE = 0), the MSB is not transmitted and is assumed to be 0.

	7	6	5	4	3	2	1	0
Register Address (MSB)	Register being targeted							
Register Address (LSB)								

7.5.1.4 Data Bytes

Data byte interpretation is based on the type of command frame being sent and the target register specified in the command frame.

For command frames targeted at the Command Register (address 2), the data will contain the command or highest responding device address and, optionally, new data for the Command Channel Select Register (address 3–6) and Averaging Register (address 7).

For command frames targeted at other registers, the data bytes will contain the data to be written into the targeted register(s) in the case of Write without Response commands, or the requested number of bytes — 1 in the case of Write with Response commands.

	7	6	5	4	3	2	1	0
Data[0] … Data[n]	Data Bytes (the number of bytes should match the DATA_SIZE field in the Frame Initialization byte)							

NOTE

Transactions with seven data bytes are not possible.

7.5.1.5 CRC Bytes

	7	6	5	4	3	2	1	0
CRC (MSB)	16-bit CRC (CRC-16-IBM—See *CRC Description*)							
CRC(LSB)								

7.5.2 CRC Description

The standard CRC-16-IBM algorithm uses the following CRC generator polynomial:

$X_{16} + X_{15} + X_2 + 1$

In general, a CRC (cyclic redundancy check) represents the remainder of a process analogous to polynomial long division, where the frame being checked is "divided" by the generator. The CRC appended to the frame is the "remainder". Because of this process, when a frame is received, the CRC calculated by the receiver across the entire frame including the transmitted CRC will be zero, indicating a correct transmission and reception. A non-zero result indicates a communication error.

The CRC calculation by the transmitter is computed in bit-stream order across the entire transmission frame (except for the CRC, of course). When determining bit-stream order for implementing the CRC algorithm, it is important to note that protocol bytes are transmitted serially, least-significant bit first.

An efficient, 8-bit parallel, C function that can be utilized directly is included at the end of this section. The following pseudo-code algorithm is a more easily described bitwise implementation of the CRC algorithm utilizing the CRC-16-IBM generator polynomial:

```
 CRC='0000_0000_0000_0000'
DIN={(frame in bit-stream order), '0000_0000_0000_0000'};
for n=0 to length_in_bits(DIN)-1{
CRC15:0={(CRC0^DINn), CRC15, (CRC14^CRC0),CRC13:2,(CRC1^CRC0)};
};
```

In this notation, subscripts represent zero-based bit selection from either the frame data bit stream or the 16-bit CRC (as it is being calculated), strings in single quotes (') represent binary constants, the caret (^) denotes a single-bit exclusive-or operation and the curly-brace – comma ({a, b, … c}) expressions denote bitwise concatenation. Underscores (_) are only to enhance readability and can be ignored.

The 16-bit CRC is initialized to all 0-bits. DIN is the frame to be transmitted or received in bit-stream order, with sixteen 0-bits appended to the end. The expression "length_in_bits(DIN)" will equal the length of the input in bytes * 8 + 2. The "for" loop is intended to iterate over DIN one bit at a time in bit-stream order. CRC15:0 is the 16-bit CRC to be transmitted (or checked in the case of a received frame). Note that the bitwise concatenation on the right-hand side of the CRC equation is also 16-bits in total length.

The bit numbers used in the equation for the CRC (inside the "for" loop) have been chosen so that X16 in a formal mathematical description (such as the specification of the CRC-16-IBM generator polynomial) corresponds with bit 0 in the subscript notation in the pseudo-code. In the pseudo-code, bit 0 is the least-significant bit and is on the right-hand side of the concatenation. Bit0 is the first bit transmitted on the wire using serial communication. An artifact of this notation and algorithmic choice is that the final CRC of the algorithm is byte-reversed with respect to how we will store the values in memory. Specifically, the byte labeled "CRC (MSB)" in the frame descriptions throughout this document is the *low* order byte of the CRC generated by both the pseudo-code and the C function, and the byte labeled "CRC (LSB)" is the *high* order-generated byte. The advantage of arranging the generated CRC word in this way is that no bit-level reversal is needed.

The following example will be useful to an algorithm implementer to verify that their final implementation is correct. In this example, an initiator (microcontroller) is generating a CRC for a command frame. The following sample frame will be used:

	7	6	5	4	3	2	1	0
Command Frame Init	1	001 (binary)			0	001 (binary)		
Device Address	03							
Register Address	07							
Data	05							
CRC (MSB)	1E							
CRC (LSB)	CF							

For this example, by the time the "for" loop in the pseudo-code above is executed, CRC is 0, and DIN (in hex bytes) is 91, 03, 07, 05, 00, 00. In bit-stream order, this becomes:

DIN = '1000_1001_1100_0000_1110_0000_1010_0000_0000_0000_0000_0000'

As the "for" loop executes, the CRC value, based on each subsequent bit of DIN, progresses as follows:

n	DINn	CRC15:0		n	DINn	CRC15:0		n	DINn	CRC15:0
0	1	1000 0000 0000 0000		16	1	0010 0001 1100 1001		32	0	0100 1010 0001 0101
1	0	0100 0000 0000 0000		17	1	0011 0000 1110 0101		33	0	1000 0101 0000 1011
2	0	0010 0000 0000 0000		18	1	0011 1000 0111 0011		34	0	1110 0010 1000 0100
3	0	0001 0000 0000 0000		19	0	1011 1100 0011 1000		45	0	0111 0001 0100 0010
4	1	1000 1000 0000 0000		20	0	0101 1110 0001 1100		36	0	0011 1000 1010 0001
5	0	0100 0100 0000 0000		21	0	0010 1111 0000 1110		37	0	1011 1100 0101 0001
6	0	0010 0010 0000 0000		22	0	0001 0111 1000 0111		38	0	1111 1110 0010 1001
7	1	1001 0001 0000 0000		23	0	1010 1011 1100 0010		39	0	1101 1111 0001 0101
8	1	1100 1000 1000 0000		24	1	1101 0101 1110 0001		40	0	1100 1111 1000 1011
9	1	1110 0100 0100 0000		25	0	1100 1010 1111 0001		41	0	1100 0111 1100 0100
10	0	0111 0010 0010 0000		26	1	0100 0101 0111 1001		42	0	0110 0011 1110 0010
11	0	0011 1001 0001 0000		27	0	1000 0010 1011 1101		43	0	0011 0001 1111 0001
12	0	0001 1100 1000 1000		28	0	1110 0001 0101 1111		44	0	1011 1000 1111 1001
13	0	0000 1110 0100 0100		29	0	1101 0000 1010 1110		45	0	1111 1100 0111 1101
14	0	0000 0111 0010 0010		30	0	0110 1000 0101 0111		46	0	1101 1110 0011 1111
15	0	0000 0011 1001 0001		31	0	1001 0100 0010 1010		47	0	1100 1111 0001 1110

The computed CRC value is '1100_1111_0001_1110'. The 16-bit CRC consists of two bytes, which are produced by this algorithm in reverse order. The correct ordering of these two bytes in the command frame is MSB first, LSB last (that is, '0001_1110' followed by '1100_1111' or in hex, 1E, CF). These two bytes are intended to be transmitted serially starting with the least-significant bit of each.

Great care must be taken when implementing the CRC algorithm to ensure that the bit ordering convention is consistent in the entire frame including the CRC. The terminology can be confusing and the fact that the algorithm has been optimized in order to eliminate the need for bit-reversal operations can contribute to the possibility of introducing an error. The implementer should check several examples from this document against the data generated by the algorithm to be used to ensure that the implementation is correct. The final command frame as it would be passed to a UART is:

	COMMAND FRAME BYTES
Command Frame Init	91
Device Address	03
Register Address	07
Data	05
CRC (MSB)	1E
CRC (LSB)	CF

The algorithm for checking a frame is similar. As an example, to check this frame, one possible implementation would be to simply CRC the first four bytes (excluding the CRC) and compare it with the received CRC value. Another option would be to take advantage of the cyclic nature of the CRC algorithm, passing all six bytes through, and then verifying that the result is 0. In this case, the initial zero padding of DIN with sixteen zeroes will not be needed. The resulting calculation would progress as follows, resulting in a final CRC value of 0, indicating a successful check:

n	DINn	CRC15:0		n	DINn	CRC15:0		n	DINn	CRC15:0
0	1	1000_0000_0000_0000		16	1	0010_0001_1100_1001		32	0	0100_1010_0001_0101
1	0	0100_0000_0000_0000		17	1	0011_0000_1110_0101		33	1	0000_0101_0000_1011
2	0	0010_0000_0000_0000		18	1	0011_1000_0111_0011		34	1	0010_0010_1000_0100
3	0	0001_0000_0000_0000		19	0	1011_1100_0011_1000		45	1	1001_0001_0100_0010
4	1	1000_1000_0000_0000		20	0	0101_1110_0001_1100		36	1	1100_1000_1010_0001
5	0	0100_0100_0000_0000		21	0	0010_1111_0000_1110		37	0	1100_0100_0101_0001
6	0	0010_0010_0000_0000		22	0	0001_0111_1000_0111		38	0	1100_0010_0010_1001
7	1	1001_0001_0000_0000		23	0	1010_1011_1100_0010		39	0	1100_0001_0001_0101
8	1	1100_1000_1000_0000		24	1	1101_0101_1110_0001		40	1	0100_0000_1000_1011
9	1	1110_0100_0100_0000		25	0	1100_1010_1111_0001		41	1	0000_0000_0100_0100
10	0	0111_0010_0010_0000		26	1	0100_0101_0111_1001		42	1	1000_0000_0010_0010
11	0	0011_1001_0001_0000		27	0	1000_0010_1011_1101		43	1	1100_0000_0001_0001
12	0	0001_1100_1000_1000		28	0	1110_0001_0101_1111		44	0	1100_0000_0000_1001
13	0	0000_1110_0100_0100		29	0	1101_0000_1010_1110		45	0	1100_0000_0000_0101
14	0	0000_0111_0010_0010		30	0	0110_1000_0101_0111		46	1	0100_0000_0000_0011
15	0	0000_0011_1001_0001		31	0	1001_0100_0010_1010		47	1	0000_0000_0000_0000

There are many good sources for algorithms and efficient techniques for generating and checking CRCs available on the Internet. The following byte-oriented C language routine has been developed and verified as a reference. The only complication that needs to be taken into account using this function is that the low byte of the CRC value returned is the CRC (MSB) and the high byte is the CRC (LSB).

```
Uint16 crc_16_ibm(uint8 *buf, uint16 len) {
            uint16 crc = 0;
            uint16 j;

            while (len--) {
            crc ^= *buf++;

            for (j = 0; j < 8 8; j++)
                  crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
            }
            return crc;
      }
```

7.5.3 Transaction Frame Examples

To illustrate the various Command and Response formats, examples of representative transaction-frame types are presented below. All numeric values are in hexadecimal unless otherwise noted. The CRC values in the examples are correct and can be utilized by the implementer to verify the CRC algorithm. Unless specifically noted otherwise, all examples use 8-bit register addressing.

Additional communication examples with matched command and response frames may be found in the *bq76PL455 Communication Examples* (SLVA617) application note.

Command Frames fall into two general categories:

1. Command frames which generate one or more response frames
2. Command frames which do not generate response frames

The REQ_TYPE field in the Frame Initialization byte determines the category to which a command frame belongs. Category 1 contains the Single Device Write with Response, Group Write with Response, and Broadcast Write with Response request types. Category 2 contains the Single Device Write without Response, Group Write without Response, and Broadcast Write without Response request types.

Command frames, which generate response frames, may generate more than one response frame. This depends on the specific command frame and the number of devices addressed by the command frame. In the case where more than one response frame is received in response to a single command frame, each response frame will be a complete frame containing the Frame Initialization, Data, and CRC bytes. A single device will not respond with more than a single-response frame in response to any single-command frame.

Special care should be taken when addressing the Command Register (address 2). When sending command frames, which generate response frames to this register, the length of a response frame is dependent on the content of the Command Channel Select Register (address 3–6). When addressing multiple devices, the response from each device may vary in length depending on the configuration of the addressed device. Additionally, there may be a delay in the expected response(s) depending on the configuration information stored in the Voltage and Internal Temperature Sampling Period Register (address 62) and other registers, which affect the channel sampling periods.

7.5.3.1 Single Device Write with Response Command Frame

Interpretation of the Data field in a Single Device Write with Response frame depends on the target register of the command.

If the target register is the Command Register (address 2), then the data bytes may contain the Command, new content for the Command Channel Select Register and new content for the Averaging Register. If the data for the Command Channel Register and Averaging Register are omitted from the Single Device Write with Response Command Frame, then the previously configured values in those registers will be used. If the data are included in the command frame, then these values will be written into the respective registers and used for the requested sampling.

If the target register is not the Command Register, then the data bytes will be interpreted as the number of bytes minus one being requested from the bq76PL455-Q1, starting at the register address provided in the Register Address byte of the command frame.

The DATA_SIZE field in the Frame Initialization byte should be written with the number of data bytes in the command frame.

7.5.3.1.1 Single Device Write with Response to Command Register (Address 2)

The value of the DATA_SIZE field in the Frame Initialization byte for this case is typically 001 (1 byte), 101 (5 bytes) or 110 (six bytes). These variations correspond to commands which:

1. Send only the sample command request and expect the bq76PL455-Q1 to use the preprogrammed sampling values in the registers that control sampling.
2. Send the sample command request and the value for the Channel Select Register (address 3–6), but expect the bq76PL455-Q1 to use the preprogrammed value in the Averaging Register (address 7). The Channel Select Register will be overwritten with the data bytes from the command frame.
3. Send the sample command request and the values for the Channel Select Register (address 3–6) and Averaging Register (address 7). Both the Channel Select Register and the Averaging Register will be overwritten with the respective data bytes from the command frame.

The size of the response frame in response to a command frame of this type is directly related to the number of channels selected by either the preprogrammed data in the Channel Select Register (address 3–6) or the data passed to the bq76PL455-Q1 in the command frame.

Three examples follow. All three examples target the device at Device Address 00, which is typically the address of a single device or the address of the lowest device in a stack of devices.

7.5.3.1.1.1 Data Contains Command Only

For the purpose of this example, assume the following start conditions:

1. Content of Channel Select Register before command: 0FFF5500
2. Content of Averaging Register before command: 00

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	001 (binary)		
Device Address	00							
Register Address	02							
Data (Command)	00							
CRC (MSB)	29							
CRC (LSB)	5C							

Notice the DATA_SIZE field in the Frame Initialization byte is 001. This means this Command Frame contains one data byte. This one data byte contains the Command for the Command Register (in this case 00). For more details regarding the Command Register, refer to the Command Register in *Register Details*.

The expected response frame to this example command frame would contain 35 bytes: one Frame Initialization byte, 32 data bytes (two bytes for each of the sixteen-selected channels), and two CRC bytes.

The content of the CHANNEL register and of the OVERSMPL register will remain unchanged.

7.5.3.1.1.2 Data Contains Command and Channel Selection

For the purpose of this example, assume the following start conditions:

1. Content of Channel Select Register before command: 0FFF5500
2. Content of Averaging Register before command: 00

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	005 (binary)		
Device Address	00							
Register Address	02							
Data (Command)	00							
Data (Channel Select MSB)	FF							
Data (Channel Select)	FF							
Data (Channel Select)	01							
Data (Channel Select LSB)	00							
CRC (MSB)	C8							
CRC (LSB)	09							

Notice the DATA_SIZE field in the Frame Initialization byte is 005. This means this Command Frame contains five data bytes. The first data byte contains the Command for the Command Register (in this case 00). The second through fifth data bytes contain the channel selection data, which will be written to the Channel Select Register as part of this command. For more details on register usage, refer to *Register Details* for details.

The expected response frame to this example command frame would contain 37 bytes: one Frame Initialization byte, 34 data bytes (two bytes for each of the seventeen-selected channels), and two CRC bytes.

The content of the Channel Select Register and the Averaging Register will change. Resulting register content will be as follows:

1. Content of Channel Select Register after command: FFFF0100
2. Content of Averaging Register after command: 00

7.5.3.1.1.3 Data Contains Command, Channel Selection, and Averaging Selection

For the purpose of this example, assume the following start conditions:

1. Content of Channel Select Register before command: 0FFF5500
2. Content of Averaging Register before command: 00

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	006 (binary)		
Device Address	00							
Register Address	02							
Data (Command)	00							
Data (Channel Select MSB)	FF							
Data (Channel Select)	FF							
Data (Channel Select)	0F							
Data (Channel Select LSB)	00							
Data (Averaging Select)	7B							
CRC (MSB)	3D							
CRC (LSB)	86							

Notice the DATA_SIZE field in the Frame Initialization byte is 006. This means this Command Frame contains six data bytes. The first data byte contains the Command for the Command Register (in this case 00). The second through fifth data bytes contain the channel selection data, which will be written to the Channel Select Register as part of this command. The sixth data byte contains the averaging configuration data, which will be written to the Averaging Register as part of this command. For more details on register usage, refer to *Register Details* for details.

The expected response frame to this example command frame would contain 43 bytes: one Frame Initialization byte, 40 data bytes (two bytes for each of the twenty selected channels), and two CRC bytes.

The content of the Channel Select Register and the Averaging Register will change. Resulting register content will be as follows:

1. Content of Channel Select Register after command: FFFF0F00
2. Content of Averaging Register after command: 7B

7.5.3.1.2 Single Device Write with Response to Register(s) Other than Command Register

The value of the DATA_SIZE field in the Framing Initialization byte for this case is typically 001 (1 byte). This value will be interpreted as the number of expected data bytes in the response frame minus one. For instance, if the expectation were to read the four bytes contained in the Channel Select Register, the data byte would contain 03 (four minus one).

Two examples follow. All examples in this section target the device at Device Address 00, which is typically the address of a single device or the address of the lowest device in a stack of devices.

7.5.3.1.2.1 Requesting Four Bytes of Data from a Single Register

This command example requests four bytes of data, all from a single register. In the case of this example, the four bytes will come from the Channel Select Register at address 3–6. The most-significant byte of the four-byte register will be the first data byte in the response frame.

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	001 (binary)		
Device Address	00							
Register Address	03							
Data (Desired Number of Bytes – 1)	03							
CRC (MSB)	68							
CRC (LSB)	CD							

Notice the DATA_SIZE field in the Frame Initialization byte is 001. This means this Command Frame contains one data byte. This data byte contains the desired number of response bytes minus one.

The response frame will contain seven bytes: one Frame Initialization byte, four data bytes, and two CRC bytes.

7.5.3.1.2.2 Requesting Multiple Bytes across Register Boundaries

It is possible to request data from multiple registers across register boundaries. When this type of read is performed, Reserved Register Addresses can also be included in the block of registers being read. Reads of Reserved Register Addresses will always return zero and these bytes must be counted in the requested number of data bytes. In this example, the data from three registers [the Channel Select Register (address 3–6), the Averaging Register (address 7) and the Device Address Register (address 10)] are requested. These registers contain six bytes of data; however, two Reserved Register Addresses (addresses 8 and 9) lie between the Averaging Register (address 7) and the Device Address Register (address 10), so eight bytes of data must be requested.

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	001 (binary)		
Device Address	01							
Register Address	03							
Data (Desired Number of Bytes - 1)	07							
CRC (MSB)	38							
CRC (LSB)	CE							

NOTE

The DATA_SIZE field in the Frame Initialization byte is 1, indicating that this command frame contains a single data byte. This data byte indicates the number of desired bytes in the response (minus one).

The response frame will contain eleven bytes: one Frame Initialization byte, eight data bytes, and two CRC bytes.

7.5.3.2 Single Device Write without Response Command Frame

A Single Device Write without Response command is indicated when FRM_TYPE = 1 and REQ_TYPE = 1. In this example, the register address size is 8-bits (ADDR_SIZE = 0) and the data length written is 1 byte (DATA_SIZE). No Response Frame is expected to be returned.

The command in the example writes a single byte value to the Averaging Register (address 7).

For the purpose of this example, assume the following start conditions:

1. Content of Averaging Register before command: 00

	7	6	5	4	3	2	1	0
Command Frame Init	1	000 (binary)			0	001 (binary)		
Device Address	03							
Register Address	07							
Data (New Data for Target Register)	05							
CRC (MSB)	1E							
CRC (LSB)	CF							

The content of the Averaging Register will change. Resulting Averaging Register content will be: 05.

To write more than one byte to the bq76PL455-Q1, the DATA_SIZE field in the Frame Initialization byte should be updated and additional data bytes added to the command frame. Up to eight, data bytes can be written with a single command frame of this type.

7.5.3.3 Group_Write_With_Response Command Frame

There are several different ways to format the Group Write with Response command frame, and the data bytes will be interpreted differently depending on the command frame configuration.

The Group Write with Response, which targets the Command register (address 2), has several different configurations. These configurations also differ from the two configurations of the Group Write with Response when it is targeted to a register other than the Command register. Primary examples of these different configurations are provided below.

It is important to note that devices in defined Groups **must** consist of devices with consecutive addresses. It is not recommended to have a group in which any devices have non-contiguous addresses. Group IDs are established by programming the Group ID Register (address 11) of all devices in a specific group to the same value.

NOTE

For the configuration examples below, assume a daisy chain of four devices with addresses 00–03 in which devices at address 01 and address 02 belong to Group ID 01, and the devices at address 00 and address 03 belong to Group ID 00.

7.5.3.3.1 Configuration 1: Group Write with Response to Command Register with Sampling Parameters Included in Command Frame

In response to the command frame in this example, each bq76PL455-Q1 in the specified group will sample the channels identified in the data parameters, store the results, write the new sample parameters into the CHANNEL and OVERSMPL registers, and send a response frame containing the sample data.

	7	6	5	4	3	2	1	0
Command Frame Init	1	010 (binary)			0	110 (binary)		
Group ID	01							
Register Address	02							
Data (Command)	02							
Data (Channel Select MSB)	FF							
Data (Channel Select)	FF							
Data (Channel Select)	55							
Data (Channel Select LSB)	00							
Data (Averaging Setting)	00							
CRC (MSB)	04							
CRC (LSB)	59							

For details on how to interpret the data, refer to *Register Details*. A simplified overview of the meaning of the data bytes in this example is provided in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
A6	1 010 0 110	Command frame, Group Write with Response = REQ_TYPE, 8-bit Register Addressing, 6 data bytes = DATA_SIZE
01	00000001	Target is Group ID = 01
02	00000010	Target Register = 02 (Command Register)
02	000 00010	Upper three bits define Command sent to Command register, lower 5 bits is address of highest device in group to respond
FF	11111111	Select Channels 16 to 9
FF	11111111	Select Channels 8 to 1
55	01010101	Select AUX6, AUX4, AUX2 and AUX0
00	00000000	Do not select temperature or additional channels
00	00000000	No averaging
04	00000100	CRC
59	01011001	CRC

7.5.3.3.2 Configuration 2: Group Write with Response to Command Register without Sampling Parameters Included in Command Frame

NOTE

Sampling parameters are taken from values already stored in the CHANNEL and OVERSMPL registers.

In response to the sample command frame in this example, each bq76PL455-Q1 in the specified group will sample the channels identified by the values currently stored in the Command Channel Select register (address 3–6) and sample them using the averaging setting currently set in the Averaging register (address 7).

	7	6	5	4	3	2	1	0
Command Frame Init	1	010 (binary)			0	001 (binary)		
Group ID	01							
Register Address	02							
Data (Command)	02							
CRC (MSB)	F2							
CRC (LSB)	9D							

For detail on how to interpret the data, refer to *Register Details* for details. A simplified overview of the meaning of the data bytes in this example is provided in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
A1	1 010 0 001	Command frame, Group Write with Response = REQ_TYPE, 8-bit Register Addressing, 1 data byte = DATA_SIZE
01	00000001	Target is Group ID = 01
02	00000010	Target Register = 02 (Command Register)
02	000 00010	Upper three bits define Command sent to Command register, lower 5 bits is address of highest device in group to respond
F2	11110010	CRC
9D	10011101	CRC

7.5.3.3.3 Configuration 3: Group Write with Response to non-Command Register

NOTE

This configuration is using two bytes for addressing and response size.

The sample command frame in this example will read the data currently stored in the Command Channel Select (address 3–6) register. Interpretation of the data bytes is shown in the left hand column of the following table. The DATA_SIZE field in the Frame Initialization byte indicates the number of data bytes in the command frame.

	7	6	5	4	3	2	1	0
Command Frame Init	1	010 (binary)			0	010 (binary)		
Group ID	01							
Register Address	03							
Data (Address of Highest Device in Group to Respond)	02							
Data (Expected Number of Response Data Bytes – 1)	03							
CRC (MSB)	49							
CRC (LSB)	44							

For detail on how to interpret the data, refer to *Register Details* for details. A simplified overview of the meaning of the data bytes in this example is provided in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
A2	1 010 0 001	Command frame, Group Write with Response = REQ_TYPE, 8-bit Register Addressing, 2 data bytes = DATA_SIZE
01	00000001	Target is Group ID = 01
03	00000011	Target Register = 03 (Command Channel Select Register)
02	00000010	Address of highest device in target group
03	00000011	Number of Data Bytes – 1 expected in response (4 bytes in this example)
49	01001001	CRC
44	01000100	CRC

The command frame in this example will generate a response frame from each of the two devices targeted by the command frame. Each response frame will contain data stored in the Command Channel Select register of the responding bq76PL455-Q1. The response frame from the bq76PL455-Q1 at the highest address in the addressed group will arrive first. If the stored data were FFFF8000 (hex) for the device at Device Address 02 in Group 01, and the data were FFFF0100 (hex) for the device at Device Address 01 in Group ID 01, then the response frames would be as shown in the following table.

	7	6	5	4	3	2	1	0
Response Frame Init	0	0000011 (binary)						
Data	FF							
Data	FF							
Data	80							
Data	00							
CRC (MSB)	25							
CRC (LSB)	E4							

	7	6	5	4	3	2	1	0
Response Frame Init	0	0000011 (binary)						
Data	FF							
Data	FF							
Data	01							
Data	00							
CRC (MSB)	45							
CRC (LSB)	B4							

The second of the two response frames will arrive immediately after the first of the response frames, so the response will typically appear to be one continuous response. It is therefore important to remember that each responding device will respond with a complete response frame with its own Frame Initialization byte, data bytes, and CRC bytes.

7.5.3.3.4 Configuration 4: Group Write with Response to Non-Command Register

NOTE

This configuration is using one byte for addressing and response size.

As in the example for Configuration 3, the sample command frame in this example will read the value currently stored in the Command Channel Select (address 3–6) register, but the message to do so is one byte shorter. The expected response frames would be the same as in the example for Configuration 3.

	7	6	5	4	3	2	1	0
Command Frame Init	1	010 (binary)			0	001 (binary)		
Group ID	01							
Register Address	03							
Data (Address of Highest Device in Group to Respond)	62							
CRC (MSB)	F3							
CRC (LSB)	25							

For detail on how to interpret the data, refer to *Register Details* for details. A simplified overview of the meaning of the data bytes in this example is provided in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
A1	1 010 0 001	Command frame, Group Write with Response = REQ_TYPE, 8-bit Register Addressing, 1 data byte = DATA_SIZE
01	00000001	Target is Group ID = 01
03	00000011	Target Register = 03 (Command Channel Select Register)
62	011 00010	Upper three bits are Number of Data Bytes – 1 expected in response, lower 5 bits is address of highest device in group to respond
F3	11110011	CRC
25	00100101	CRC

NOTE

Although not recommended, each of the configurations above can also be configured to use 16-bit register addressing, which would add another byte for the MSB of the register address to the command frame.

7.5.3.4 Group Write without Response Command Frame

A Group Write without Response command is indicated when FRM_TYPE = 1 and REQ_TYPE = 3 (011 binary). In this example, the register address size is 8-bits (ADDR_SIZE = 0) and the data length written is 1 byte (DATA_SIZE). No Response Frame is expected to be returned.

In response to this example command frame, each bq76PL455-Q1 in the target group will write the value in the data byte to the target register (the Averaging Register in this example). For more information on the effect of this example command frame, see *Register Details* for details.

	7	6	5	4	3	2	1	0
Command Frame Init	1	011 (binary)			0	001 (binary)		
Group ID	01							
Register Address	07							
Data	7B							
CRC (MSB)	34							
CRC (LSB)	EF							

7.5.3.5 Broadcast Write with Response Command Frame

As with the Single- and Group Write with Response command frames, the Broadcast Write with Response command frame bytes will be interpreted differently when the target register is the Command Register (address 2) compared to when the target is another register. Response frame lengths when the command frame targeted the Command Register will be determined by the content of the Channel Select Register of each targeted bq76PL455.

Broadcast Write command frames do not contain a Device Address/Group ID byte. This is the primary deviation from the examples already provided in the Group Write with Response section.

With the above exception, Broadcast Write with Response command frames can be formed in a similar fashion to the various configuration examples in the Group Write with Response section.

As with the Group Write with Response commands frames, Broadcast Write with Response command frames can utilize one of two formats to indicate the address of the highest device to respond and the number of bytes expected in response from each targeted device. One of the formats uses one byte to specify both the address of the highest board in the response chain and the number of desired response bytes. The other method uses two bytes to specify the address of the highest responding device and the desired number of response bytes separately (first the address, then the number of bytes-1).

The two command frames that follow provide an example of each format.

An example of the two-byte method (to read the Communication Configuration register):

	7	6	5	4	3	2	1	0
Command Frame Init	1	110 (binary)			0	002 (binary)		
Register Address	10							
Data (Address of highest responder)	03							
Data (Number of response data bytes – 1)	01							
CRC (MSB)	F6							
CRC (LSB)	8D							

For further details on how to interpret the data, refer to *Register Details* for details. A simplified overview of the meaning of the data bytes in this example is provided in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
E2	11100010	Command frame, Broadcast Write with Response = REQ_TYPE, 8-bit Register Addressing, 2 data bytes = DATA_SIZE
10	00010000	Target Register Address (Communication Configuration Register)
03	00000011	Address of highest (first) device to respond
01	00000001	Number of data bytes –1 expected in response (that is, 2 bytes)
F6	11110110	CRC
8D	10001101	CRC

An example of the one-byte method (to read the Communication Configuration register):

	7	6	5	4	3	2	1	0
Command Frame Init	1	110 (binary)			0	001 (binary)		
Register Address	10							
Data (Data Size and Address of highest responder)	22							
CRC (MSB)	DC							
CRC (LSB)	1F							

For further details on how to interpret the data, refer to *Register Details* for details. A simplified overview of the meaning of the data bytes in this example is provided in the following table.

BYTE (HEX)	BYTE (BINARY)	DESCRIPTION
E1	11100001	Command frame, Broadcast Write with Response = REQ_TYPE, 8-bit Register Addressing, 1 data byte = DATA_SIZE
10	00010000	Target Register Address (Communication Configuration Register)
22	001 00010	Upper three bits are Number of Data Bytes – 1 expected in response, lower 5 bits is address of highest device to respond
DD	11011101	CRC
EF	11101111	CRC

7.5.3.6 Broadcast Write without Response Command Frame

A Broadcast Write without Response command is indicated when FRM_TYPE = 1 and REQ_TYPE = 7 (111 binary).

In this example, the register address size is 8-bits (ADDR_SIZE = 0) and the data length written is 1 byte (DATA_SIZE). Note that since this command is for all devices, there is no Device Address/Group ID byte in the command frame.

No Response Frame is expected to be returned.

	7	6	5	4	3	2	1	0
Command Frame Init	1	111 (binary)			0	001 (binary)		
Register Address	C8							
Data	12							
CRC (MSB)	86							
CRC (LSB)	3E							

This example writes 12 (hex) into one of the Scratchpad Register bytes at address 200 (C8 hex) on all targeted devices. See *Register Details* for further information on the effects of changing register values.

7.5.4 Response Frame

A Response Frame is indicated when FRM_TYPE = 0. Note that bits 6 through 0 in the Frame Initialization byte are a different format from the Command Frame format, as described above in *Frame Initialization Byte*.

In this example, the response data length is 3 bytes (RESP_BYTES – 1 = 2). Data lengths from 1 through 128 bytes are supported. Since the protocol described here is for a single initiator (microcontroller) system, the initiator is always the intended target of a Response Frame.

If a command frame targets more than one device, responses will be sent back to the initiator first from the device at the highest address in the targeted group, then the next highest address, and so forth until all devices in the targeted group have responded. Each device will respond with a complete response frame, which includes a Frame Initialization byte, one or more data bytes, and two CRC bytes.

If the command frame targets more than one device and the target register of that command frame is the Command Register, then there may be a delay in the responses. This delay is due to the time required for the targeted bq76PL455-Q1 devices to sample, store, and respond with their newly sampled data. The delay in the responses will be dependent on the sampling period and channel selection configuration of each targeted device.

	7	6	5	4	3	2	1	0
Response Frame Init	0 (binary)					0000010 (binary)		
Data	9B							
Data	8C							
Data	7D							
CRC (MSB)	D4							
CRC (LSB)	B6							

7.6 Register Maps

7.6.1 Conventions and Notations

The conventions discussed here are also used throughout the document.

- Keywords that refer to specific software registers are in ALL CAPITALS.
- Each byte in a multi-byte register can be addressed individually. The format is big endian with the most-significant byte stored in the lowest physical address. Data are returned in lowest-to-highest address order.
- Locations marked "RESERVED" should not be written to, and always return 0.
- Bits marked "RESERVED" or "reserved" should be written as 0, unless otherwise specified.

NOTE

FAILURE TO COMPLY WITH THE PRECEDING TWO STATEMENTS MAY RESULT IN UNEXPECTED DEVICE BEHAVIOR.

- The bq76PL455-Q1 contains two sets of registers. One set, simply referred to as "registers" or "User space" in this data manual, is intended for normal R/W operations by users. Another set, referred to as "factory registers" or "TI space", contains factory test and trim parameters and is not used during normal operations, with the exception that certain test operations may be performed as a part of self-testing, for example, checksum calculations.

7.6.1.1 Register Usage

All registers, except the Command Register (CMD), operate in the same manner. For all registers except CMD, reading will return the value stored in the addressed register, and writing will store a new value into the addressed register.

The Command Register (CMD) is a special register that accepts commands. A value written to CMD causes a specific action to be carried out by the bq76PL455-Q1, and this may include the generation of a response from the bq76PL455-Q1. For example, a Synchronous Sample command written to CMD causes a response that contains the conversion values for any selected channels.

NOTE

New commands should not be written until the current command is complete and any requested response has been received in its entirety, or a timeout has occurred.

All unused bits in the registers should always be written as 0, unless otherwise noted.

The register space is byte addressable. Reads or writes can cover any number of bytes. Multi-byte registers (16-bit or 32-bit, and so forth) can be read as individual bytes, one at a time, or read as a single register. The most-significant byte of multi-byte registers is stored in the lower address.

Register addresses shown as "RESERVED" and addresses not shown in *Register Summary* should not be written to by user firmware. Reserved Register Addresses will return zero if read, unless otherwise noted.

Register Maps (continued)

7.6.2 Register Summary

KEY: ADDR = Address; **R** = Read; **W** = Write; **EE** = EEPROM: **Y** = (Yes) value stored in non-volatile EEPROM after written by user; **N** = value is volatile storage only; **CSUM** = Checksum: **Y** = value included in checksum calculation; **N** = value not included in calculation; **N/A** = not applicable; **"—"** indicates that the location reserved for future TI use.

Table 5. Register Summary

ADDR HEX	ADDR DECIMAL	BITS	NAME	DESCRIPTION	DEFAULT 0x		R/W	CS[3]
					RAM[1]	EE[2]		
00–01	0–1	16	SREV	Silicon Revision	0705(7)	N/A	R	N
02	2	8	CMD	Command	00	N/A	W	N
03–06	3–6	32	CHANNEL	Command channel select	0000 0000	FFFF 0000	R/W	Y
07	7	8	OVERSMPL	Command averaging (oversampling)	00	7B	R/W	Y
08–09	8–9	16	RESERVED	*Reserved for future use*	00	—	R/W	N
0A	10	8	ADDR	Device address	00	00	R/W	Y
0B	11	8	GROUP_ID	(Device) Group Identifier	00	00	R/W	Y
0C	12	8	DEV_CTRL	Device control	20	N/A	R/W	N
0D	13	8	NCHAN	Number of channels enabled for conversion	00	10	R/W	Y
0E	14	8	DEVCONFIG	Device configuration	00	10	R/W	Y
0F	15	8	PWRCONFIG	Power configuration	00	80	R/W	Y
10–11	16–17	16	COMCONFIG	Communications configuration	1000	1080	R/W	Y
12	18	8	TXHOLDOFF	UART Transmitter holdoff	00	00	R/W	Y
13	19	8	CBCONFIG	Cell balancing (equalization) configuration	00	00	R/W	Y
14–15	20–21	16	CBENBL	Cell balancing enables	0000	N/A	R/W	Y
16–1D	22–29	64	RESERVED	*Reserved for future use*	00	—	R/W	N
1E–1F	30–31	16	TSTCONFIG	Built-In Self-Test (BIST) configuration	0000	N/A	R/W	Y
20–21	32–33	16	TESTCTRL	BIST control	0000	N/A	R/W	N
22–24	34–36	24	TEST_ADC	ADC BIST control	0000	N/A	R/W	Y
25	37	8	TESTAUXPU	Test control—AUX pull-up resistors	00	N/A	R/W	Y
26–27	38–39	16	RESERVED	*Reserved for future use*	00	—	R/W	N
28	40	8	CTO	Communications time-out	00	DC	R/W	Y
29–2B	41–43	24	CTO_CNT	Communications time-out counter	0000	N/A	R/W	N
2C–31	44–49	40	RESERVED	Reserved for future use	0000	—	R/W	N
32	50	8	RESERVED	Reserved for future use	00	0	R/W	Y
33–36	51–54	32	RESERVED	Reserved for future use	0000	0000	R/W	Y
37	55	8	RESERVED	Reserved for future use	00	00	R/W	Y
38–3C	56–60	40	RESERVED	*Reserved for future use*	0000	—	R/W	N
3D	61	8	SMPL_DLY1	Initial sampling delay	00	0	R/W	Y
3E	62	8	CELL_SPER	Cell and die temperature measurement period	00	BC	R/W	Y
3F–42	63–66	32	AUX_SPER	AUX channels sampling period	0000 0000	4444 4444	R/W	Y
43–44	67–68	16	TEST_SPER	ADC test sampling period	0000	F999	R/W	Y
45–4F	69–79	88	RESERVED	*Reserved for future use*	00	—	R/W	N
50	80	8	SHDN_STS	Shutdown recovery status	00	N/A	R	N
51	81	8	STATUS	Device status	81[4]	N/A	R/W	N
52–53	82–83	16	FAULT_SUM	Fault summary	0100[4]	N/A	R/W	N
54–55	84–85	16	FAULT_UV	Undervoltage faults	0000[4]	N/A	R/W	N
56–57	86–87	16	FAULT_OV	Overvoltage faults	0000[4]	N/A	R/W	N
58–59	88–89	16	FAULT_AUX	AUX threshold exceeded faults	0000[4]	N/A	R/W	N
5A–5B	90–91	16	FAULT_2UV	Comparator UV faults	0000[4]	N/A	R/W	N
5C–5D	92–93	16	FAULT_2OV	Comparator OV faults	0000[4]	N/A	R/W	N

Register Maps (continued)

Table 5. Register Summary (continued)

ADDR HEX	ADDR DECIMAL	BITS	NAME	DESCRIPTION	DEFAULT 0x		R/W	CS[3]
					RAM[1]	EE[2]		
5E–5F	94–95	16	FAULT_COM	Communication faults	0000[4]	N/A	R/W	N
60	96	8	FAULT_SYS	System fault	80[4]	N/A	R/W	N
61–62	97–98	16	FAULT_DEV	Device fault	0000[4]	N/A	R/W	N
63	99	8	FAULT_GPI	General purpose input (GPIO) fault	00[4]	N/A	R/W	N
64–67	100–103	32	RESERVED	*Reserved for future use*	00	—	R/W	N
68–69	104–105	16	MASK_COMM	Communications FAULT mask register	0000	0000	R/W	Y
6A	106	8	MASK_SYS	System FAULT mask register	0	00	R/W	Y
6B–6C	107–108	16	MASK_DEV	Chip FAULT mask register	0000	0000	R/W	Y
6D	109	8	RESERVED	*Reserved for future use*	0	—	R/W	N
6E–6F	110–111	16	FO_CTRL	FAULT output control	0000	FFC0	R/W	Y
70–77	112–119	64	RESERVED	*Reserved for future use*	0	—	R/W	N
78	120	8	GPIO_DIR	GPIO direction control	00	00	R/W	Y
79	121	8	GPIO_OUT	GPIO output control	00	00	R/W	Y
7A	122	8	GPIO_PU	GPIO pull-up resistor control	00	00	R/W	Y
7B	123	8	GPIO_PD	GPIO pull-down resistor control	00	00	R/W	Y
7C	124	8	GPIO_IN	GPIO input value	00	N/A	R	N
7D	125	8	GP_FLT_IN	GPIO input 0/1 FAULT assertion state	00	00	R/W	Y
7.00E–81	126–129	32	RESERVED	*Reserved for future use*	00	—	R/W	N
82–85	130–133	32	MAGIC1	"Magic" value enables EEPROM write	0000 0000	N/A	W	N
86–8B	134–139	48	RESERVED	*Reserved for future use*	00	—	R/W	N
8C	140	8	COMP_UV	Comparator undervoltage threshold	00	00	R/W	Y
8D	141	8	COMP_OV	Comparator overvoltage threshold	00	FE	R/W	Y
8E–8F	142–143	16	CELL_UV	Cell undervoltage threshold	0000	0000	R/W	Y
90–91	144–145	16	CELL_OV	Cell overvoltage threshold	0000	FFFC	R/W	Y
92–93	146–147	16	AUX0_UV	AUX0 undervoltage threshold	0000	0000	R/W	Y
94–95	148–149	16	AUX0_OV	AUX0 overvoltage threshold	0000	FFFC	R/W	Y
96–97	150–151	16	AUX1_UV	AUX1 undervoltage threshold	0000	0000	R/W	Y
98–99	152–153	16	AUX1_OV	AUX1 overvoltage threshold	0000	FFFC	R/W	Y
9A–9B	154–155	16	AUX2_UV	AUX2 undervoltage threshold	0000	0000	R/W	Y
9C–9D	156–157	16	AUX2_OV	AUX2 overvoltage threshold	0000	FFFC	R/W	Y
9E–9F	158–159	16	AUX3_UV	AUX3 undervoltage threshold	0000	0000	R/W	Y
A0–A1	160–161	16	AUX3_OV	AUX3 overvoltage threshold	0000	FFFC	R/W	Y
A2–A3	162–163	16	AUX4_UV	AUX4 undervoltage threshold	0000	0000	R/W	Y
A4–A5	164–165	16	AUX4_OV	AUX4 overvoltage threshold	0000	FFFC	R/W	Y
A6–A7	166–167	16	AUX5_UV	AUX5 undervoltage threshold	0000	0000	R/W	Y
A8–A9	168–169	16	AUX5_OV	AUX5 overvoltage threshold	0000	FFFC	R/W	Y
AA–AB	170–171	16	AUX6_UV	AUX6 undervoltage threshold	0000	00000	R/W	Y
AC–AD	172–173	16	AUX6_OV	AUX6 overvoltage threshold	0000	FFFC	R/W	Y
AE–AF	174–175	16	AUX7_UV	AUX7 undervoltage threshold	0000	00000	R/W	Y
B0–B1	176–177	16	AUX7_OV	AUX7 overvoltage threshold	0000	FFFC	R/W	Y
B2–BD	178–189	96	RESERVED	*Reserved for future use*	0000	—	R/W	N
BE–C5	190–197	64	LOT_NUM	Device Lot Number	00…	Factory[5]	R	N
C6–C7	198–199	16	SER_NUM	Device Serial Number	00…	Factory[5]	R	N
C8–CF	200–207	64	SCRATCH	User-defined data	00…	00…	R/W	Y
D0-D1	208–209	16	RESERVED	*Reserved for future use*	00	—	R/W	N
D2	210	8	VSOFFSET	ADC voltage offset correction	00	00	R/W	Y
D3	211	8	VSGAIN	ADC voltage gain correction	00	00	R/W	Y

Register Maps (continued)

Table 5. Register Summary (continued)

ADDR HEX	ADDR DECIMAL	BITS	NAME	DESCRIPTION	DEFAULT 0x		R/W	CS[3]
					RAM[1]	EE[2]		
D4-D5	212–213	16	AX0OFFSET	AUX0 ADC offset correction	0000	0000	R/W	Y
D6-D7	214–215	16	AX1OFFSET	AUX1 ADC offset correction	0000	0000	R/W	Y
D8-D9	216–217	16	AX2OFFSET	AUX2 ADC offset correction	0000	0000	R/W	Y
DA-DB	218–219	16	AX3OFFSET	AUX3 ADC offset correction	0000	0000	R/W	Y
DC-DD	220–221	16	AX4OFFSET	AUX4 ADC offset correction	0000	0000	R/W	Y
DE-DF	222–223	16	AX5OFFSET	AUX5 ADC offset correction	0000	0000	R/W	Y
E0–E1	224–225	16	AX6OFFSET	AUX6 ADC offset correction	0000	0000	R/W	Y
E2–E3	226–227	16	AX7OFFSET	AUX7 ADC offset correction	0000	0000	R/W	Y
E4–E5	228–229	16	RESERVED	*Reserved for future use*	00	—	R/W	N
E6–ED	230–237	64	TSTR_ECC	ECC Test Results	00…	N/A	R	N
EE–EF	238–239	16	RESERVED	*Reserved for future use*	0	—	R/W	N
F0–F3	240–243	32	CSUM	Saved checksum value	1234 5678	C9B0 12F7	R/W	N
F4–F7	244–247	32	CSUM_RSLT[6]	Checksum Readout	C9B0 12F7	N/A	R/W	N
F8–F9	248–249	16	TEST_CSUM	Checksum Test Result	0000	N/A	R	N
FA	250	8	EE_BURN	EEPROM Burn Count; up-counter	FA	Y	R	N
FB	251	8	RESERVED	*Reserved for future use*	00	—	R/W	N
FC–FF	252–255	32	MAGIC2	"Magic" value enables EEPROM write	0000 0000	N/A	W	N

(1) Initial value loaded at device RESET or POR.

(2) Value stored in EEPROM from factory, which may be overwritten by the user. This value is loaded after initial RESET or POR value (see note (1)) only if the ECC is valid or correctable for the block. See text for details.

(3) *CS*: This register is included ('Y') or not included ('N") in the USER checksum calculation.

(4) Value shown after wakeup and only the FAULT_SYS[SYS_RESET] fault conditions exist.

(5) Factory programmed values will vary from IC to IC.

(6) This register value is set indirectly by the contents of all register values included in the checksum. The value updates after any register change for registers included in the checksum.

(7) Some early versions of the IC will contain the value 0605 (hexadecimal).

Table 6. Registers in Alphabetical Order

NAME	DESCRIPTION	ADDR HEX	ADDR DECIMAL
ADDR	Device address	0A	10
AUX_SPER	AUX channels sampling period	3F–42	63–66
AUX0_OV	AUX0 overvoltage threshold	94–95	148–149
AUX0_UV	AUX0 undervoltage threshold	92–93	146–147
AUX1_OV	AUX1 overvoltage threshold	98–99	152–153
AUX1_UV	AUX1 undervoltage threshold	96–97	150–151
AUX2_OV	AUX2 overvoltage threshold	9C–9D	156–157
AUX2_UV	AUX2 undervoltage threshold	9A–9B	154–155
AUX3_OV	AUX3 overvoltage threshold	A0–A1	160–161
AUX3_UV	AUX3 undervoltage threshold	9E–9F	158–159
AUX4_OV	AUX4 overvoltage threshold	A4–A5	164–165
AUX4_UV	AUX4 undervoltage threshold	A2–A3	162–163
AUX5_OV	AUX5 overvoltage threshold	A8–A9	168–169
AUX5_UV	AUX5 undervoltage threshold	A6–A7	166–167
AUX6_OV	AUX6 overvoltage threshold	AC–AD	172–173
AUX6_UV	AUX6 undervoltage threshold	AA–AB	170–171

Table 6. Registers in Alphabetical Order (continued)

NAME	DESCRIPTION	ADDR HEX	ADDR DECIMAL
AUX7_OV	AUX7 overvoltage threshold	B0–B1	176–177
AUX7_UV	AUX7 undervoltage threshold	AE–AF	174–175
AX0OFFSET	AUX0 ADC offset correction	D4–D5	212–213
AX1OFFSET	AUX1 ADC offset correction	D6–D7	214–215
AX2OFFSET	AUX2 ADC offset correction	D8–D9	216–217
AX3OFFSET	AUX3 ADC offset correction	DA–DB	218–219
AX4OFFSET	AUX4 ADC offset correction	DC–DD	220–221
AX5OFFSET	AUX5 ADC offset correction	DE–DF	222–223
AX6OFFSET	AUX6 ADC offset correction	E0-E1	224–225
AX7OFFSET	AUX7 ADC offset correction	E2-E3	226–227
CBCONFIG	Cell balancing (equalization) configuration	13	19
CBENBL	Cell balancing enables	14–15	20–21
CELL_OV	Cell overvoltage threshold	90–91	144–145
CELL_SPER	Cell and die temperature measurement period	3E	62
CELL_UV	Cell undervoltage threshold	8E–8F	142–143
CHANNEL	Command channel select	03–06	3-6
CMD	Command	02	2
COMCONFIG	Communications configuration	10–11	16–17
COMP_OV	Comparator overvoltage threshold	8D	141
COMP_UV	Comparator undervoltage threshold	8C	140
CSUM	Saved checksum value	F0–F3	240–243
CSUM_RSLT	Checksum Readout	F4–F7	244–247
CTO	Communications time-out	28	40
CTO_CNT	Communications time-out counter	29–2B	41–43
DEV_CTRL	Device control	0C	12
DEVCONFIG	Device configuration	0E	14
EE_BURN	EEPROM Burn Count; up-counter	FA	250
FAULT_AUX	AUX threshold exceeded faults	58–59	88–89
FAULT_COM	Communication faults	5E–5F	94–95
FAULT_2OV	Comparator OV faults	5C–5D	92–93
FAULT_2UV	Comparator UV faults	5A–5B	90–91
FAULT_DEV	Device fault	61–62	97–98
FAULT_GPI	General purpose input (GPIO) fault	63	99
FAULT_OV	Overvoltage faults	56–57	86–87
FAULT_SUM	Fault summary	52–53	82–83
FAULT_SYS	System fault	60	96
FAULT_UV	Undervoltage faults	54–55	84–85
FO_CTRL	FAULT output control	6E–6F	110–111
GP_FLT_IN	GPIO input 0/1 FAULT assertion state	7D	125
GPIO_DIR	GPIO direction control	78	120
GPIO_IN	GPIO input value	7C	124
GPIO_OUT	GPIO output control	79	121
GPIO_PD	GPIO pull-down resistor control	7B	123
GPIO_PU	GPIO pull-up resistor control	7A	122
GROUP_ID	(Device) Group Identifier	0B	11
LOT_NUM	Die Lot Identifier	BE–C5	190–197
MAGIC1	"Magic" value enables EEPROM write	82–85	130–133

Table 6. Registers in Alphabetical Order (continued)

NAME	DESCRIPTION	ADDR HEX	ADDR DECIMAL
MAGIC2	"Magic" value enables EEPROM write	FC–FF	252–255
MASK_COMM	Communications FAULT mask register	68–69	104–105
MASK_DEV	Chip FAULT mask register	6B–6C	107–108
MASK_SYS	System FAULT mask register	6A	106
NCHAN	Number of channels enabled for conversion	0D	13
OVERSMPL	Command averaging (oversampling)	07	7
PWRCONFIG	Power configuration	0F	15
RESERVED	*Reserved for future use*	08-09	9-Aug
RESERVED	*Reserved for future use*	16–1D	22–29
RESERVED	*Reserved for future use*	26–27	38–39
RESERVED	*Reserved for future use*	2C–31	44–49
RESERVED	*Reserved for future use*	32	50
RESERVED	*Reserved for future use*	33–36	51–54
RESERVED	*Reserved for future use*	37	55
RESERVED	*Reserved for future use*	38–3C	56–60
RESERVED	*Reserved for future use*	45–4F	69–79
RESERVED	*Reserved for future use*	64–67	100–103
RESERVED	*Reserved for future use*	6D	109
RESERVED	*Reserved for future use*	70–77	112–119
RESERVED	*Reserved for future use*	7.00E–81	126–129
RESERVED	*Reserved for future use*	86–8B	134–139
RESERVED	*Reserved for future use*	B2–BD	178–189
RESERVED	*Reserved for future use*	D0–D1	208–209
RESERVED	*Reserved for future use*	E4-E5	228–229
RESERVED	*Reserved for future use*	EE-EF	238–239
RESERVED	*Reserved for future use*	FB	251
SCRATCH	User-defined data	C8–CF	200–207
SER_NUM	Device serial number	C6–C7	198–199
SHDN_STS	Shutdown recovery status	50	80
SMPL_DLY1	Initial sampling delay	3D	61
SREV	Silicon Revision	00–01	0–1
STATUS	Device status	51	81
TEST_ADC	ADC BIST control	22–24	34–36
TEST_CSUM	Checksum Test Result	F8–F9	248–249
TEST_SPER	ADC test sampling period	43–44	67–68
TESTAUXPU	Test control—AUX pull-up resistors	25	37
TESTCTRL	BIST control	20–21	32–33
TSTCONFIG	Built-In Self-Test (BIST) configuration	1E–1F	30–31
TSTR_ECC	ECC Test Results	E6-ED	230–237
TXHOLDOFF	UART Transmitter holdoff	12	18
VSGAIN	ADC voltage gain correction	D3	211
VSOFFSET	ADC voltage offset correction	D2	210

7.6.3 Register Details

NOTE

The terms "Write without Response" and "Write" or "write" are equivalent and synonymous. The words "Read" or "read" are equivalent to "Write with Response."

FORMAT:			
Name:	ADDRESS Hex	ADDRESS Decimal	Description

7.6.3.1 SREV 0x00-01 (0-1.) Device Version

This register provides the digital and analog die revisions used in the bq76PL455-Q1.

BIT	NAME	DESCRIPTION
[15:8]	DDIE_VER	Digital die version number (byte address 0)
[7:0]	ADIE_VER	Analog die version number (byte address 1)

7.6.3.2 CMD 0x02 (2) Command

Write requests directly targeted to this register cause the specified command to be executed.

Write_With_Response requests directly targeted to this register cause the specified command to be executed and the corresponding results to be returned. The number of bytes returned will be based on the bits selected in the CHANNELS register. Some bits in the CHANNELS register cause more than one value to be returned, refer to their descriptions under the CHANNELS register. *This transaction will return results from the command, not a read of register values.*

It is not possible to read the last value written to this register. Indirect reads of this register produce an undefined value for this register.

If a command is sent to this register without writing the CHANNELS or OVERSMPL registers in the same frame, the values currently in those registers will be used for the command. If a command is sent to the register that writes the CHANNELS or OVERSMPL registers in the same frame, the new register values will overwrite the current register values, and the new values are used in the execution of the command.

Requested values will be returned MSB first in the order that they exist in the CHANNELS register, starting with the MSB (Cell 16, Cell 15 …). No values will be returned for bits not selected in the CHANNELS register.

BIT	NAME	DESCRIPTION
[7:6]	Reserved	Write these bits as 0.
[5]	RQST	= 0 Synchronously sample channels—If this COMMAND is set by a Write With Response request, the values will be sampled and returned. If set by a Write Without Response request, they will only be sampled and stored. = 1 Read sampled values—If this COMMAND is set by a Write_With_Response request, the current set of sampled values will be returned. The response will wait for any ongoing sampling to complete so returned values will be from the same set of samples. If this COMMAND is set by a Write_Without_Response request, it will have no effect.
[4:0]	resp_addr	If set by a Broadcast_Write_With_Response or Group_Write_With_Response request, devices will respond in successive order. These bits set the address of the highest device in the group/set to respond. This value has no effect for other transaction types.

7.6.3.3 CHANNELS 0x03–06 (3–6) Channel Select

When the indicated bit is set, the named channel is included when a CMD (COMMAND) is executed in the Command register.

BIT	NAME	DESCRIPTION
[31:16]	CMD_VSEL	This bitmask determines which battery cell voltages are used when a COMMAND is executed. CMD_VSEL[0] (bit 16) corresponds to cell 1, bit 31 corresponds to cell 16. For each bit in this field: 0 = Do not include this cell voltage. 1 = Include this cell voltage.
[15:8]	CMD_ASEL	This bitmask determines which auxiliary channels are used when a COMMAND is executed. CMD_ASEL[0] (bit 8) corresponds to AUX0. For each bit in this field: 0 = Do not include this AUX channel. 1 = include this AUX channel.
[7]	CMD_GTSEL	Digital die temperature. Usually used as part of self-testing.
[6]	CMD_HTSEL	Analog die temperature. Usually used as part of self-testing.
[5]	CMD_V18SEL	VDD18 internal digital supply. This command is generally used for self-testing purposes.
[4]	RSVD	Reserved — Always write a 0.
[3]	RSVD	Reserved — Always write a 0.
[2]	CMD_REFSEL	4.5-V analog die reference (window comparator ref) is included when a COMMAND is executed. Both the 4.5-V reference and the ground output from the reference MUX are selected by this bit. Sampling and reporting will be 4.5 V and then ground. This command is generally used for self-testing purposes.
[1]	CMD_MODULESEL	Sum-of-cells (VMODULE) monitor is included when a COMMAND is executed. Two conversions are performed to get this value, but only the average of the two is stored and reported. TST_CONFIG[MODULE_MON_EN] is used to enable the measurement. This command is generally used for self-testing purposes.
[0]	CMD_VMMONSEL	VM (negative supply charge pump) voltage monitor. TST_CONFIG[VM_MON_EN] is used to enable the measurement. This command is generally used for self-testing purposes.

7.6.3.4 OVERSMPL 0x07 (7) Command Oversampling

BIT	NAME	DESCRIPTION
[7]	CMD_OVS_CYCLE	This bit only applies to voltage and AUX averaging (oversampling). = 0: Average channels by sampling multiple times on the same channel before changing channel. The initial sample period for the first sample on each channel is made per the respective ADC_PERIOD_VOL and ADC_PERIOD_AUXx time period settings, and then each subsequent average occurs at the respective CMD_OVS_HPER and CMD_OVS_GPER period settings. = 1: Average channels by cycling through all channels one sample per channel before resampling. All voltage averages are completed before any AUX sampling begins, and then all AUX are completed before anything else. The settling time before voltage sampling is set by ADC_PERIOD_VOL and the settling time before AUX sampling is set by ADC_PERIOD_AUXx.
[6:5]	CMD_OVS_HPER	= 3: CMD_OVS_HPER sets the averaging period for the: • Internal temperature measurement of the analog die • Thermal shutdown internal nodes of the analog die • 4.5-V voltage reference of the analog die • VM monitor • Sum-of-cells (V_{MODULE}) monitor When CMD_OVS_CYCLE = 0, this value also sets the period for the averaging on all the voltage channels. These bits must be set to 3 (0b11), which selects 12.6 µs as the average period. Other settings are Reserved and should not be used.

BIT	NAME	DESCRIPTION
[4:3]	CMD_OVS_GPER	CMD_OVS_GPER sets the averaging period for: • Internal temperature measurement of the digital die • Thermal shutdown internal nodes of the digital die • VDD18 When CMD_OVS_CYCLE = 0, this value also sets the period for the averaging on all the auxiliary channels. = 0 4.13 µs = 1 5.96 µs = 2 8.02 µs = 3 12.6 µs: *This setting is recommended for best accuracy in most designs. See the bq76PL455-Q1 Design Reference Manual (TIDU245) for detailed information on using other settings.*
[2:0]	CMD_OVSMP	These bits set the number of times each ADC converted value will be averaged before being stored. Each converted signal will be sampled the requested number of times, averaged, and the results convergent rounded to 16 bits. = 0 Single sample (no averaging) = 1 2 samples are averaged. = 2 4 samples are averaged. = 3 8 samples are averaged. = 4 16 samples are averaged. = 5 32 samples are averaged. = 6–7 *Reserved, do not use this value.*

7.6.3.5 ADDR 0x0A (10) Device Address

BIT	NAME	DESCRIPTION
[7:5]	RSVD	Reserved — always write as zero.
[4:0]	DEV_ADDR	These bits set the device address that the device will respond. These bits can only be written when AUTO_ADDRESS is set to 1. Otherwise, writes to these bits are ignored. The address may also be stored and loaded from EEPROM or using GPIO bits. See text for details.

7.6.3.6 GROUP_ID 0x0B (11) Group ID

BIT	NAME	DESCRIPTION
[7:4]	RSVD	Reserved — always write as zero.
[3:0]	GROUP_ID	These bits set the lower 4 bits of the group identifier that the device will respond to for Group Broadcast requests. The upper 4 bits of the group identifier are fixed at 0 and cannot be changed.

7.6.3.7 DEV_CTRL 0x0C (12) Device Control

BIT	NAME	DESCRIPTION
[7]	SOFT_RESET	Writing a '1' will return the IC to its reset state, causing it to rerun its initialization sequence. This bit is self-clearing and will always return '0' when read.
[6]	PWRDN	Writing a '1' will cause the IC to shut down. This is usually broadcast to the entire stack of ICs to shut down all of the bq76PL455-Q1 devices at the same time.
[5]	STACK_WAKE	Writing a '1' will cause a wakeup tone to be sent from the high-side communication interface to the next device up the stack. Note that setting this bit blocks communication to devices higher in the stack until the wakeup tone sequence is complete. The time to complete depends on the state of that device when the tone is received. This bit is self-clearing and will return '1' while a wakeup tone is in process, and '0' after it has completed.
[4]	WRITE_EEPROM	Writing a '1' while MAGIC1 is set to 0x8C2DB194 and MAGIC2 is set to 0xA375E60F causes the EEPROM to save (be programmed with) the current register values. This bit is self-clearing and will return '1' while the programming cycle is in progress, and '0' after the programming cycle is complete. This bit should not be written while a programming cycle is in progress. Communication timeout power-down will not occur until EEPROM burn is complete. **Do not write to registers while a programming cycle is in progress.** **Do not shut down the IC while a programming cycle is in progress.**

BIT	NAME	DESCRIPTION
[3]	AUTO_ADDRESS	If ADDR_SEL = 0, writing a '1' will cause the device to sample the GPIO pins and store the resulting value in DEV_ADDR. If ADDR_SEL = 1, writing a '1' will cause the device to enter auto addressing mode. When ADDR_SEL = 1, this bit is self-clearing and will be set to '0' after the next frame is received, even if that frame does not set DEV_ADDR. When ADDR_SEL = 0 this bit is self-clearing and will always read 0.
[2:0]	RSVD	Reserved — always write as zero

7.6.3.8 NCHAN 0x0D (13) Number of Channels

BIT	NAME	DESCRIPTION
[7:5]	RSVD	Reserved — always write as zero.
[4:0]	NUM_CHAN	This register sets the number of VSENSE channels (battery inputs) that will be used by the device. Unused channels are dropped consecutively starting from channel 16. The idle channel (the channel the MUX "rests" on between sample intervals) is set to this value. A setting of 0 is not recommended. If 0 is set, the idle channel = VSENSE1. This value masks cell overvoltage and undervoltage faults for unused channels, and turns off the comparators associated with the channel. Values greater than 16 are reserved and should not be used.

7.6.3.9 DEVCONFIG 0x0E (14) Device Configuration

BIT	NAME	DESCRIPTION
[7:6]	Reserved	These bits must always be set to 0.
[5]	REG_DISABLE	0 = Internal regulator (NPN drive for VP/VDIG) is enabled. 1 = Internal regulator (NPN drive) is disabled. In this case, the bq76PL455-Q1 VP, VDIG, and VIO **must** be externally supplied. Regardless of the state of this bit, the regulator will always be enabled while FAULT_SYS[SYS_RESET] = 0.
[4]	ADDR_SEL	0 = Address will be set using the GPIO inputs. 1 = Address will be set using auto addressing. *Note: Changing this bit will not change the current device address.*
[3:2]	COMP_CONFIG	0 = Overvoltage (OV) and undervoltage (UV) comparators are enabled. 1 = OV and UV comparators are disabled. 2 = Comparators are disabled. 3 = Reserved
[1]	COMP_HYST_EN	0 = Comparator hysteresis is disabled. 1 = Comparator hysteresis is enabled.
[0]	UNLATCHED_FAULT	0 = Faults are latched and write fault register to clear. 1 = Faults are unlatched and clear automatically. This setting only applies only to some fault registers. See individual fault register descriptions for details. *The UNLATCHED_FAULT bit should only be changed while no fault bits are set (= 1). The latched/unlatched status of fault bits is undefined when the UNLATCHED_FAULT bit is changed while a fault bit = 1.*

7.6.3.10 PWRCONFIG (0x0F) (15) Power Configuration

BIT	NAME	DESCRIPTION
[7]	AFE_PCTL	It is required that this bit be set to 1. Cell voltage sampling will be delayed by 100 µs every time sampling is requested, regardless of whether or not the AFE was already powered up. This provides time for the AFE to power up and ensures that the sampling synchronization is maintained between multiple devices. In the event a change to this register is made, changes to this register may not take effect until after the next AFE sample is taken.
[6:0]	RSVD	Reserved — always write as zero.

7.6.3.11 COMCONFIG 0x10–11 (16–17) Communications Configuration

BIT	NAME	DESCRIPTION
[15:14]	RSVD	Reserved — always write/read as zero.
[13:12]	BAUD	0 = 125 kbaud 1 = 250 kbaud 2 = 500 kbaud 3 = 1 Mbaud This register will be reset to 250 kbaud by a communication reset.
[11:8]	RSVD	Reserved — always write/read as zero.
[7]	UART_EN	0 = Disable single-ended transmitter interface (RX always enabled) 1 = Enable single-ended transmitter interface
[6]	COMM_HIGH_EN	0 = Disable high-side differential receiver interface 1 = Enable high-side differential receiver interface
[5]	DIFF_COMM_EN	0 = Disable differential low-side transmission interface 1 = Enable differential low-side transmission interface
[4]	FAULT_HIGH_EN	0 = Disable high-side fault differential interface 1 = Enable high-side fault differential interface
[3]	DIFF_FAULT_EN	0 = Disable differential fault output heartbeat 1 = Enable differential fault output heartbeat
[2:0]	RSVD	Reserved—Always write/read as zero.

7.6.3.12 TXHOLDOFF 0x12 (18) UART Transmitter Holdoff

BIT	NAME	DESCRIPTION
[7:0]	TX_HOLDOFF	This sets how many bit periods after a received stop bit the UART transmitter needs to wait before it starts to transmit response data.

7.6.3.13 CBCONFIG 0x13 (19) Balance Configuration

BIT	NAME	DESCRIPTION
[7:4]	BAL_TIME	This sets the time that balancing will be enabled before it is automatically disabled. This is independent of the communication timeout counter and is not reset by communication. The counter is reset any time the BALANCE_EN register is written with a non-zero value. 0 = Until stopped (timer disabled) 1 = 1 second 2 = 1 minute 3 = 2 minutes 4 = 5 minutes 5 = 10 minutes 6 = 15 minutes 7 = 20 minutes 8 = 30 minutes 9 = 60 minutes 10–15 = Reserved
[3]	BAL_CONTINUE	This controls how CBENBL[BALANCE_EN] bits are handled when faults occur. 0 = CBENBL is set to 0 when any fault bit is set, except CUST_CKSUM_ERR, which is ignored. 1 = CBENBL is not changed if a fault occurs.
[2:0]	RSVD	Reserved — always write/read as zero.

7.6.3.14 CBENBL 0x14–15 (20–21) Balancing Enable

BIT	NAME	DESCRIPTION
[15:0]	BALANCE_EN	When EQ_SQUEEZE_EN = 0, these bits control the channels which are balancing . When EQ_SQUEEZE_EN = 1, these bits control the squeeze resistors used in open-wire-detection (OWD). BALANCE_EN[0] controls pin EQ1 for balancing cell1, bit1 controls EQ2, etc. For each bit: 0 = Balancing (or squeeze) is disabled on this channel. 1 = Balancing (or squeeze) is enabled on this channel. If BAL_CONTINUE = 0, all bits in this register will be set to '0' and writes will be ignored if any fault bit (except CUST_CKSUM_ERR) is set. CUST_CKSUM_ERR is ignored. If BAL_CONTINUE = 1, fault bits have no effect on this register.

7.6.3.15 TSTCONFIG 0x1E–1F (30–31) Test Configuration

BIT	NAME	DESCRIPTION
[15:12]	RSVD	Reserved — always write/read as zero.
[11:8]	LDO_TEST	These bits directly control the VDD18 LDO test. Set to 0 for normal operation.
[7]	CCNT_RST_OFF	When this bit is set, the communication counter does not reset when a valid communications packet is received, allowing the communications timeout counters to be tested. COMM_PD_PER should not be changed while this bit is set. If COMM_PD_PER is inadvertently set to a value less than COMM_TIM_CNT while this bit is set, the communications timeout may be missed and not occur for up to 70 min after loss of communications. If COMM_PD_PER is inadvertently written while this bit is set, writing a new value to COMM_TIM_CNT (new value before the timeout should occur) will avoid the issue.
[6]	VDIG_TEST	This bit is used to cause the device to enter SHUTDOWN when the $VDIG_{FLT\_TRIP}$ is tripped as part of a suite of self-test functions. Note: Once set, subsequently clearing this bit will not disable this control even though the bit will read 0. It will not be disabled until the device enters shutdown.
[5]	RSVD	Reserved — always write as zero.

BIT	NAME	DESCRIPTION
[4]	EQ_SQUEEZE_EN(1)	This bit is used to enable the internal resistors connected across the VSENSE inputs, and changes the behavior of the CBENBL register. In the event of a broken wire, applying the resistor should cause any stored charge on the VSENSEn capacitor to bleed off. This bit is normally used for self-testing purposes. When using this feature, CBCONFIG[BAL_CONTINUE] must be set to '1'.
[3]	RSVD	Reserved — always write as zero
[2]	VM_MON_EN	0 = Disable VM (–5 V charge pump) monitor so the monitor ground can be measured using CMD_VMMONSEL. 1 = Enable VM monitor so it can be measured using CMD_VMMONSEL. This bit is normally used for self-testing purposes.
[1]	RSVD	Reserved — always write as zero.
[0]	MODULE_MON_EN	0 = Disable V_{MODULE} monitor so the monitor ground can be measured using CMD_MODULESEL. 1 = Enable V_{MODULE} monitor so it can be measured using CMD_MODULESEL. This bit is normally used for self-testing purposes.

(1) Please see Section *Window Comparator Special Considerations* for additional considerations for the use of this function.

7.6.3.16 TESTCTRL 0x20–21 (32–33) Test Control

CAUTION

Do *NOT* run more than one test simultaneously.

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero.
[9:8]	CKSUM_TEST_RUN	0 = Do nothing. 1 = Perform a USER space checksum test. 2 = Perform a TI space checksum test. 3 = Reserved This bit is normally used for self-testing purposes. This bit is self-clearing and will return the programmed value while the test is running and '0' when it is complete. During this test, each tested register bit is changed twice, and toggles of the fault line are counted. Notes: 1) Writes to the device while this test is running may be ignored or may corrupt the test results and should be avoided. 2) Running this test may cause unexpected fault conditions that should be ignored. 3) User registers ADDR, COMCONFIG, and CBENBL are not included in this test. *Changes in ADDR and COMCONFIG will be detected by communication failure and/or fault testing. Register CBENBL should be tested manually.* 4) Ensure CBENBL = 0 before running this test or it will produce invalid results. Expected results in register TEST_CSUM[CKSUM_TEST] are: User space test: 0x0596 (1430) – [715 register bits tested] TI space test: 0x0778 (1912) – [956 register bits tested]
[7:5]	ECC_TEST	0 = Do nothing. 1 = Load USER space register correctable error to ECC_TEST_RSLT(x). 2 = Load USER space register uncorrectable error to ECC_TEST_RSLT(x). 3 = Load TI space register correctable error ECC_TEST_RSLT(x). 4 = Load TI space register uncorrectable error to ECC_TEST_RSLT(x). 5–7 = Reserved This bit is used normally for self-testing purposes.

BIT	NAME	DESCRIPTION
[4]	ADC_FCAL_TEST	0 = Do nothing. 1 = Perform a full calibration test of the ADC. This bit is self-clearing and will return '1' while the test is running and '0' when it is complete. This test can be used to confirm the ADC is functioning for self-test purposes. Test pass or fail is reported in register FAULT_DEV[ADC_CAL_ERR] (0x61[4]). *Note: This bit should not be set at the same time that ADC_PCAL_TEST is set.*
[3]	ADC_PCAL_TEST	0 = Do nothing 1 = Perform a partial calibration test of the ADC. This bit is self-clearing and will return '1' while the test is running and '0' when it is complete. This test can be used to confirm the ADC is functioning for self-test purposes. Test pass or fail is reported in register FAULT_DEV[ADC_CAL_ERR] (0x61[4]). *Note: This bit should not be set at the same time that ADC_FCAL_TEST is set.*
[2]	GTSD_TRIP	This bit directly forces the thermal shutdown of the digital die to trip. Setting this bit to 1 will cause the device to reset. 0 = Normal operation. 1 = Simulate over temperature (triggers thermal shutdown). This bit is normally used for self-testing purposes.
[1]	HTSD_TRIP	This bit directly forces the thermal shutdown of the analog die to trip. Setting this bit to 1 will cause the device to reset. 0 = Normal operation 1 = Simulate over temperature (triggers thermal shutdown) This bit is normally used for self-testing purposes.
[0]	NPN_OC_TRIP	0 = Normal operation, no NPN protection check is triggered. 1 = Simulate NPN protection check (triggers power-down). Setting this bit will cause the device to reset. This bit is normally used for self-testing purposes.

7.6.3.17 TEST_ADC 0x22–24 (34–36) ADC Output Test

BIT	NAME	DESCRIPTION
[23]	ADC_OUTTST_EN	Setting this bit forces the ADC_PCAL_TEST and the ADC_FCAL_TEST (see TESTCTRL) to fail. Additionally, when this bit is set and a Sample and Store command is run, the ADC conversion will not really be run, but instead the value of ADC_TEST_OUT will be used as the ADC output value. This test is normally used for self-testing purposes.
[22:20]	RSVD	Reserved — always write as zero.
[19:14]	RSVD	Reserved — always read/write as zero.
[13:0]	ADC_TEST_OUT	These 14 bits in two's complement format, set the false ADC output value that will be used when enabled. The default value of 0x0000 represents middle range (nominally 2.5000 V). The maximum positive value (nominally 4.9997 V) is 0x1FFF and the maximum negative value is 0x2000 (nominally 0.0000 V).

7.6.3.18 TESTAUXPU 0x25 (37) AUX Pull-up Test Control

BIT	NAME	DESCRIPTION
[7:0]	AUX_PULLUP_EN	These bits enable pull-ups on the AUX inputs for self-test or system configuration purposes. Bit zero corresponds to AUX0. Setting a bit (1) enables the resistor. Clearing the bit (0) disables the resistor.

7.6.3.19 CTO 0x28 (40) Communication Timeout

BIT	NAME	DESCRIPTION
[7:4]	COMM_PD_PER	This register sets the period at which the system will automatically power-down if no valid communication frames have been received. 0 = Communication power-down disabled 1 = 0.1 second 2 = 0.5 second 3 = 1 second 4 = 2 seconds 5 = 5 seconds 6 = 10 seconds 7 = 30 seconds 8 = 1 minute 9 = 2 minutes 10 = 5 minutes 11 = 10 minutes 12 = 30 minutes 13 = 1 hour 14–15 = Reserved *Note: This setting should be greater than the COMM_TMOUTPER setting (below), if it is necessary to trigger a fault, and code has the time to address it before the device enters SHUTDOWN as a part of testing.*
[3:0]	COMM_TMOUTPER	This register sets the period at which the system will set the COMM_TIMEOUT fault if no valid communication frames have been received. 0 = Communication timeout fault disabled 1 = 0.1 second 2 = 0.5 second 3 = 1 second 4 = 2 seconds 5 = 5 seconds 6 = 10 seconds 7 = 30 seconds 8 = 1 minutes 9 = 2 minutes 10 = 5 minutes 11 = 10 minutes 12 = 30 minutes 13 = 1 hour 14–15 = Reserved *Note: This setting should be less than the COMM_PD_PER setting above, if it is necessary to trigger a fault, and code has the time to address it before the device enters SHUTDOWN as a part of testing.*

7.6.3.20 CTO_CNT 0x29–2B (41–43) Communication Timeout Counter

BIT	NAME	DESCRIPTION
[23:0]	COMM_TIM_CNT	This register sets and reports the current value of the communication timeout up-counter running from a 4-kHz clock source. This is the counter used for both COMM_PD_PER and COMM_TMOUTPER. Writing these bits sets the current value of the communication timeout counter.

7.6.3.21 SMPL_SLY1 0x3D (61) Initial Sampling Delay

BIT	NAME	DESCRIPTION
[7]	RSVD	Reserved — always write/read as zero.
[6:4]	INIT_VOL_DLY	This value specifies the delay from changing the MUX to the first cell voltage until the channel is sampled. This delay is applied only once per sample request, even if oversampling is used. 0 = no delay (*Recommended*(1))* 1 = 2 µs 2 = 5 µs 3 = 10 µs 4 = 20 µs 5 = 50 µs 6 = 100 µs 7 = 200 µs This value is useful when all the cell voltages should return values that are nearly the same, as it allows one settling delay and shorter channel-to-channel delays. See the *bq76PL455-Q1 Design Reference Manual* (TIDU245) for using non-zero settings in accordance with specific design criteria requirements.
[3]	RSVD	Reserved — always write/read as zero
[2:0]	INIT_AUX_DLY	This value specifies the delay from changing the MUX to the first auxiliary channel until the channel is sampled. This delay is applied only once per sample request, even if oversampling is used. 0 = no delay (*Recommended*(1))* 1 = 2 µs 2 = 5 µs 3 = 10 µs 4 = 20 µs 5 = 50 µs 6 = 100 µs 7 = 200 µs This value is useful when all the AUX voltages should return values that are nearly the same, as it allows one settling delay and shorter channel-to-channel delays. See the *bq76PL455-Q1 Design Reference Manual* (TIDU245) for using non-zero settings in accordance with specific design criteria requirements.

(1) *Recommended setting: 0x00*

7.6.3.22 Cell_CSPER 0x3E (62) Cell Voltage and Internal Temperature Sampling Interval

BIT	NAME	DESCRIPTION
[7:4]	ADC_PERIOD_VOL	This value sets the ADC sampling interval that will be used for the cell voltages.
[3:0]	ADC_PERIOD_HTEMP	This value sets the ADC sampling interval that will be used for the analog die internal temperature channel. See Table 7 for settings.

Table 7. ADC Sample Intervals, Registers 62–68

SAMPLING(1)		NOTE
PERIOD(1) µs	ADC_PERIOD_*	
4.13	0	Not Recommended
5.96	1	Not Recommended
8.02	2	Not Recommended
10.0	3	Not Recommended
12.6	4	OK
14.9	5	OK
17.4	6	OK
19.9	7	OK
24.9	8	OK
30.0	9	OK
40.1	A	OK
60.0	B	OK
100	C	OK
200	D	OK
500	E	OK
1000	F	OK

(1) Sampling interval and averaging mode will affect device accuracy.

7.6.3.23 AUX_SPER 0x3F–42 (63–66) AUX Sampling Period

BIT	NAME	DESCRIPTION
[31:28]	ADC_PERIOD_AUX0	This value sets the ADC sampling interval that will be used for the specified AUX channel. See Table 7 for settings.
[27:24]	ADC_PERIOD_AUX1	
[23:20]	ADC_PERIOD_AUX2	
[19:16]	ADC_PERIOD_AUX3	
[15:12]	ADC_PERIOD_AUX4	
[11:8]	ADC_PERIOD_AUX5	
[7:4]	ADC_PERIOD_AUX6	
[3:0]	ADC_PERIOD_AUX7	

7.6.3.24 TEST_SPER 0x43–44 (67–68) Test Sampling Periods

BIT	NAME	DESCRIPTION
[15:12]	ADC_PERIOD_MOD	This value sets the ADC sampling interval that will be used for the Module monitor. See Table 7 for settings.
[11:8]	RSVD	Reserved — to maintain compatibility with default configuration, the user should program these bits to "1001" (binary).
[7:4]	ADC_PERIOD_REF	This value sets the ADC sampling interval that will be used for the 4.5-V ANALOG reference. See Table 7 for settings.
[3:0]	ADC_PERIOD_VM	This value sets the ADC sampling interval that will be used for the VM monitor. See Table 7 for settings.

7.6.3.25 SHDN_STS 0x50 (80) Shutdown Recovery Status

Bits in this register indicate the cause of the last power down. They are not set on the event, but are set during the subsequent initialization. When waking up from SHUTDOWN, at least one bit should be set. This register is only populated on the first digital initialization cycle after a shutdown. If a reset occurs (either requested or due to POR), all bits in the register will be zero.

BIT	NAME	DESCRIPTION
[7]	GCL_PD_STAT	This bit is set after a general control logic power down event. It indicates that shutdown was requested by the controller. This is caused by writing the POWER_DOWN = 1 bit or the communication power down timeout expiring
[6]	GTSD_PD_STAT	This bit is set after a thermal shutdown power down event. It indicates that shutdown was caused by the Digital TSD or by VIO being held low long enough to cause shutdown.
[5]	V5VAO_PD_STAT	This bit is set by a falling V5VAO reaching the V5VAO POR voltage $V5VAO_{SD}$.
[4]	ANALOG_PD_STAT	This bit is set due to the analog die requesting shutdown. See the details for bits 0:1 (below) for the specific cause. In proper operation, if this bit is set either NPN_PD_STAT bit [1] or HTSD_PD_STAT, bit [0] should also be set.
[3:2]	RSVD	Reserved — always read as zero.
[1]	NPN_PD_STAT	This bit is set any time the (VP regulator circuit) external NPN took too long to get VP into proper operating range. This bit is only valid when ANALOG_PD_STAT is set; otherwise, it should be ignored.
[0]	HTSD_PD_STAT	This bit is set when the Analog die TSD occurs. This bit is only valid when ANALOG_PD_STAT is set; otherwise, it should be ignored.

7.6.3.26 STATUS 0x51 (81) Device Status

BIT	NAME	DESCRIPTION
[7]	FAULT_CONDITION	Write '1': No effect Write '0': No effect Read '1': A fault bit is currently set in one or more of the fault registers. This does not include bits in this register even if they do affect the fault output.
[6]	STACK_FAULT	Write '1': No effect Write '0': No effect Read '1': A fault is currently detected on the differential fault input. The state of this bit is always included in the fault output. This fault is masked if FAULT_HIGH_EN == 0. This fault is self-clearing when the fault condition goes away.
[5]	STACK_FAULT_DET	Write '1': Reset the bit to zero. Write '0': No effect Read '1': A fault was detected on the differential fault input. This is a latched version of STACK_FAULT and indicates that some stack fault has been seen since the last time this bit was reset. The state of this bit does not affect the fault output. It is provided for informational purposes and for debugging transient faults. This fault is masked if FAULT_HIGH_EN == 0.
[4]	COMM_CLEAR	Write '1': Reset the bit to zero. Write '0': No effect Read '1': A communication clear has been detected. The state of this bit does not affect the fault output.
[3]	COMM_RESET	Write '1': Reset the bit to zero. Write '0': No effect Read '1': A communication reset has been detected. The state of this bit does not affect the fault output.
[2]	RSVD	Reserved — always write/read as zero
[1]	NEW_DATA	This read-only bit indicates ADC conversion data are available when set. Writing to the bit has no effect. The bit is reset by reading *any* conversion result (sample) data. This can be used to tell if some new sample data has been collected since the last COMMAND to report sample data. This only indicates if some sample has been collected since the last report. It does not track what channel was reported or collected. This bit will not be set by the automatic internal temperature sampling or initialization sampling.

BIT	NAME	DESCRIPTION
[0]	SYS_INIT	Write '1': Stop waiting for VM and continue with initialization. Write '0': No effect Read '0': System initialization is complete. Read '1': System initialization is in progress. This can be useful to speed up the wakeup sequence. Device accuracy may be impaired and is not specified until VM is in the correct range. This is useful when waking the device quickly for ASIL testing purposes or performing tests that will cause shutdown or reset. Setting this bit allows code to perform other functions while waiting for VM to ramp up.

7.6.3.27 FAULT_SUM 0x52–53 (82–83) Fault Summary

BIT	NAME	DESCRIPTION
[15]	UV_FAULT_SUM	For each of these bits: Write '1': Reset all fault conditions of this type. Write '0': No effect Read '1': One or more of the individual fault bits of this type are currently set. These bits always reflect the state of the underlying bits in the other fault registers, which may be latched or not, depending on the setting of the UNLATCHED_FAULT bit.
[14]	OV_FAULT_SUM	
[13]	AUXUV_FAULT_SUM	
[12]	AUXOV_FAULT_SUM	
[11]	CMPUV_FAULT_SUM	
[10]	CMPOV_FAULT_SUM	
[9]	COMM_FAULT_SUM	
[8]	SYS_FAULT_SUM	
[7]	CHIP_FAULT_SUM	
[6]	GPI_FAULT_SUM	
[5:0]	RSVD	Reserved — always read as zero.

7.6.3.28 FAULT_UV 0x54–55 (84–85) Cell Undervoltage Fault

BIT	NAME	DESCRIPTION
[15:0]	UV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': The stored result for the corresponding battery channel is less than UV_THRES_CELL. UV_FAULT[0] corresponds to cell 1. If UNLATCHED_FAULT is set, this register is self-clearing.

7.6.3.29 FAULT_OV 0x56–57 (86–87) Cell Overvoltage Fault

BIT	NAME	DESCRIPTION
[15:0]	UV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': The stored result for the corresponding battery channel is greater than OV_THRES_CELL. OV_FAULT[0] corresponds to cell 1. If UNLATCHED_FAULT is set, this register is self-clearing.

7.6.3.30 FAULT_AUX 0x58–59 (88–89) Auxiliary Under/Over-Threshold Fault

BIT	NAME	DESCRIPTION
[15:8]	AUX_UV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': The stored result for the corresponding auxiliary channel is less than UV_THRES_AUX*. AUX_UV_FAULT[0] corresponds to AUX0. If UNLATCHED_FAULT is set, this register is self-clearing.

BIT	NAME	DESCRIPTION
[7:0]	AUX_OV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': The stored result for the corresponding auxiliary channel is greater than OV_THRES_AUX*. AUX_OV_FAULT[0] corresponds to AUX0. If UNLATCHED_FAULT is set, this register is self-clearing.

7.6.3.31 FAULT_2UV 0x5A–5B (90–91) Comparator Undervoltage Fault

BIT	NAME	DESCRIPTION
[15:0]	CMPUV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': Corresponding battery cell comparator has detected an undervoltage condition. CMPUV_FAULT[0] corresponds to cell 1. When UNLATCHED_FAULT is set, these comparator faults only automatically clear if no other Analog die based fault exists. This is true even for faults that are masked. Analog die faults include FAULT_SYS[0:3] or any bit in registers FAULT_2UV or FAULT_2OV.

7.6.3.32 FAULT_2OV 0x5C–5D (92–93) Comparator Overvoltage Fault

BIT	NAME	DESCRIPTION
[15:0]	CMPOV_FAULT	For each bit in this bitmask: Write '1': Reset the fault condition. Write '0': No effect Read '1': Corresponding battery cell comparator has detected an overvoltage condition. CMPOV_FAULT[0] corresponds to cell 1. When UNLATCHED_FAULT is set, these comparator faults only automatically clear if no other Analog die based fault exists. This is true even for faults that are masked. Analog die faults include FAULT_SYS[0:3] or any bit in registers FAULT_2UV or FAULT_2OV.

7.6.3.33 FAULT_COM 0x5E–5F (94–95) Communications Fault

BIT	NAME	DESCRIPTION
[15]	COMP_ERR_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A bit on the high-side interface failed to compare with its complement. This is notification only; the frame is processed by the communications interface logic.
[14]	COMP_ERR_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A bit on the low-side interface failed to compare with its complement. This is notification only; the frame is processed by the communications interface logic.
[13]	COMP_FLT_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A frame on the high-side interface (COMMH) was stopped due to two or more complement errors (COMP_ERR_H).
[12]	COMP_FLT_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A frame on the low-side interface (COMML) was stopped due to two or more complement errors (COMP_ERR_L).
[11]	EDGE_ERR_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A falling edge was not detected on the high-side interface by the 4th bit. This is caused by an inability to stay synchronized between the expected edges (based on the protocol) and the actual detected edges.

BIT	NAME	DESCRIPTION
[10]	EDGE_ERR_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A falling edge was not detected on the low-side interface by the 4th bit. This is caused by an inability to stay synchronized between the expected edges (based on the protocol) and the actual detected edges.
[9]	ABORT_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A framing bit with value "1" was detected on the high-side differential interface. A data byte was stopped and ignored. If this occurs on the high-side interface, it is always due to a communication problem. Sending COMM_RESET or COMM_CLEAR to the UART interface on the bottom chip will cause this fault on the low-side interface. When it occurs on the high side, it may have caused this chip to fail to return its frame in a broadcast or group response (although the microcontroller should already have detected this before this bit was read).
[8]	ABORT_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A framing bit with value "1" was detected on the low-side differential interface. A data byte was stopped and ignored. Sending COMM_RESET or COMM_CLEAR to the UART interface on the bottom chip will cause this fault on the low-side interface. If this is the only error on the low side, no frames were missed.
[7]	CRC_FAULT_H	Write '1': Reset the fault condition. Write '0': No effect Read '1': A CRC fault has been detected on the high-side interface. The frame was discarded. If it occurs on the high side, it may have caused this chip to fail to return its frame in a broadcast or group response.
[6]	CRC_FAULT_L	Write '1': Reset the fault condition. Write '0': No effect Read '1': A CRC fault has been detected on the low-side interface (either single-ended UART or differential VBUS). The frame was discarded.
[5]	FRAME_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': A framing error has been detected. This indicates that the chip saw a start of frame before it had completed the prior frame. If a partial frame is sent to the UART of the bottom device followed by a COMM_CLEAR, this will occur.
[4]	RSVD	Reserved — always read as zero
[3]	STOP_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': The UART receiver detected an invalid stop bit on the single-ended low-side interface. This error only appears on chips using the UART interface. COMM_CLEAR and COMM_RESET will also cause this fault. This error is specific to the UART interface.
[2:1]	RSVD	Reserved — always read as zero
[0]	STK_FAULT_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': Stack fault input (FAULTH±) is too noisy or is running at the wrong frequency. *Note: The STK_FAULT_ERR flag may not be clearable under some conditions. If a STK_FAULT_ERR is detected, and then no more edges appear on the high-side fault pins (as would be the case if the chip above had a fault condition), it may be impossible to clear the STK_FAULT_ERR flag. Once proper signaling resumes on the high-side fault pin, it will again be possible to clear this fault.* *Masked STK_FAULT_ERR is not cleared during initialization. As a result, there is a approximately 5-µs window at startup where, if the high-side fault receiver detects more than four falling edges, the STK_FAULT_ERR will be set even though it is masked.*
NOTE: COMM_CLEAR will cause a STOP_ERR, FRAM_ERR, and ABORT on the bottom (base) device and a FRAM_ERR and ABORT on the chips higher in the stack. COMP_ERR_L, COMP_FLT_L, and EDGE_ERR_L should never occur on the bottom (base) device.		

7.6.3.34 FAULT_SYS 0x60 (96) System Fault

BIT	NAME	DESCRIPTION
[7]	SYS_RESET	Write '1': Reset the bit to zero. Write '0': No effect Read '1': A system reset has been detected.
[6]	COMM_TIMEOUT	Write '1': Reset the fault condition. Write '0': No effect Read '1': Communications timeout has been detected.
[5]	VDIG_WAKE_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': VDIG supply was already high on wakeup. This could happen if the NPN transistor were leaking and preventing VDIG from going away when VP/VDIG shuts down. It could also occur if the chip is reset (in which case the VDIG supply remained on) or if it was shut down too briefly to allow the supply time to ramp down. This bit is provided to allow detection of leakage current into the supply during shutdown. This is checked immediately after EEPROM loading completes. Once cleared, it will not set again until the block is reset.
[4]	INT_TEMP_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': Overtemperature condition in the digital die If UNLATCHED_FAULT is set, this bit is self-clearing.
[3]	VDIG_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': VDIG supply failure detected in the analog die.
[2]	VM_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': VM supply failure detected in analog die.
[1]	VP_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': VP supply failure detected in analog die.
[0]	VP_CLAMP	Write '1': Reset the fault condition. Write '0': No effect Read '1': Clamp circuit turned on to keep VP from going over voltage.

7.6.3.35 FAULT_DEV 0x61–62 (97–98) Chip Fault

BIT	NAME	DESCRIPTION
[15]	USER_CKSUM_ERR	Write '1': No effect Write '0': No effect Read '1': A checksum error was detected in the registers. This fault is self-clearing when the condition goes away.
[14]	FACT_CKSUM_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': A checksum error was detected in the factory registers.
[13]	ANALOG_FAULT_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': The analog die is reporting an error, but it cannot tell what the error is (no error condition has been detected). This may be caused by a single event upset, or possibly the IC has failed.
[12]	HREF_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': Analog die 4.5-V reference measurement was out of range.

BIT	NAME	DESCRIPTION
[11]	HREF_GND_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': Analog-die reference ground measurement was out of range.
[10:5]	RSVD	Reserved — always read as zero
[4]	ADC_CAL_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': An ADC test (ADC_FCAL_TEST or ADC_PCAL_TEST) failed.
[3]	USER_ECC_COR	Write '1': Reset the fault condition. Write '0': No effect Read '1': A ECC fault was corrected while loading from EEPROM.
[2]	USER_ECC_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': An uncorrectable ECC fault was detected while loading from EEPROM. Registers in the block (not all registers) have been loaded with their default values.
[1]	FACT_ECC_COR	Write '1': Reset the fault condition. Write '0': No effect Read '1': A ECC fault was corrected while loading from factory registers.
[0]	FACT_ECC_ERR	Write '1': Reset the fault condition. Write '0': No effect Read '1': An uncorrectable ECC fault was detected while loading from factory registers. Registers in the block (not all registers) have been loaded with their default values. The device is operating abnormally and has probably failed. Functionality, behavior, and results are suspect and should not be relied upon.

7.6.3.36 FAULT_GPI 0x63 (99) GPI Fault

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always read as zero.
[5:0]	GPI_FAULT	Write '1': Reset the fault condition. Write '0': No effect Read '1': A fault was detected on one of the GPIO inputs configured as a fault input in GPI_FAULT_CONFIG. If UNLATCHED_FAULT is set, this register is self-clearing.

7.6.3.37 MASK_COMM 0x68–69 (104–105) Communications Fault Masks

BIT	NAME	DESCRIPTION
[15]	COMP_ERR_H_MSK	For each of these bits: 0 = Do not mask this fault. 1 = Mask this fault.
[14]	COMP_ERR_L_MSK	
[13]	COMP_FLT_H_MSK	
[12]	COMP_FLT_L_MSK	
[11]	EDGE_ERR_H_MSK	
[10]	EDGE_ERR_L_MSK	
[9]	ABORT_H_MSK	
[8]	ABORT_L_MSK	
[7]	CRC_FAULT_H_MSK	
[6]	CRC_FAULT_L_MSK	
[5]	FRAM_ERR_MSK	
[4]	RSVD	Reserved — always write/read as zero
[3]	STOP_ERR_MSK	0 = Do not mask this fault. 1 = Mask this fault.

BIT	NAME	DESCRIPTION
[2:1]	RSVD	Reserved — always write/read as zero
[0]	STK_FAULT_ERR_MSK	0 = Do not mask this fault. 1 = Mask this fault. *Masked STK_FAULT_ERR is not cleared during initialization. As a result, there is an approximately 5-µs window at startup where, if the high-side fault receiver detects more than four falling edges, STK_FAULT_ERR will be set even though it is masked.*

7.6.3.38 MASK_SYS 0x6A (106) System Fault Masks

BIT	NAME	DESCRIPTION
[7]	SYS_RESET_MSK	For each of these bits: 0 = Do not mask this fault. 1 = Mask this fault.
[6]	COMM_TIMEOUTMSK	
[5]	RSVD	Reserved — always write/read as zero
[4]	INT_TEMP_FAULT_MSK	For each of these bits: 0 = Do not mask this fault. 1 = Mask this fault.
[3]	VDIG_FAULT_MSK	
[2]	VM_FAULT_MSK	
[1]	VP_FAULT_MSK	
[0]	VP_CLAMP_MSK	

7.6.3.39 MASK_DEV 0x6B–6C (107–108) Chip Fault Masks

BIT	NAME	DESCRIPTION
[15]	USER_CKSUM_MSK	For each of these bits: 0 = Do not mask this fault. 1 = Mask this fault.
[14]	FACT_CKSUM_MSK	
[13]	ANALOG_FERR_MSK	
[12:0]	RSVD	Reserved — always write/read as zero

7.6.3.40 FO_CTRL 0x6E–6F (110–111) Fault Output Control

BIT	NAME	DESCRIPTION
[15]	UV_FAULT_OUT	For each of these bits: 0 = Do not include these faults in the fault output. 1 = Include these faults in the fault output.
[14]	OV_FAULT_OUT	
[13]	AUXUV_FAULT_OUT	
[12]	AUXOV_FAULT_OUT	
[11]	CMPUV_FAULT_OUT	
[10]	CMPOV_FAULT_OUT	
[9]	COMM_FAULT_OUT	
[8]	SYS_FAULT_OUT	
[7]	CHIP_FAULT_OUT	
[6]	GPI_FAULT_OUT	
[5:0]	RSVD	Reserved — always write/read as zero

7.6.3.41 GPIO_DIR 0x78 (120) General Purpose IO Direction

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always write/read as zero
[5:0]	GPO_EN	This bitmask enables the GPIO pins to behave as GPI or GPO: 0: Input 1: Output GPO_EN[0] corresponds to GPIO0.

7.6.3.42 GPIO_OUT 0x79 (121) General Purpose Output

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always write/read as zero
[5:0]	GPO	This bitmask sets the output state for each GPIO pin when the corresponding bit of GPO_EN = 1. GPO[0] corresponds to GPIO0.
		0: the GPIO output is 0.
		1: the GPIO output is 1.

7.6.3.43 GPIO_IN 0x7A (122) General Purpose Pull-Up

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always write/read as zero
[5:0]	GPO_PU	Setting any bit to 1 turns the respective GPIO pull-up on. ***Note: Care should be taken not to turn on a bit at same time as the corresponding GPO_PD bit in register GPIO_PD.***

7.6.3.44 GPIO_PD 0x7B (123) General Purpose Pull-Down

BIT	NAME	DESCRIPTION
[7:6]	RSVD	Reserved — always write/read as zero
[5:0]	GPO_PD	Setting any bit to 1 turns the respective GPIO pull-down on. ***Note: Care should be taken not to turn on a bit at same time as the corresponding GPO_PU bit in register GPIO_PU.***

7.6.3.45 GPIO_IN 0x7C (124) General Purpose Input

[7:6]	RSVD	Reserved — always read as zero
[5:0]	GPI	Reports the current value of the GPIO pin inputs. GPI[0] corresponds to GPIO0. Inputs are not latched.

7.6.3.46 GP_FLT_IN 0x7D (125) General Purpose Fault Input

BIT	NAME	DESCRIPTION
[7]	RSVD	Reserved — always read as zero
[6]	GPI_FAULT_SENSE	0 = GPIO fault inputs will create a fault if low. 1 = GPIO fault inputs will create a fault if high.
[5:0]	GPI_FAULT_CONFIG	This bitmask sets which of the GPIO pins are treated as fault inputs. Note that this setting does not prevent the I/O pin from being driven by the device. This feature may be used as a part of self-test.

7.6.3.47 MAGIC1 0x82–85 (130–133) Magic1

BIT	NAME	DESCRIPTION
[31:0]	MAGIC1	Magic value to enable EEPROM programming. This value must be written in a single frame. Reads always return zero.

7.6.3.48 COMP_UV 0x8C (140) Comparator Undervoltage Threshold

BIT	NAME	DESCRIPTION
[7:1]	CMP_UV_THRES	These bits set the comparator undervoltage-threshold value between in 25-mV steps. The range is determined by the CMP_TST_SHF_UV bit.
[0]	CMP_TST_SHF_UV	This bit sets the operating range for the undervoltage comparators. 0 = Normal range of 0.7 V to 3.875 V 1= Shifted range of 2.0 V to 5.175 V (used for BIST purposes)

7.6.3.49 COMP_OV 0x8D (141) Comparator Overvoltage Threshold

BIT	NAME	DESCRIPTION
[7:1]	CMP_OV_THRES	These bits set the comparator undervoltage-threshold value between in 25-mV steps. The range is determined by the CMP_TST_SHF_OV bit.
[0]	CMP_TST_SHF_OV	This bit sets the operating range for the undervoltage comparators. 0 = Normal range of 2.0 V to 5.175 V 1= Shifted range of 0.7 V to 3.875 V (used for BIST purposes).

7.6.3.50 CELL_UV 0x8E–8F (142–143) Cell Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_CELL	This register sets the undervoltage threshold value that will be used for all of the ADC cell voltage measurements. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.51 CELL_OV 0x90–91 (144–145) Cell Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_CELL	This register sets the overvoltage threshold value that will be used for all of the ADC cell voltage measurements. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.52 AUX0_UV 0x92–93 (146–147) AUX0 Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX0	This register contains the undervoltage threshold that will be used for the AUX0 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.53 AUX0_OV 0x94–95 (148–149) AUX0 Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX0	This register contains the overvoltage threshold that will be used for the AUX0 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.54 AUX1_UV 0x96–97 (150–151) AUX1 Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX1	This register contains the undervoltage threshold that will be used for the AUX1 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.55 AUX1_OV 0x98–99 (152–153) AUX1 Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX1	This register contains the overvoltage threshold that will be used for the AUX1 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.56 AUX2_UV 0x9A–9B (154–155) AUX2 Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX2	This register contains the undervoltage threshold that will be used for the AUX2 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.57 AUX2_OV 0x9C–9D (156–157) AUX2 Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX2	This register contains the overvoltage threshold that will be used for the AUX2 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.58 AUX3_UV 0x9E–9F (158–159) AUX3 Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX3	This register contains the undervoltage threshold that will be used for the AUX3 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.59 AUX3_OV 0xA0–A1 (160–161) AUX3 Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX3	This register contains the overvoltage threshold that will be used for the AUX3 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.60 AUX4_UV 0xA2–A3 (162–163) AUX4 Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX4	This register contains the undervoltage threshold that will be used for the AUX4 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.61 AUX4_OV 0xA4–A5 (164–165) AUX4 Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX4	This register contains the overvoltage threshold that will be used for the AUX4 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.62 AUX5_UV 0xA6–A7 (166–167) AUX5 Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX5	This register contains the undervoltage threshold that will be used for the AUX5 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.63 AUX5_OV 0xA8–A9 (168–169) AUX5 Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX5	This register contains the overvoltage threshold that will be used for the AUX5 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.64 AUX6_UV 0xAA–AB (170–171) AUX6 Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX6	This register contains the undervoltage threshold that will be used for the AUX6 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.65 AUX6_OV 0xAC–AD (172–173) AUX6 Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX6	This register contains the overvoltage threshold that will be used for the AUX6 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.66 AUX7_UV 0xAE–AFB (174–175) AUX7 Undervoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	UV_THRES_AUX7	This register contains the undervoltage threshold that will be used for the AUX7 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.67 AUX7_OV 0xB0–B1 (176–177) AUX7 Overvoltage Threshold

BIT	NAME	DESCRIPTION
[15:2]	OV_THRES_AUX7	This register contains the overvoltage threshold that will be used for the AUX7 samples. This is a scaled offset-binary value from 0 V to 5 V.
[1:0]	RSVD	Reserved — always write/read as zero

7.6.3.68 LOT_NUM 0xBE–C5 (190–197) Device Lot Number

BIT	NAME	DESCRIPTION
[31:0]	LOT_NUM(x)	IC lot number

7.6.3.69 SER_NUM 0xC6–C7 (198–199) Device Serial Number

BIT	NAME	DESCRIPTION
[15:0]	SERIAL_NUM	IC serial number

7.6.3.70 SCRATCH 0xC8–CF (200–207) Scratch Registers

BIT	NAME	DESCRIPTION
[63:0]	SCRATCH(x)	This register contains user-defined data (for example, post-assembly calibration coefficients) that can be written and read by the host microcontroller.

7.6.3.71 VSOFFSET 0xD2 (210) Cell Offset Correction

BIT	NAME	DESCRIPTION
[7:0]	CCOFFSET	User offset-adjustment register for VSENSE cell voltage channels. This 2's complement value will be added to all cell voltage channels. The range is approximately –9.77 mV to 9.69 mV full scale in 255 steps. The offset is approximately equal to (5 V × CCOFFSET / 2^{16}). It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.72 VSGAIN 0xD3 (211) Cell Gain Correction

BIT	NAME	DESCRIPTION
[7:0]	CCGAIN	User gain-adjustment register for VSENSE cell voltage channels. This is a 2's complement value where positive values represent a gain > 1.0 and negative values represent a gain < 1.0, and is applied to all cell voltage channels. The range is approximately –9.77 mV to 9.69 mV full scale in 255 steps. The gain correction is approximately equal to (input value × (1 + CCGAIN / 2^{16})). It can be used to compensate for gain error induced by the user design (such as larger values of input resistor) or PCB mounting.

7.6.3.73 AX0OFFSET 0xD4–D5 (212–213) AUX0 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET0	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to (5 V × AUXCOFFSET0 / 2^{16}). See Section *AUX Channel Post-Assembly Calibration Adjustment* for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.74 AX1OFFSET 0xD6–D7 (214–215) AUX1 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET1	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to (5 V × AUXCOFFSET0 / 2^{16}). See Section *AUX Channel Post-Assembly Calibration Adjustment* for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.75 AX2OFFSET 0xD8–D9 (216–217) AUX2 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET2	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to (5 V × AUXCOFFSET0 / 2^{16}). See Section *AUX Channel Post-Assembly Calibration Adjustment* for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.76 AX3OFFSET 0xDA–DB (218–219) AUX3 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET3	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to (5 V × AUXCOFFSET0 / 2^{16}). See Section *AUX Channel Post-Assembly Calibration Adjustment* for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.77 AX4OFFSET 0xDC–DD (220–221) AUX4 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET4	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to (5 V × AUXCOFFSET0 / 2^{16}). See Section *AUX Channel Post-Assembly Calibration Adjustment* for details. It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.78 AX5OFFSET 0xDE–DF (222–223) AUX5 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET5	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to (5 V × AUXCOFFSET0 / 2^{16}). *See text for details.* It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.79 AX6OFFSET 0xE0-E1 (224–225) AUX6 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET6	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to (5 V × AUXCOFFSET0 / 2^{16}). *See text for details.* It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.80 AX7OFFSET 0xE2-E3 (226–227) AUX7 Offset Correction

BIT	NAME	DESCRIPTION
[15:10]	RSVD	Reserved — always write/read as zero
[9:0]	AUX_COFFSET7	User offset-adjustment register for AUX0 input. This 2's complement value will be added to the AUX channel. The range is approximately –38.99 mV to 39.06 mV full scale in 1023 steps. The offset is approximately equal to (5 V × AUXCOFFSET0 / 2^{16}). *See text for details.* It can be used to compensate for offsets induced by the user design or PCB mounting.

7.6.3.81 TSTR_ECC 0xE6-ED (230–237) ECC Test Result[1:0]

BIT	NAME	DESCRIPTION
[31:0]	ECC_TEST_RSLT(x)	These values display the test result from running an ECC test using the TEST_CTRL[ECC_TEST] bits. Expected output for User ECC Test 0x18C3 FF8A 68A9 8069. Expected output for Factory ECC Test 0xCC72 D182 80BA 9767.

7.6.3.82 CSUM 0xF0–F3 (240–243) Checksum

BIT	NAME	DESCRIPTION
[31:0]	USER_CKSUM	This register contains the programmed checksum for the registers. See Table 5, column "CS" for included registers. The FAULT_DEV[USER_CKSUM_ERR] flag will be set when this value does not match the internally calculated value shown in *CSUM_RSLT 0xF4–F7(244–247) Checksum Readout*.

7.6.3.83 CSUM_RSLT 0xF4–F7(244–247) Checksum Readout

BIT	NAME	DESCRIPTION
[31:0]	USER_CKSUM_RD	This register contains the current internally calculated checksum for the registers.

7.6.3.84 TEST_CSUM 0xF8–F9 (248–249) Checksum Test Result

BIT	NAME	DESCRIPTION
[15:0]	CKSUM_TEST	This register contains the most recent test result, from either a User or TI space checksum test.

7.6.3.85 EE_BURN 0xFA (250) EEPROM Burn Count

BIT	NAME	DESCRIPTION
[7:0]	EE_BURN_CNT	This register contains the EEPROM burn count. It is incremented every time the EEPROM is programmed.

7.6.3.86 MAGIC2 0xFC–FF (252–255) Magic2

BIT	NAME	DESCRIPTION
[31:0]	MAGIC2	Magic value to enable EEPROM programming. This value must be written in a single frame. Reads always return zero.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Special Pin Considerations

8.1.1.1 Unused VSENSE Inputs (Designs with < 16 Cells)

VSENSE inputs should be used starting from VSENSE0, VSENSE1, etc. Inputs should be used in ascending order, with all unused inputs located at the highest end, that is, for a 13-cell design, inputs VSENSE14, VSENSE15, and VSENSE16 are not used. Unused VSENSE inputs are then connected to the highest VSENSE pin which in turn is connected to a cell through the resistor of the input low-pass filter. As an example, VSENSE13 is connected to cell 13 via 100 Ω; pins VSENSE14, VSENSE15, and VSENSE16 are then connected to pin VSENSE13. A 100-Ω resistor is used here as an example only, all inputs should use the same resistor as chosen by the designer to meet filter requirements for their circuit implementation.

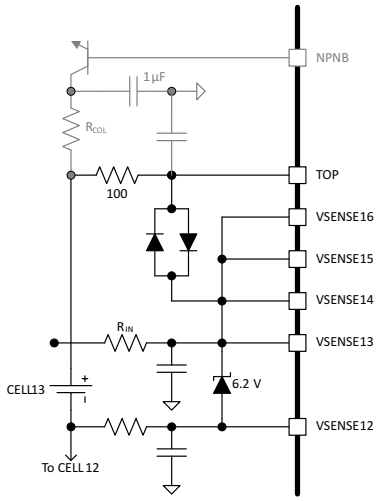


Figure 22. Example Connection for Less than 16 Cells (Some Components Omitted for Clarity)

8.1.1.2 Unused AUX Inputs

Unused AUX inputs can be allowed to float, tied to VSS, or pulled up to VP/VDIG through a nominal 10-kΩ to 1-MΩ resistor. An internal pull-up can be enabled by setting the TESTAUXPU register. The resistor is supplied from the VP pin internally.

8.1.1.3 TOP and VSENSE16 Pins

The TOP pin has a special relationship requirement to the VSENSE16 pin. To prevent violating the "ABSOLUTE MAXIMUM RATINGS" and "RECOMMENDED OPERATING CONDITIONS" during hot-plug or other unusual conditions, the VSENSE16 pin (or highest cell used) should be connected to the TOP pin using two back-to-back signal diodes. This will help to ensure that the specified requirements are met under most conditions. The TOP pin should also include a low-pass filter using a 0.1-µF capacitor and a 100-Ω to 300-Ω resistor to avoid voltage stress during cell connection (hot-plug).

Application Information (continued)

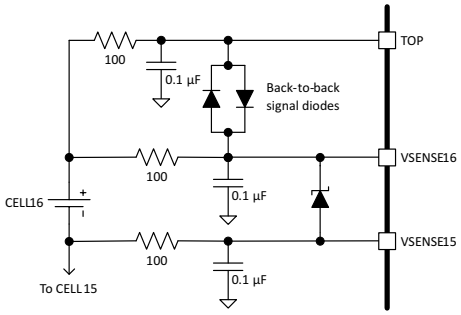


Figure 23. Connecting the TOP and VSENSE16 Pins

8.1.1.4 Grounding

The bq76PL455-Q1 has three analog ground pins, AGND1, AGND2, and AGND3. AGND1 is a general-purpose analog ground associated with the integrated linear regulator controller VP, while AGND2 and AGND3 are quiet analog grounds for the 2.5-V reference, ADC, AFE, and Secondary Protector (window comparators) circuitry. It also has three DGND pins for the digital core and one CGND pin for the differential communications I/Os.

Creation of a good ground plane in the layout is crucial to getting optimal performance from the part. A good ground plane on a dedicated layer will improve measurement accuracy, reduce noise, and provide the necessary ESD, EMI, and EMC performance. A minimum of four layers in the PCB, with one fully dedicated as an unbroken VSS plane (except thermal reliefs) is strongly recommended. Avoid placing tracks on this layer to maintain the unbroken integrity of the plane structure.

All seven IC grounds should be connected to the ground plane with as short as possible track sections to minimize the effects of stray inductance on noise performance.

If more than one bq76PL455-Q1 is included on a single PCB assembly, each will require its own plane in the area surrounding the IC. This is required because each IC has its own VSS reference, and they are often separated by more than 60 V from VSS to VSS of adjacent ICs in the stack. These can exist on the same physical layer, with correct separation to meet creepage and clearance requirements.

Although the plane is employed as a solid GND reference with all grounds connected to it, good layout practice still requires locating any decoupling capacitors as close to the pin they are associated with as possible. This reduces inductance and keeps the loop area as small as possible, which in turn keeps the capacitors as effective as possible in reducing noise.

The combined grounds connected to the ground plane are referred to in this document as "ground" or GND.

8.1.1.5 AGND1 and VSENSE0 Pins

The AGND1 pin has a special relationship requirement to the VSENSE0 pin. To prevent violating the "ABSOLUTE MAXIMUM RATINGS" and "RECOMMENDED OPERATING CONDITIONS" during hot-plug or other unusual conditions, the VSENSE0 pin should be connected to the AGND1 pin using two back-to-back signal diodes. This will help to insure that the specified requirements are met under most conditions.

Application Information (continued)

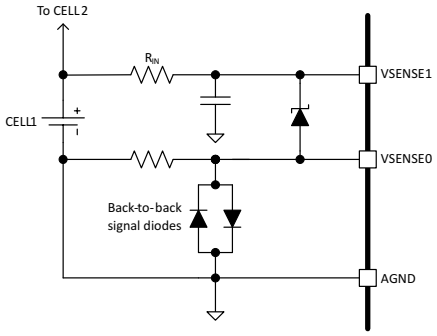


Figure 24. Connecting the AGND1 and VSENSE0 Pins

8.1.2 Differential Communications

The bq76PL455-Q1 uses two differential communications links to transmit signals between ICs in a stack. Differential links are employed to provide superior noise immunity. The base IC then translates the differential signals back to a single-ended signal.

It is important to maintain the signal integrity of each differential pair to maximize immunity to interfering signals from external sources.

1. Keep wires and PCB traces as short as possible. Do not exceed datasheet recommendations.
2. For any single-signal pair between two nodes (ICs), individual wires and traces should have the same length.
3. Unshielded, twisted pair wiring is required for any cable runs.
4. PCB traces should be run in parallel, on the same layer, without any other traces or planes in between. Long runs should avoid "noisy" traces and/or be stitched at intervals similar to twisted pair wire.
5. Capacitors used for voltage isolation between ICs should be high quality and in close physical proximity to each other as part of the parallel track layout.
6. Follow data sheet and application note recommendations for capacitor and resistor values closely.
7. Use of common-mode chokes will significantly increase immunity to interference (EMC).
8. It is the responsibility of the designer to ensure that isolation capacitors are rated for the stack voltage plus a user-determined safety margin in the event of an unforeseen fault. Capacitor pads on the PCB must be laid out to provide adequate creepage and clearance for safety and to meet applicable regulations for high voltage circuits.
9. The minimum recommended series capacitance between ICs in the COMMH/L of FAULTH/L pairs is 380 pF. A typical value is 500 pF, which is usually implemented as two 1000 pF capacitors in series. These capacitors are recommended to have a minimum initial tolerance of 10% and a ±15% temperature coefficient.
10. The maximum recommended capacitance between tracks or twisted pair wires per pair is 70 pF.
11. The maximum recommended capacitance from any single wire or track to GND is 20 pF.

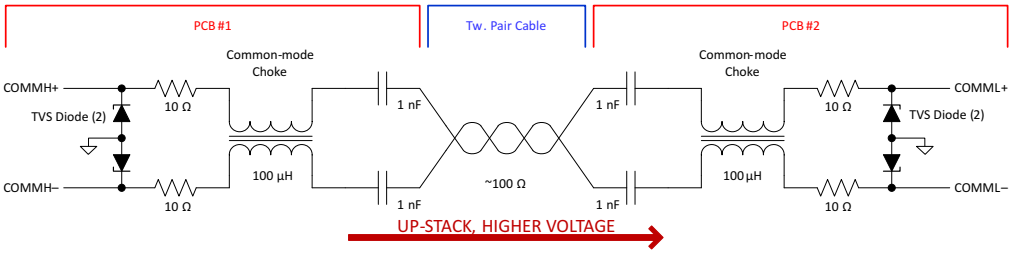


Figure 25. Typical Differential Communications Link Wiring

Application Information (continued)

8.1.2.1 Unused Differential Communications Pins

Unused stack communications pins (COMMH+/–, COMML+/–, FAULTH+/–, FAULTL+/–) are terminated internally, no external pull-up or pull-down resistors are required on these pins if not used. Allow these pins to float if not used.

A properly configured stack should have the unused COMMH and FAULTH receivers disabled. The COMMH drivers cannot be disabled.

8.1.3 ADC

8.1.3.1 Idle (Parking) Channel Errors

Between acquisition cycles, the mux idles on the highest VSENSE channel enabled for conversion by the CHANNEL registers. This allows the OUT1 pin to hold the filter capacitor at the voltage, which will be sampled first on the next cycle.

Parking also introduces a very small error to the idle channel due to the input impedance of the IC causing a small IR drop through the external resistor, which is part of the LP filter. Texas Instruments requires PWRCONFIG[AFE_PCTL] = 1, which will minimize these small errors. This is most helpful for resistor values greater than the default recommendation of 100 Ω. See the *bq76PL455-Q1 Design Reference Manual* (TIDU245) for further design information. When AFE_PCTL is set, cell voltage sampling will be delayed by 100 µs every time sampling is requested, regardless of whether or not the AFE was already powered up. This also helps ensure that the sampling synchronization is maintained between multiple chips. Changes to this bit may not take effect until after the next AFE sample is taken.

8.1.3.2 VSENSE Channel Post-Assembly Calibration Adjustment

Post-assembly calibration adjustment can be used to improve device accuracy further after exposure to soldering and/or bake cycles in the user's manufacturing process. Since the process used, by an individual customer, cannot be predicted or may vary by lot, two registers are provided to tweak ADC gain and offset-correction factors. The total range of adjustment is limited for both factors from –9.77 mV to +9.69 mV.

These gain and offset corrections are applied globally to all VSENSE channels. They are not applied to the AUX channels. The corrections are applied last to the raw ADC values and after factory stored offset and gain corrections have been applied.

The correction procedures should be performed at room temperature (RT) using a stable, high-accuracy DC source and / or voltmeter. The registers contain signed 2's complement values. A zero value in either register indicates no correction. Two voltage points VIN1 and VIN2 are measured for each correction. The users' expected minimum and maximum values for the cell can be used, however the lowest VIN_{MIN} value should be greater than or equal to 2.0 V, and the highest VIN_{MAX} should be less than or equal to 4.5 V.

For best results in most designs, both VIN1 and VIN2 should use the average voltage measured by each channel VSENSE1–16, after correcting for any errors in the stimulus (source) voltages at each input.

Gain Error Correction: –9.77 mV to +9.69 mV in 255 steps (8 bits) in register VSGAIN

Procedure:

1. Apply voltage VIN1, read back from ADC VOUT1, and record both.
2. Apply voltage VIN2, read back from ADC VOUT2, and record both.
3. Calculate slope m = (VOUT2–VOUT1) / (VIN2–VIN1).
4. Find the gain error correction (GEC) at 5 V in 16-bit LSB (5 V is used regardless of VINx value).

$$GEC = \left(\frac{1}{m} - 1\right) * \frac{5}{\left(\frac{5}{2^{16}}\right)} = \left(\left(\frac{1}{m}\right) - 1\right) * 2^{16}$$

Application Information (continued)

NOTE

The final GEC should be an 8-bit 2's-complement value in the range –128 to +127 after discarding the upper 8 bits of the 16-bit value. Values exceeding this are suspect and probably indicate an error. If such a value must be used, the resulting 8-bit value should be saturated (–128 or +127) and sign corrected as necessary.

This gain adjustment is input dependent—A correction of 9 mV at full scale input, results in a correction of 4.5 mV at half scale input.

5. Write the 8-bit value to the VSGAIN register.
6. Perform the Offset Error Correction step below.

Offset Error Correction: –9.77 mV to +9.69 mV in 255 steps (8 bits) in register VSOFFSET

Procedure: (Use m, VIN1 and VOUT1 from the GAIN correction procedure above.)

1. Find the offset error correction (OEC) at 5 V in 16 bit LSB (5 V is used regardless of VINx value).

$$OEC = \frac{VIN1 - \left(\frac{1}{m}\right) * VOUT1}{\frac{5}{2^{16}}} = \left(VIN1 - \left(\frac{1}{m}\right) * VOUT1\right) * \frac{2^{16}}{5}$$

NOTE

The final OEC should be an 8-bit 2's-complement value in the range –128 to +127 after discarding the upper 8-bits of the 16-bit value. Values exceeding this are suspect and probably indicate an error. If such a value must be used, the resulting 8-bit value should be saturated (–128 or +127) and sign corrected as necessary.

2. Write the 8-bit value to the VSOFFSET register.
3. Save the new values to EEPROM by setting DEV_CTRL[WRITE_EEPROM]. The EEPROM checksum will also require re-calculation and saving due to this (or any) change.

8.1.3.3 AUX Channel Post-Assembly Calibration Adjustment

Post-assembly calibration adjustment can also be used to improve the AUX channel accuracy further after exposure to soldering and/or bake cycles in the user's manufacturing process. The process is similar to the steps above for the VSENSE channel correction, with three differences:

- Offset correction only is provided for the AUX channels, there is no gain correction.
- Each AUX channel has an individual offset correction register, rather than a single global correction.
- The correction range is extended from –39.06 mV to +38.99 mV in 1023 steps (10 bits).

The correction procedures should be performed at room temperature (RT) using a stable, high-accuracy DC source and / or voltmeter. The registers contain 10-bit, signed, 2's-complement values. A zero value in any register indicates no correction. Two voltage points are measured for each correction. The user's expected minimum and maximum values for the cell can be used. However, the lowest VIN_{MIN} value should be greater than or equal to 2.0 V and the highest VIN_{MAX} should be less than or equal to 4.5 V.

Although no AUX gain error correction is provided by the bq76PL455-Q1, the required correction can be performed in the host microcontroller using the slope value calculated above as part of the GEC for the VSENSE channels. The value stored in VSGAIN can be read back and used, or a different value stored separately in one of the SCRATCH registers of the bq76PL455-Q1. Using a value stored in the bq76PL455-Q1 permits the value to follow the device in distributed systems. Optionally the value can be stored in microcontroller memory. Because gain error corrections are primarily correcting for VREF errors, a single-gain error correction for the AUX channels is sufficient.

AUX Offset Error Correction: –39.06 mV to +38.99 mV in 1023 steps (10 bits) in registers AX0OFFSET through AX7OFFSET, one 16-b register per AUX input channel

Application Information (continued)

Procedure: (use m from the VSENSE GAIN correction procedure above, or recalculate separately using any AUX channel as desired)

1. Apply voltage VINn, read back from ADC VOUTn, where 'n' is the AUX channel number. Record both.
2. Find the AUX offset correction (AOC) at 5V in 16 bit LSB (5V is used regardless of VINn value). This is the same formula used above for the VSENSE offset correction (OEC) but a larger adjustment range is possible.

$$AOCn = \frac{VINn - \left(\frac{1}{m}\right) * VOUTn}{\frac{5}{2^{16}}} = \left(VINn - \left(\frac{1}{m}\right) * VOUTn\right) * \frac{2^{16}}{5}$$

NOTE

The final AOC should be a 10-bit 2's-complement value in the range –512 to +511 after discarding the upper 6-bits of the 16-bit value. Values exceeding this are suspect and probably indicate an error. If such a value must be used, the resulting 10-bit value should be saturated (–512 or +511) and sign corrected as necessary.

3. Write the 10-bit value to the 16-b AXnOFFSET register, where 'n' is the AUX channel number.
4. Repeat steps 1–3 for each AUX channel 0–7.
5. Save the new values to EEPROM by setting DEV_CTRL[WRITE_EEPROM]. The EEPROM checksum will also require re-calculation and saving due to this (or any) change.

8.1.4 Device Addressing

8.1.4.1 Using a Stored Address

The value in ADDR is restored from EEPROM as part of the reset process. If DEVCONFIG[ADDR_SEL] ==0, this value is overridden by the value sampled from the GPIOs.

8.1.4.2 GPIO Addressing

When DEVCONFIG[ADDR_SEL] ==0, the device uses the address sampled from GPIO[4:0] to set ADDR. The address is sampled as part of the reset process or by setting DEV_CTRL[AUTO_ADDRESS].

8.1.4.3 Auto Addressing

Prior to using the Auto-Addressing function in a stack, all devices must be woken up. A small delay to allow for the IC power to come up and stabilize must also be provided. These steps are described in detail elsewhere in this document, but typically require a few milliseconds per device.

Very simple "stacks" consisting of a single device may use address 0x00 (or any other valid address) for the device. Address 0x00 may also be used for the first device in stacks of more than one device.

When DEVCONFIG[ADDR_SEL] ==1 and DEV_CTRL[AUTO_ADDRESS] ==1, then the device enters automatic addressing mode. In this mode, the device turns off the high-side communications transmitters for one frame (so the next frame received is not retransmitted) and enables writes to ADDR[DEV_ADDR]. It is expected that the next frame will set the address of the part. Normally, the address is not writeable, so a Broadcast write transaction can be used and will only affect the one part waiting for an address. After receiving the frame, writes to ADDR[DEV_ADDR] are again disabled and the high-side transmitter is re-enabled.

To auto-address the stack of bq76PL455-Q1 devices, the microcontroller should:

1. Broadcast write DEV_CTRL[AUTO_ADDRESS] = 1
2. Broadcast write consecutive addresses to ADDR[DEV_ADDR] until all parts have been assigned a valid address.

Good practice dictates that all devices be checked by reading back their address registers, at a minimum, to establish that the addressing function worked properly. Subsequent reading and writing depend on correctly addressed devices in the stack.

Application Information (continued)

8.1.5 Balancing

If the part is configured to disable balancing on a fault condition and any fault occurs while balancing is occurring (CBCONFIG[BAL_CONTINUE] = 1 && CBENBL ≠ 0), there is an approximately 2 µs window where writes to the part are blocked immediately after the fault occurs. If the user attempts a write in this window, the write will not occur. After the fault tone is interrupted following detection of a fault, the user firmware should wait at least 2 µs before writing to the part.

8.2 Typical Application

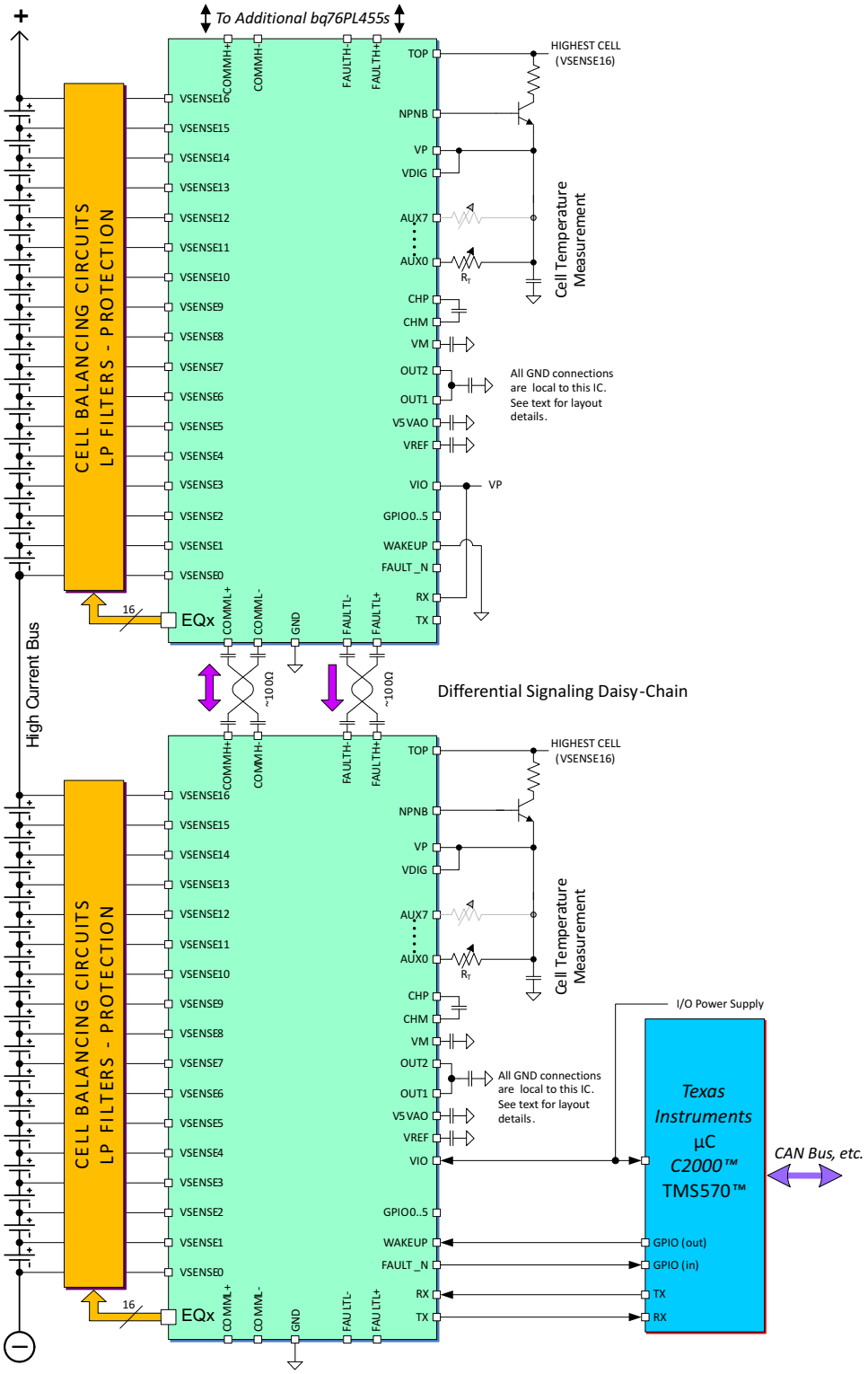


Figure 26. Typical Implementation

Typical Application (continued)

8.2.1 Design Requirements

In order to extract the best performance from the bq76PL455-Q1, it is imperative that care be taken in the choice of external components and the design of the PCB to which the device and the associated components are mounted. The user is directed to *bq76PL455-Q1 Design Reference Manual* (TIDU245) for a more detailed discussion of the hardware considerations that should be made.

8.2.2 Detailed Design Procedure

The user is directed to *bq76PL455-Q1 Design Reference Manual* (TIDU245) for a more detailed discussion of the design considerations that should be made.

8.3 Initialization Set Up

8.3.1 Factory Configuration Summary

When the bq76PL455-Q1 leaves the factory, its EEPROM memory holds a configuration suitable for many applications, but may need some tweaking for your design.

From the factory (see *Register Summary*):

1. The address is set to 0x00.
2. All digital and communications faults are enabled.
3. All analog faults (OV, UV) are disabled (masked).
4. Any fault that occurs and is not masked will control the FAULT_N and FAULTL± outputs.
5. Sampling is set for 8-sample averaging, 60 µs for the first sample, and 12.6 µs for the other samples (7). This setup requires a 390-pF capacitor on pin OUT1.
6. All sixteen VSENSE inputs, no AUX channels, and no auxiliary channels are enabled for conversions.
7. No user-settable gain or offset corrections are applied to the VSENSE or AUX ADC channels – these allow post-assembly or end-of-line corrections to ADC results.
8. The UART interface is enabled at 250 kBaud.
9. GPIO pins are all programmed as inputs, no pull-up or pull-down resistor is enabled, leaving the inputs floating. The pins should be reprogrammed to become outputs, or inputs with a pull-up/down enabled if none are provided externally. The pins should not be allowed to remain as floating inputs, because unpredictable operation is possible accompanied by excess current draw.

8.3.2 Device Setup/User Configuration Summary

An abbreviated version of starting up a stack of devices is described below. Many more details are available in the *bq76PL455-Q1 Communication Examples* (SLVA617), including validated communications sequences.

1. Set an address for each device in the stack, using GPIO pins or Auto-Addressing (detailed below)
   (a) Make sure all devices are awake and are ready to receive the Auto-Address Enable command
   (b) Turn on the downstream communications drivers on all devices in the chain.
   (c) Place all devices into Auto-Address learn mode.
   (d) Send out new addresses to all possible bq76PL455-Q1 device addresses, in incrementing order starting at zero.
   (e) Read back the value stored in the Device Address register from each newly addressed device, starting at address zero and proceeding sequentially. The last bq76PL455-Q1 to respond successfully is the last device in the serial chain. Steps d and e may be shortened if the range of possible devices is known in advance. Limit the number addressed to the expected quantity.
   (f) Turn off the high-side communications receiver on the last (top-most) device in the chain.
   (g) Turn off the single-ended transmitter on all but the lowest device in the chain.
   (h) Starting at the top of the stack of devices, clear all existing faults. It is important to start clearing faults from the top of the stack to prevent faults from "higher" units from re-enabling faults as they propagate down the stack.
2. Configure the AFE (Channel Selections and Fault Thresholds)

Initialization Set Up (continued)

Prior to reading voltages from daisy-chain networked devices, the AFE on each of the stacked devices should be properly configured to scan the desired channels at the desired timing. Once each device has been properly configured, reading voltages from each device can begin.

The following listed steps should be performed as a group for each stacked device, starting from the top device, continuing through, and ending with the bottom-most device of the stack.

(a) Configure GPIO pins as required by your design
(b) Configure the initial sampling delay
(c) Configure voltage and internal sample intervals/periods
(d) Configure the oversampling rate
(e) Select number of cells and desired channels to sample
(f) Set overvoltage and undervoltage thresholds
(g) Check and clear faults, which may have occurred because of the configuration.

3. Reading Voltages from Daisy-Chain Networked Devices

When bq76PL455-Q1 devices are networked, wherein each device monitors a section of a stack of cells, it is important to try to capture the voltages of each sub-stack as synchronously as possible. This "snapshot" can be obtained if all devices in the stack are sampling in parallel.

Summary of Steps for Reading Voltages from Daisy-Chain Networked Devices

(a) Broadcast a trigger to all devices in the network to start sampling the selected cell and auxiliary channels and temperature.
(b) Query each device individually in sequence for the data collected during the last "snapshot" read.

9 Power Supply Recommendations

In most cases, the bq76PL455-Q1 is powered from the same cells it monitors and generates additional required VP and VDIG supplies from this input. For best performance, it is important to take care in the choice and placement of external components related to power. The user is directed to the *bq76PL455-Q1 Design Reference Manual* (TIDU245) for details.

10 Layout

10.1 Layout Guidelines

Since the bq76PL455-Q1 measures small changes in voltage, care should be taken in the layout of signals to and from the device to avoid coupling noise onto sensitive inputs. The layout of ground and power connections, as well as communication signals should also be made carefully. The *bq76PL455-Q1 Design Reference Manual* (TIDU245) contains additional information regarding concerns that should be taken into consideration.

10.2 Layout Example

To ensure the best possible accuracy performance, it is recommended to follow some basic layout guidelines for the bq76PL455-Q1 to provide best EMI and BCI performance.

An unbroken ground plane layer as part of a four or more layer board is recommended, with all AGND, DGND, CGND connections (listed below) made directly to the plane. The common GND planes are star connected directly to BAT0. There should also be a keep-out area on plane area adjacent to the isolation capacitors if daisy-chain communication is implemented.

- AGND1 – Power section (noisy GND)
- AGND2 – GND for Front end output
- AGND3 – GND for ADC input
- DGND1, DGND2, DGND3 – Digital GND
- CGND – Communications digital GND

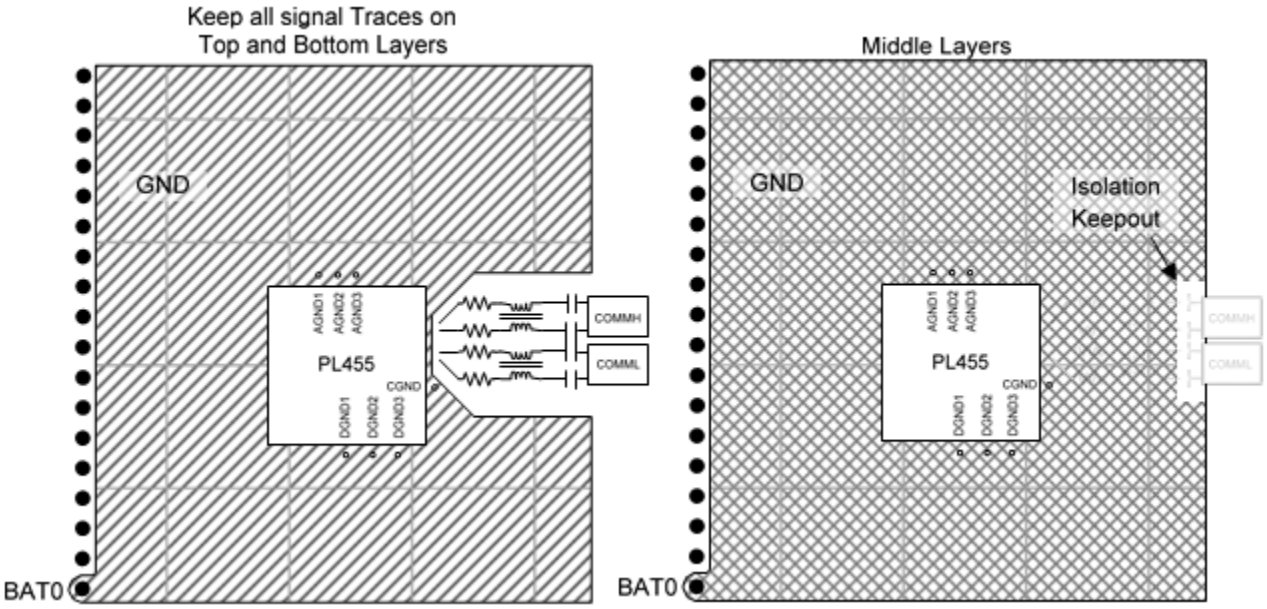


Figure 27. Simplified Layout Guideline

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

An evaluation module (EVM), with an associated PC-based Graphical User Interface (GUI) program, is available. Please see Related Documentation for the reference numbers for the evaluation module and its associated interface software.

11.1.2 Device-Specific Terminology

AFE Analog front-end. A set of analog signal-conditioning circuitry that uses operational amplifiers and filters to provide a configurable and flexible-electronics functional block, which is needed to interface a variety of sensors to a microcontroller or an analog-to-digital converter.

Battery A collection of series and parallel connected cells with a single set of high voltage (+) and (–) outputs, which power the vehicle.

BIST Built-in-Self-Test. A feature of the part allowing testing of critical and other blocks for correct operation. Testing is user controlled and may include external components. Built-In Self Tests can be used optionally to improve the safety of the system into which the bq76PL455 is designed.

BMS Battery Monitor System, a system of bq76PL455-Q1s connected together and then to a microcontroller (µC) for measuring, monitoring, and controlling a stacked series of cells forming a battery pack.

Bridge Mode If the bq76PL455-Q1 is operated as a communications extender to build a distributed, modular BMS system, then the base device (device closest in the communications chain to the microcontroller) is not connected to cells and instead is powered from external sources. The device is used to convert the UART signals from a microcontroller (µC) to the differential signaling used by the bq76PL455-Q1 communications daisy-chain. The signal conversion is done locally, a short distance from the µC. The VBUS differential interface (see below) maintains the signal integrity using cabling over relatively long distances in a noisy environment. This in turn facilitates building modular systems with distributed ‘bq76PL455-Q1 nodes close to the cells they are monitoring.

Cell An individual cell or group of cells connected in parallel. Cells are connected to VSENSE inputs, connected in series to form modules, and stacks of cells to form a battery.

Communications Extender See “Bridge Mode” above.

Daisy-Chain A series connected string of monitoring devices, that is, bq76PL455-Q1 devices communicating to a base device by passing the communications signals through DC blocking devices and the bq76PL455-Q1 integrated circuits (ICs) in the string. In the case of the bq76PL455-Q1, a suitably rated capacitor is used as the DC block. A differential communications link is used to form the daisy-chain of the bq76PL455-Q1. “Daisy-chain” usually refers to just the communications links, but is sometimes used to refer to the collection of devices and cells.

Differential-Signaling Differential signaling sends a digital signal and its complement simultaneously over a pair of wires. The receiver is sensitive to the difference of the two signals, not the absolute amplitude of either signal by itself. The wire pair is usually twisted so that any interfering signal affects both equally as a common-mode signal. The result is that differential signaling offers much higher common-mode rejection ratios (CMRR) than single-ended signals, and results in much better noise rejection.

FMEA Failure Mode and Effects Analysis is an analysis of possible failure modes of the IC and the overall effect on operation. This type of analysis is important when evaluating a device for safety performance in a system environment.

ISO26262 International Standardization Organization, standard number 26262. This broad standard covers automotive Functional Safety of electrical/electronic (EE) systems and comprises elements of design, documentation, qualification, and proper operation required for the safe design and use of automotive EE systems. Refer to http://www.iso.org for further information.

LPF Low Pass Filter made up of one or more R/C combinations where the resistor is in series with the

Device Support (continued)

signal and the capacitor is on the load side and connected to “ground”. Each R/C element contributes one time constant or tau.

Module A collection of cells connected in series monitored by one bq76PL455-Q1. This is typically 16 cells, but may be fewer as needed. Modules may be connected in series to form stacks and complete battery packs. The bq76PL455-Q1s are also typically connected in a series daisy-chain to facilitate communications to a microcontroller.

Stack A collection of modules of cells. Stack and battery are synonymous in most applications.

V_{CELL} The voltage from one cell or group of parallel connected cells, which is measured across two VSENSE pins, for example, VSENSEn and VSENSEn-1.

V_{MODULE} The voltage from a collection of series connected cells forming a module. The voltage is measured by the device from the TOP pin to GND.

V_{STACK} The voltage from a collection of series connected cells forming a stack or battery pack. This is often a high voltage. The voltage is not measured directly by the bq76PL455-Q1, but may be calculated by adding all of the individual cell voltages in the stack or by adding together all of the V_{MODULE} voltages in the stack. These should produce approximately the same value.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *bq76PL455 Communication Examples* (SLVA617)
- *bq76PL455 EVM and GUI User Guide* (SLUUAT2)
- *bq76PL455-Q1 Design Reference Manual* (TIDU245)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *JEDEC Standard JESD51-2A, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- *JEDEC Standard JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- *JEDEC Standard JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions - Junction-to-Board*

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

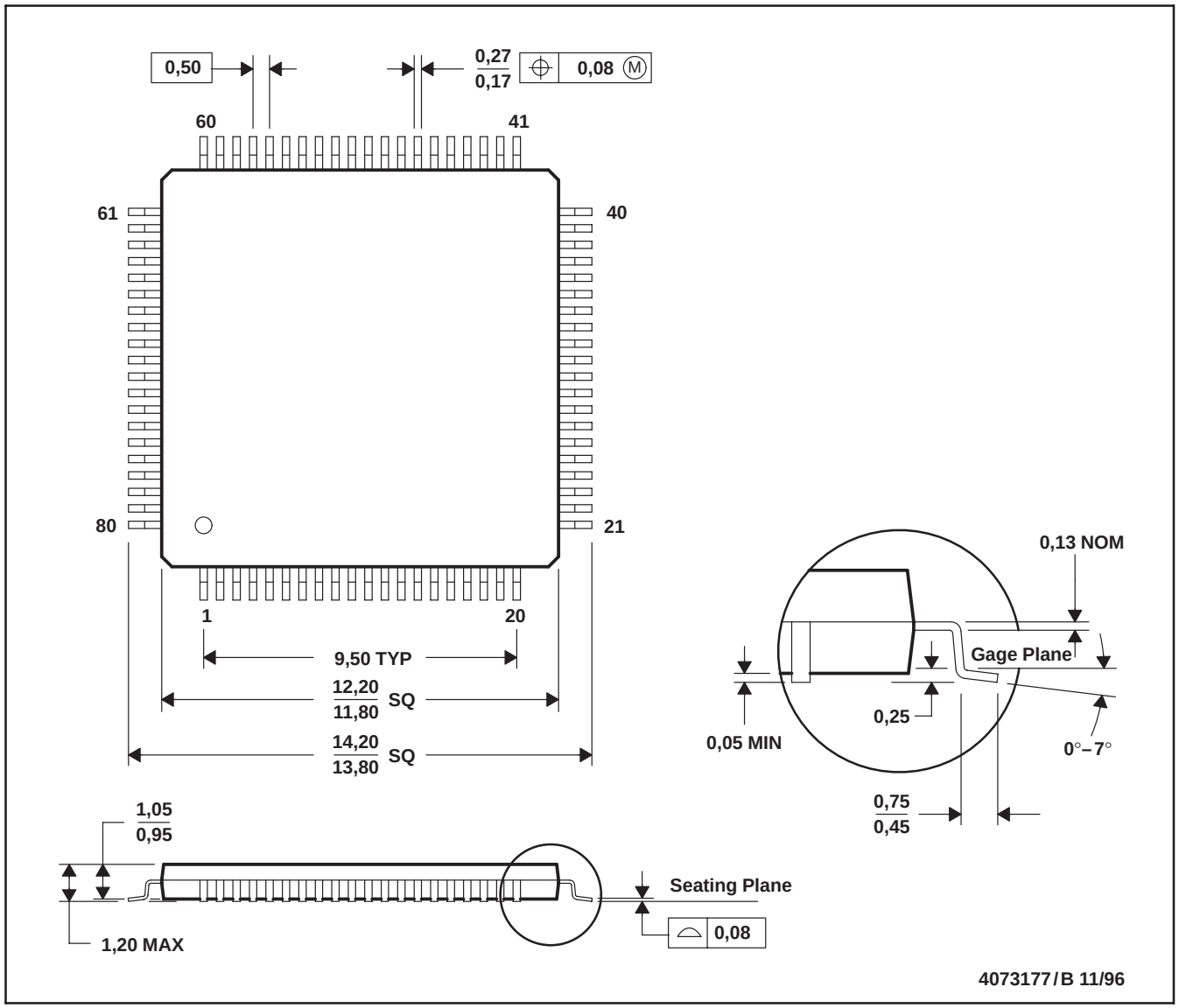
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data are subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

For packaging and ordering information, please contact your TI representative.

MTQF009A – OCTOBER 1994 – REVISED DECEMBER 1996

PFC (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (1)	MSL Peak Temp (2)	Op Temp (°C)	Device Marking(3)(4)
BQ76PL455TPFCRQ1	TQFP	PFC	80	1000	Green (RoHS & no Sb/Br)	Level-3-260C-168 HR	-40 to 105	BQ76PL455T
BQ76PL455TPFCTQ1	TQFP	PFC	80	250	Green (RoHS & no Sb/Br)	Level-3-260C-168 HR	-40 to 105	BQ76PL455T

(1) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(2) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(3) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(4) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265