bq76PL455-Q1 Reference Design Guide

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1 Introduction

This document provides system design information for the TI bq76PL455-Q1 Passive Cell Balancing IC. The information provided here should be used in addition to the device datasheets.

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2 Conventions and Acronyms

This section describes the conventions and acronyms used in this document.

2.1 Conventions

'0'	Binary digit zero; a logic low level (a low voltage for active high logic, and a high voltage for active low logic)
'1'	Binary digit one; a logic high level (a high voltage for active high logic, and a low voltage for active low logic)
"d…"	A binary number with more than one digit (d is 0-1)
d…	A decimal number (d is 0-9)
0xd…	A hexadecimal number (d is 0-F)
d..h	A hexadecimal number (d is 0-F)
k	kilo; 1000
K	kilo; 1024 (note: this is not official SI usage)
b	bit
B	byte

2.2 Acronyms

ADC	Analog to Digital Converter
AFE	Analog Front End
BCI	Bulk Current Injection
BMS	Battery Management System
BSP	Battery Stack Protection
CAN	Controller Area Network
DAC	Digital to Analog Converter
EEPROM	Electrically Erasable Programmable Read Only Memory
EMI	Electro-Magnetic Interference
GPIO	General Purpose Input Output
MCU	Micro-Controller Unit
Module	Series connection of cells managed by the bq76PL455-Q1
OC	Over Current
OV	Over Voltage
OVP	Over Voltage Protection
OT	Over Temperature
PWM	Pulse Width Modulation
Stack	Series connection of modules managed by the pack controller
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UV	Under Voltage
UVP	Under Voltage Protection

2.3 bq76PL455-Q1

IC	Description	Quantity	Order number
bq76PL455-Q1	16-channel passive cell balance monitor and protector	1000 (tape and reel)	bq76PL455TPFCRQ1
bq76PL455-Q1	16-channel passive cell balance monitor and protector	250 (tray)	bq76PL455TPFCTQ1

Table 1 - Passive Chipset IC List

2.4 System Critical Circuits

This section describes circuits that are global in nature and required for reliable system performance, such as survival of hot-plug events including protection for in-rush currents and ESD protection.

2.4.1 Module Transient Suppression Diode

The transient suppression diode (TVS) can be seen as Z19 in the schematic in Appendix C, Figure 19.

The primary purpose of the TVS diode is to provide clamping of transient voltages to below bq76PL455-Q1 ABS MAX (96 V). These transients usually occur during hot-plug events.

2.4.2 ESD Protection

The back-to-back diodes D7 and D1 (Appendix C, Figure 20 or Figure 21 and highlighted in Figure 1 below) are required to ensure VSENSE16 stays close to TOP (see V_{TOP_DELTA} in bq76PL455-Q1 datasheet) even in the event of an open wire on VSENSE16 and during hot plugging. Select diodes that can withstand the continuous currents during a wire disconnect and also can withstand inrush currents during hot plug. Use diodes that have a higher Vf, such as an ultrafast or fast diode. Low Vf diodes such as Schottkey diodes should not be used because noise on the TOP pin could potentially get coupled onto the VSENSE16 pin (or highest sense line used).

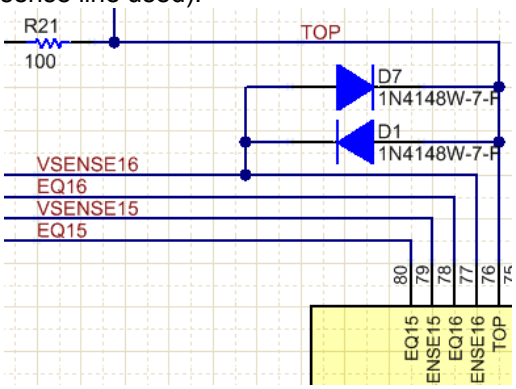

Figure 1 - D7 and D1

The back-to-back diodes D2 and D3 (Appendix C, Figure 20 or Figure 21 and highlighted in Figure 2 below) are required to off-load current from internal ESD diode during hot plug or open wire faults. Select diodes that can withstand the continuous currents during a wire disconnect and also can withstand inrush currents during hot plug. Use diodes that have a higher Vf, such as an ultrafast or fast diode. Low Vf diodes such as Schottkey diodes should not be used because noise on the GND pin could potentially be coupled onto the VSENSE0 pin.

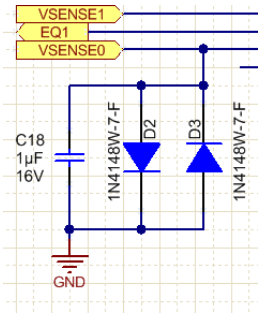

Figure 2 - D2 and D3

2.4.3 In-Rush Protection

The in-rush current protection for the bq76PL455-Q1 can be seen in Appendix C Figure 20 or Figure 21, as R21 on the bq76PL455-Q1 TOP pin. R21 (summed with any other resistance which may be present on BAT16 (e.g. fuses)) should be max 300Ω.

C33 is recommended to be a 0.1µF capacitor

2.4.4 Hot-Plug

2.4.4.1 Zener Diodes

Zener diodes are required to be placed close to the input pin on the system PCB, with one zener diode across each input channel. The zener diodes are necessary to the system and serve two functions:

1. Provide overvoltage protection to the AFE inputs
2. Provide a path for in-rush currents during hot plug-in

The zener diode can be seen in the schematic in Appendix C, Figure 19 and Figure 3 below.

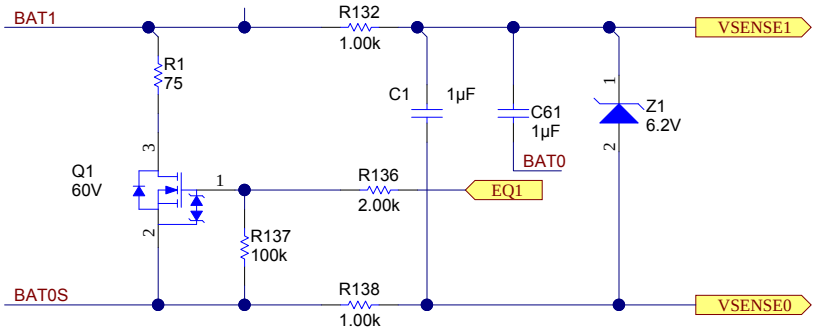

Figure 3 - Protection Zener Current Limit

The zener diodes should be selected to ensure the following conditions are met:

1. The bq76PL455-Q1 inputs are protected from input voltage transients and kept below 7V.
2. The zener max reverse current (I_z) at normal battery cell voltage levels should be as low as possible to keep the quiescent system current draw low.
3. The zener should be capable of withstanding instantaneous or continuous currents that the bq76PL455-Q1 may experience in a fault event. These events can include cable

connect/disconnect, inrush, or reverse battery voltage. Depending on the fault and the direction of current flow, the max power dissipation for the zener diode should not be exceeded to stay within max operating conditions.

For example, the zener diodes used in the reference schematic (Diodes Inc. DDZ6V2B-7) are rated at 6.2V, with a max reverse current (Iz) ≈ 0.5µA at 4V.

2.4.4.2 Front-End In-Rush Protection and Nyquist Filter

The series resistors on the bq76PL455-Q1 sense inputs (e.g., R69 in the schematic provided in Appendix C, Figure 19) are necessary to the system and serve two functions:

1. They protect the AFE inputs from in-rush currents during hot plug-in. This requirement limits the input series R to a minimum of 100Ω. This resistance should be kept as low as possible to minimize input voltage offset, which will also be subject to drift over temperature. For this reason, they should be kept below 1kΩ. Note that the error due to input bias currents on the front end of the AFE is directly proportional to the value of the resistors. The voltage measurement error can be calculated as:

$$voltage\ measurement\ error = 2 \times R \times I_{SENSE}$$

2. Together with the capacitors on each input, they provide an RC filter for high-frequency noise on the AFE inputs.

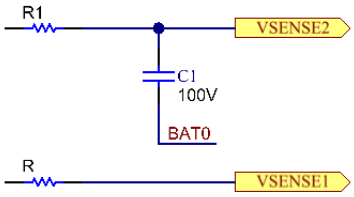

Figure 4 - Cell Input Single Ended Nyquist Filter

The tuning of this filter cutoff is up to the customer and the noise, which may be present in the end application. A minimum 0.1uF capacitor is typically selected, connected to GND (BAT0). The cutoff frequency can be calculated with the following equation:

$$fc = \frac{1}{2\pi R1C1}\ Hz$$

3. For applications that require a very low filter cutoff frequency, a differential capacitor can be used to provide the bulk of the AFE input filtering.

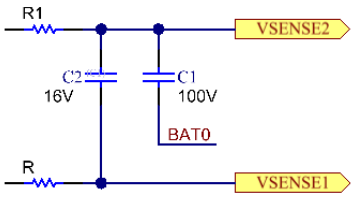

Figure 5 - Cell Input Differential Nyquist Filter

The cutoff frequency can be calculated with the following equation:

$$fc = \frac{1}{2\pi 2R1C2} Hz$$

4. Keep low-pass RC filter components close to the IC wherever possible, especially the capacitors.

2.4.4.3 EMC Susceptibility on Cell Inputs

Extra components are necessary to improve EMC performance in automotive applications in electrically noisy environments.

- Use ferrite beads or small inductors in series with the cell inputs. The bead and small capacitor should be located near each other.
- Add a 0.0033µf capacitor from each cell input to the VSS (cell1-) of that IC. This value may need adjustment for your PCB layout and field conditions.

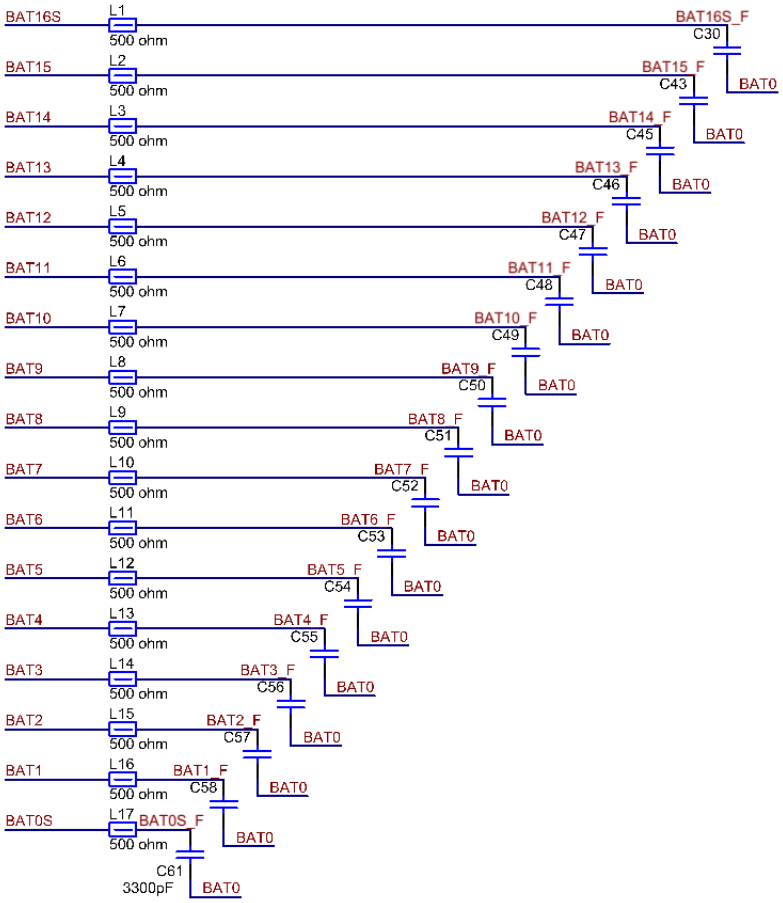

Figure 6 - EMC Filter on Cell Inputs

2.5 Power Supply Requirements

2.5.1 NPN circuit

The NPN Transistor should be selected based on the following criteria:

1. Collector-Emitter Breakdown Voltage ($BV_{CEO)}$ > 100V (or whatever the module voltage is plus any derating)
2. DC gain (β or ~= to hfe (AC gain)) > 100 at the expected load current (a few mA)
3. Collector-base capacitance < 35pF at typical base voltage range
4. Power handling > 500mW (this is assuming we have 1k resistance in series with the collector)
5. Current handling > 100mA

The series resistors R163 and R164 in Appendix C, Figure 26 serve several purposes:

1. They act as a means to limit the current in the event of a fault.
2. They are also used to shift some constant power dissipation in the regulator away from the transistor onto the resistor.
3. They also combine with the input capacitor on the transistor collector to serve as a filter.

The typical calculation used looks like:

$$R\ max = \frac{(\min module\ voltage - (VP_{MAX} + V_{CE\_SAT}))}{\max expected\ transistor\ current}$$

Where V_{CE_SAT} = V_{CE} min at $V_{BE(on),}$ from transistor datasheet.

Allowing for the lowest possible module voltage (V_{BAT} min) of 16V, using VP max = 5.5V, V_{CE_SAT} = 0.25 V (from transistor datasheet) and max load current (bq76PL455-Q1 I_{ACTIVE} max + any additional load connected to VP) ~=7mA, results in R max = ~1.464kΩ.

The R78 and R80 series resistors in the VDIG and VIO supplies (respectively) are present to help to isolate large load capacitance from the voltage regulator to help with loop stability.

The filter on the VP supply (R23 and C36) should have a small resistance on the order of 390mOhm if a ceramic cap is used. This is needed for stability.

2.5.2 Handling of Supplies in Shutdown Mode

If the NPN circuit is not used (external supply), VP and VDIG should be turned off immediately after entering shutdown mode. Lowering VP and VDIG will also put the device in shutdown mode.

While in shutdown mode, VIO and any other external supply indirectly connected to the communication, fault, GPIO and AUX inputs should also be turned off or disabled to avoid back powering of the device via internal ESD structures. The bq76PL455-Q1 will immediately go into reset when VIO is lowered. In version pg4.0, if VIO is held low for ~5 seconds the device will enter shutdown mode.

2.6 bq76PL455-Q1 Circuit Schematic

The schematic for the bq76PL455-Q1 is provided in Appendix C, Figure 20 for Single Ended Communications and Appendix Figure 21 for Daisy Chain Communications.

2.6.1 AFE Output RC Filter

The bq76PL455-Q1 AFE output has RC filter circuit comprised of an internal 1kΩ series R, and an external capacitor on the OUT1 pin (C44) can be added to form a simple first order RC filter to provide a limited amount of noise filtering before the signal is converted by the integrated ADC. Each input channel is converted sequentially according to the channel conversion time, e.g. ADC_PERIOD_VOL, programmed in register 62 (see bq76PL455-Q1 datasheet), and the OUT1 line must change quickly and settle to the new measured channel value within this time period. The RC filter, while reducing noise, slows the settling speed of the OUT1 line to the ADC and so must be selected with care. Too big an external capacitor will not allow the OUT1 line to settle to the required accuracy within the programmed channel conversion period.

Ideally to maximize measurement accuracy the AFE output should be allowed to settle to within <1/2 of the ADC LSB. As a worst case, the AFE output could have to move the full-range that is possible in the system, for example, 4.2V when there are extreme imbalance conditions, or there is a broken cell sense connection. In more typical conditions where cell-to-cell variation will only be within 100mV, the AFE output will not need as much time to settle as a new channel is selected. The required value of C can be calculated based on the maximum channel-to-channel voltage transition and the actual available settling time, which is dependent on the programmed channel conversion period and oversampling mode if oversampling is programmed.

It is found that a value of 390pF provides best accuracy with 60µS ADC conversion period and 8x oversampling (on the same channel before changing channels – CMD_OVS_CYCLE = 0).

For help in selecting C44 for other sampling periods and modes and when it is desired to sample a mixture of channel types, e.g., temperature, internal test voltages as well as external cells please contact the factory via your FAE.

2.7 Voltage Reference

A decoupling cap (sum of C60 and C39 in the schematic in Appendix C, Figure 20 or Figure 21) of no greater than 2µF, with minimum temperature stability rating of X7R (COG/NPO are even better).

2.8 Balance FET

The Balance FET should be selected based on the following criteria:

1. The V_{DS} should be considered and depending on derating requirements selected based on stack voltage.
2. V_{GS} should be selected so that it is large and preferably have ESD protection from gate to source. This will protect the part during hot plug.
3. The V_{GS} threshold should be of concern only if the discharge resistors are going to be turned on at low battery voltages.

The 2V7002K is suggested because of its $60V_{DS}$, $+/-20V_{GS}$, and the gate ESD protected with an internal zener diode.

R_{DS} value is of little consideration with the discharge currents for this application.

Power dissipation of the FET will be a function of discharge current selected and the resistance value of FET at that worst-case condition, usually at hot temperature. I^2R will be the power dissipated. Take caution in selecting size if using very small packages.

The V_{GS} resistor is placed there to make sure that the gate of the FET is turned off and does not float into a linear or on state causing excessive leakage currents on that cell in case of FET failure or PCB open.

A series resistor between the EQ pin and the FET gate should be in place to limit current going into the FET during hot plug or other transient events.

2.9 Balance Resistor

The balance resistor should be selected to set the desired balance current. If present, the resistors in series with the cell connections (top and bottom, in front of the zener diode) should also be included in this calculation. These resistors will need to be sized appropriately to handle the thermal dissipation of continuous cell balancing.

2.10 WAKEUP Pin

The WAKEUP pin should have a pull-down to ensure it is not left to float high to cause an unintended wakeup (active high).

2.11 Single-Ended Communication

When the device is connected to a host controller via the Single-Ended Communication interface (UART), there are few requirements:

1. COMML- should be connected by 100k pull-down to DGND.
2. COMML+ should be connected by 100k pull-up to V5VAO.
3. FAULT_N should have a 50k pull-down to make sure a fault is generated when VIO is not present. The pull-down on the FAULT_N helps to notify the host controller in the case of an inadvertent shutdown. If this is not desired then a pull-up can be used.
4. TX and RX should be pulled-up to VIO via 100k and not left to float. The TX is pulled high because the idle state of TX is high and if allowed to float could falsely trigger a fault by causing what looks like an invalid communications frame. If a serial cable is used to connect to the host controller, the TX pull-up should be on the host side and the RX pull-up should be on the bq76PL455-Q1 side.

2.12 Daisy-Chain Communication

When the device is connected via the Daisy-Chain Communication interface only (Single-Ended interface not used) there are few requirements:

1. FAULT_N should have a 50k pull-down to make sure a fault is generated when VIO is not present.
2. TX and RX should be pulled-up to VIO via 100k and not left to float.

2.12.1 Stacked Devices on Same PCB

The recommended circuit is as defined in Figure 7 below.

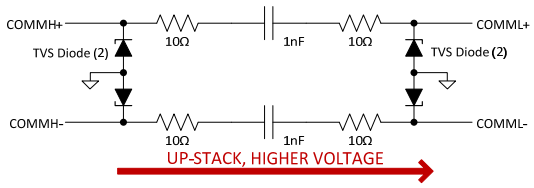

Figure 7 - Components required for Daisy-Chain Communication between Devices on same PCB

2.12.2 Stacked Devices Separated by Cables

The recommended circuit is as defined in Figure 8 and Figure 9 below.

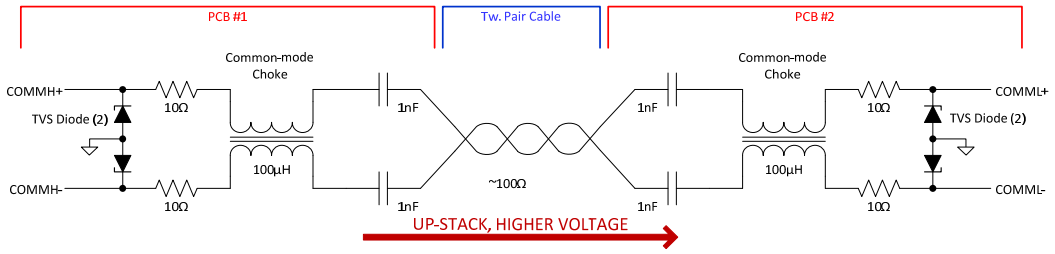

Figure 8 - Components required for Daisy-Chain Communication between PCBs

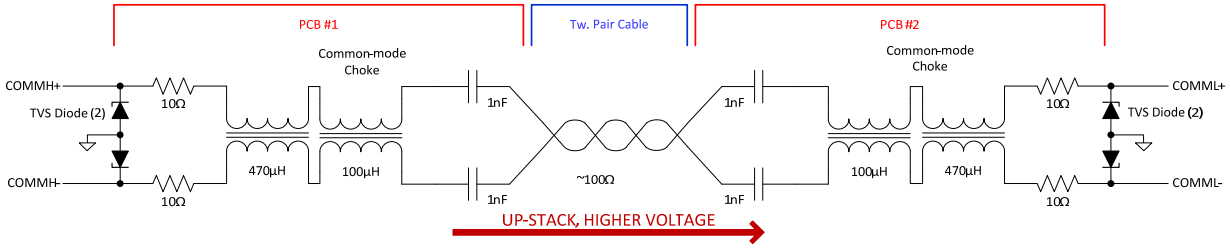

Figure 9 - Components required for Daisy-Chain Communication between PCBs in noisy environments

2.12.3 TVS Diodes

The daisy chain communication TVS diodes are required for protection of the communication interface signals during hot-plug events and also for absorption of high-voltage transients in operation.

The daisy chain communication TVS diodes should be selected for the lowest possible capacitance as they can affect the rise-time of the communications signal. The NXP PESD5V0U1UA is used on the reference design, which has a max C_d of 2.6pF.

2.12.4 Resistance

It is recommended that the total resistance of each COMML+/-, COMMH+/- or FAULT_N+/- signal is no more than 20Ω (10Ω on each end of the signal connection between bq76PL455-Q1 devices). This series resistance is required to limit in-rush current in a hot-plug event.

Using the cable described in the section above, the contribution to the total resistance in the COMML+/-, COMMH+/- or FAULT_N+/- signals by the wire is ~25mΩ/ft.

2.12.5 Common-Mode Filter

It is recommended at a minimum to use an automotive grade 50–100µH common-mode filter. To achieve the best performance in noisy environments, dual common-mode filters (100µH and 470µH) should be utilized.

For single common-mode filter applications, a TDK 51µH 2.8kΩ choke (part number ACT45B-510-2P-TL003) is recommended. This device has an input capacitance of ~18pF.

For dual common-mode filter applications it is recommended to use a TDK 100µH 5.8kΩ choke (part number ACT45B-101-2P-TL003) and Wurth 470µH 2.2kΩ (part number 74242471). The total capacitance is ~40pF.

2.12.6 Isolation Capacitor

The differential signal lines are isolated between IC's by a DC blocking capacitor. The capacitor is typically rated at a minimum of 2x the stack voltage to provide plenty of standoff margin in the event of a fault in the system, which may expose the IC to a local hazardous voltage. One capacitor is sufficient for the normal operation of the IC. The system designer may elect to use two capacitors, one at each end of the cable or PCB wiring, for and additional safety factor. In this case, the capacitor value is doubled from the normal requirement such that the two capacitors in series result in the same value in the signal path.

The recommended value is a minimum of 1nF, with +/-10% or better tolerance with a voltage rating appropriate for the application. In noisy environments, a 2nF value is recommended.

2.12.7 Daisy-Chain Communication Cables

There are specific requirements for the captive load and resistance that can be supported by the bq76PL45-Q1 COMML+/-, COMMH+/- or FAULT_N+/- pins.

2.12.7.1 Daisy-Chain Capacitance Load

The communication cables should selected/designed so that the total sum of capacitance on any COMML+/-, COMMH+/- or FAULT_N+/- signal (between ICs) is no greater than 140pF to support the maximum number of stacked ICs.

The capacitance of the cable can be calculated in the equation below.

$$unshielded\ twisted\ pair\ cable\ C = \frac{2.2\varepsilon}{\log\left(\frac{1.3D}{f \times d}\right)}$$

Where:

C = mutual capacitance, pF/ft
Ɛ = insulation dielectric constant (e.g. PVC = 5)
f = stranding factor (e.g. 1 strand = 1, 7 strand = 0.939, 19 strand = 0.970, 37 strand = 0.980)
D = diameter over the insulation, inches
d = diameter of the conductor, inches

The unshielded twisted cable used for bench testing (Alpha Wire 3050 series, Digi-Key part number A2015W-1000-ND) had the following specifications:

Ɛ = 5 (PVC)
f = 0.939 (7 strand)
D = 0.056”
d = 0.024” (0.056” – 2 x 0.016” insulation thickness)
conductor DCR = 25Ω/1000ft

∴ resulting in capacitance of ~21.6pF/ft.

An automotive-grade unshielded twisted cable designed for CAN is a better choice. Waytek SAE J1939/15 CAN data bus cable is ~17pF/ft.

The input capacitance presented by the common-mode filter (see Section 2.12.3) should also be included in the total capacitance budget. Only one TVS diode is used as they are connected to both sides of the differential pair.

$$allowable\ cable\ length\ in\ ft = \frac{140pF - 2 \times common\ mode\ filter - 1 \times TVS\ diode\ capacitance}{cable\ capacitance/ft}$$

3 bq76PL455-Q1 PCB Layout Guidelines

To ensure the best possible accuracy performance, it is recommended to follow some basic layout guidelines for the bq76PL455-Q1 to provide best EMI and BCI performance.

An unbroken ground plane layer as part of a 4 or more layer board is recommended, with all AGND, DGND, CGND connections (listed below) made directly to the plane. The common GND planes are star connected directly to BAT0. There should also be a keepout area on plane area adjacent to the isolation capacitors if daisy-chain communication is implemented.

AGND1 – power section (noisy GND)
AGND2 – GND for Front end output
AGND3 – GND for ADC input
DGND1, DGND2, DGND3 – Digital GND
CGND – Communications digital GND

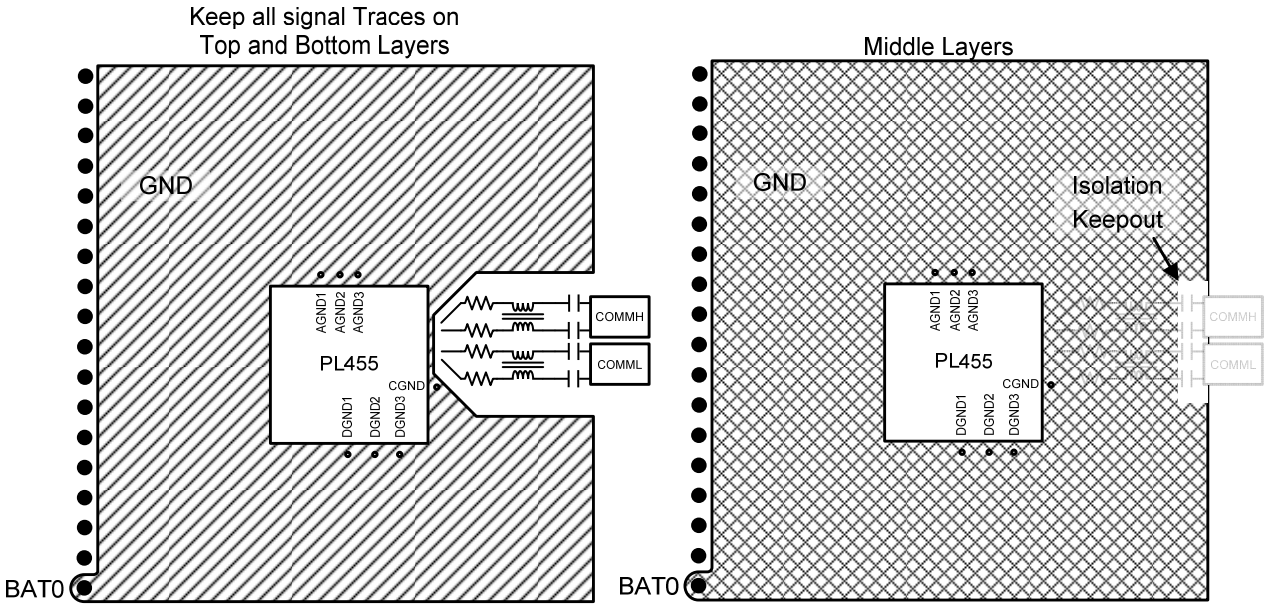

Figure 10 - Simplified Layout Guideline

3.1 Device Placement

The isolation caps should be placed close to the edge of the board. The Common Mode Chokes should be close to the daisy-chain cable connector to provide a high impedance path to common mode noise as it enters the board. The series resistors and TVS diodes can be place next to the bq76PL455-Q1.

4 System Architectures

The bq76PL455 can be used in a system several different ways. This document will describe the known ways a bq76PL455 can be used in a battery pack.

4.1 Single IC

Figure 11 below shows a single bq76PL455 interfaced with a microcontroller.

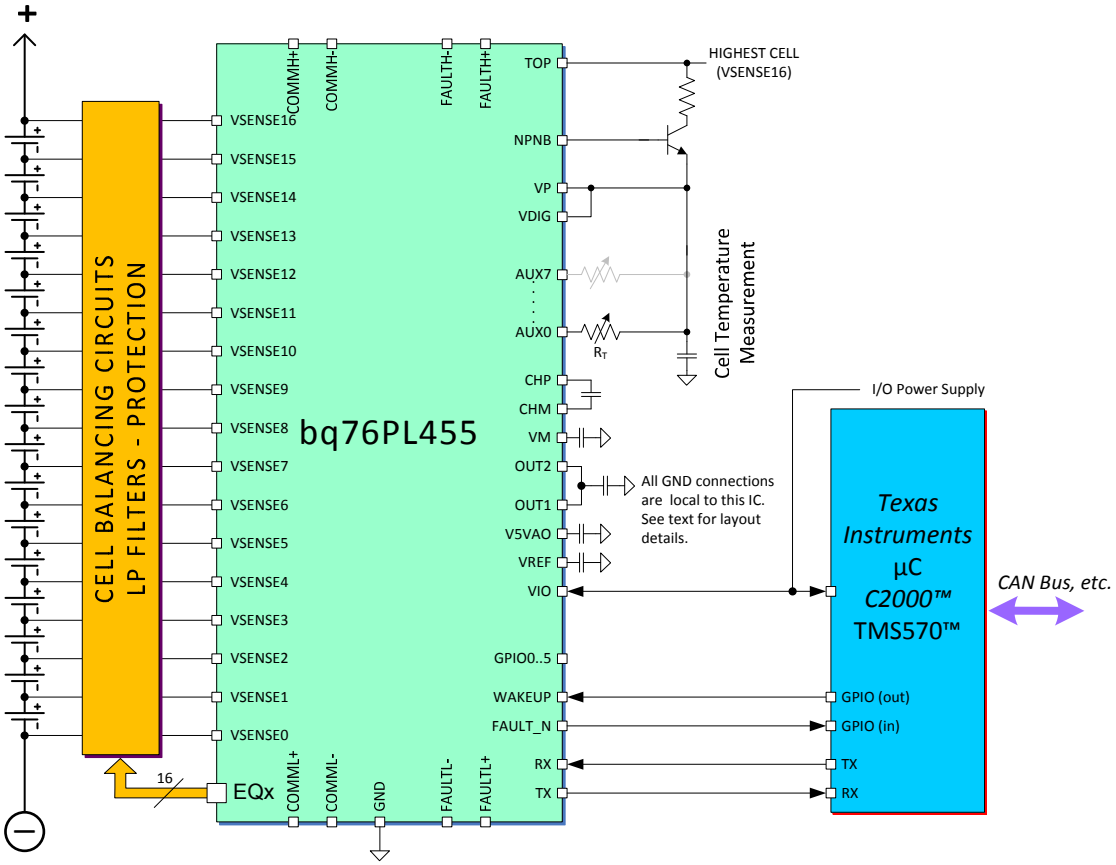

Figure 11 - Single Board

4.2 Stacked ICs

4.2.1 Multi-Drop

The bq76PL455 can be connected in a multi-drop configuration, with a microcontroller local to each module as shown in Figure 12.

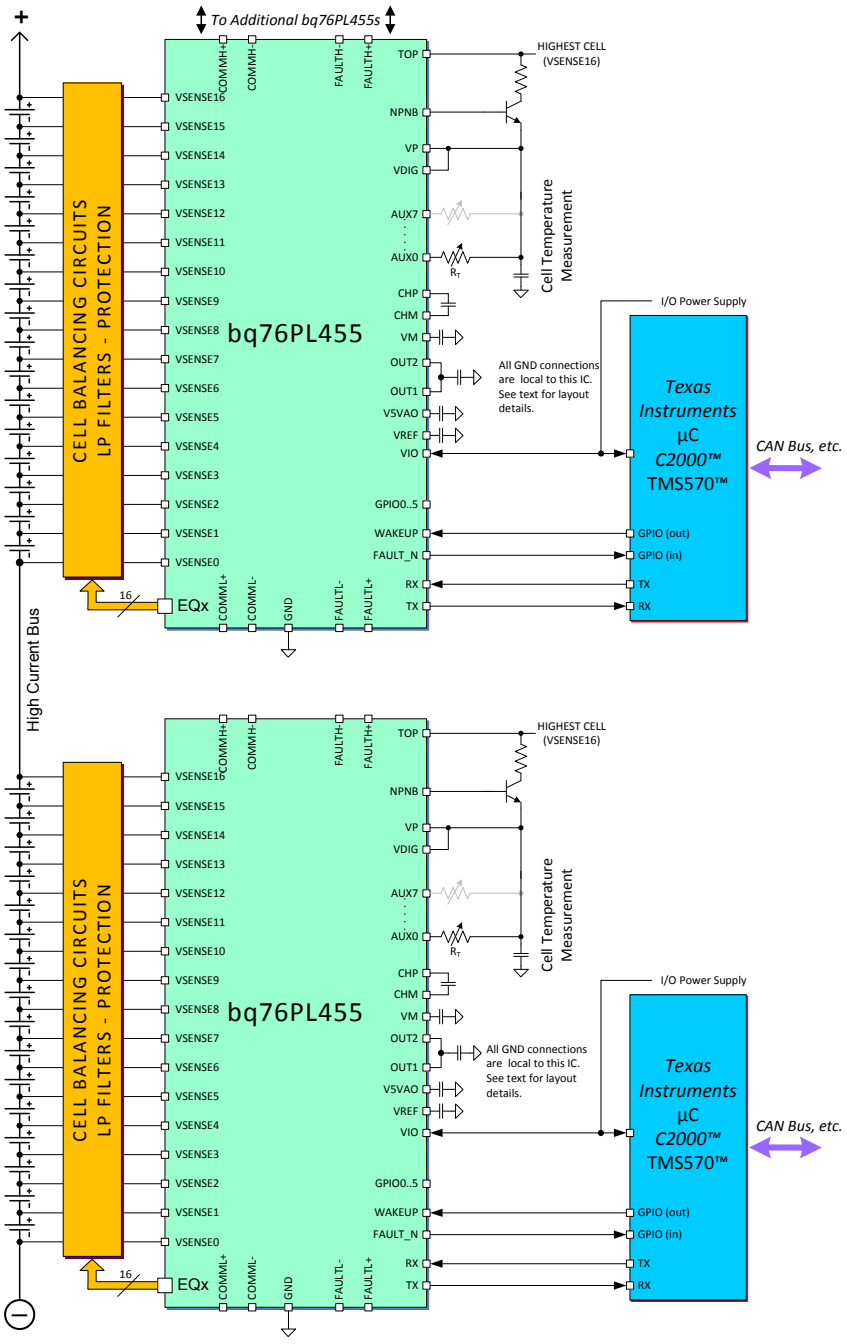

Figure 12 - Multi-drop System Architecture, local microcontroller

4.2.2 Daisy-Chain

The bq76PL455 can be connected in a daisy-chain configuration as shown in Figure 13.

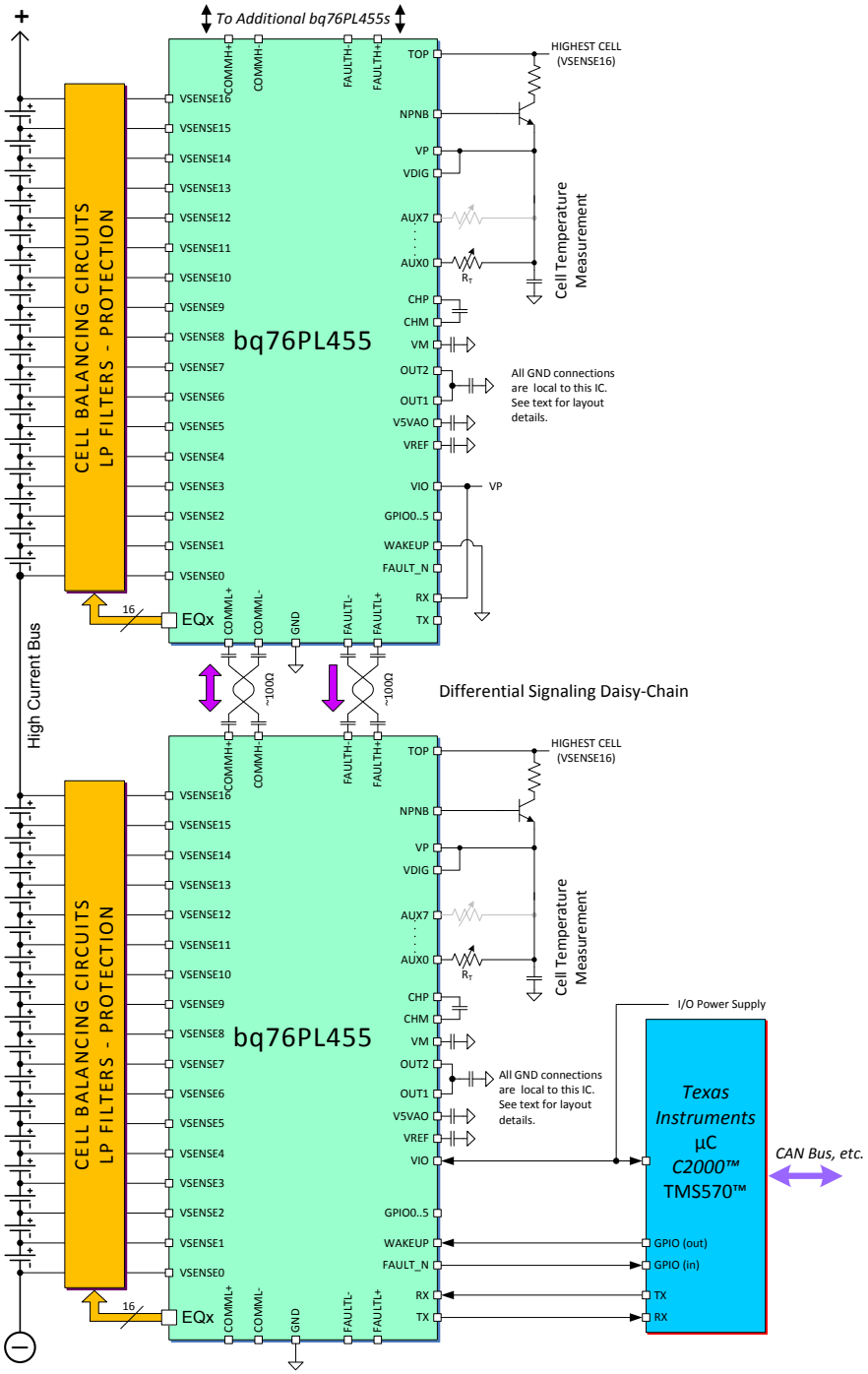

Figure 13 - Daisy-chain System Architecture, without bridge

4.3 External Supply

It is possible to provide an external supply source local bq76PL455 circuit operation. An example system diagram is shown in Figure 14. The internal regulator should be disabled by setting REG_DISABLE = 1 in DEVCONFIG register (address 14).

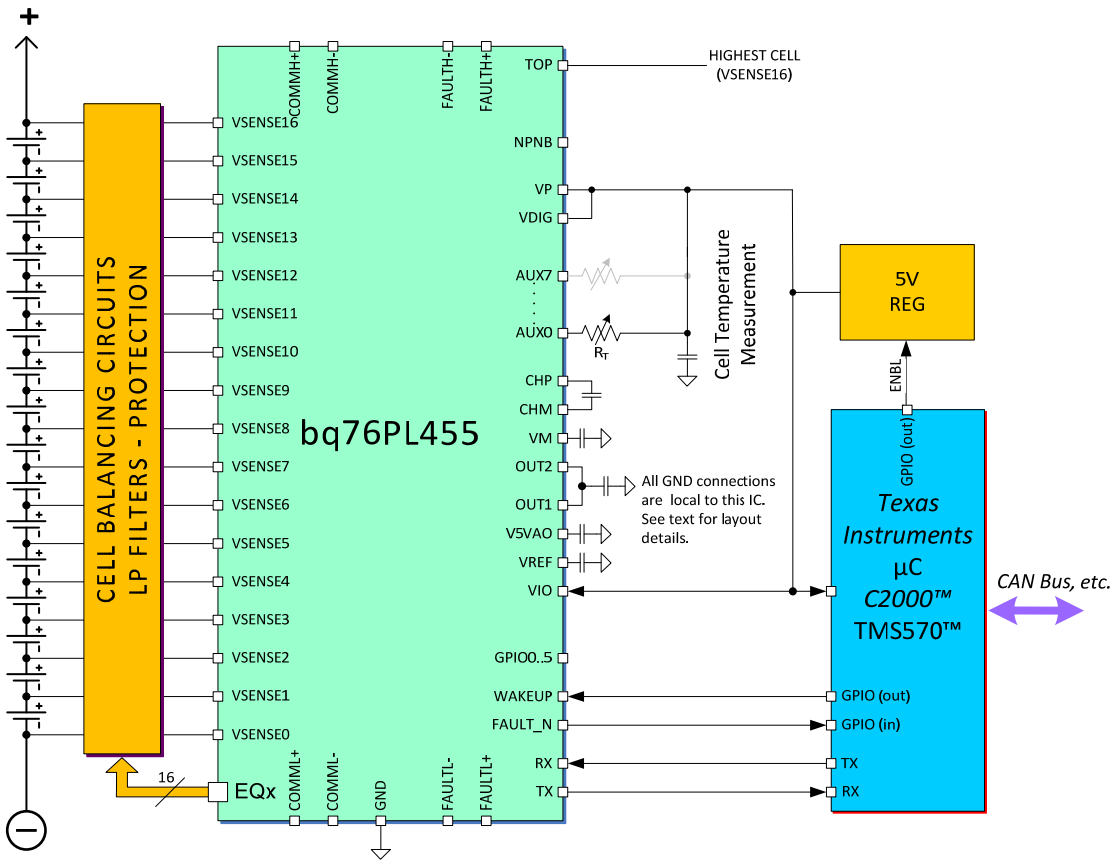

Figure 14 - External supply

4.4 Reduced Cell Count

Minimum VSENSE16, TOP voltage = 16V, so number of cells is dependent on cell operating range. In the example below, 12 cells are connected.

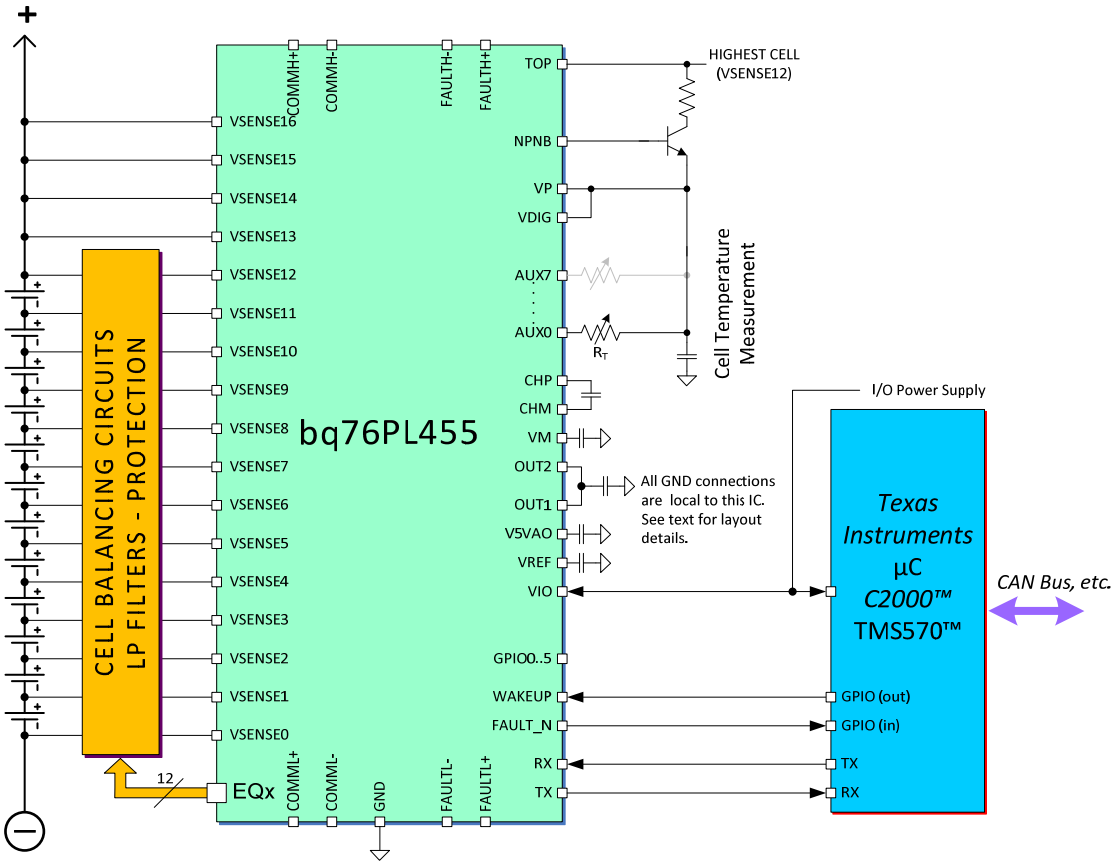

Figure 15 – Minimum Cell Count

4.5 Active Balancing

14 cell Active Balance is shown below with the addition of the EMB1428 and EMB1499 ICs.

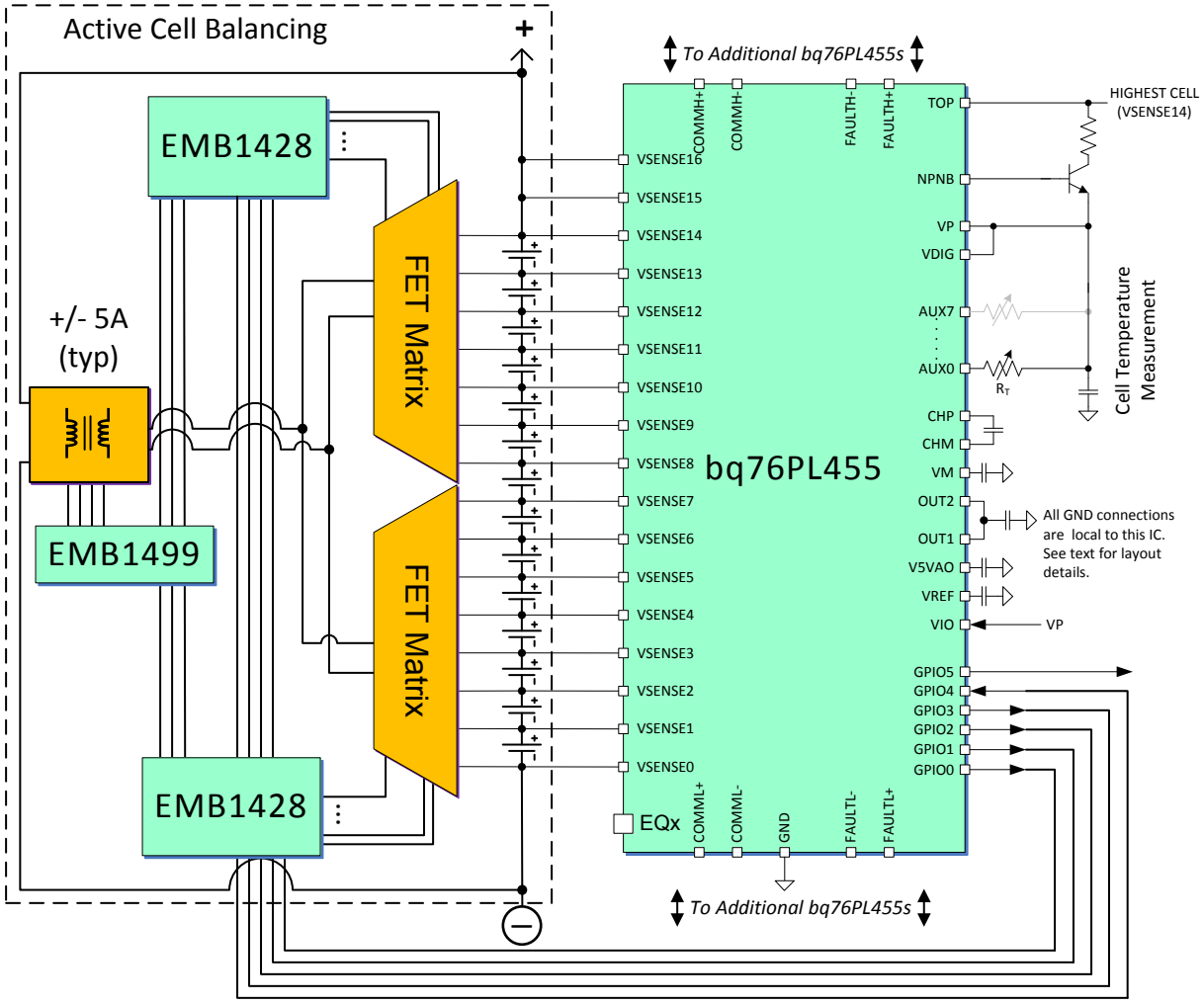

Figure 16 - Active Balancing

4.6 Using the bq76PL455 as a Communications Extender Bridge

The bq76PL455 can be used as a communications bridge or extender. In this mode, it is not used to measure or balance cells, although the AUX ADC inputs may be utilized for local temperatures, diagnostics, etc. The main purpose of the device in this mode is to translate the single-ended UART communications and signals from the microcontroller to differential signals suitable for communicating over relatively long distances in a noisy environment. The device is translating the UART TX/RX and FAULT_N signals and bit formats to the differential signals used by the COMMx and FAULTx differential pairs.

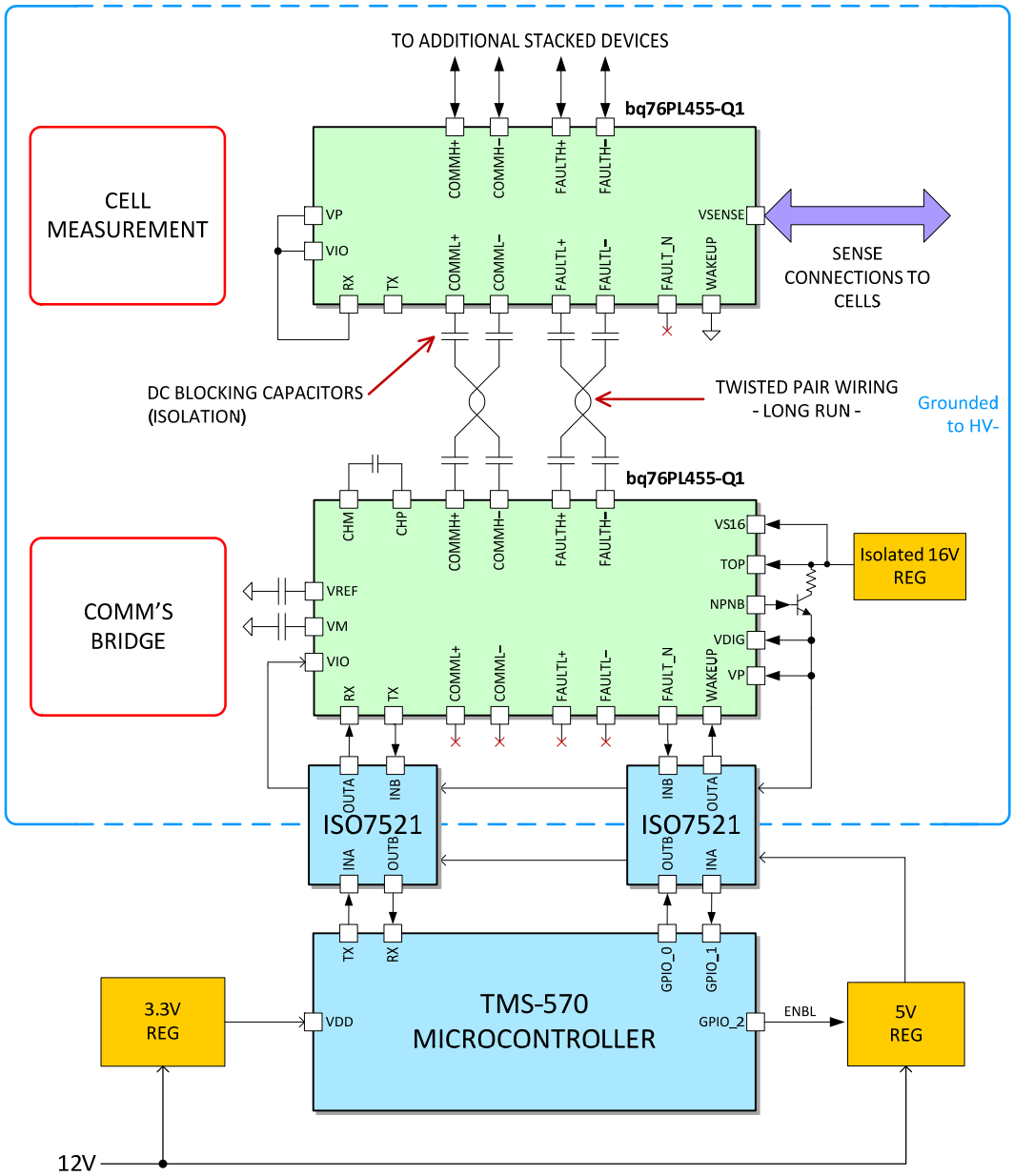

Figure 17 – Communications Bridge

The GPIO pins are also available in this mode, making the part useful as an I/O expander to control local circuits or devices.

In this mode, typical connections are:

1. VSENSE inputs should be connected as shown in the schematic in Figure 22 - bq76PL455-Q1 Schematic (Communications Bridge)
2. The TOP pin is tied to 16V supply.
3. The VM, CHM and CHP pins are usually left floating.
4. VP, VDIG and V5VAO are connected together and supplied the NPN regulator or external with regulated 5V.
   Note – If the AUX channels are used for measurements, the maximum voltage that can be measured is limited by VP, which may reduce the measurement range.
5. VIO is externally supplied with the same rail as the microcontroller it is sharing signals with, usually 3.3V or 5V.
6. All power supplies and VREF are bypassed as recommended in the pin list.
7. COMML+ is pulled up, COMML- is pulled down (see pin list for recommendations).
8. COMMH+/- are tied to the COMML+/- pins of the bottom IC monitoring the stack of cells with capacitors per recommendations (see.

Table 2 - Typical external supply voltages in Communications Bridge application

Supply Pin	Nominal Current (3)(4)	Externally Regulated Voltage (1)			
		Min	Typ	Max	Units
TOP	0mA	16		80	V
VP (2)(3)	10mA	4.75	5	5.3	V
V5VAO		4.75	5	5.3	V
VDIG		4.75	5	5.3	V
VIO (4)	20 µA	3.3 ±5%		5V ±5%	V

(1) With respect to VSS (AGND2-3, DGND).

(2) AUX pin measurements are limited to the supplied VP voltage.

(3) IC current only. Current used by externally connected devices i.e. thermistor loads, must be added to this value.

(4) IC current only. Current used by externally connected devices i.e. GPIO loads, pull-up resistors, etc. must be added to this value.

5 Appendix A

5.1 Interface Signals

Signal	Pin	Description	Type
WAKEUP	49	Single-ended wake up signal from host to bq76PL455	Input to bq76PL455
RX	39	Single-ended transmit from bq76PL455 to host	Input to bq76PL455
TX	38	Single-ended transmit from bq76PL455 to host	Output from bq76PL455
FAULT_N	40	Single-ended active low fault output to host	Output from bq76PL455
FAULTH+	57	Differential (+) input signal to receive fault information from device higher in daisy chain	Input to bq76PL455
FAULTH-	56	Differential (-) input signal to receive fault information from device higher in daisy chain	Input to bq76PL455
FAULTL+	50	Differential (+) input signal to communicate fault information to device lower in daisy chain	Output from bq76PL455
FAULTL-	51	Differential (-) input signal to communicate fault information to device lower in daisy chain	Output from bq76PL455
COMMH+	55	Bi-directional differential (+) input/output signal to communicate information to device higher in daisy chain	Input/output on bq76PL455
COMMH-	54	Bi-directional differential (-) input/output signal to communicate information to device higher in daisy chain	Input/output on bq76PL455
COMML+	52	Bi-directional differential (+) input/output signal to communicate information to device lower in daisy chain	Input/output on bq76PL455
COMML-	53	Bi-directional differential (-) input/output signal to communicate information to device lower in daisy chain	Input/output on bq76PL455

5.2 Optional Interface Signals

These are extra signals, which may be necessary for additional optional features such as temperature sensing or power supply control.

Signal	Pin	Description	Type
AUX0..7	66..59	Auxiliary input signal to bq76PL455, typically used to monitor NTC temperature sensors	Analog input to bq76PL455
GPIO0..5	47..42	General Purpose Input/Output pins. Internal pull-up or pull-down resistors may be enabled using register controls. When configured as inputs, pins may be programmed to generate faults when pin transitions to either a high or a low logic level.	Digital I/O on bq76PL455

6 Appendix B

6.1 Power Supply Rails

The supplies listed below are separate power supply rails or planes and the respective pin connections on the bq76PL455. Please refer to the system schematic for detailed description.

Supply	IC	Signal	Pin	Description
V5VAO	bq76PL455-Q1	V5VAO	58	Always On 5V Output
VP	bq76PL455-Q1	VP	70	5.3V Voltage Input
VM	bq76PL455-Q1	VM	31	-5V Integrated Charge Pump
VIO	bq76PL455-Q1	VIO	41	I/O Voltage Input
VREF	bq76PL455-Q1	VREF	67	2.5V Reference Output
AGND1	bq76PL455-Q1	AGND2	72	VREF and Power Section GND
AGND2	bq76PL455-Q1	AGND1	74	AFE output GND
AGND3	bq76PL455-Q1	AGND3	69	ADC input GND
CGND	bq76PL455-Q1	GND	48	Communications GND referenced to V5VAO
DGND	bq76PL455-Q1	DGND1	30	Digital GND
DGND	bq76PL455-Q1	DGND2	35	Digital GND
DGND	bq76PL455-Q1	DGND3	37	Digital GND

7 Appendix C

7.1 Chipset Schematic

7.1.1 Top Level

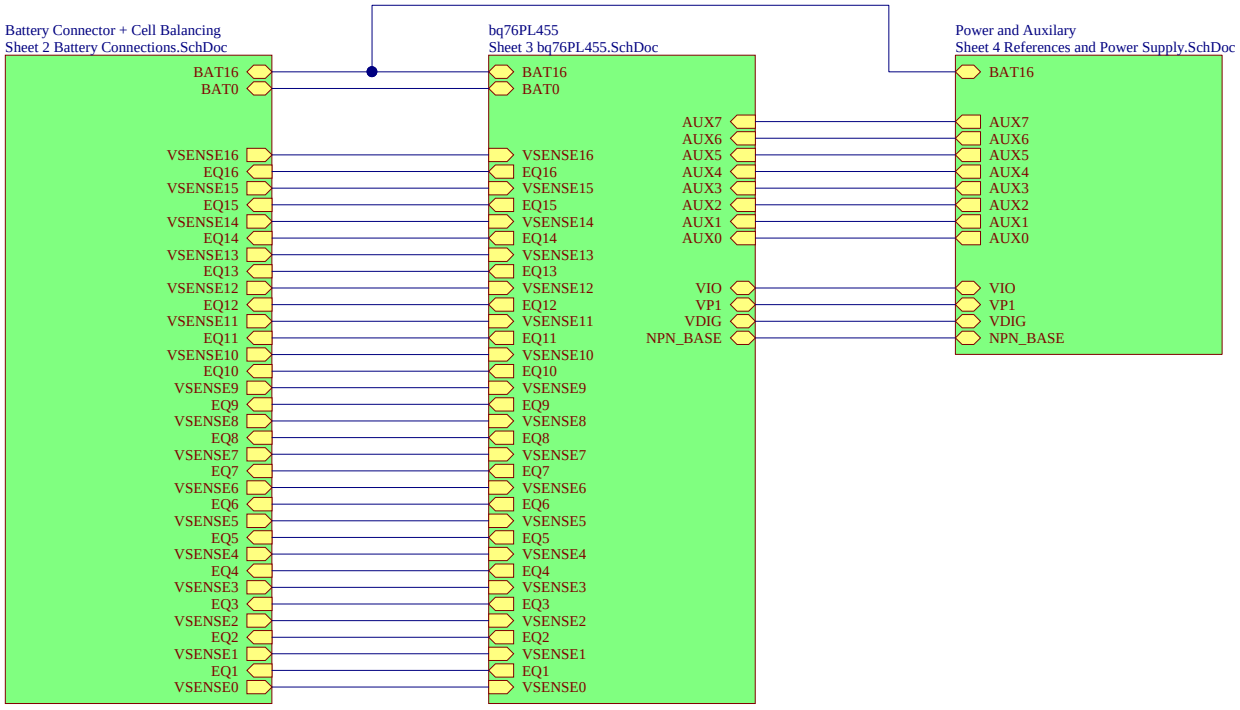

Figure 18 - Top Level Schematic

7.1.2 Battery Connection and Cell Balancing

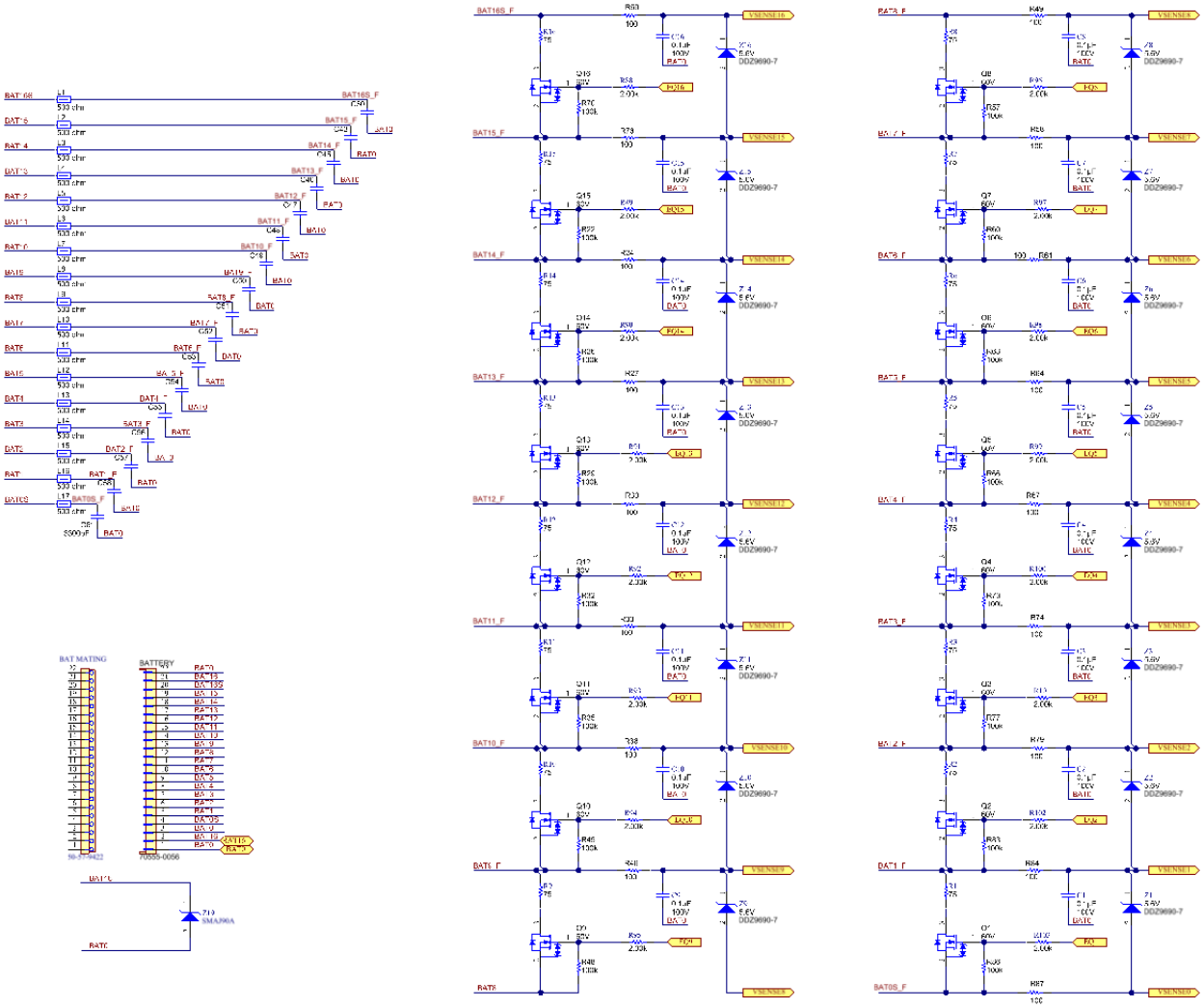

Figure 19 – Battery Connection and Cell Balancing Schematic

7.1.3 bq76PL455-Q1 – Single Ended

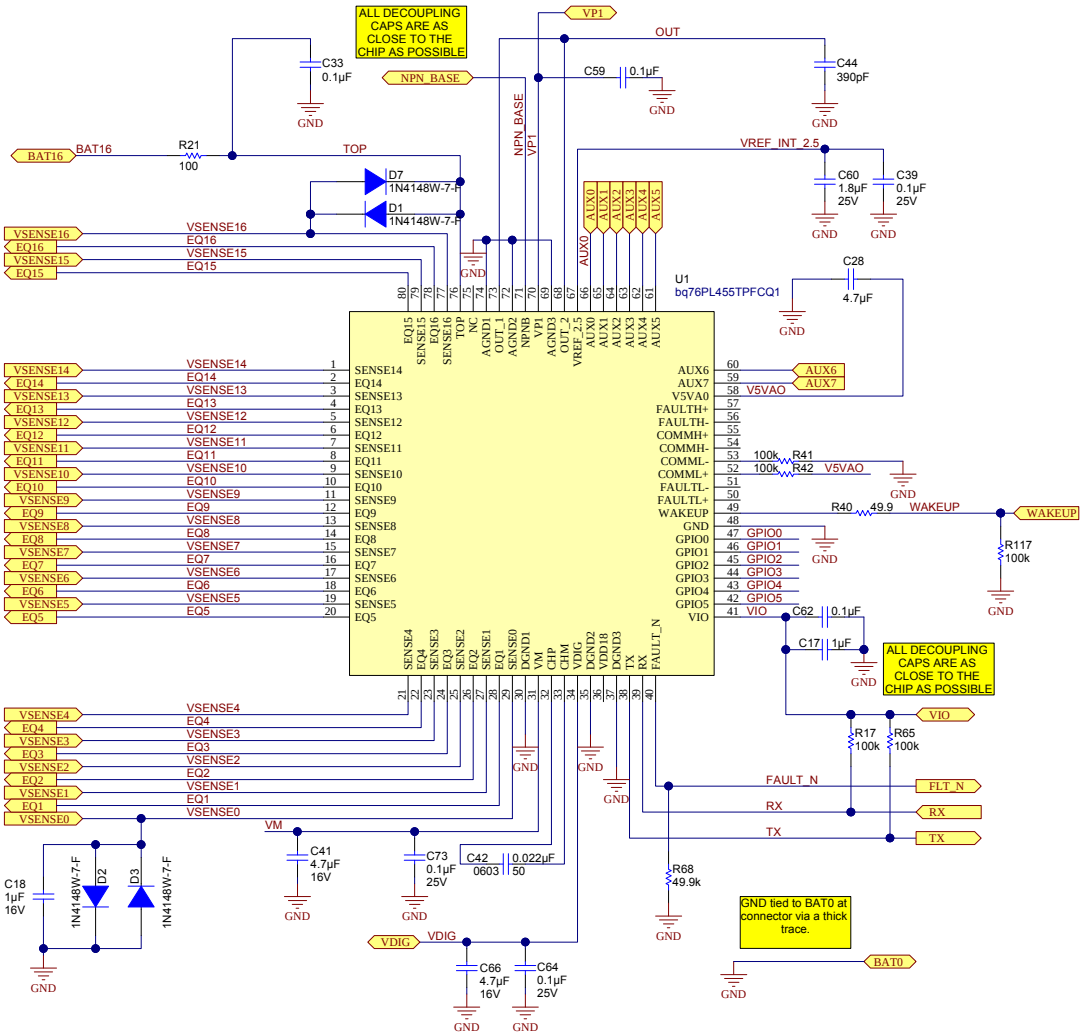

Figure 20 – bq76PL455-Q1 Schematic (Single-Ended Communications)

7.1.4 bq76PL455-Q1 – Daisy Chain

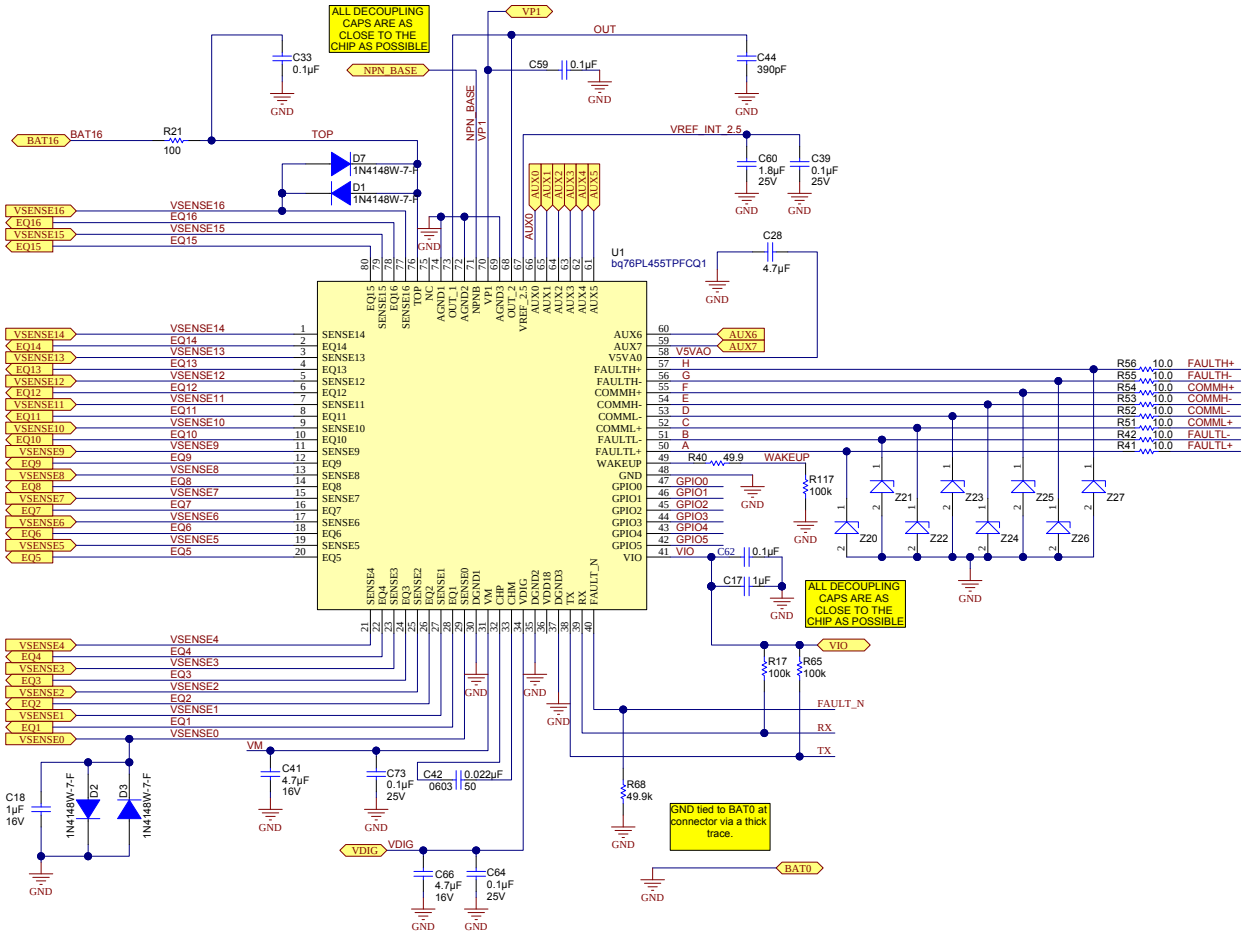

Figure 21 – bq76PL455-Q1 Schematic (Daisy Chain Communications)

7.1.5 Communications Bridge

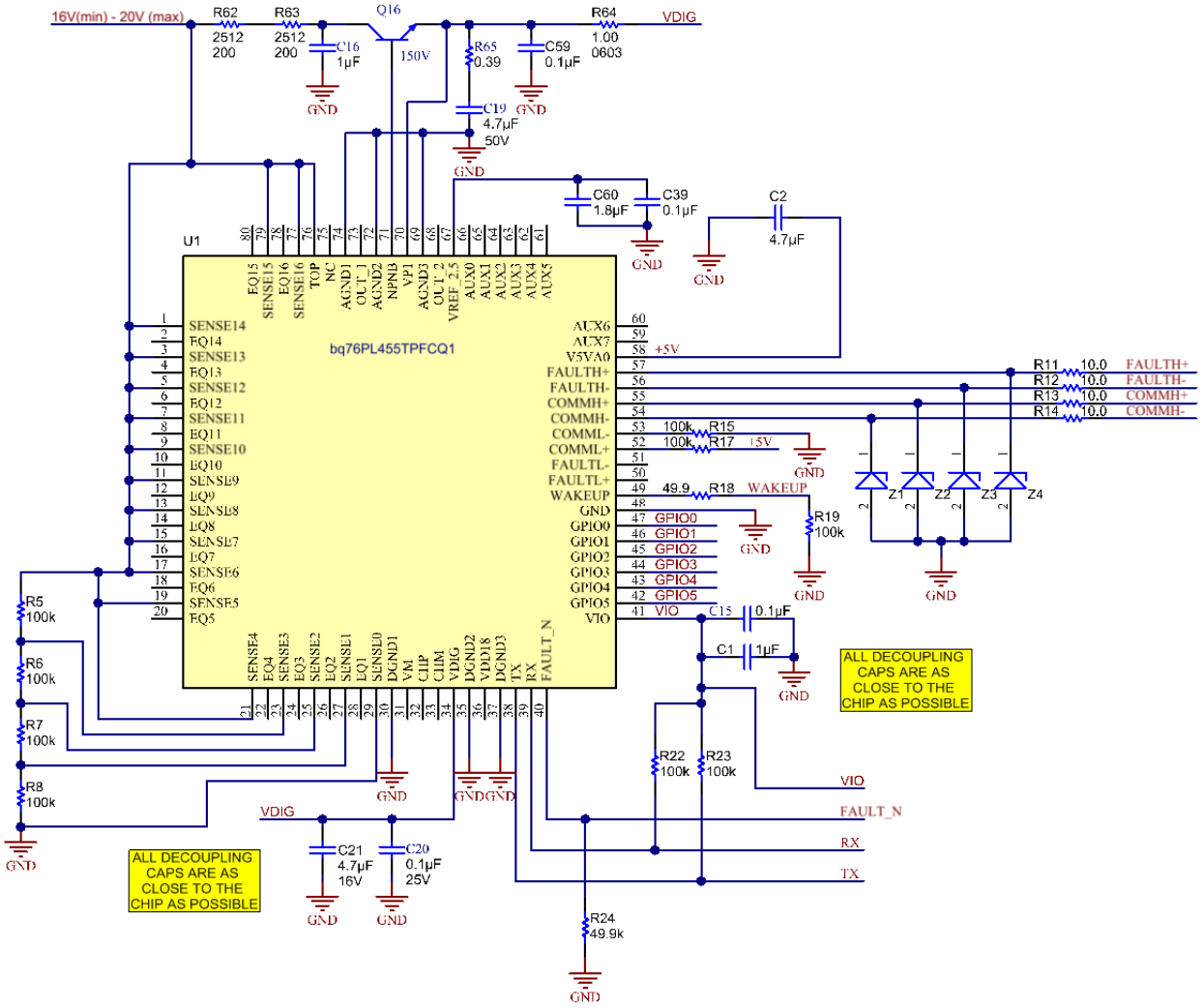

Figure 22 - bq76PL455-Q1 Schematic (Communications Bridge)

7.1.6 Daisy Chain Communications

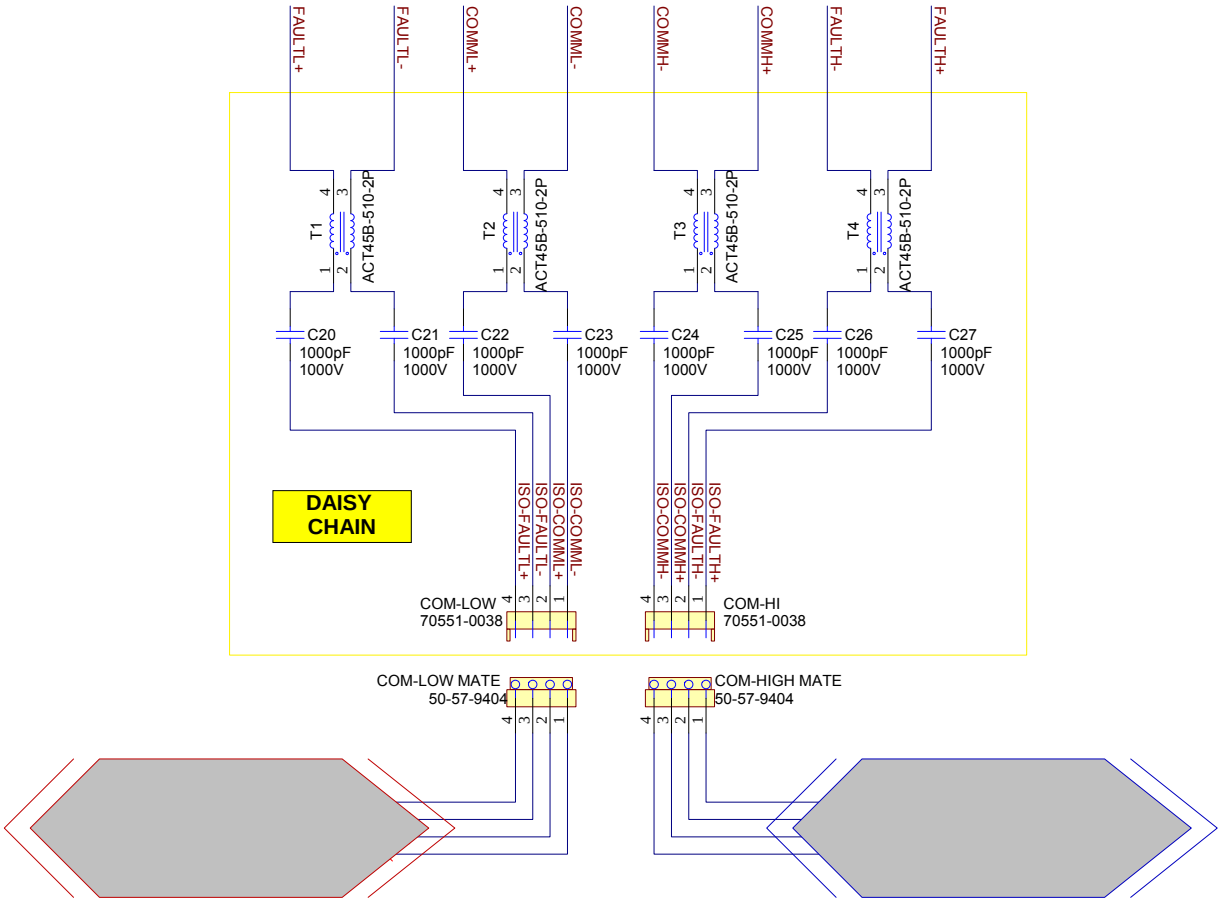

Figure 23 - Daisy Chain Communications Schematic

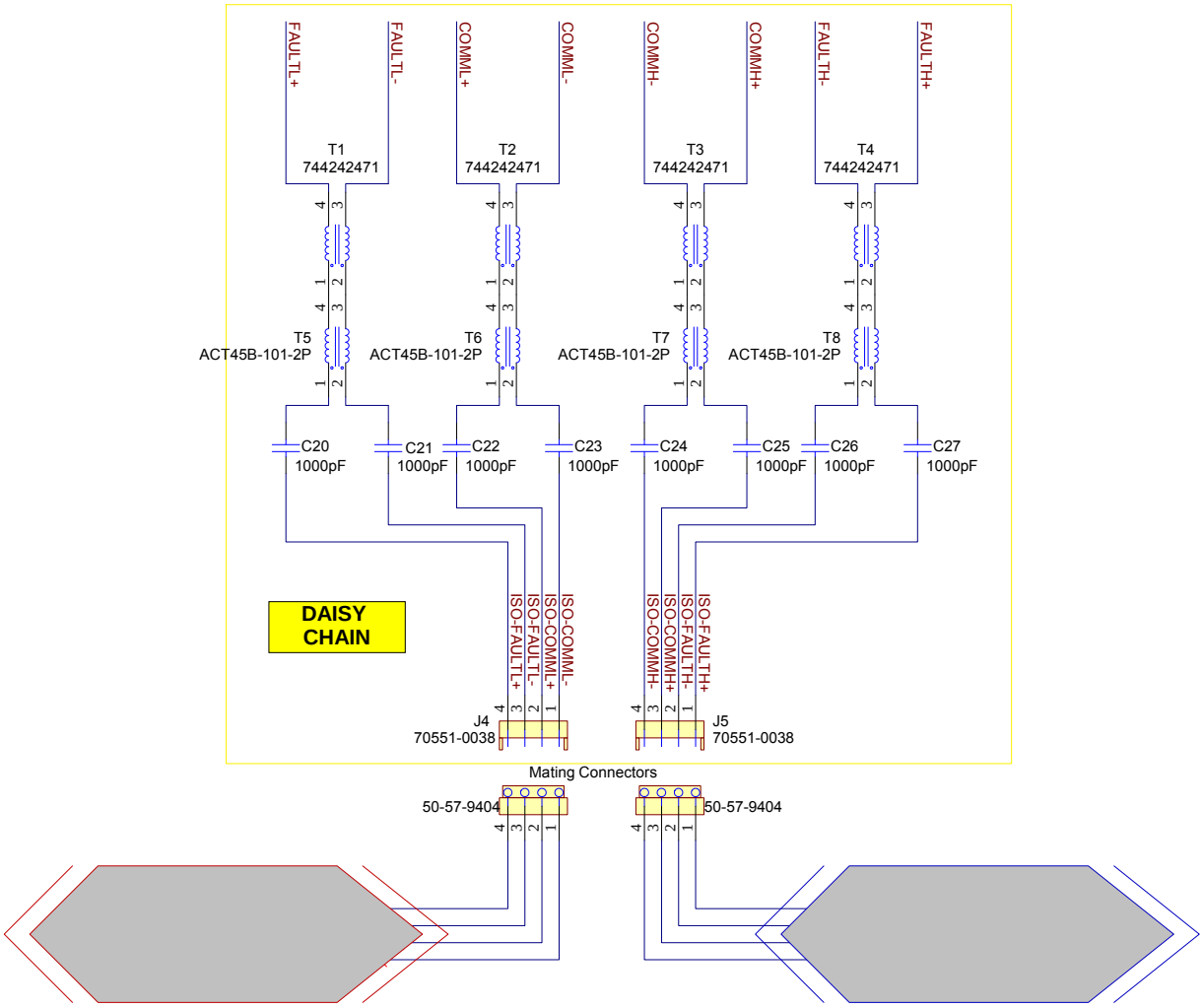

Figure 24 - Daisy Chain Communications Schematic (for noisy environments)

7.1.7 Temperature Sensing

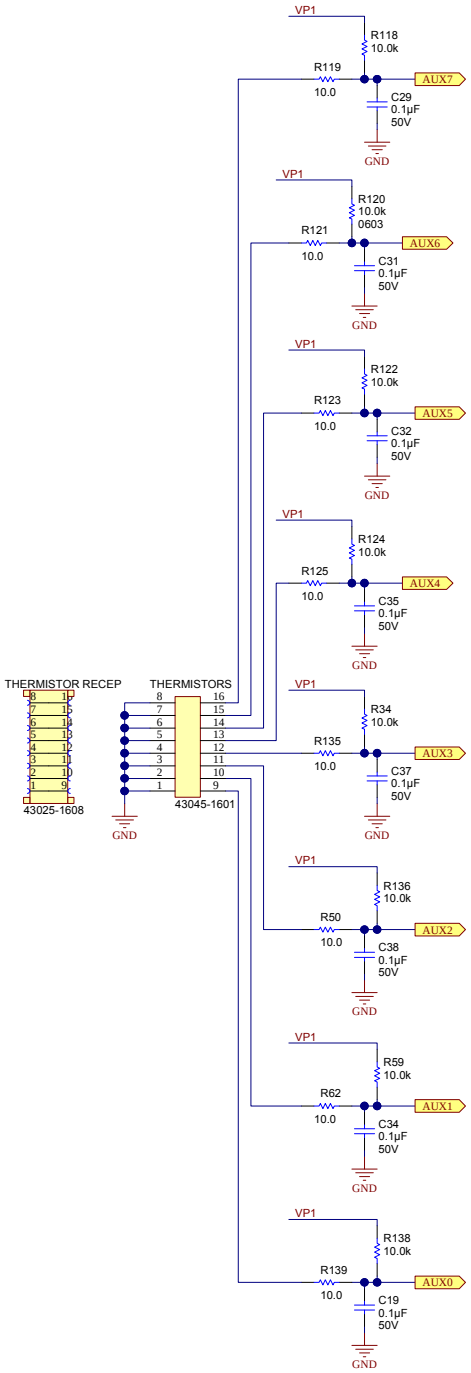

Figure 25 - Temperature Sense Schematic

7.1.8 Power Supply

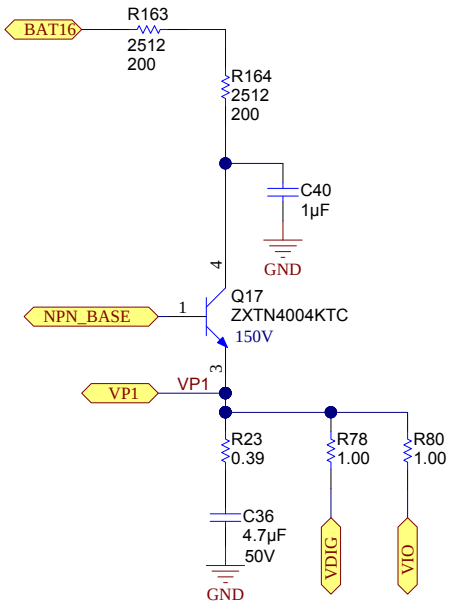

Figure 26 - Power Supply Schematic

8 Revision History

This section records a brief summary of changes to each revision of this document.

Revision	Date	Description of Changes from Previous Revision
1.0	1/18/2013	First release
1.01	1/21/2013	Re-organized Hot-Plug, In-Rush and ESD circuit descriptions to include single module applications. Updated heading formatting. Minor clarification in balance FET selection criteria. Added description of TVS diodes on COMM signals.
1.02	2/20/1013	Fixed mistake in balance FET part number from 2V7001K (mistake) to 2V7002K
1.03	3/07/2013	Added simplified layout guideline diagram
1.04	4/02/2013	Added detail to TVS diode device selection inputs Clarified TOP capacitor value description Updated schematics due to change in FAULT_N pull-down value Values provided for COMM+/-, TX, RX and FAULT_N pull-up/pull-down resistors
1.05	4/02/2013	Clarified TOP capacitor value description
1.06	4/23/2013	Added further description of TX, RX and FAULT_N pull-up/pull-down resistors
1.07	4/25/2013	Added further description of communication cable spec
1.08	4/29/2013	Fixed incorrect cross-reference
1.09	10/23/2013	Added section detailing daisy chain communication TVS diode selection Updated schematics to latest revision Updated layout guidelines
1.10	11/12/2013	Updated recommended ADC settings Updated zener diode position in front end circuit Updated to latest recommended schematics
1.11	12/02/2013	Moved TVS diodes from daisy-chain communication schematic to bq76PL455-Q1 schematic Changed Footer to “NDA Required”
1.12	12/10/2013	Added description of handling supply inputs during shutdown mode
1.13	01/22/2014	Added description of daisy-chain components between devices on the same PCB
1.14	01/27/2014	Added System Architectures chapter Added single board use case
1.15	01/28/2014	Updated cable capacitance recommendation
1.16	01/29/2014	Updated system architecture drawings
1.17	02/04/2014	Updated twisted pair wire color in figure 5 Figure 3 updated
1.18	02/05/2014	Updated extender to show 16V TOP supply requirement
1.19	02/07/2014	Updated extender diagram to show more detail of isolation requirement
1.20	02/10/2014	Updated extender diagram to show more detail of power supply requirement

1.21	02/12/2014	Updated TOP RC filter description with example values Added description of TOP = GND for extender operation
1.22	02/17/2014	Updated TOP cap value recommendation Added TOP to VSENSE16 connection to figure 13
1.23	02/20/2014	Updated figures 4 and 5 to have same look as data manual
1.24	03/24/2014	Added daisy-chain communication device placement recommendations
1.25	04/21/2014	Added guidance for dual common-mode filters in noisy environment Added guidance for achieving very low cutoff frequency filter for AFE, and added equations
1.26	04/22/2014	Changed recommended zener diode for AFE input protection to 6.2V Added daisy-chain schematic reference for dual common-mode filters
1.27	05/04/2014	Modified Figure 17 to show VDIG connection
1.28	09/24/2014	Corrected section 4.3 description of DEVCONFIG[REG_DISABLE] bit for disabling the internal regulator. REG_DISABLE should be 1.
1.29	10/08/2014	Added EMC filters for cell inputs in noisy environments Added figures for Nyquist filters and improved equations
1.30	11/18/2014	Removed DRAFT markings Added Important Notice and changed copyright to 2014
1.31	01/30/2015	*Section 4.6 Using the bq76PL455 as a Communications Extender Bridge*: Updated the first connection, changing "The VSENSE pins are tied to AGND" to "VSENSE inputs should be connected as shown in the schematic in "Figure 22 - bq76PL455-Q1 Schematic (Communications Bridge." Added "Figure 22 - bq76PL455-Q1 Schematic (Communications Bridge."