Project Statement: High-Speed CMOS Frequency Divider

Course: ECE 271 – Digital Integrated Circuits / Measurement and Lab

Academic Year: Fall 2025

Project Weight: 30% of Total Course Grade (30)

Group Size: 5-6 Students

Technology: 65 nm CMOS Process Design Kit (PDK)

1. Objective

The primary objective of this project is to design, and simulate a high-speed CMOS digital frequency divider circuit using the provided 65 nm process design kit. You will apply knowledge of digital logic (D flip-flops), timing constraints, and transistor-level design to achieve the highest possible speed-power efficiency.

2. Deliverable (The Circuit)

Your group must design a **divide by 2 Frequency Divider**

The Core Circuit: A Divide-by-N circuit.

- **Mandatory (Minimum Goal):** A **Divide-by-2** circuit with **input clock frequency = 2 GHz**
- **Bonus: Challenge/Innovation:** Design a **Divide-by-N** circuit where N is an odd number (e.g., N=3,5,...) or a **Dual-Modulus divider** (e.g., Divide-by-2/3, 8/9).

Required Implementation Details:

1. **Logic Style:** report your choice of high-speed logic (e.g., TSPC, CML, or highly optimized Transmission Gate/Static CMOS).
2. **Transistor Sizing:** All transistors size (W/L ratio)

3. Performance Metrics (Competition)

Your design will be evaluated competitively based on the following three metrics:

1. **Functionality:** The circuit must correctly perform frequency division by 2 for a continuous input clock signal.
2. **Maximum Operating Frequency ($f_{CLK,max}$):** The highest input clock frequency at which the output is stable and correct.

3. **Figure of Merit (FoM):** The most critical competitive metric, defined as:

$$\text{FoM} = \frac{f_{CLK,\max}(\text{GHz})}{\text{Power}_{\text{total}}(\text{mW})}$$ *(The group with the highest FoM wins the speed-power competition.)*

4. Project Deliverables and Grading Breakdown (30 Grades)

Deliverable	Grading (30 Total Grades)	Submission Requirement
I. circuit schematic & TB schematic	**5 Grades**	Screenshots of circuit & test bench
II. Transistor sizing	**5 Grades**	Screenshot of all transistor sizes (W/L) or a table
III. Results	**10 Grades**	Transient waveforms of input & output clock for 8 ns
IV. FOM @ 2 GHz	**5 Grades**	Report supply used, current consumed from supply, total power and FOM
V. Discussion	**5 Grades**	Write down your conclusion. Trade-offs you observed. Anything new you learned
VII. Innovation	**3 Grades**	Bonus for designing a programmable divider (divide by N) or Modulus divider working at 2 GHz Please include all deliverables (I – V) for this divider
VIII. Competition	**3 Grades**	Bonus for the highest FOM achieved “for clock frequency >= 2GHz” Please include all deliverables (I – V) for the clock frequency if higher than 2 GHz.

5. Recommended Steps

1. **Theory & Topology Selection:** Review the D flip-flop and frequency divider concepts (e.g., TSPC) from the lecture and research high-speed topologies (CML, ILFD, etc.).
2. **Schematic Entry & Sizing:** Design and size the transistors for speed, aiming for minimum channel length and appropriate W/L ratios.

3. **Simulation & Optimization:** Simulate for fCLK,max and power consumption. Optimize the circuit for the best FoM.
4. **Reporting:** Document all design choices, trade-offs, and results clearly.

6. Project Submission & Management

All project management, communication, and submission will be handled through our course's official **Google Classroom**.

A. Group Formation (Mandatory First Step)

1. Groups of 5–6 students must be formed.
2. A single designated team representative must send an email by **Oct 18th** to the lecturer (drahmedyasser@cu.edu.eg) with the following information:
    - **Subject:** ECE2XX Project Group Formation
    - **Body:** A list of all group members, including **Full Name**, **Student ID**, and **Student Email**.
3. Upon receipt of the group list, the lecturer will reply to the team representative, assigning the official **Group Number** (e.g., Group 1, Group 2, etc.) for internal reference.

B. Submission Deliverables

The following file must be submitted to the **Google Classroom assignment link**:

1. **Final Project Report (PDF Format):** A professionally written PDF report.

C. Final Submission and Locking Policy

1. The lecturer will create a **Group Assignment** in Google Classroom.
2. **Only one student per group** needs to upload the required files (PDF and ZIP archive) to the assignment link. This single upload will automatically be marked as submitted for all 5–6 members of the group.
3. The submission deadline in Google Classroom is **final**.
4. **Late submissions** will be automatically tracked and marked as late by the platform and will incur a grade penalty.