

Cairo University - Faculty Of Engineering

EECE Department – Fall 2025

Basic Electronic Circuits - EECG221 Project

**DESIGN AND SIMULATION OF A PROGRAM-
MABLE LOW-DROPOUT REGULATOR AND
AN OPERATIONAL TRANSCONDUCTANCE
AMPLIFIER**

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1 Introduction

Low-Dropout Regulators play a crucial role in modern electronic systems by providing stable and regulated output voltages despite varying input voltages and load conditions. The dropout voltage of the LDO represents the difference between the input supply voltage and the regulated output voltage. The LDO operates within a "regulation region," where the Pass Device is in the saturation region & delivers a stable output over various input supplies and output loads. An LDO includes a reference voltage, an error amplifier (OTA), a feedback network, and a series pass element. LDO Schematic in is shown in figure 1.

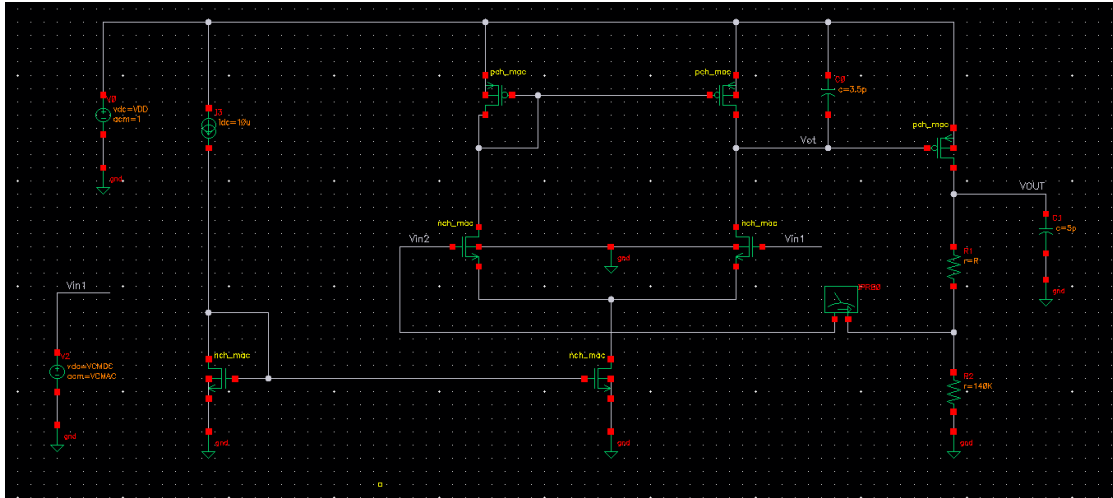


Figure 1 LDO Schematic in CADENCE

2 OTA DESIGN

Figure 2 shows the schematic of OTA in Cadence.

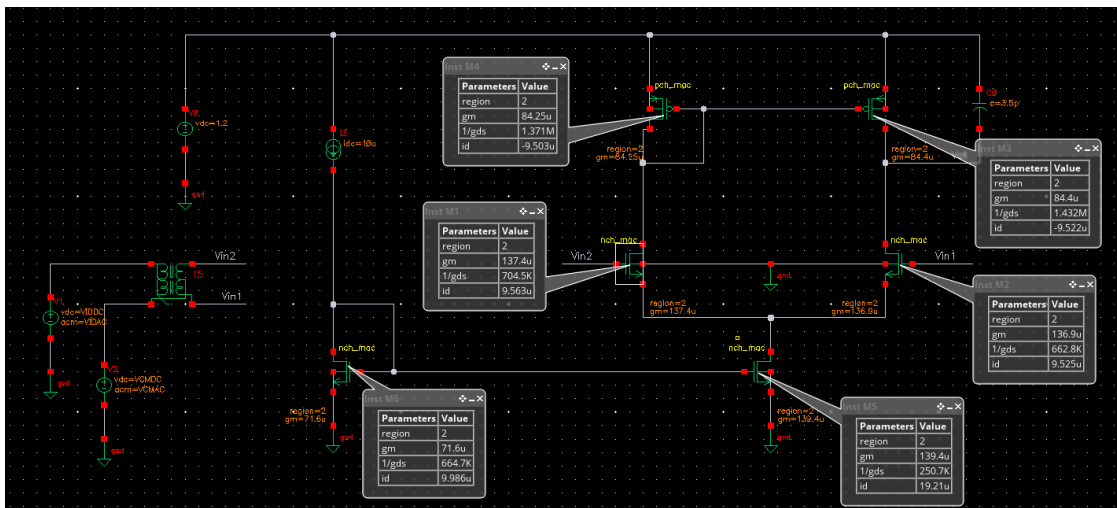


Figure 2 OTA Schematic in CADENCE

2.1 Design Charts

We designed the OTA based on g_m/I_D Methodology, figures 1 (a, b) show NMOS design charts over g_m/I_D . Figures 2 (a, b) show PMOS design charts.

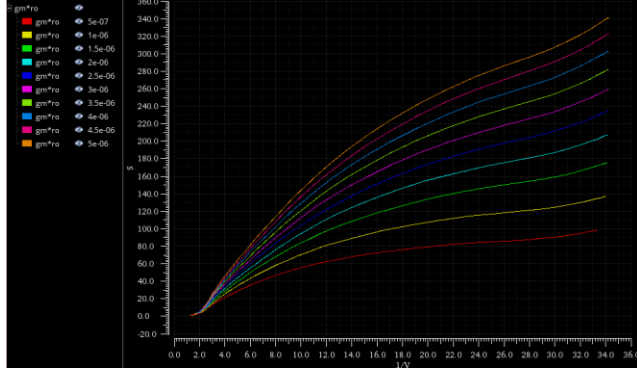


Figure 3 (a) NMOS $g_m.r_o$ chart

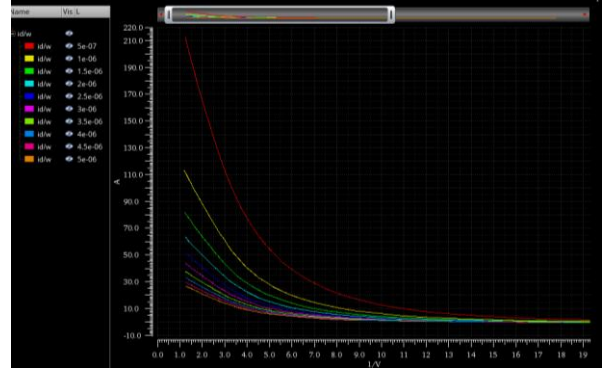


Figure 3 (b) NMOS I_D/w chart

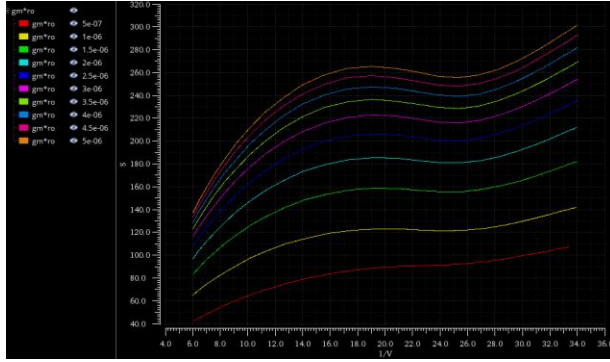


Figure 4 (a) PMOS $g_m.r_o$ chart

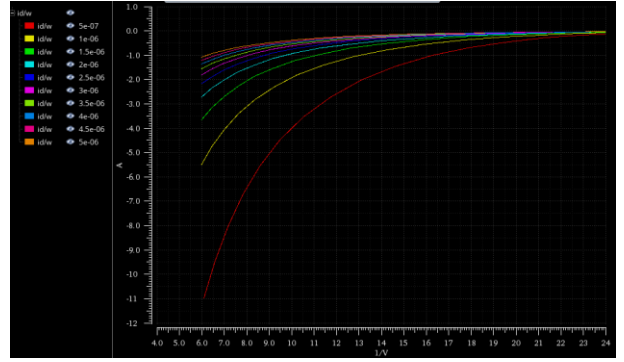


Figure 4 (b) PMOS I_D/w chart

2.2 Design of the Input Pair (M1, M2)

- Based on the relation $g_{m1,2} \geq 2\pi C_c f_u$, $g_{m1,2}$ is calculated as:

$$g_{m1,2} = 2\pi \times 3.5 \text{ pf} \times 6.5 \text{ MHz} \approx 140 \mu\text{S}.$$

- We selected that $r_{on} = r_{op}$ for simplicity, so based on the equation of the gain $A_v = g_{m1,2} (r_{on} \parallel r_{op}) = g_{m1,2} \cdot \frac{r_o}{2} \geq 50$, so $r_o \geq 714 \text{ K}\Omega$, so that:
- $g_{ds1,2} = g_{ds3,4} = \frac{1}{r_o} \leq 1.4 \mu\text{S}$.
- From the g_m/g_{ds} design chart, we find the required length is $L = 2.5 \mu\text{m}$. And from ID/w design chart we find that the required width is $w = 12 \mu\text{m}$.

2.3 Design Of the Current Mirror Load (M3, M4)

- From the DC gain requirement, the output conductance of transistors M3 and M4 must satisfy $g_{ds3,4} < 1.4 \mu\text{S}$.
- Assuming a relatively high transconductance efficiency of $\frac{g_m}{I_D} = 14$, and a drain current of $I_D = 10 \mu\text{A}$, the resulting transconductance is $g_{m3,4} = 14 \times 10 \mu\text{A} = 140 \mu\text{S}$.
- This leads to a ratio $\frac{g_{m3,4}}{g_{ds3,4}} > 100$, which satisfies the required intrinsic gain for meeting the DC gain specification.
- From the g_m/g_{ds} design chart, we find the required length is $L = 1.5 \mu\text{m}$.
- To satisfy $\text{CMIR}_{\text{MAX}} \geq 1$ the following relationship is used based on the chosen topology: $\text{CMIR}_{\text{MAX}} = V_{DD} - V_{SG3} + V_{GS1} - |V_{DS,\text{sat}1}|$
- From the V_{GS1} design chart, we find that $V_{GS1} = 0.384 \text{ V}$, so $V_{GS3,\text{max}} = 0.484 \text{ V}$,
- From the V_{GS3} design chart, we find that $\frac{g_m}{I_{D,\text{min}}} = 12$.
- From the ID/w design chart, we find that required width is $w = 8 \mu\text{m}$.

2.4 Design of the Tail Current Source (M5)

- To satisfy the required $\text{CMRR} = \frac{A_d}{A_{cm}} \geq 45$, The common-mode gain is given by $A_{cm} = \frac{1}{2 g_{m3,4} R_{SS}} \leq -40 \text{ dB}$, so $A_{cm} \leq 0.01$, then $g_{ds5} < 2.8 \mu\text{S}$.
- Assuming a reasonably large transconductance efficiency of $\frac{g_m}{I_D} = 10$, so $g_{m5,6} = 10 \times 20 \mu\text{A} = 200 \mu\text{S}$. Accordingly, the intrinsic gain satisfies $\frac{g_{m5,6}}{g_{ds5}} > 70$.
- From the g_m/g_{ds} design chart, we find that channel lengths are $L_5 = L_6 = 1 \mu\text{m}$
- $\text{CMIR}_{\text{min}} = V_{GS5} + V_{DS,\text{sat}5} < 0.65 \text{ V}$

- From the V_{GS5} design chart, we find that $V_{GS3} = 0.3\text{ V}$, so $V_{DS,sat5} < 0.35\text{ V}$.
- From the $V_{DS,sat5}$ design chart, we find that $\frac{g_m}{I_{D,min}} = 7$, then to keep some margin we use $\frac{g_m}{I_D} = 10$.
- From the I_D/w design chart, we find that the required channel length is $w_5 = 1.5\text{ }\mu\text{m}$ and $w_6 = 0.75\text{ }\mu\text{m}$.

2.5 Sizing of OTA Transistors

MOSFET	M1	M2	M3	M4	M5	M6
W (μm)	12	12	8	8	1.5	0.75
L (μm)	2.5	2.5	1.5	1.5	1	1
g_m/I_D	14	14	12	12	10	10

2.6 Differential Gain Simulation

Figure 5 show the frequency response for the open loop gain of the OTA in Cadence.

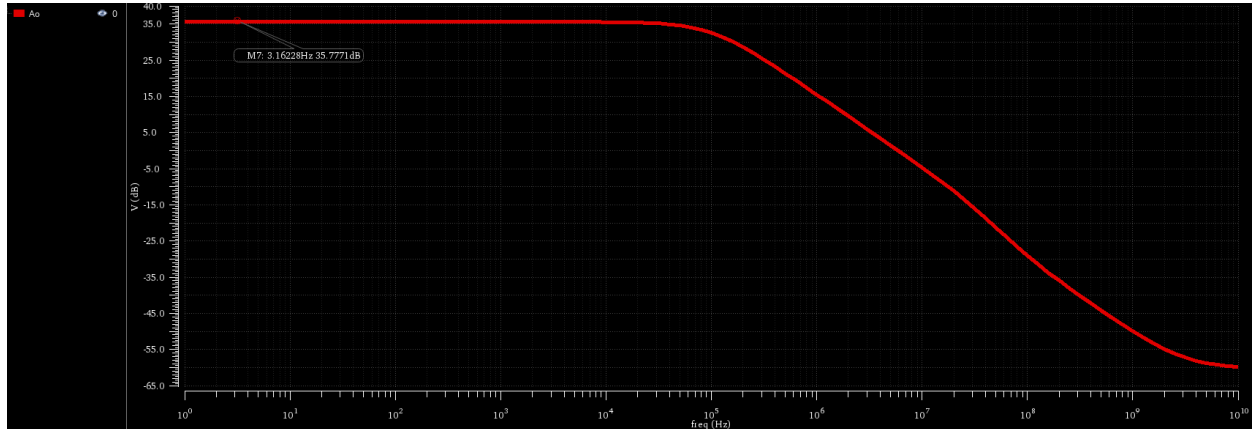


Figure 5 Open Loop gain simulation

Simulation results for OTA gain

Parameter	Achieved value in Simulation
DC Open Loop gain	35.78 dB
GBW	6.2 MHz

2.7 CMRR

Figure 6 shows the frequency response of the CMRR in simulation.

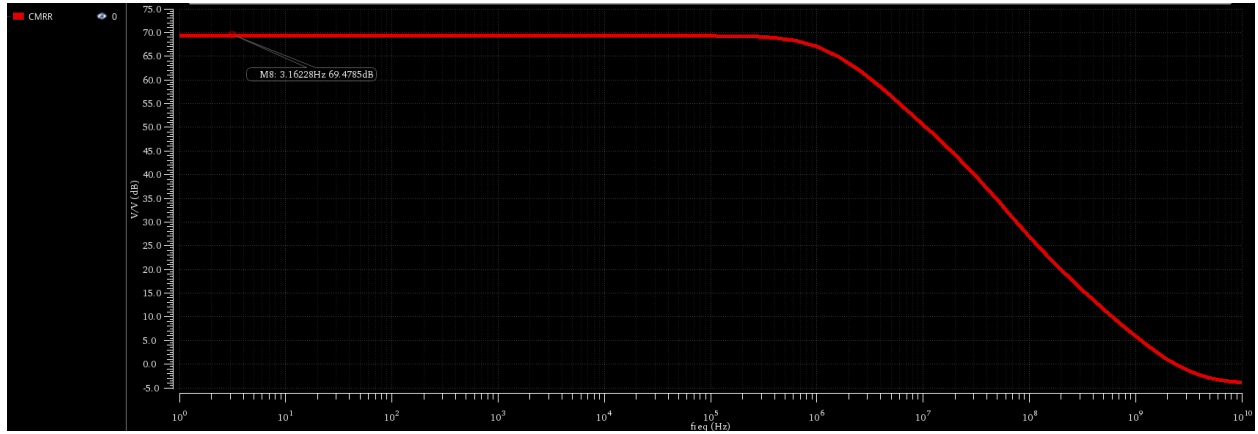


Figure 6 Simulation of the CMRR

Simulation results for CMRR and Phase Margin

Parameter	Achieved value in Simulation
CMRR	69.47 dB
Phase Margin	86.3°

2.8 CM large signal ccs (GBW vs V_{CM,DC})

Figure 7 shows the large signal analysis of the CM, showing the GBW vs $V_{CM,DC}$.

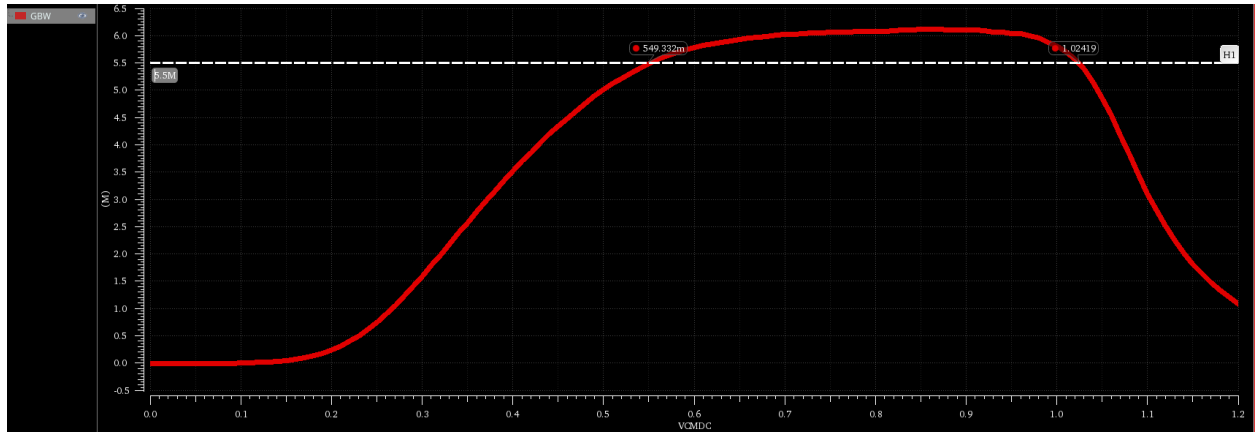


Figure 7 GBW vs $V_{CM,DC}$ simulation

The input range as the range over which the GBW is within 90% of the max GBW.

Simulation results for CMIR

Parameter	Achieved value in Simulation
CM input range – low	0.55 V
CM input range – high	1.024 V

2.9 Regions of Operation

Figure 8 shows the region of operation for M4 across $V_{CM, DC}$.

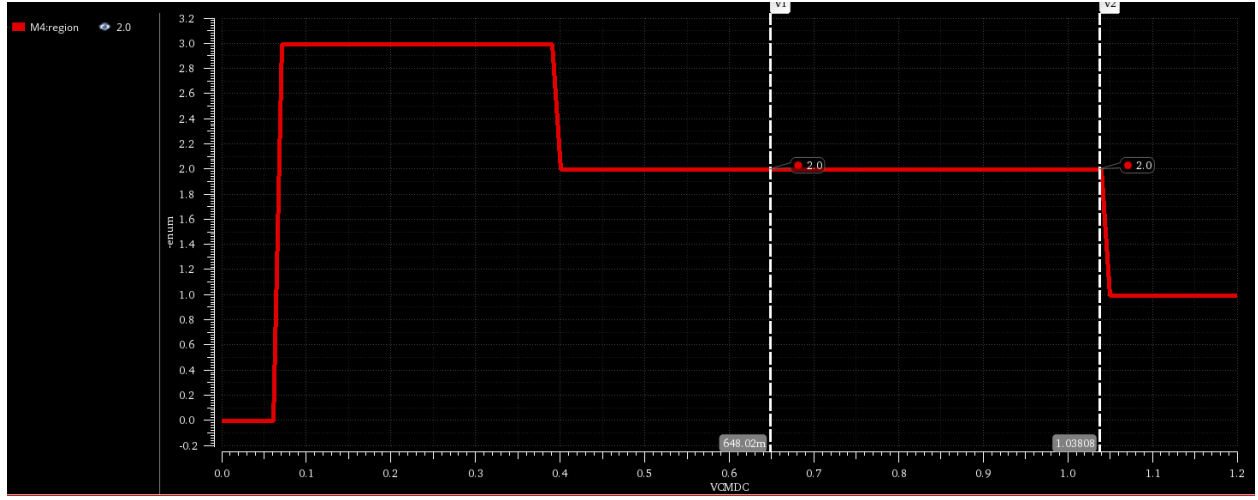


Figure 8 Region of operation across VCM, DC

Within the CMIR the transistors are all in saturation.

3 LDO Analysis

$$V_{OUT} = V_{IN} \frac{A_{ol}}{1 + A_{ol} * B}$$

$$B = \frac{R_2}{R_1 + R_2}$$

- If we put $A_{ol} = \infty$ we will get: $V_{OUT} = V_{IN}(1 + \frac{R_1}{R_2})$
- We need the ration $\frac{R_1}{R_2} = \frac{V_{OUT}}{V_{IN}} - 1$ to determine the required V_{OUT} , we will set V_{IN} , it must be $< V_{OUT, min}$ so we will put $V_{IN}=0.7$

$$\frac{R_1}{R_2} \max = \frac{1.05}{0.7} - 1 = 0.5 \quad \frac{R_1}{R_2} \min = \frac{0.75}{0.7} - 1 = \frac{1}{14}$$

- Assume that the current in the pass transistor M7 will be $5 \mu A$, Then

$$R_{total} = R_1 + R_2 = \frac{1.05}{5} = 210 \text{ k}\Omega$$

- Put a fixed value for $R_2 = 140 \text{ k}\Omega$ so R_1 will be variable to determine V_{OUT} with step 50 mV: $R_1 = 140(\frac{V_{out}}{0.7} - 1) \text{ k}\Omega$

Estimation of the values of R_1 to achieve required V_{OUT} steps based on calculations

Targeted V_{OUT} (V)	0.75	0.8	0.85	0.9	0.95	1	1.05
Value for R_1 (k Ω)	10	20	30	40	50	60	70

3.1 Resistance sweep (R1)

Figure 9 shows the Value of V_{OUT} across R_1 .

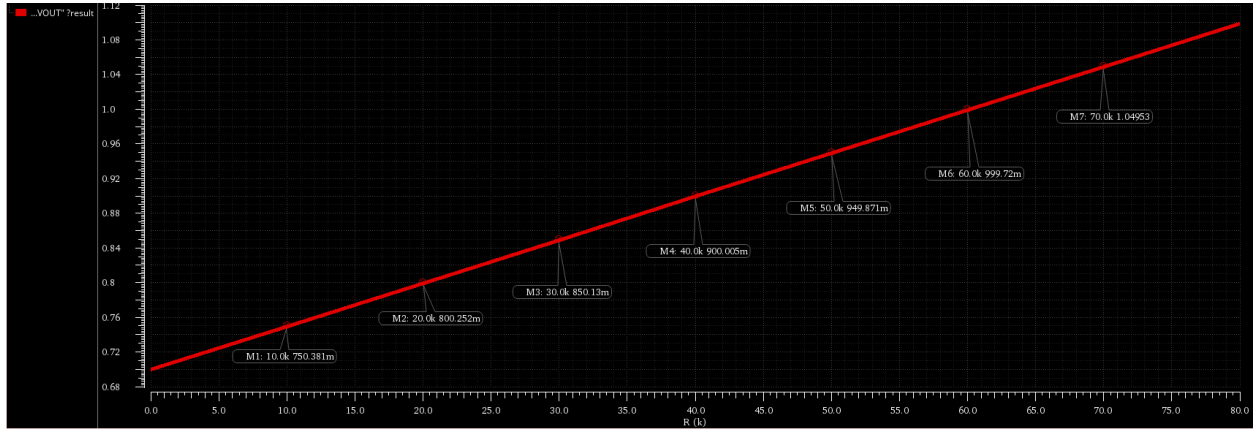


Figure 9 Simulation results for V_{OUT} vs R_1

Values of V_{OUT} across different R_1 values from simulation results

R_1 (K Ω)	10	20	30	40	50	60	70
V_{OUT} (V)	0.7503	0.8003	0.8501	0.9	0.9499	0.9997	1.0495

Max Current Consumption is 34 μA .

Figure 10 Cadence Snapshot for the max. current consumption

EECE:LDO:1	VDC("/VOUT")	1.05
EECE:LDO:1	IDC("/V0/PLUS")	-33.67u

3.2 BONUS: PVT Analysis

Adding Corners, Temperature sweep from -40° to 85° with V_{DD} 1.18, 1.2, 1.22 V (Fig. 11).

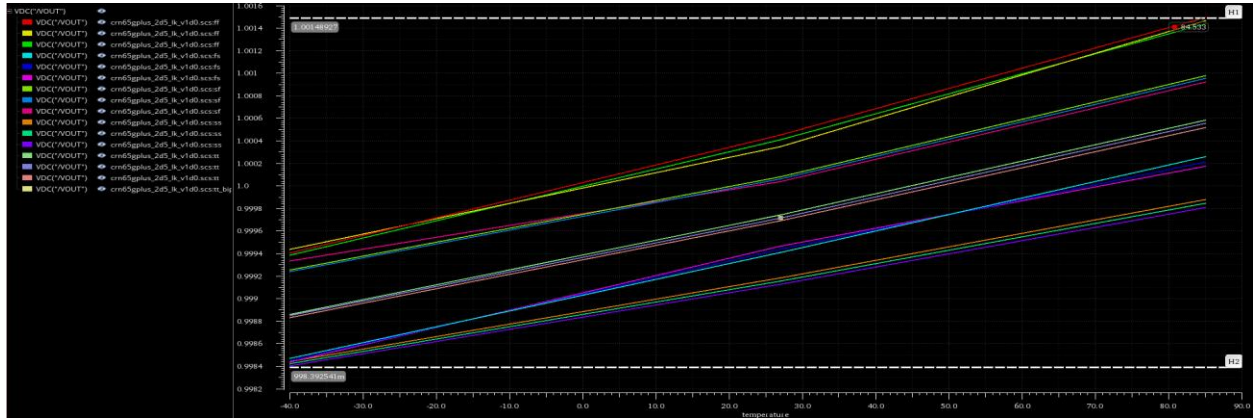


Figure 11 Simulation for V_{OUT} across PVT

Accuracy Analysis

- Target Voltage: 1.000 V
- Actual Range: from 0.9984 V to 1.0015 V.
- Total Error: The maximum variation is only 3.1 mV.

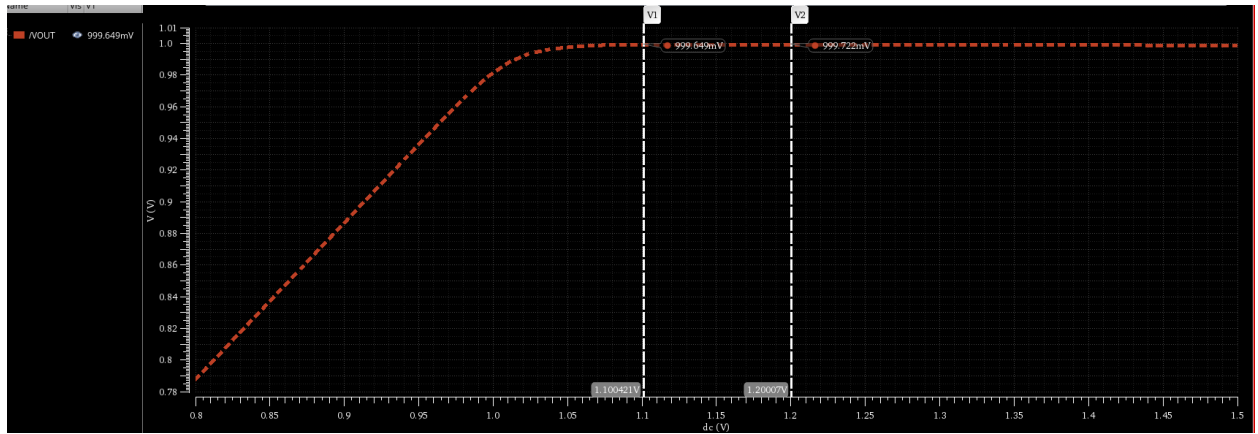
- Percentage Error: $\frac{3.1 \text{ mV}}{1000 \text{ mV}} = 0.31 \%$

Simulation results for VOUT across PVT

Temp. (C °)	-40	25	85	-40	25	85	-40	25	85
V _{DD} (V)	1.18			1.2			1.22		
V _{OUT} (V)	0.9984	1	1.0004	0.9988	1	1.0005	0.999	1	1.0015

3.3 Line Regulation

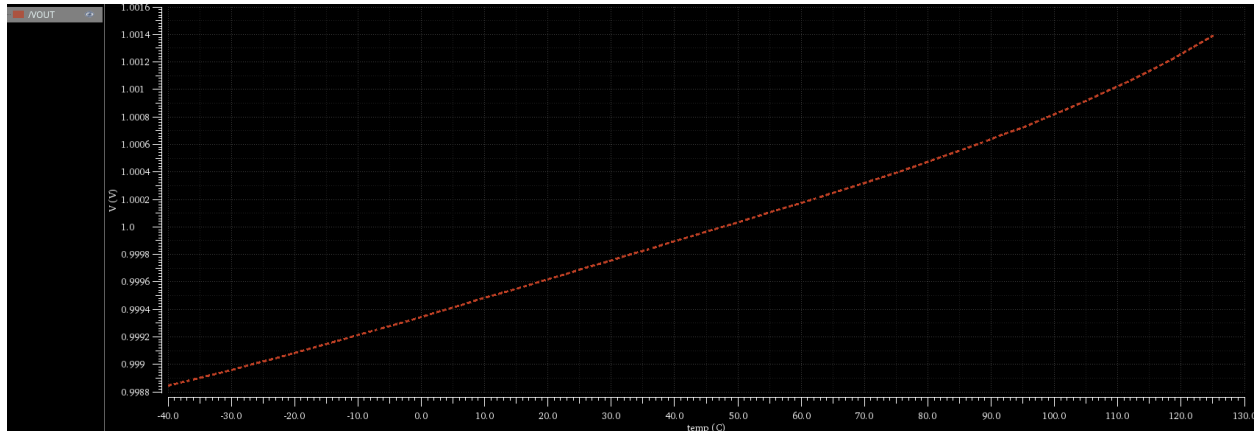
Figure 12 shows the simulation results for V_{DD} sweep from 0.8 V to 1.5 V at R₁ = 60 kΩ, so the required V_{OUT} = 1 V

Figure 12 Simulation results for V_{DD} sweep

$$\text{LNR} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{999.65 - 999.72}{1.1 - 1.2} = 0.7 \text{ mV}$$

3.4 Temperature Sweep Analysis

Figure 13 shows the simulation results for temperature sweep from -40 ° to 125 ° at V_{DD} = 1.2 V, with R₁ = 60 kΩ, so the required V_{OUT} = 1 V

Figure 13 Simulation for V_{OUT} changes across Temp. (-40°-125°)

- Max error is 1.6 mV
- $V_{\max}(T=125) = 1.0016 \text{ V}$
- $V_{\min}(T=-40) = 0.9988 \text{ V}$
- $V_{\text{nom}}(T=27) = 0.99972 \text{ V}$

$$\text{Temperature Coefficient} = \frac{1}{V_{\text{nom}}} * \frac{V_{\max} - V_{\min}}{T_{\max} - T_{\min}} * 10^6$$

$$TC = 16.97 \text{ ppm}/^{\circ}\text{C}$$

3.5 PSRR

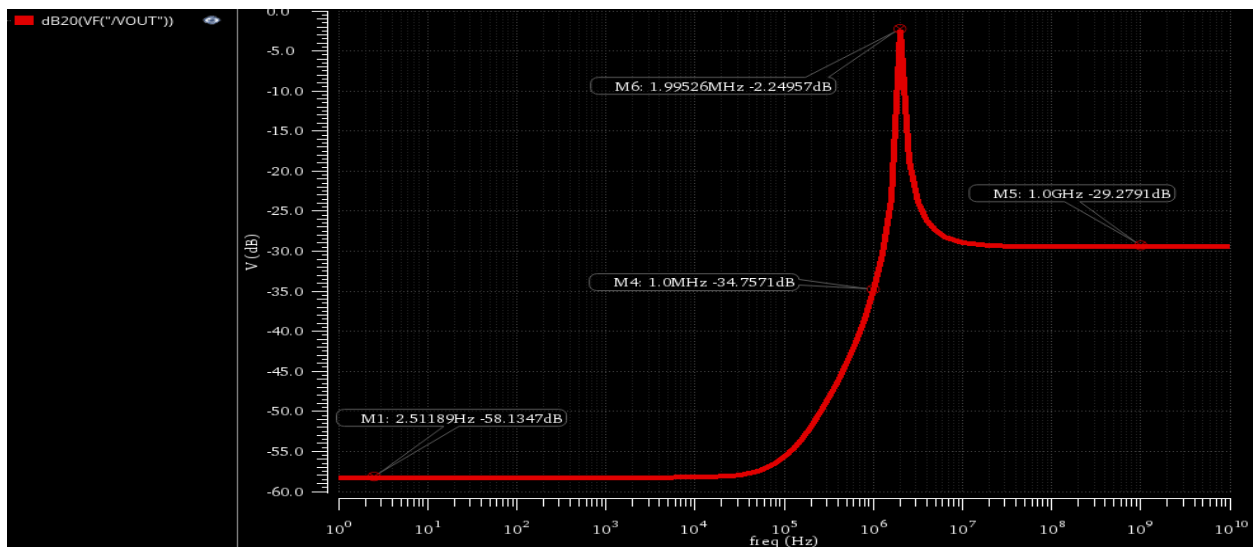


Figure 14 Simulation results for PSRR across frequency

Figure 14 shows the simulation results for Power Supply Rejection Ration

(PSRR vs frequency), where $\text{PSRR} = -20 \log_{10} \left(\frac{V_{\text{out}}}{V_{\text{supply}}} \right)$.

PSRR @DC = 58 dB

Worst case = 2.25 dB

4 Summary of Final Results

Parameter	Required	Achieved
Technology	65nm CMOS	
Supply Voltage	1.2 V	
Reference Voltage (VIN)	0.7 V	
Regulated Voltage	Programmable with step 50 mv	Done as required
Current consumption	$\leq 60 \mu A$	34 μA
Load Capacitor (CL)	$\leq 5 pF$	5 pF
Compensation Capacitor (Cc)	Good	3.5 pF
LNR	Good	0.7 mV
PSR	@ DC	58 dB
	@ 1 MHz	34 dB
	@ 1GHz	29 dB
	Worst case	2.25 dB
TC	Good	16.97 ppm/°C
OTA		
Open loop DC voltage gain	$\geq 34 dB$	35.78 dB
GBW	$\geq 5 MHz$	6.2 MHz
Phase margin	$\geq 60^\circ$	86.3 °
CMRR @ DC	$\geq 45 dB$	69.47 dB

5 Simulation Files & GitHub repo.

<https://github.com/a7med57/LDO-OTA-Design.git>