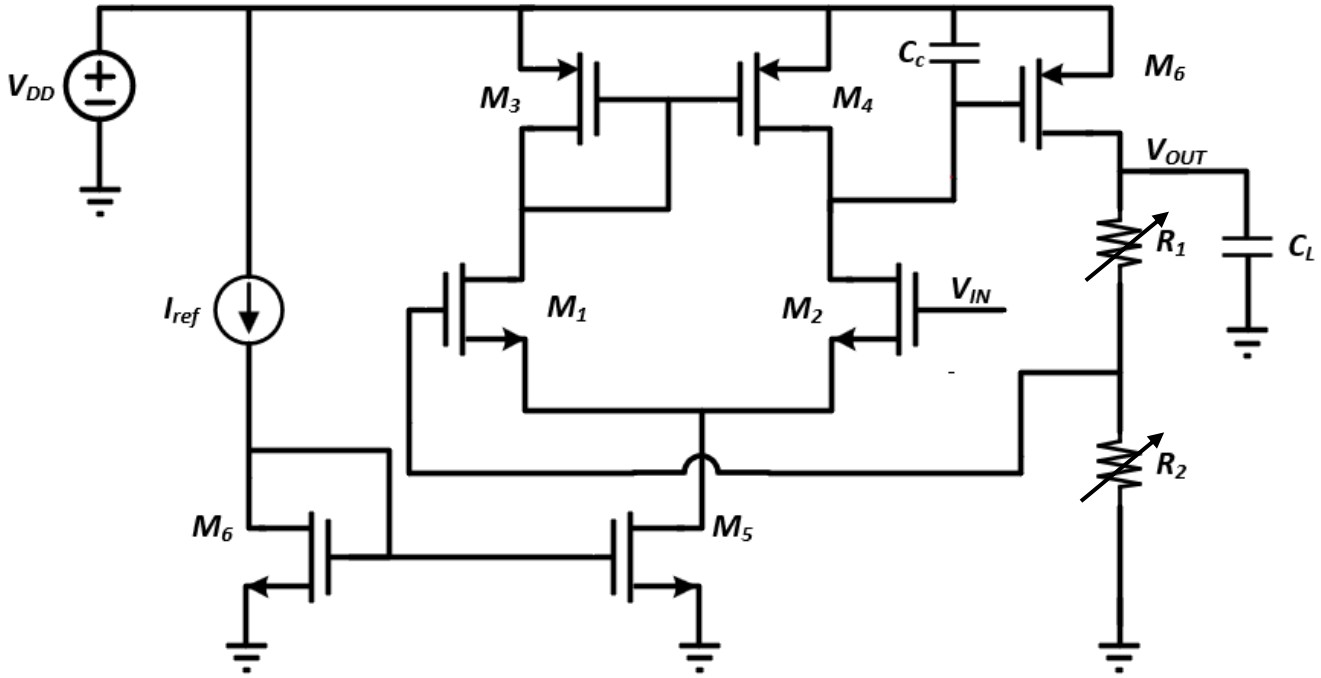
Project - Due Date Thursday Dec 25th, 2025

- This project can be done in groups of 3 students or less, each group has a unique number
- Project grade will be based on the submitted report; any copied reports will be given zero.
- You should provide the required simulations using CADENCE.
- The report is limited to 10 pages without the cover, half a point will be lost for each extra page.
- Project submission will be online through a link that will be provided later.
- The cover page must contain the group number.
- All graphs and figures should be clear with readable axes and traces.

Low Dropout Regulator:

You are required to simulate a simple LDO to generate a constant voltage across Temperature, Supply and Process Variation (PVT) and should have a good power supply rejection (PSR)

Low Dropout Regulator Block Diagram:



LDO Design:

You are required to design a programmable LDO with following Specs:

LDO Specs	
Technology	65nm CMOS
Supply Voltage	1.2 V
Output Voltage Range	0.75 V – 1.05V
Output Voltage step	50 mV
LDO current consumption	60 uA
Reference Current	10 uA
Max Load Capacitance (C_L)	5pF

Operational Transconductance Amplifier Design:

You are required to design an OTA with following Specs:

OTA Specs	
Technology	65nm CMOS
Supply Voltage	1.2 V
Open loop DC voltage gain	>= 34dB
CM input range – low	<= 0.65 V
CM input range – high	>= 1 V
GBW	>= 5MHz
Phase margin	>= 60^0
CMRR @ DC	>= 45 dB