ZYNQ Based Real-Time Data Logger with 256 kSPS Sampling using Ethernet Interface

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***Abstract*— This research has designed and implemented a medium-speed and high-precision data logger using ZYNQ XC7Z020 FPGA and AD7768 ADC. The sampling rate of 256 kSPS and high-speed data transfer via Ethernet were the goals of this research, and the implementation results indicate the success of this project. In this system, ADA4807 amplifiers were used to amplify analog signals, ensuring that input signals with gains between 1 and 10 were sent to the ADC. The delta-sigma architecture of the AD7768 guarantees 24-bit resolution and significant noise reduction. After digital processing in the FPGA, the data were transmitted to the computer through the Ethernet port. Tests demonstrated that the system is capable of real-time sampling and transmission of various signals with high accuracy and efficiency, making it suitable for industrial applications, measurements, power quality analysis, and medical monitoring.**

Keywords*— *ZYNQ, FPGA, Data Logger, Ethernet, ADC, Real time, electronic measurement

I. Introduction

High-speed data acquisition systems, commonly referred to as data loggers, are used for industrial data acquisition applications, real time digital control systems, electronic measurement, environmental research, and medical diagnostics [1]. Data loggers collect, store, and process sensor data after an analog-to-digital converter stage [2]. Data loggers must capture data at high velocities to accurately represent swift environmental changes and for real-time analysis [3].

The significance of data loggers arises from their capacity to deliver prompt and precise information across many contexts[4]. In industrial settings, data loggers are employed to assess machinery performance, energy usage, and environmental conditions [5]. By acquiring real-time data, operators can detect anomalies, enhance operational efficiency, and avert equipment failure, thus minimizing downtime and maintenance expenses [6]. Data loggers help improve the quality of patient care by continuously monitoring the condition of patients and healthcare workers in medical applications, monitoring vital signs and quickly sending data to a control center [7].

Moreover, the advent of the Internet of Things (IoT) has underscored the need of high-speed data loggers [8]. With the increasing development of smart sensors, the generation of various data has also increased [9]. High-speed data loggers improve the processing and rapid transmission of data, enabling real-time analysis and decision-making [10]. The described feature is essential in areas such as environmental monitoring, where data loggers collect information on air quality, temperature, and humidity, and help in plans to combat climate change and public health issues [1]. Data loggers integrate capabilities such as wireless connectivity, cloud connectivity, and multi-channel data collection, in addition to speed and accuracy [11]. These advancements give customers increased flexibility and scalability to design systems for different applications and situations. With the increasing importance of data-driven decision-making in our connected world, high-speed data collection systems are becoming a critical tool for innovation and progress [12].

High-speed data loggers have significant challenges in achieving optimal sampling rates, efficient data transfer, and reliable connectivity, which has led to much research [13], [14], [15], [16], [17], [18]. Sampling rate is important because of its direct impact on the accuracy and integrity of the collected data. Using the Nyquist theorem, the sampling rate must be greater than twice the highest frequency of the signal. The complexity of this need increases when addressing high-frequency signals, necessitating intricate signal conditioning to preserve signal integrity. Furthermore, hardware components like ADCs and FPGAs must proficiently manage the requisite data without causing latency or bottlenecks[19].

Data transport and communication represent equally significant issues in high-speed data collecting systems. Efficient data transfer systems, such as direct memory access (DMA), are crucial for managing the substantial volumes of data produced at elevated sampling rates. The accurate configuration of these systems is intricate and necessitates meticulous attention to memory management to avert data loss. Choosing the right communication protocol, such as Ethernet or high-speed USBs, to transfer accurate and fast data to external systems is a design necessity. The system must have appropriate scalability to accommodate changing requirements without the need for redesign, as more sensors are added or connected to different networks [19]. Numerous research have examined the application of FPGAs and high-speed ADCs in the development of high-speed data acquisition systems [20]. Using the LDVS inputs of an FPGA, a low-complexity system-on-chip design was proposed for acquiring signals from MOS gas sensor applications. Kim et al. developed a digital data logger for a dual-scattering Compton camera using an FPGA-based interface, demonstrating the adaptability of FPGAs in handling the communication between the sensor signal and the necessary information retrieval [21]. Gist et al. presented a high-speed data transfer interface solution between a microcontroller and an FPGA, highlighting the FPGA

component because SPI is a fully integrated peripheral in many microcontrollers [22].

The application of FPGAs with high-speed ADCs in high-speed data acquisition systems has been explored in several additional contexts, including time-to-digital conversion and Fourier transform spectroscopy [23], [24]. Research has also been conducted on digital multichannel analyzers [25]. These experiments illustrate the efficacy of FPGAs with high-speed ADCs in overcoming the obstacles associated with high-speed data acquisition, encompassing sampling rate, data transfer, and communication.

II. System Design

A. Key components

The 24-Bits AD7768 analog-to-digital converter (ADC) acquires amplified analog signals from four ADA4807 signal conditioner blocks, selected for their excellent precision and capability to minimize noise and DC-Offsets in the input signals for the ADC. The precise functioning of these conditioners and their noise attenuation ability guarantee the transmission of high-quality analog signals to the ADC.

The ADC receives two channels from each of the ADA4807 amplifiers as well as flexible programable gain stages. Specifically, for channels 1–4, the amplifier gain is set to 1. This setting allows us to amplify and sample standard amplitude input signals with high accuracy. Additionally, for channels 5 to 8, the amplifier gains are set to 10. Using these settings to sample weaker signals, which makes it possible to amplify and transmit low-amplitude signals with high accuracy.

This configuration ensures a wide dynamic range and high accuracy in sampling and processing even weak signals. Using the ADA4807 not only helps improve the accuracy and noise reduction of the system but also enhances its overall efficiency in terms of power consumption, signal integrity, and data processing speed. Using the ADA4807 not only helps improve the accuracy and noise reduction of the system but also enhances its overall efficiency in terms of power consumption, signal integrity, and data processing speed. This setup and careful selection of components play an important role in achieving a high-precision and high-speed data acquisition system, which provides flexibility for use in various applications. The overall view of the implemented circuit board is shown in Figure 1.

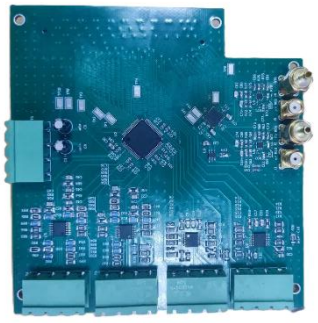

Fig. 1. View of the designed board with four ADA4807 amplifiers connected to an AD7768 ADC.

The AD7768 ADC provides high-precision analog-to-digital conversion with 24-bit resolution, utilizing a delta-sigma architecture that significantly reduces signal noise through an internal digital filter. The ADC operates in multiple power modes and can be configured to adjust the sampling rate and power consumption for specific applications. With eight input channels, it is ideal for applications that require high accuracy and wide dynamic range. The AD7768's high sampling rate and robust performance in harsh industrial environments make it an ideal choice for accurate analog-to-digital conversion.

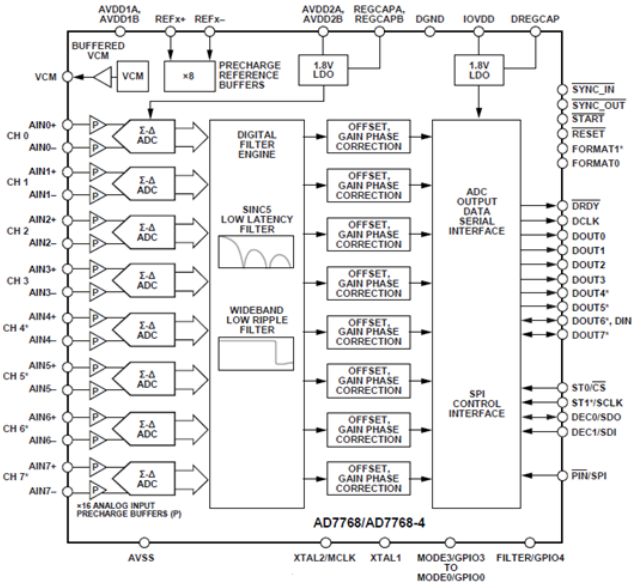

Fig. 2. Block diagram of the AD7768, a 24-bit, 8-channel ADC with simultaneous sampling [26].

B. System architecture

This project utilizes the ZYNQ XC7Z020 FPGA for data processing and communication management. This platform, which integrates ARM processors with hardware acceleration, enables fast and concurrent data processing. Using this configuration, digitally processed signals from the ADC can be transferred from the programmable logic (PL) to the processing system (PS) with minimal latency. In this system, the FPGA is responsible for processing and transmitting data. After the ADC samples the analog signals and converts them into digital form, the digital data is transferred directly from the PL to the PS, which is finally transmitted to the computer via the Ethernet port. In applications that require accurate and timely data analysis, this architecture allows for high-speed and efficient data transfer and processing.

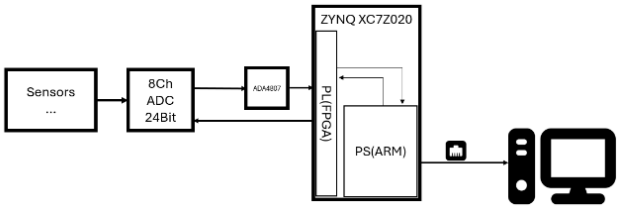

Fig. 3. Overall implemented system block diagram including: analog system, data processing and data transmission

The overall system architecture and its interconnections are divided into three main parts, the analog system, which includes ADC and amplifiers, data processing, which is implemented by FPGA, and data transmission, where data is directly transferred from PL to PS and sent via Ethernet port, as shown in Figure 3. In the processing stage, which is done in PS, an initial signal analysis is performed, including determining the sign (positive or negative) of the data points based on a reference curve before transmission.

In this system, instead of using DMA, the data is directly transferred from PL to PS using AXI_GPIO after processing. This method allows the PL to fully focus on maximizing data reception from the ADC, while the PS is responsible for processing and sending. Furthermore, since the data is transmitted using TCP/IP and lwIP, utilizing the PS for optimal network communication is essential. This method simplifies system design while maintaining data transfer speeds over Ethernet at more than 1000 Mbps per second. However, data transfer with AXI_GPIO is appropriate when the number of ADC channels and data rates are within reasonable limits. In this design, with 8 channels and a sampling rate of 256 kHz, data transfer through AXI_GPIO does not have a significant impact on system performance. But with the increase in the number of channels and data rates, processing in the PS may come under pressure. In this situation, using DMA as an efficient solution to reduce processor load and improve system performance will be essential.

C. ADC Working Mode

In this system, the "1000" mode is used for the AD7768 ADC. The "1000" mode means Fast Mode, in which three key features are used for different system settings: sampling rate, power consumption and type of conversion operation. The Fast Mode settings are as follows:

TABLE I. AD7768 ADC OPERATING MODES, SHOWING DIFFERENT CONFIGURATIONS FOR RECEIVING AND PROCESSING DATA [26]

Mode Hex	MODE3	MODE2	MODE1	MODE0	Power Mode	DCLK Frequency	Data Conversion
0x0	0	0	0	0	Low Power	MCLK/1	Standard
0x1	0	0	0	1	Low Power	MCLK/2	Standard
0x2	0	0	1	0	Low Power	MCLK/4	Standard
0x3	0	0	1	1	Low Power	MCLK/8	Standard
0x4	0	1	0	0	Median	MCLK/1	Standard
0x5	0	1	0	1	Median	MCLK/2	Standard
0x6	0	1	1	0	Median	MCLK/4	Standard
0x7	0	1	1	1	Median	MCLK/8	Standard
0x8	1	0	0	0	Fast	MCLK/1	Standard
0x9	1	0	0	1	Fast	MCLK/2	Standard
0xA	1	0	1	0	Fast	MCLK/4	Standard
0xB	1	0	1	1	Fast	MCLK/8	Standard
0xC	1	1	0	0	Low Power	MCLK/1	One-shot
0xD	1	1	0	1	Median	MCLK/1	One-shot
0xE	1	1	1	0	Fast	MCLK/2	One-shot
0xF	1	1	1	1	Fast	MCLK/1	One-shot

1. Sampling rate and power consumption mode: In Fast Mode, the sampling rate is at its highest and power consumption is higher than other modes. For this mode, the data clock (DCLK) is divided by 1, which gives us the highest sampling rate. In general, this mode is suitable when we need fast and accurate sampling and power consumption is less important.

2. Conversion operation: In this mode, the conversion operation is performed continuously and in a standard manner, and the data is converted from analog to digital instantaneously.

According to Table 1, this mode allows us to process data at high speed.

Setting the sampling rate and ODR for AD7768: In this system, the MCLK input clock with a frequency of 32.768 MHz is used to set the sampling rate. To set the sampling mode and speed, we use specific settings that include the mode selection and the Decimation Rate. Given the Fast mode selection from Table 2, the modulator clock fMOD is set to MCLK/4. Therefore, given that MCLK is 32.768 MHz, the modulator clock is 8.192 MHz.

Next, using Table 3, for the settings DEC1 = 0 and DEC0 = 0, the reduction rate is set to ×32. This means that for each sample, the data is reduced by a factor of 32.

TABLE II. CLOCK MODULATOR (FMOD) DIVISION IN THREE DIFFERENT AD7768 POWER MODES [26]

Power Mode	Modulator Rate, f_{MOD}
Fast	MCLK/4
Median	MCLK/8
Low Power	MCLK/32

TABLE III. CONTROLLING THE DECIMATION RATIO PINS ON THE AD7768 [26]

DEC1	DEC0	Decimation Rate
0	0	×32
0	1	×64
1	0	×128
1	1	×1024

Equation (1) calculates the output data rate (ODR) to be 256 kHz with these settings in mind [26]. According to the datasheet, this sampling rate is optimal for this type of ADC and provides a balance between speed and accuracy. This sampling rate ensures that the system captures fast signal changes while providing reliable digital conversion. The ODR rate chosen is high enough to sample the input signals without aliasing while preserving fine details of the analog waveform.

$$ODR = \frac{f_{MOD}}{Decimation\_Ratio} \quad (1)$$

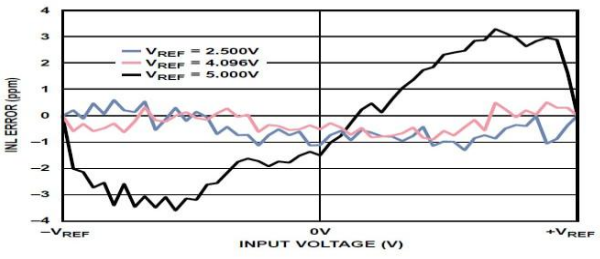

Fig. 4. INL Error vs. Input Voltage for Different Reference Voltages (V_{REF}) in Fast Mode [26]

In Fast Mode, the Integral Nonlinearity (INL) error is one of the most important factors that determines how accurate analog-to-digital converters (ADCs) are. Figure X shows the INL error for different reference voltages (V_{REF}) in this mode. According to Figure 4, when $V_{REF} = 5\,V$, the INL error increases significantly at higher input voltages, leading to greater nonlinearity. In contrast, when $V_{REF} = 2.5\,V$, INL becomes more stable, and its accuracy increases. By applying a correction processing step to the output data, the measurement accuracy increases. This processing is performed in the PS after data acquisition and before transmission over Ethernet and reduces nonlinearity, making the signal response more linear. As a result, the transmitted digital data achieves higher accuracy and minimizes the impact of INL error.

III. EXPERIMENTAL RESULTS

In the experiments, various signals with a frequency of 20 Hz were generated, such as pulses, sine waves, and triangle waves. The 20 Hz signal was chosen because with a sampling rate of 256 kHz, a larger number of samples can be taken in one period of the signal. However, if the signal frequency is higher, for example, 50 kHz, with a sampling rate of 256 kHz, a maximum of 5 samples can be taken in one period of the signal, which is not enough to draw the signal clearly, and the signal shape will not be displayed accurately and legibly. In this situation, for accurate signal reconstruction, it is necessary to use filters to reconstruct the real signal based on these five samples. The FPGA first received the signals and performed the initial processing role. Then the data was transferred to the computer via an Ethernet connection using the TCP protocol. Due to the large volume of data, a delay of 100 microseconds was considered between each data transmission to avoid overloading the system and to ensure transmission stability. Thereafter, the data was processed in QT/MATLAB software and displayed continuously. It should be noted that in this experiment, the internal digital filter of the ADC type Sinc5 was disabled so that the raw ADC data could be displayed without preliminary processing. This caused distortions in the received signals. However, activating this filter can significantly improve the quality of the signals and reduce noise and distortions caused by quantization. The obtained signals can be saved to the hard disk or SD card in formats such as CSV or text. This process is shown in Figures 5, 6, and 7 for square, sinusoidal, and triangular signals, respectively.

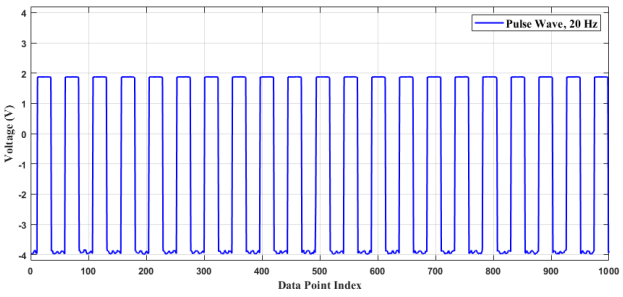

Fig. 5. Real-Time output square signal with a frequency of 20 Hz

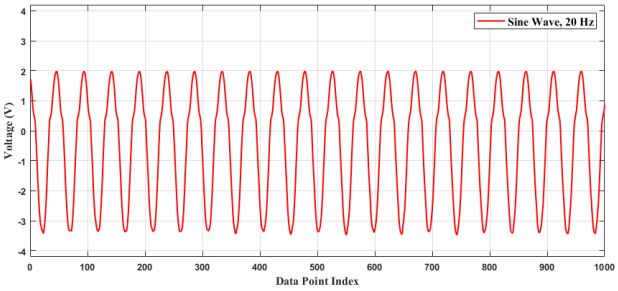

Fig. 6. Real-Time output sinusoidal signal with a frequency of 20 Hz

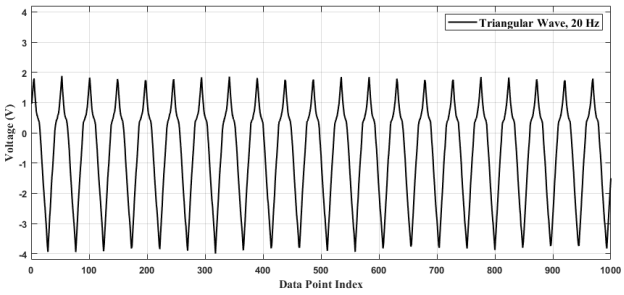

Fig. 7. Real-Time output triangular signal with a frequency of 20 Hz

Fig. 8. Comparison of the accuracy of the system with a voltmeter: Figure A shows a voltage of 0.781 V and Figure B shows a voltage of 1.553 V, which is also shown with high accuracy in the system

Also, to check the accuracy of the analog-to-digital data conversion, the analog signals measured by the voltmeter and the digital system were compared. As can be seen in Figure 8, the system accurately converts analog values to digital

values and a perfect match between the measurements is observed, for two DC input examples.

IV. Conclusion

This paper reports the design and implementation of a multichannel datalogger using the ZYNQ XC7Z020 FPGA and the AD7768 ADC. It presents implementation details and some advances in the field of analog-to-digital data acquisition and real-time processing and transmission via Ethernet ports. Operating menus and tools were developed in QT/MATLAB environments, which makes it simple and user-friendly to configure, calibrate, real-time analyze, display, and save data in different modes.

To achieve high-speed data acquisition and real-time transmission, the ZYNQ architecture was chosen over a conventional FPGA. The combination of ARM processors (PS) and FPGA fabric (PL) makes it possible to efficiently process data before sending it over Ethernet. This makes the host system's computing tasks easier. The PS section handles initial data processing, applies linearization techniques to correct ADC non-linearity, and manages data transmission, ensuring stability and minimizing latency. This hybrid architecture significantly enhances the performance compared to using a standalone FPGA.

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