Instruction	Opcode		Control Signals				
	Signal Selector	ALU Operation	rori	branch	aluordm	regwrite	memwrite
ADD	1 0 0	0 0 0 (Add)	1	0	1	1	0
SUB	1 0 0	0 0 1 (Subtract)	1	0	1	1	0
AND	1 0 0	0 0 2 (And)	1	0	1	1	0
ORR	1 0 0	0 0 3 (Or)	1	0	1	1	0
SLT	1 0 0	0 0 4 (Set Less Than)	1	0	1	1	0
LSL	1 0 0	0 0 5 (Logical Shift Left)	1	0	1	1	0
LSR	1 0 0	0 0 6 (Logical Shift Right)	1	0	1	1	0
ADDI	1 0 1	0 0 0 (Add)	0	0	1	1	0
SUBI	1 0 1	0 0 1 (Subtract)	0	0	1	1	0
ANDI	1 0 1	0 0 2 (And)	0	0	1	1	0
ORRI	1 0 1	0 0 3 (Or)	0	0	1	1	0
SLTI	1 0 1	0 0 4 (Set Less Than)	0	0	1	1	0
LSLI	1 0 1	0 0 5 (Logical Shift Left)	0	0	1	1	0
LSRI	1 0 1	0 0 6 (Logical Shift Right)	0	0	1	1	0
CBE	0 0 0	0 0 1 (Sub)	0	1	0	0	0
LDUR	0 0 1	0 0 0 (Add)	0	0	0	1	0
STUR	0 1 0	0 0 0 (Add)	0	0	0	0	1