ai14865b
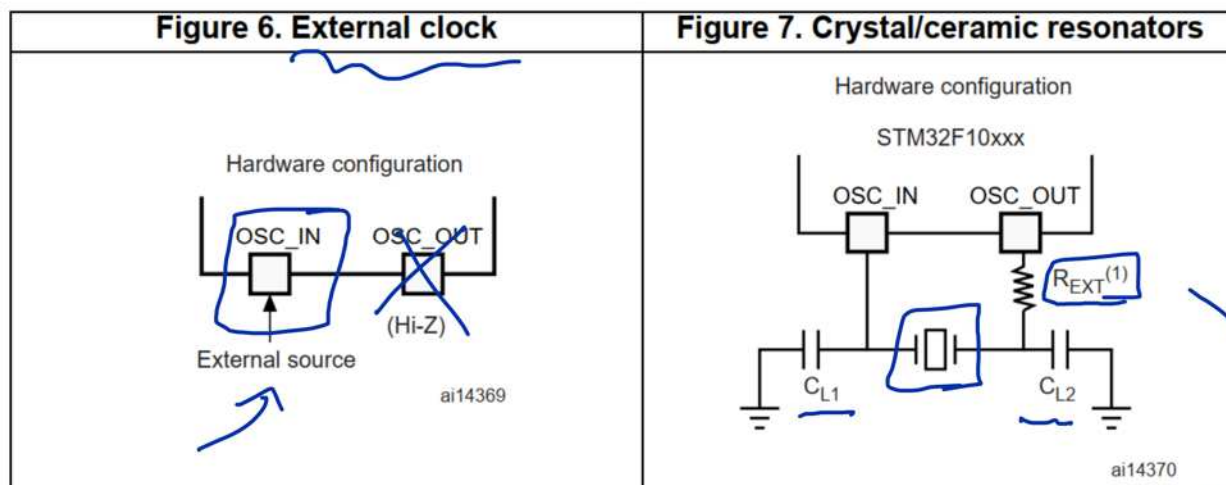

HSE OSC clock

The high-speed external clock signal (HSE) can be generated from two clock sources:

- HSE external crystal/ceramic resonator (see *Figure 7*)
- HSE user external clock (see *Figure 6*)

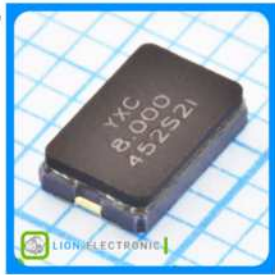| Figure 6. External clock	Figure 7. Crystal/ceramic resonators

1. The value of R_{EXT} depends upon the crystal characteristics. Typical value is in the range of 5 to 6 R_S (resonator series resistance).

2. Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 and 7 pF. Refer to *Section 6* to minimize its value.

کریستال (YSX530GA) XTAL 8MHZ

Part Number	XTAL 8MHZ(YSX530GA)
Lion Part	2158
Manufacturer	YXC — YXC
Description	کریستال 8 مگاهرتز پکیج SMD5032-2P — 8MHz 20pF ±10ppm SMD5032-4P Crystals

Electrical Specifications

Item / Type	YSX530GA
Nominal Frequency Range	8 ~ 54 MHz
Vibration Mode	AT Fundamental
Load Capacitance	12pF, 20pF, or specify
Frequency Tolerance (at 25 ℃)	± 10 ppm, ± 20 ppm, or specify
Frequency Versus Temperature Characteristics	±20 ppm, or specify
Operating Temperature	- 20 ~ + 70 ℃ , - 40 ~ + 85 ℃, or specify
Storage Temperature	- 40 ~ + 85 ℃ , or specify
Shunt Capacitance	7 pF Max.
Level Of Drive	1~100 μ W Max. (10 uW typical)
Frequency Aging (at 25 ℃)	± 3 ppm / year Max.
Insulation Resistance	More Than 500MΩ at DC 100V

Equivalent Series Resistance(ESR)

Fundamental	
8 ~ 12 MHz	60 Ω ~ 80 Ω
12 ~ 25 MHz	40 Ω ~ 60 Ω
25 ~ 54 MHz	30 Ω ~ 40 Ω

3.1.1 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to:

- 24 MHz for STM32F100xx value line devices
- 25 MHz for STM32F101xx, STM32F102xx and STM32F103xx devices
- 50 MHz for connectivity line devices

The external clock signal (square, sine or triangle) with a duty cycle of about 50%, has to drive the OSC_IN pin while the OSC_OUT pin must be left in the high impedance state (see *Figure 7* and *Figure 6*).

3.1.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator frequency ranges from:

- 4 to 16 MHz on STM32F101xx, STM32F102xx and STM32F103xx devices
- 4 to 24 MHz for STM32F100xx value line devices
- 3 to 25 MHz on connectivity line devices

The external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in *Figure 7*.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF-to-25 pF range (typ.), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitances must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).
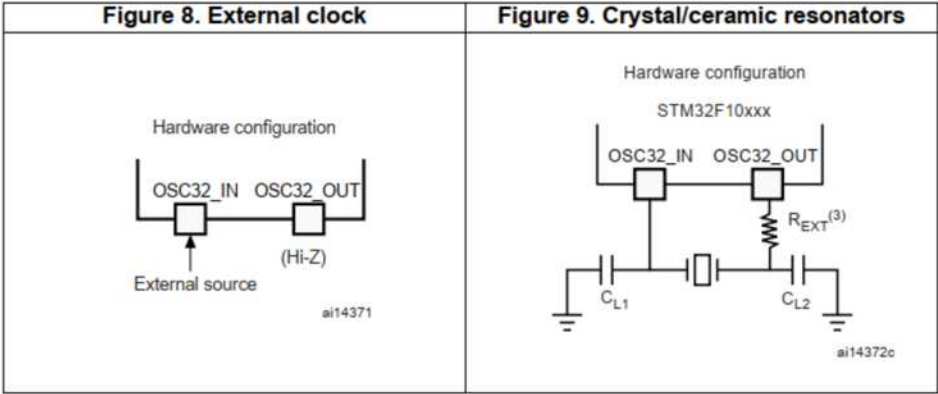
Refer to the electrical characteristics sections in the datasheet for more details.

3.2 LSE OSC clock

The low-speed external clock signal (LSE) can be generated from two possible clock sources:

- LSE external crystal/ceramic resonator (see *Figure 9*)
- LSE user external clock (see *Figure 8*)

Figure 8. External clock	Figure 9. Crystal/ceramic resonators

Note: 1   **"External clock" figure:**
To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF), it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.

2   **"External clock" and "crystal/ceramic resonators" figures:**
OSC32_IN and OSC_OUT pins can be used also as GPIO, but it is recommended not to use them as both RTC and GPIO pins in the same application.

3   **"Crystal/ceramic resonators" figure:**
The value of R_{EXT} depends on the crystal characteristics. A 0 Ω resistor works, but it is not optimal. Typical value is in the range of 5 to 6 R_S (resonator series resistance). To fine tune R_S value refer to AN2867 - Oscillator design guide for ST microcontrollers.

کریستال ساعت XKXGI-SUA-32.768K

Part Number	XKXGI-SUA-32.768K
Lion Part	4290
Manufacturer	YXC
Description	کریستال 32.768 کیلوهرتز پکیج SMD3215-2P 32.768kHz 12.5pF ±20ppm SMD3215-2P Crystals

موجودی محصول 🛒 2,006

خرید 1

Full Reel: 3000

در صورت کمبود موجودی محصول می توانید آنرا به لیست استعلام اضافه نمایید تا توسط کارشناسان واحد سفارشات خارجی بررسی شده و نتیجه به شما اطلاع داده شود

افزودن به لیست استعلام

قیمت محصول

1.Absolute maximum ratings

Parameter(电气参数)	Symbol	Min.（最小值）	Typ.(典型值）	Max.（最大值）	Unit（单位）
Storage temperature（储存温度）	T_stg	-55	-	125	°C
Maximum drive level（最大激励功率）	GL	-	0.1	-	µW

2.Specifications (characteristics)(规格参数)

Parameter(电气参数)	Symbol	Min.（最小值）	Typ.(典型值）	Max.（最大值）	Unit（单位）
Type (型号)			YST310S		
Cutting Mode （切割方式）			☑ X +2°		
Nominal frequency（标称频率）	f_nom	-	32.768	-	KHz
Frequency tolerance at 25ºC（常温频差）	f_tol	-20	-	20	x 10⁻⁶
Parabolic Coefficient(温飘系数)	B	-	-	- 0.04	x 10⁻⁶ / ℃2
Load capacitance(负载电容)	CL	-	12.5	-	pF
Motional resistance (ESR)（等效谐振电阻）	R1	-	-	70	KΩ
Shunt capacitance （静电容）	C0	-	-	1.4	pF
Motional capacitance （动态电容）	C1	-	-	3	fF
Operating temperature （工作温度）	T_use	-40	-	85	°C
Frequency aging（老化率）	f_age	-3	-	3	x10⁻⁶ /year

3.2.1 External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency up to 1 MHz. The external clock signal (square, sine or triangle) with a duty cycle of about 50% must drive the OSC32_IN pin, while the OSC32_OUT pin must be left high impedance (see *Figure 9* and *Figure 8*).

3.2.2 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator. It has the advantage of providing a low-power, but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

4.1 Boot mode selection

In the STM32F10xxx, three different boot modes can be selected by means of the BOOT[1:0] pins, as shown in *Table 2*.

Table 2. Boot modes

BOOT mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main flash memory	Main flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

The values on the BOOT pins are latched on the fourth rising edge of SYSCLK after a reset. It is up to the user to set the BOOT1 and BOOT0 pins after reset to select the required boot mode.

The BOOT pins are also resampled when exiting the Standby mode. Consequently, they must be kept in the required Boot mode configuration in the Standby mode. After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, and starts code execution from the boot memory, starting from 0x0000 0004.

4.3 Embedded boot loader mode

The Embedded boot loader mode is used to reprogram the flash memory using one of the available serial interfaces:

- In low-density, low-density value line, medium-density, medium-density value line, and high-density devices, the boot loader is activated through the USART1 interface. For further details refer to AN2606.
- In XL-density devices, the boot loader is activated through the USART1 or USART2 (remapped) interface. For further details refer to AN2606.
- In connectivity line devices the boot loader can be activated through one of the following interfaces: USART1, USART2 (remapped), CAN2 (remapped) or USB OTG FS in Device mode (DFU: device firmware upgrade).
  The USART peripheral operates with the internal 8 MHz oscillator (HSI). The CAN and USB OTG FS, however, can only function if an external 8 MHz, 14.7456 MHz or 25 MHz clock (HSE) is present. For further details, refer to AN2662.

This embedded boot loader is located in the System memory and is programmed by ST during production.

ai14373
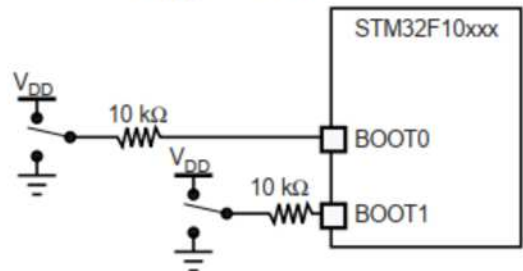
Figure 12. JTAG connector implementation
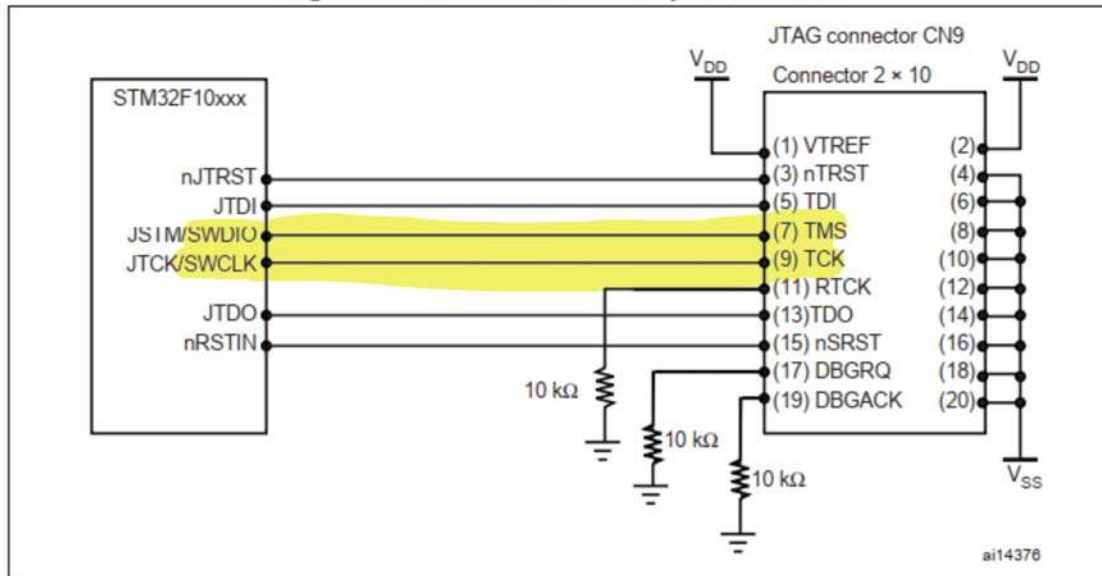
Table 5. Mandatory components

Id	Name	Reference	Quantity	Comments
1	Microcontroller	STM32F103ZE(T6)	1	144-pin package
2	Capacitors	100 nF	11	Ceramic capacitors (decoupling capacitors)
3	Capacitor	10 µF	1	Ceramic capacitor (decoupling capacitor)

Table 6. Optional components

Id	Name	Reference	Quantity	Comments
1	Resistor	10 kΩ	5	Pull-up and pull-down for JTAG and Boot mode.
2	Resistor	390 Ω	1	Used for HSE: the value depends on the crystal characteristics. This resistor value is given only as a typical example.
3	Resistor	0 Ω	1	Used for LSE: the value depends on the crystal characteristics. This resistor value is given only as a typical example.
4	Capacitor	100 nF	3	Ceramic capacitor
5	Capacitor	1µF	2	Used for VDDA and VREF.
6	Capacitor	10 pF	2	Used for LSE: the value depends on the crystal characteristics.
7	Capacitor	20 pF	2	Used for HSE: the value depends on the crystal characteristics.
8	Quartz	8 MHz	1	Used for HSE
9	Quartz	32 kHz	1	Used for LSE
10	JTAG connector	HE10	1	-
11	Battery	3V3	1	If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}
12	Switch	3V3	2	Used to select the correct boot mode.
13	Push-button	B1	1	-

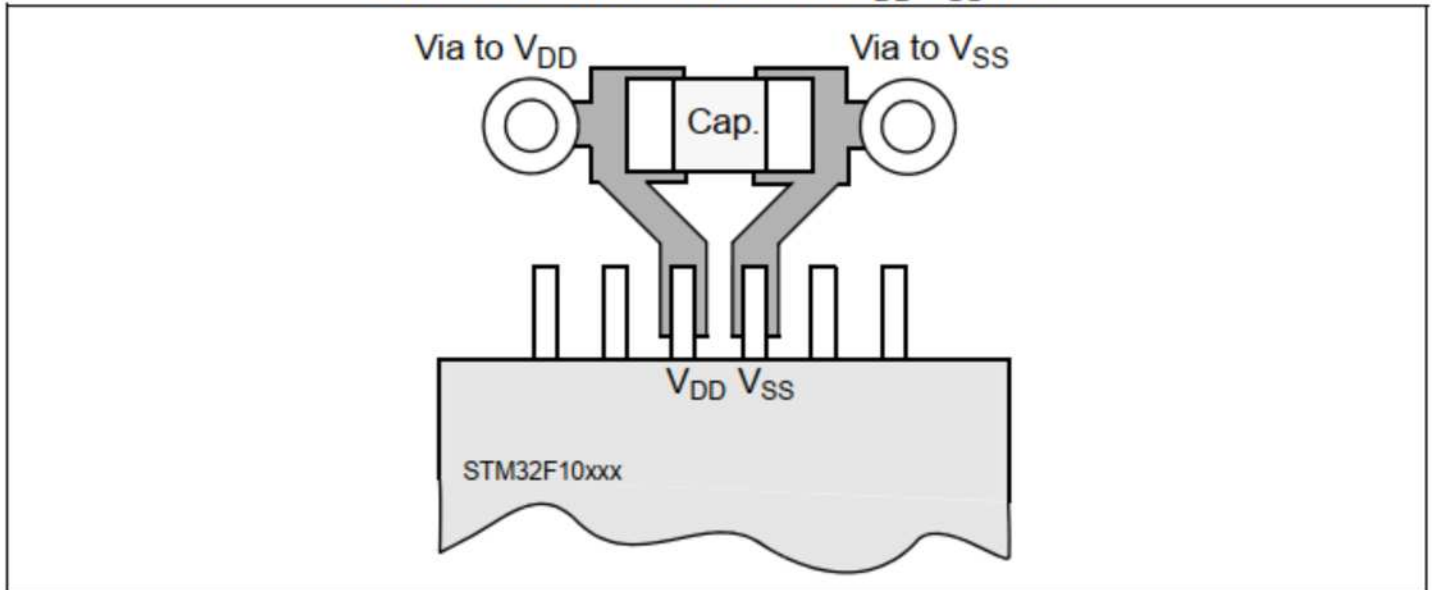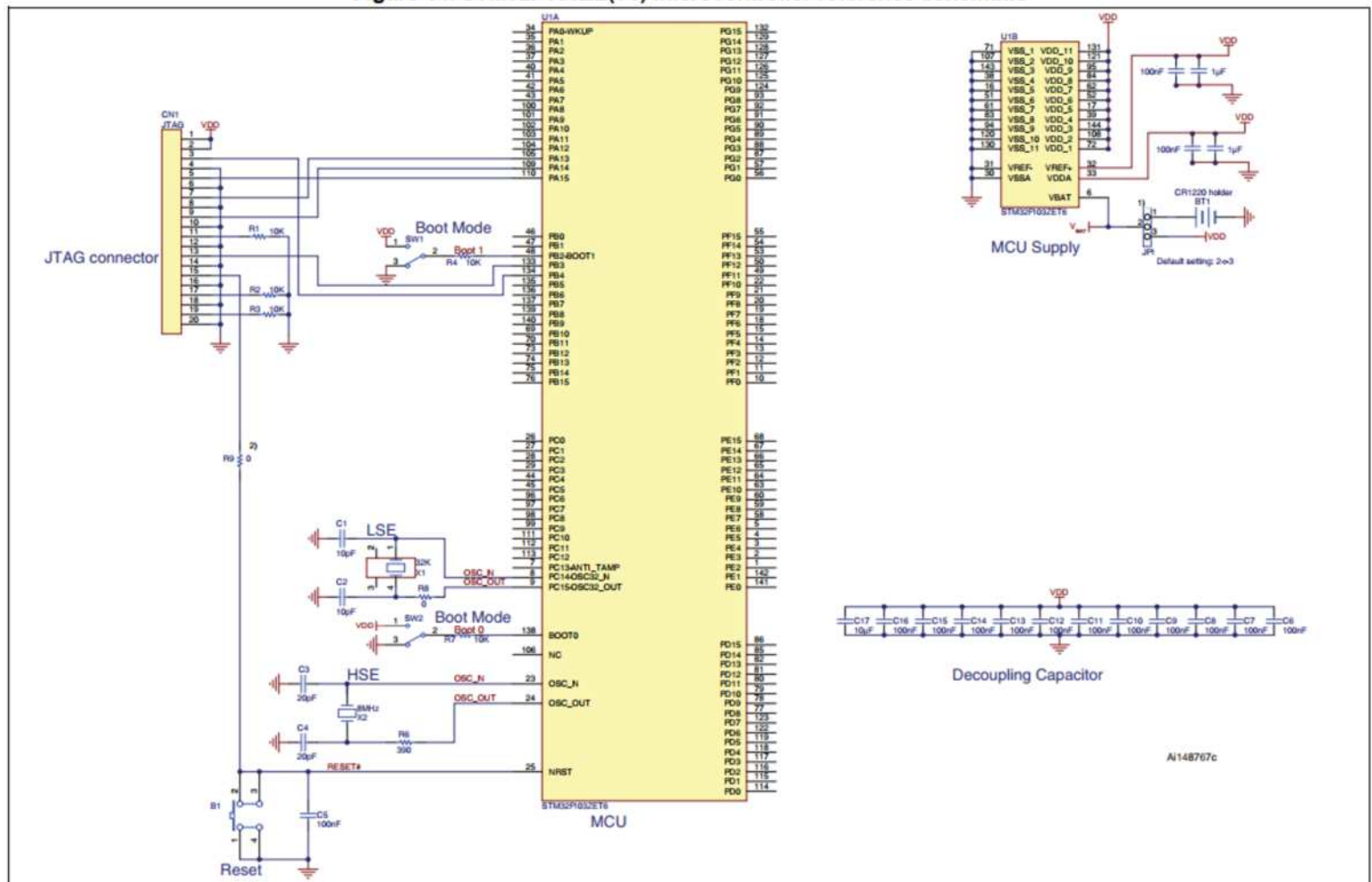# Figure 13. Typical layout for V_{DD}/V_{SS} pair

Figure 14. STM32F103ZE(T6) microcontroller reference schematic

1. If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.
2. To be able to reset the device from the tools this resistor must be kept.