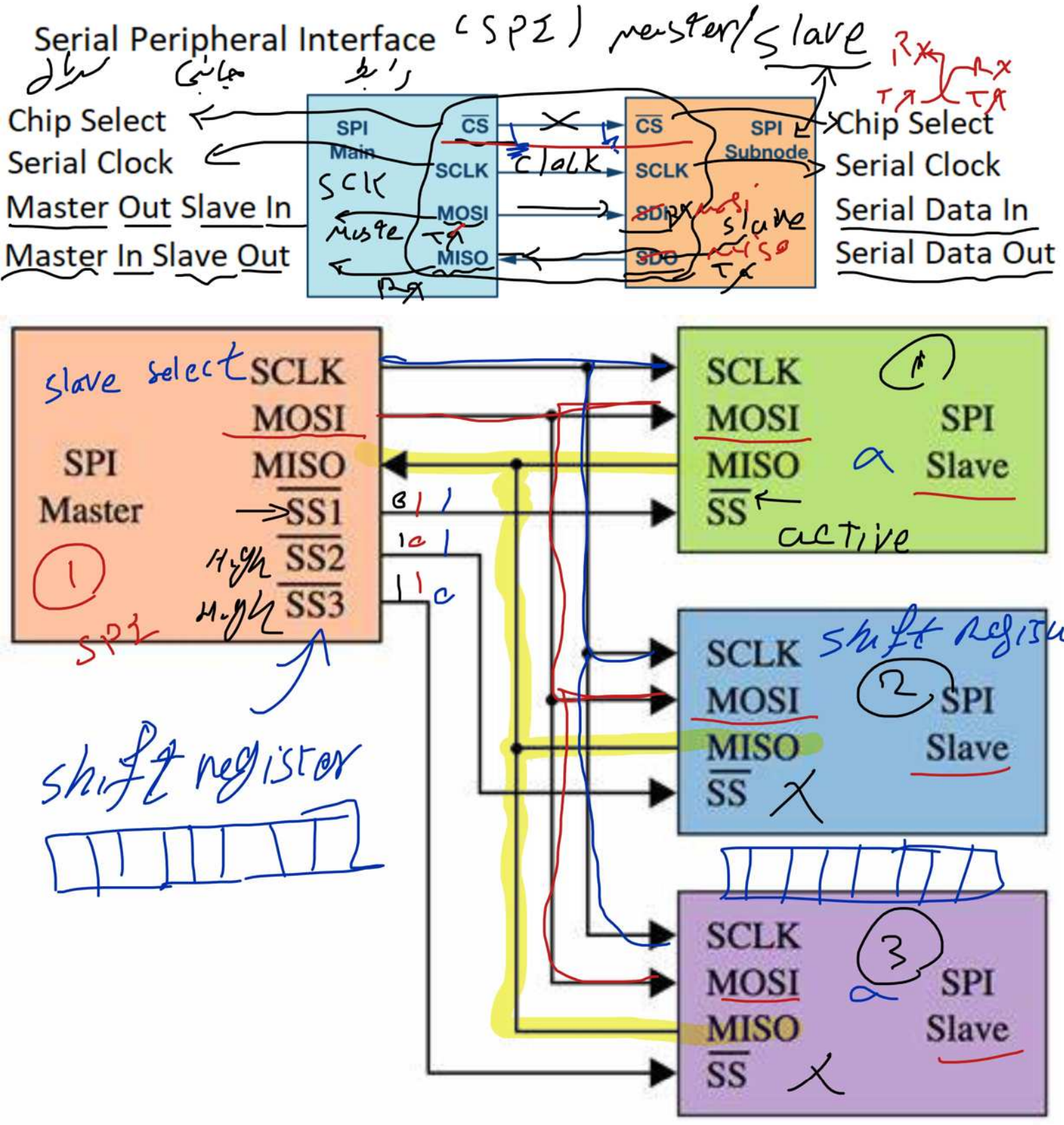
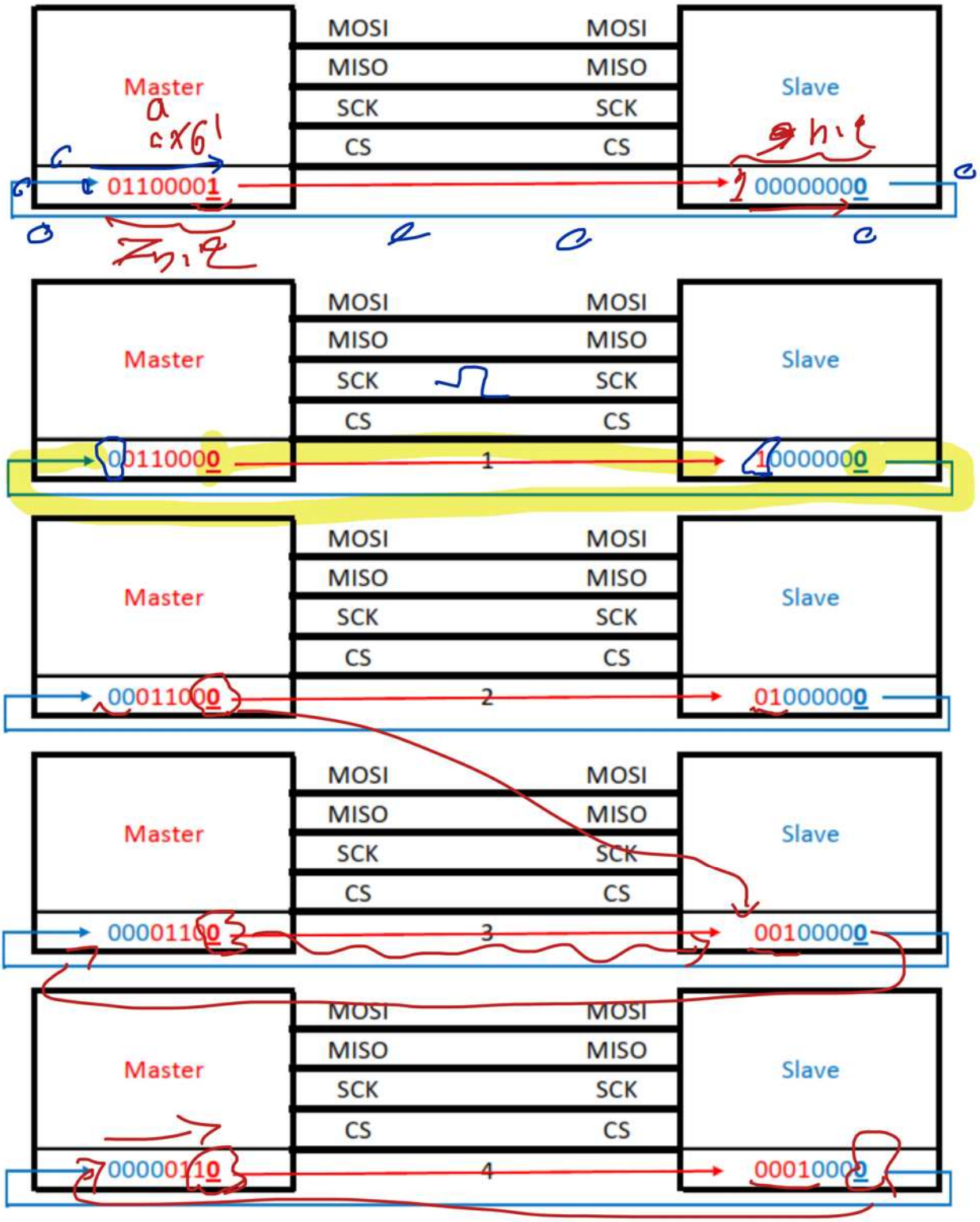

Serial Peripheral Interface
Chip Select
Serial Clock
Master Out Slave In
Master In Slave Out
SPI Main
CS
SCLK
MOSI
MISO
SPI Subnode
Chip Select
Serial Clock
Serial Data In
Serial Data Out
SPI Master
SCLK
MOSI
MISO
SS1
SS2
SS3
SPI Slave
active
shift register
Shift Register
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
Data In
Data Out
Clock
MOSI
SCK
MISO
Master
Slave


Master
Slave
MOSI
MISO
SCK
CS
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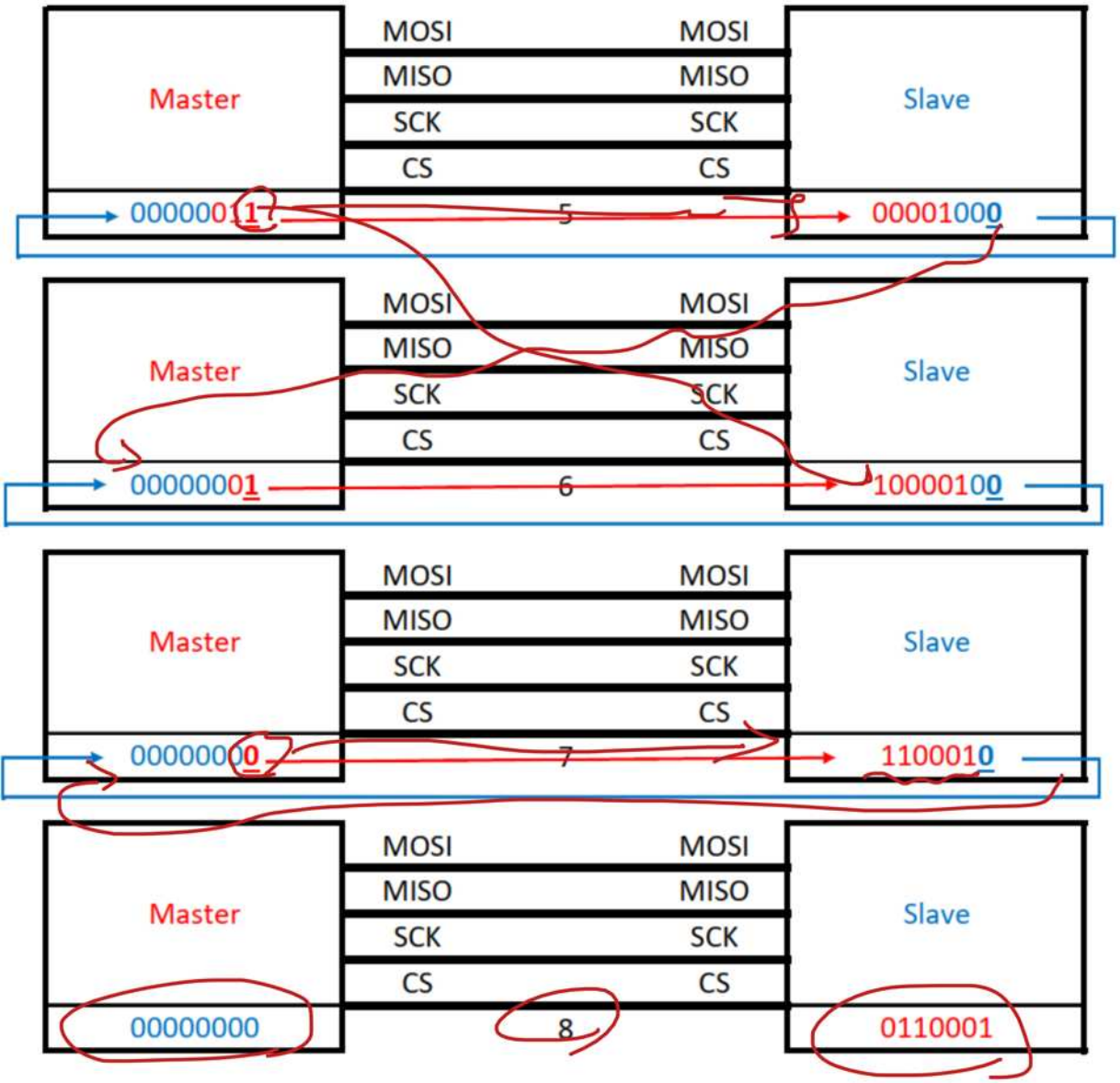
00000000
00110000
10000000
00011000
01000000
00001100
00100000
00000110
00010000
1
2
3
4


Master
Slave
MOSI
MISO
SCK
CS
MOSI
MISO
SCK
CS
00000011
5
00001000
Master
Slave
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MISO
SCK
CS
MOSI
MISO
SCK
CS
00000001
6
10000100
Master
Slave
MOSI
MISO
SCK
CS
MOSI
MISO
SCK
CS
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Slave
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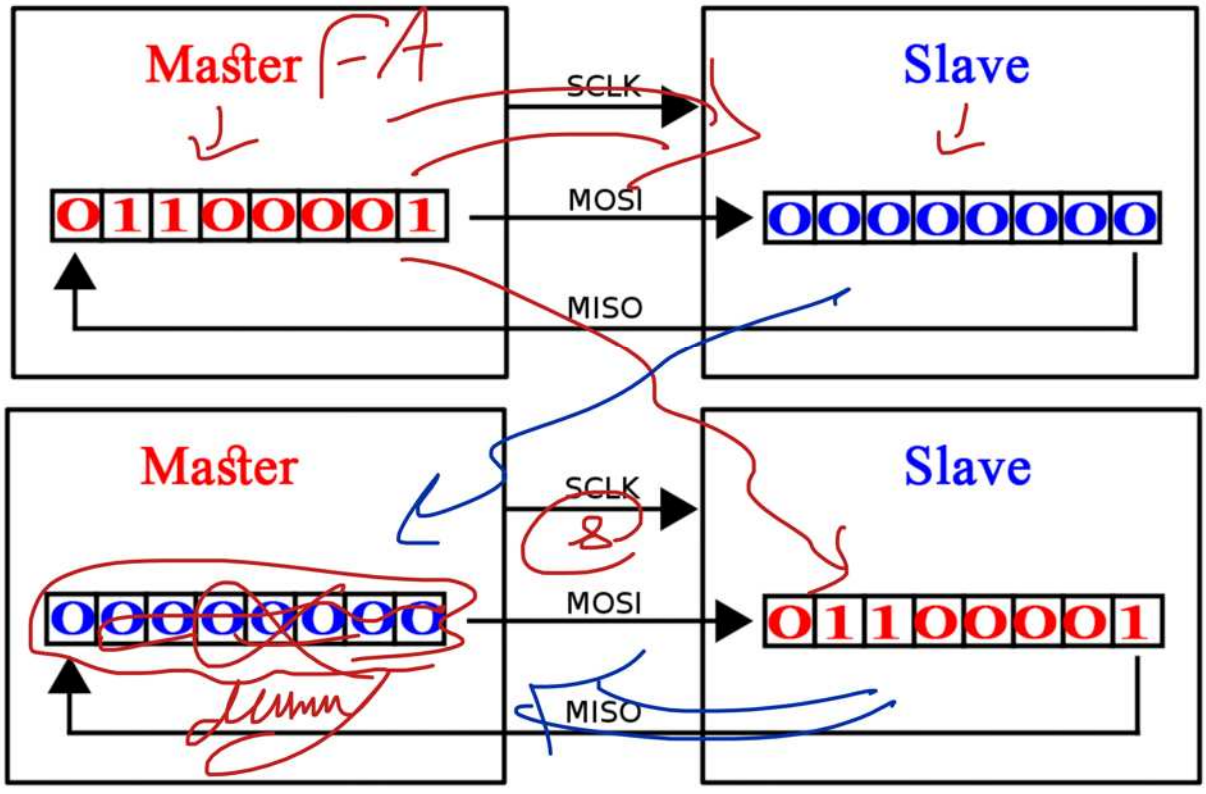
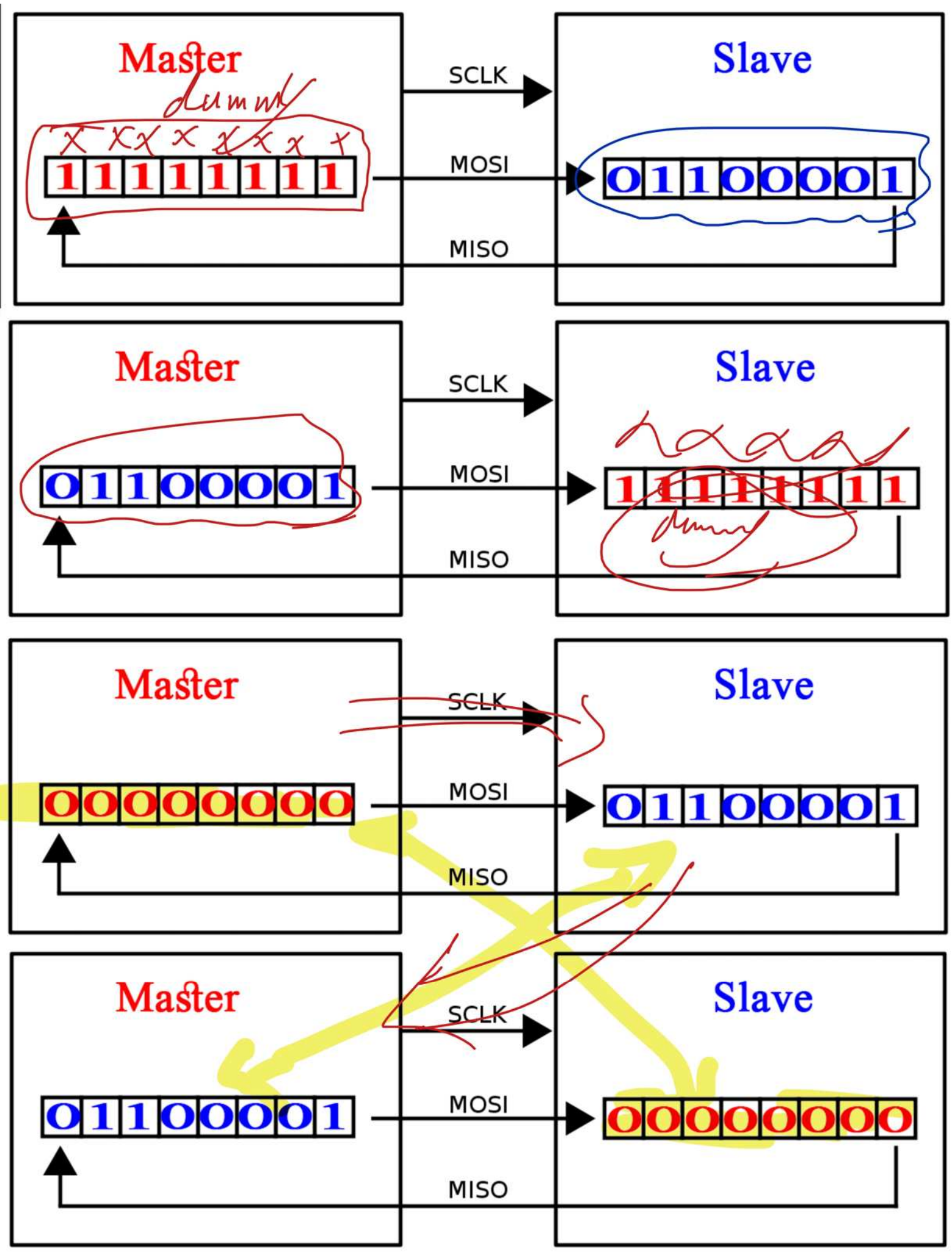
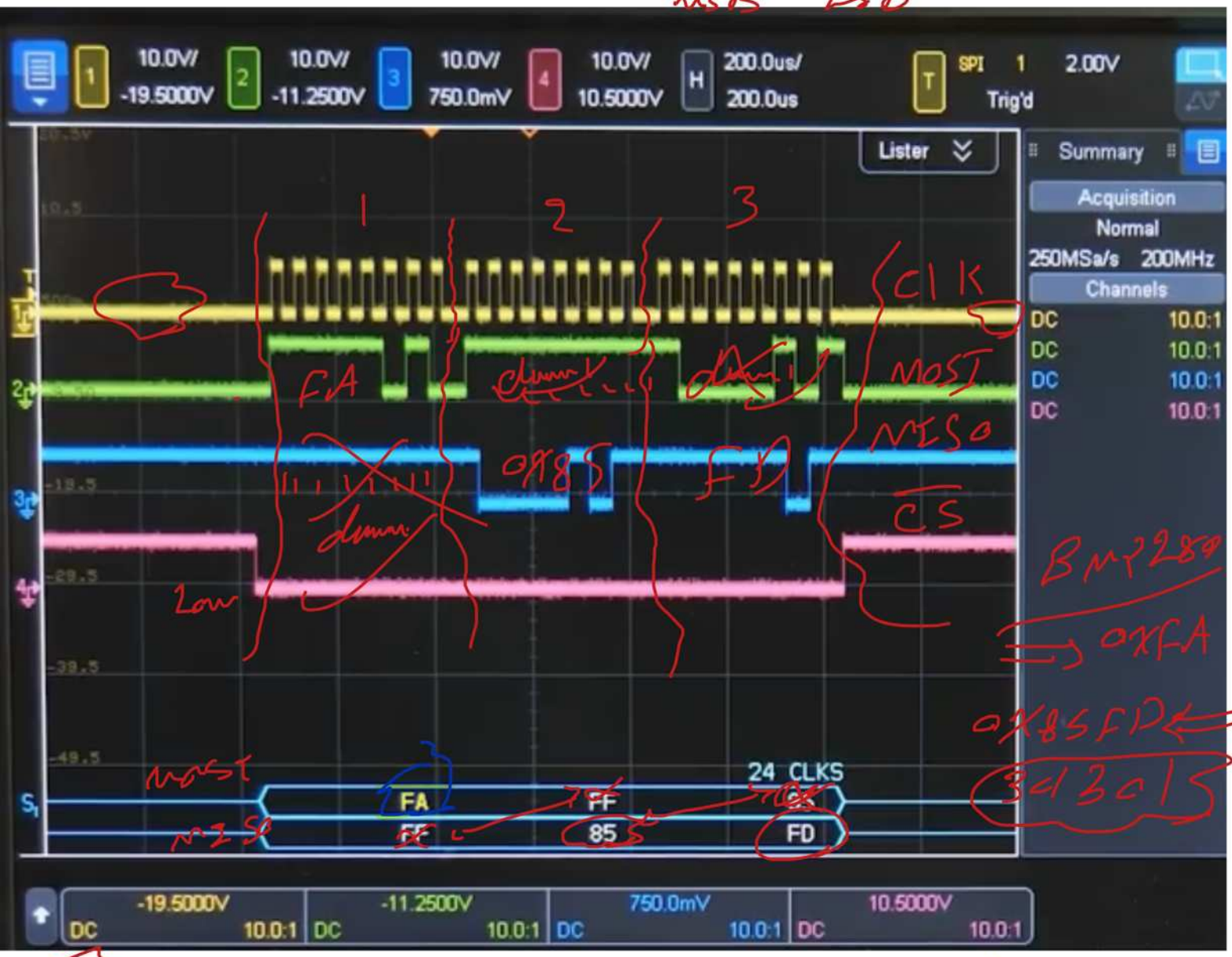
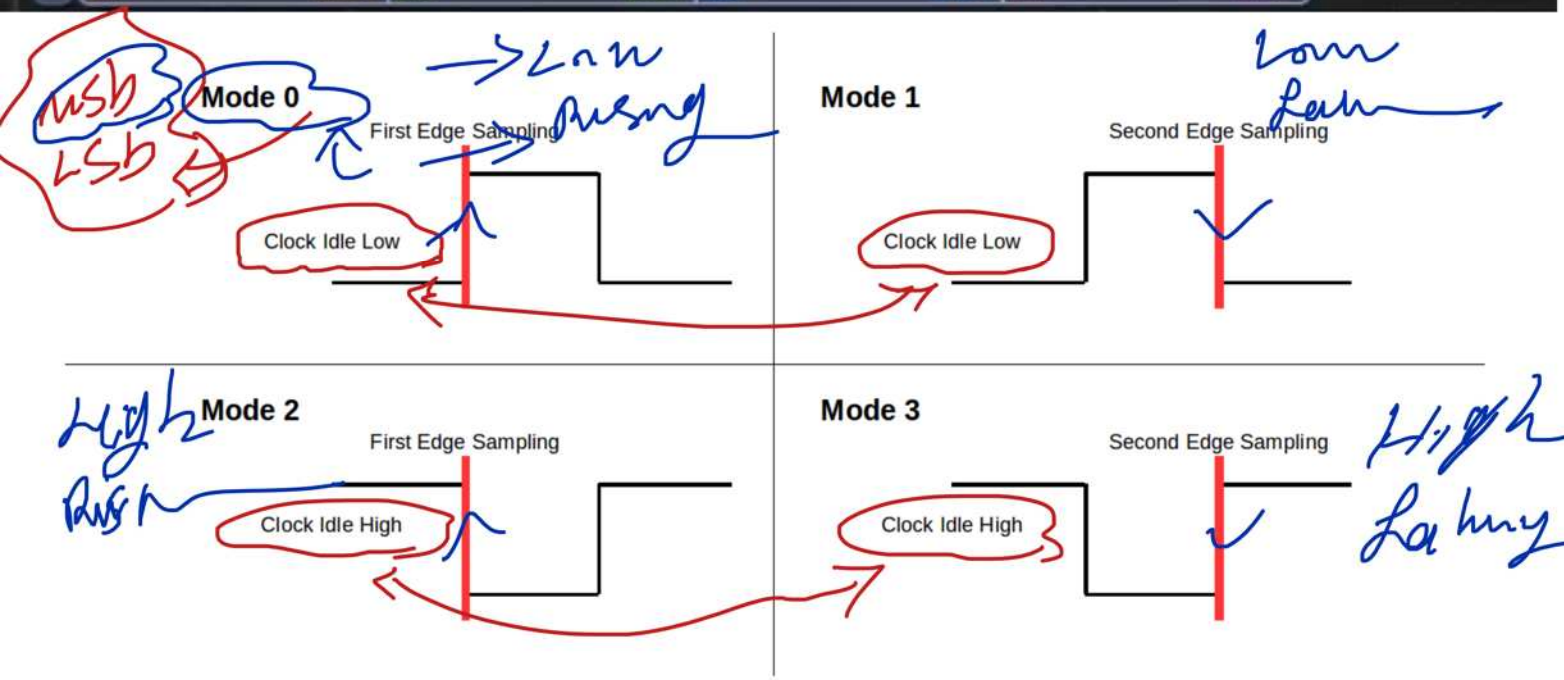
MISO
SCK
CS
MOSI
MISO
SCK
CS
00000000
8
0110001

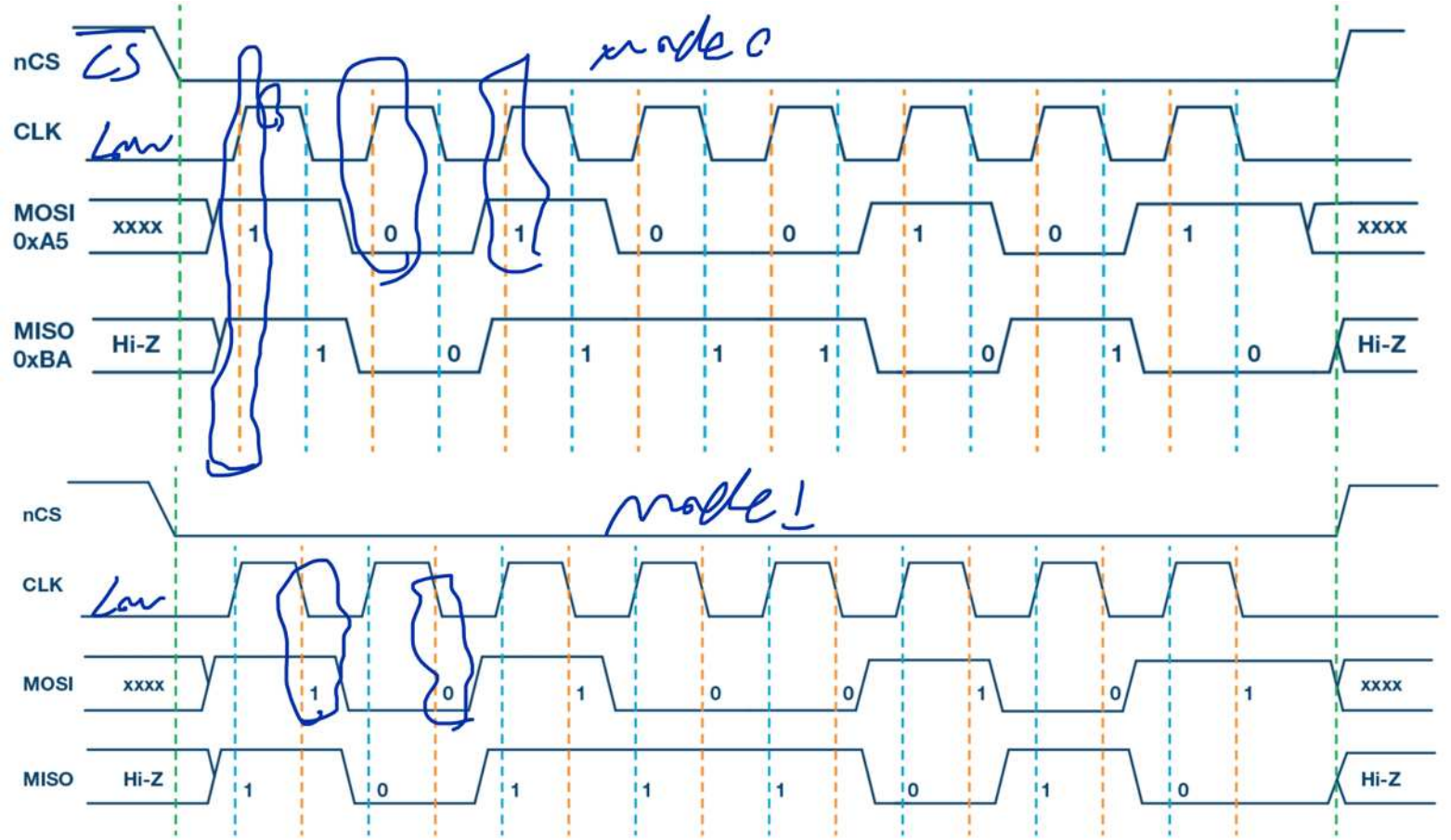

Master
Slave
SCLK
MOSI
MISO
0 1 1 0 0 0 0 1
0 0 0 0 0 0 0 0
Master
Slave
SCLK
8
MOSI
MISO
0 0 0 0 0 0 0 0
0 1 1 0 0 0 0 1


Master
Slave
SCLK
MOSI
MISO
1 1 1 1 1 1 1 1
0 1 1 0 0 0 0 1
Master
Slave
SCLK
MOSI
MISO
0 1 1 0 0 0 0 1
1 1 1 1 1 1 1 1
Master
Slave
SCLK
MOSI
MISO
0 0 0 0 0 0 0 0
0 1 1 0 0 0 0 1
Master
Slave
SCLK
MOSI
MISO
0 1 1 0 0 0 0 1
0 0 0 0 0 0 0 0

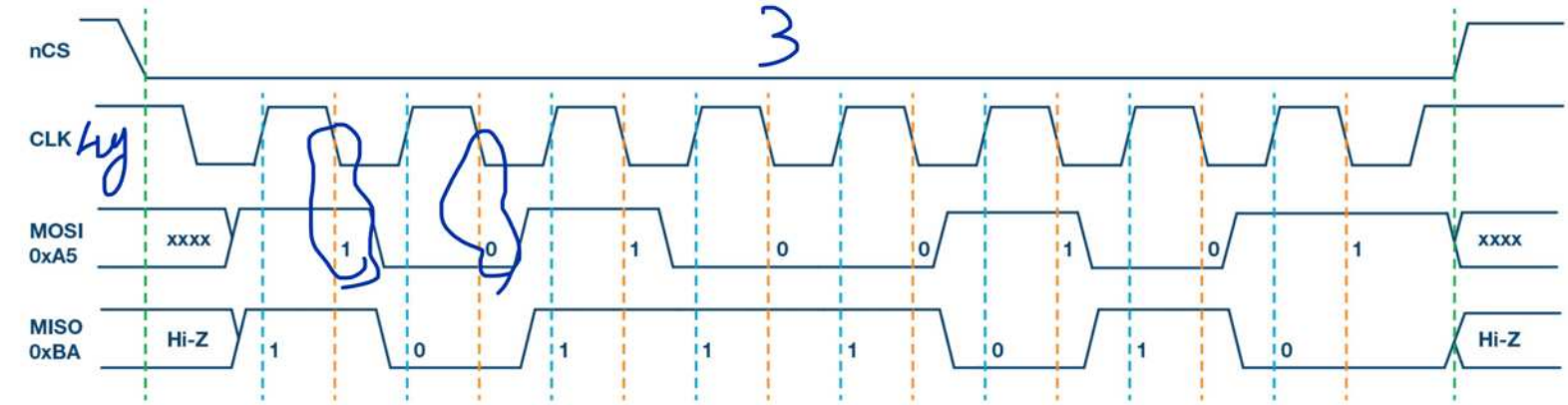
BMP280 0xFA 0x~ 0x~
MSB LSB

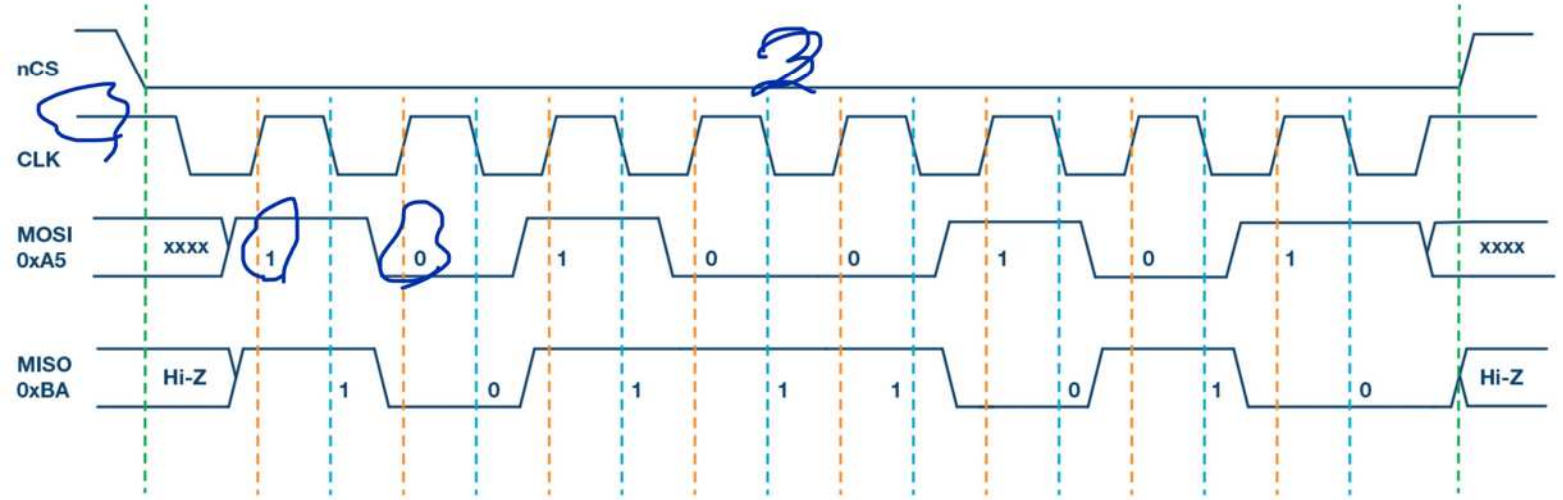


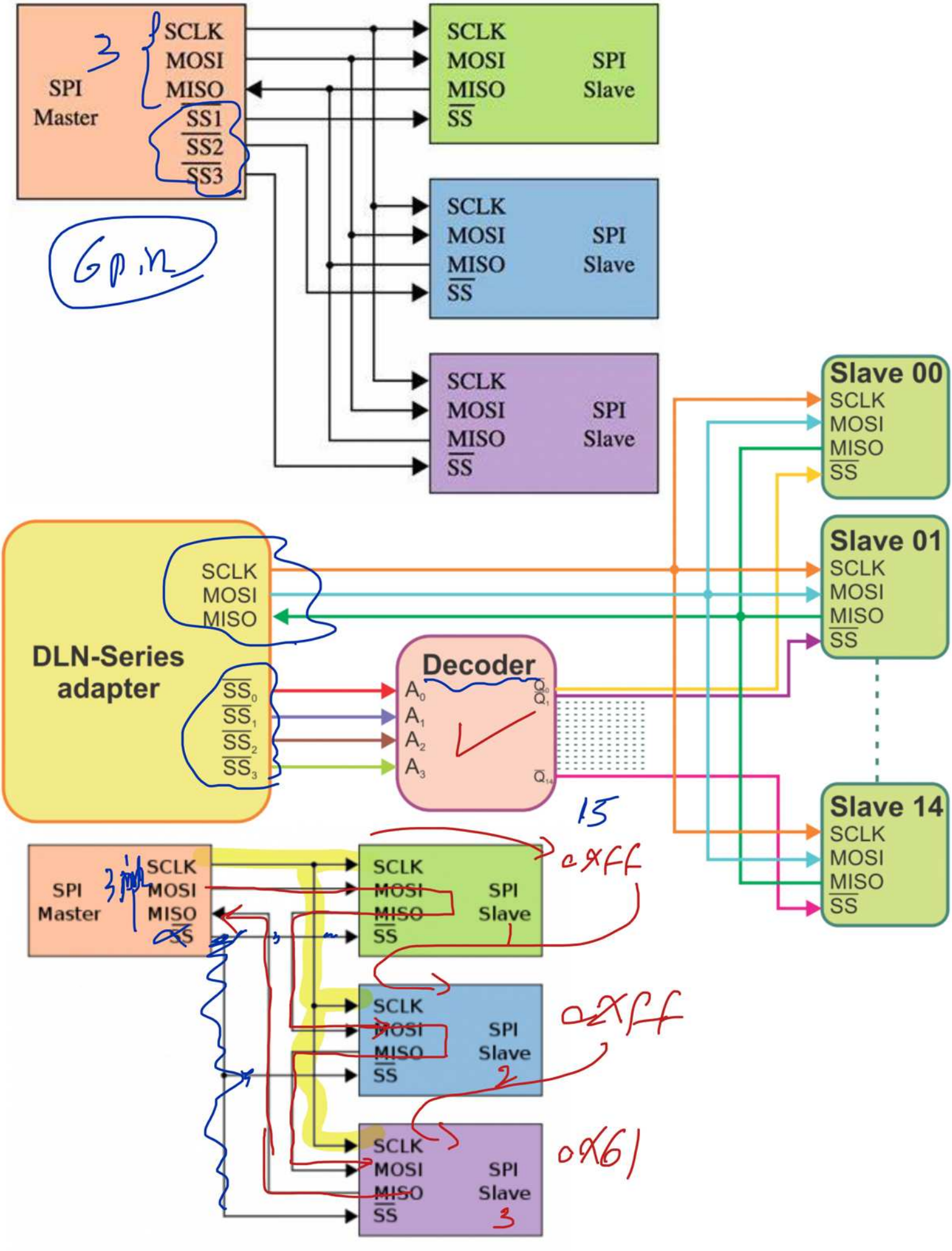


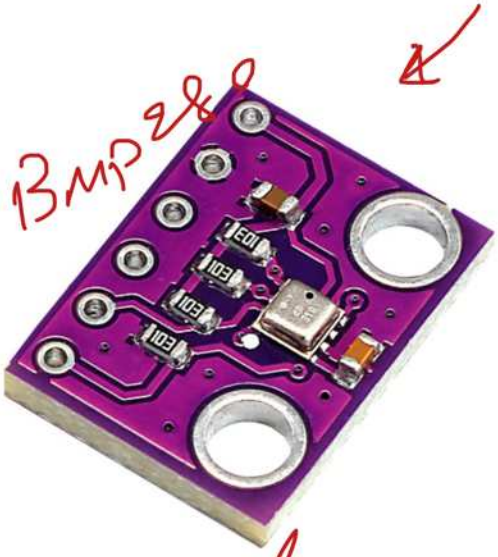

nCS
CLK
MOSI
0xA5
MISO
0xBA
xxxx
Hi-Z
1
0
1
0
0
1
0
1
xxxx
1
0
1
1
1
0
1
0
Hi-Z

nCS
CLK
MOSI
MISO
xxxx
Hi-Z
1
0
1
0
0
1
0
1
xxxx
1
0
1
1
1
0
1
0
Hi-Z


nCS
CLK
MOSI
0xA5
MISO
0xBA
xxxx
Hi-Z
1
0
1
0
0
1
0
1
xxxx
1
0
1
1
1
0
1
0
Hi-Z

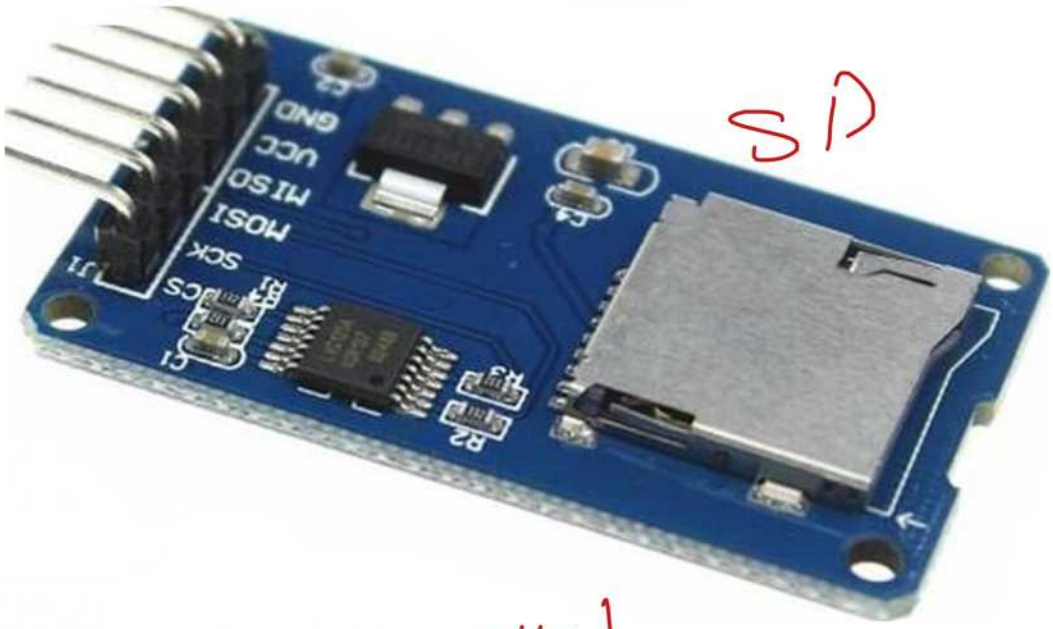

nCS
CLK
MOSI
0xA5
MISO
0xBA
xxxx
Hi-Z
1
0
1
0
0
1
0
1
xxxx
1
0
1
1
1
0
1
0
Hi-Z


SPI Master
SCLK
MOSI
MISO
SS1
SS2
SS3
SPI Slave
SCLK
MOSI
MISO
SS
SPI Slave
SCLK
MOSI
MISO
SS
SPI Slave
SCLK
MOSI
MISO
SS
Slave 00
SCLK
MOSI
MISO
SS
Slave 01
SCLK
MOSI
MISO
SS
Slave 14
SCLK
MOSI
MISO
SS
DLN-Series adapter
SCLK
MOSI
MISO
SS0
SS1
SS2
SS3
Decoder
A0
A1
A2
A3
Q0
Q1
Q14
15
SPI Master
SCLK
MOSI
MISO
SS
SPI Slave
SCLK
MOSI
MISO
SS
SPI Slave
SCLK
MOSI
MISO
SS
SPI Slave
SCLK
MOSI
MISO
SS
0xff
0xff
0x61

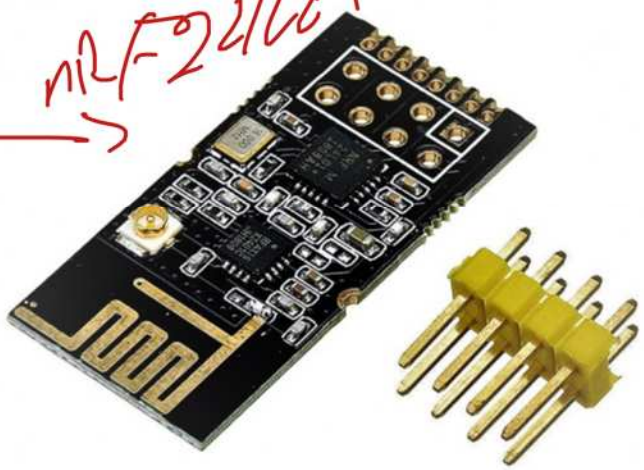

Bmp280


RFID-RC522
RFID

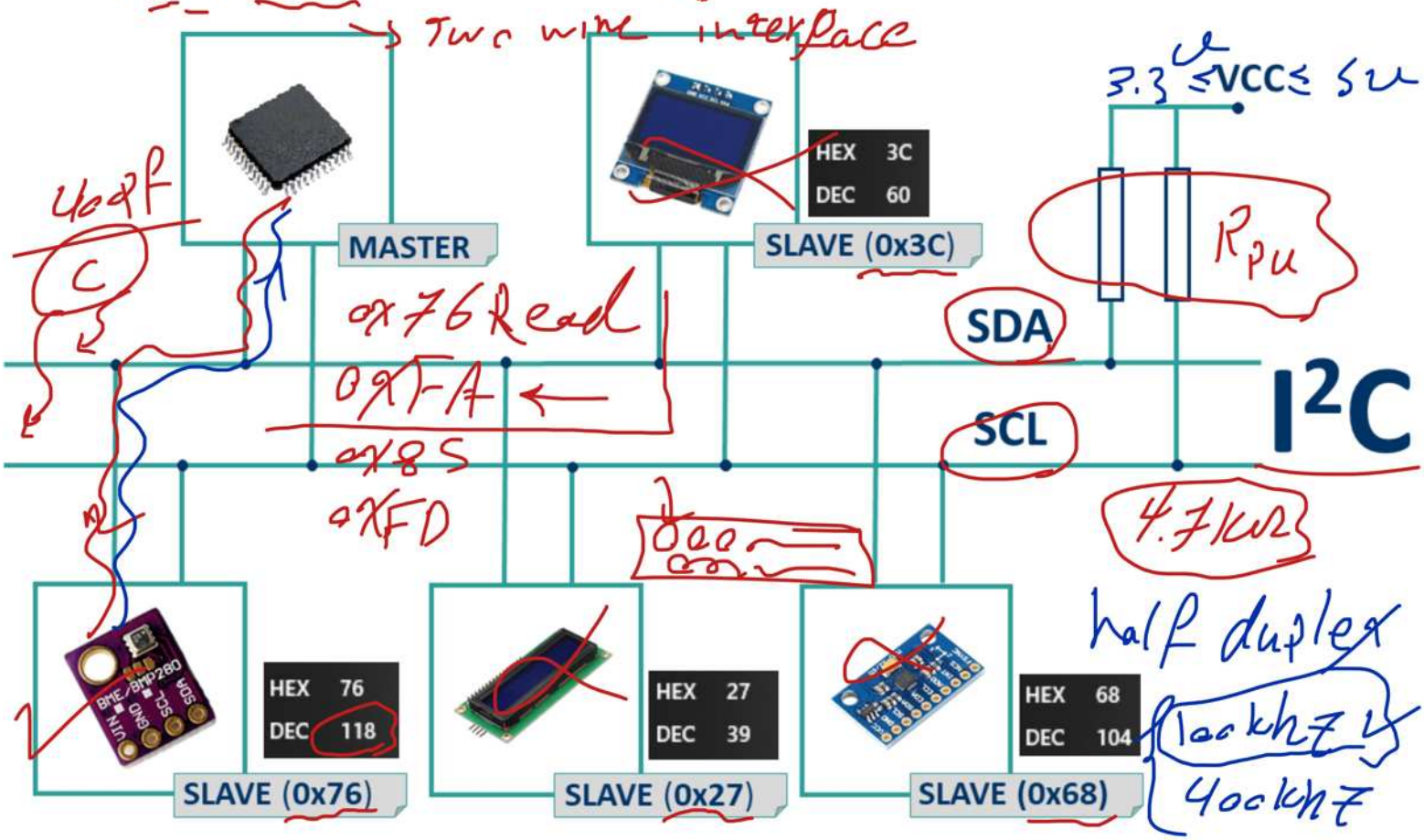

oled
Color: Yellow Blue

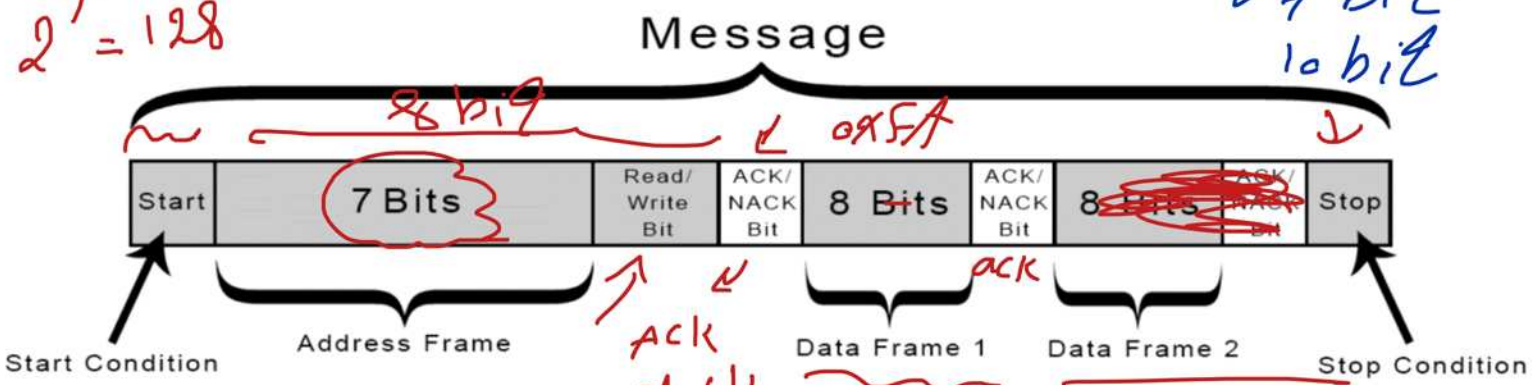

SD
GND
VCC
MISO
MOSI
SCK
CS

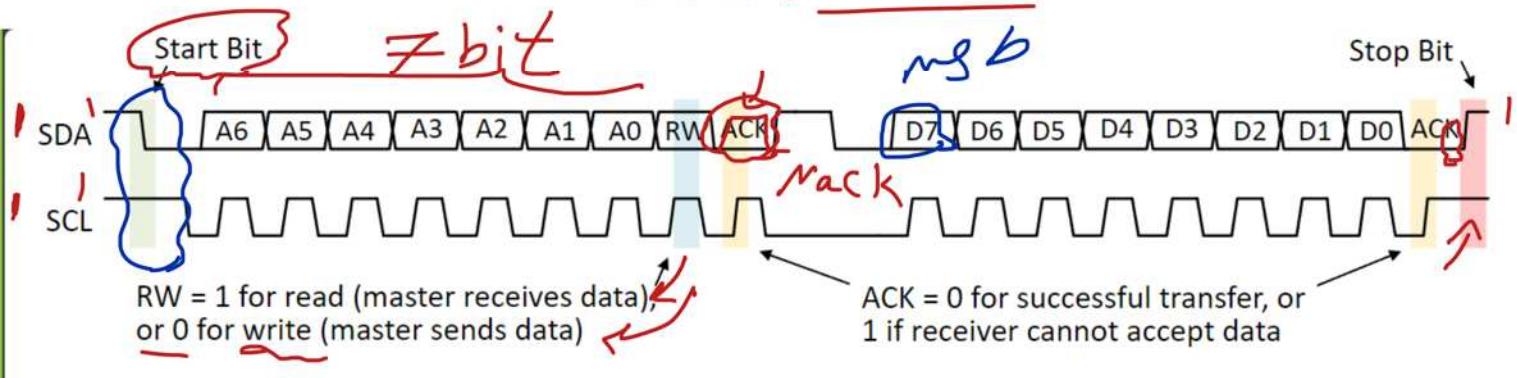

Lora

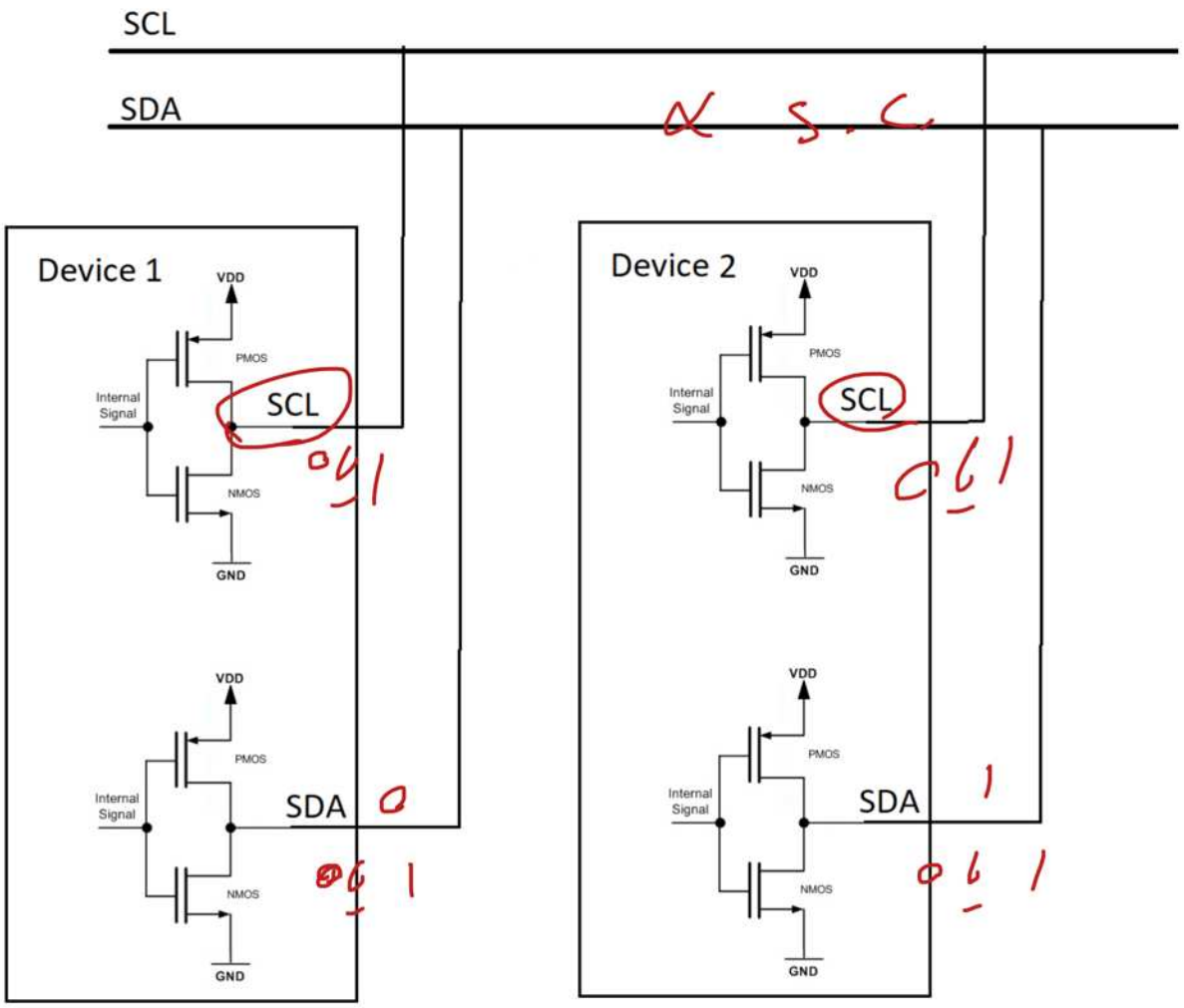

nRF24l01

I2C, IIC, TWI = Inter-Integrated Circuit

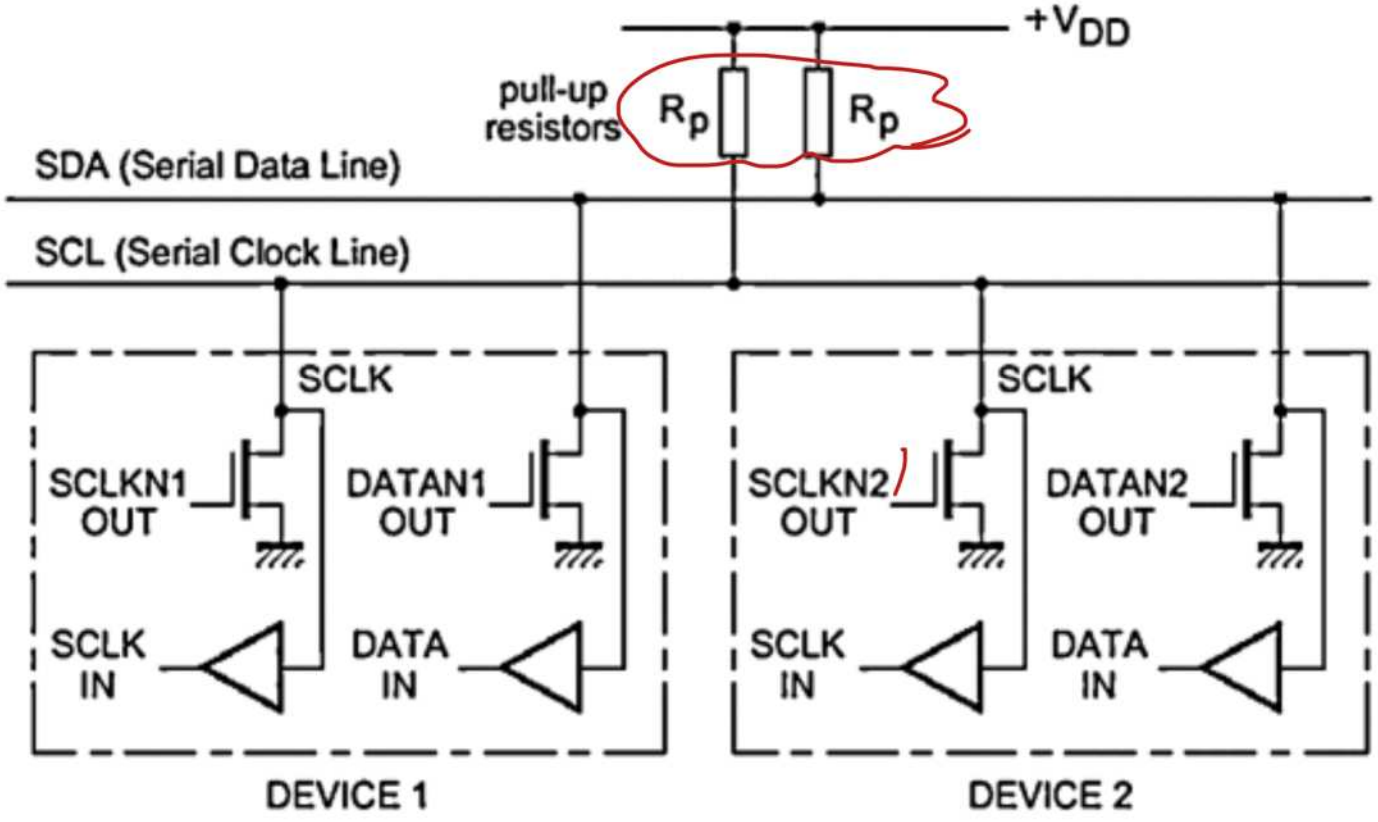







SCL
SDA
Device 1
VDD
PMOS
Internal Signal
SCL
NMOS
GND
SDA
Device 2

push-pull

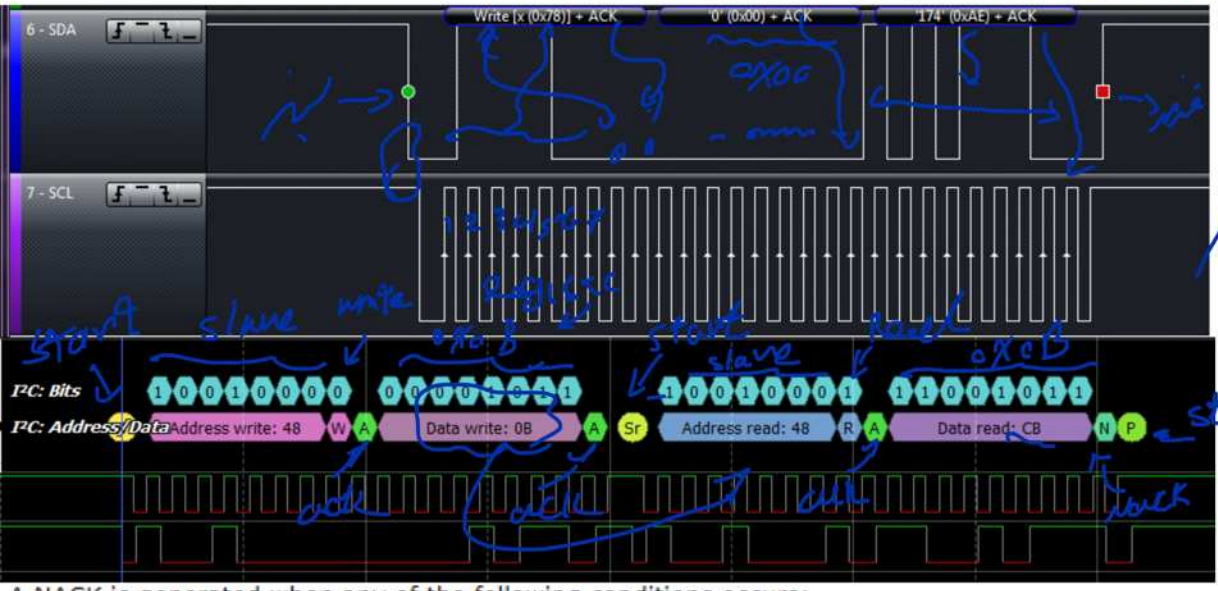

+VDD
pull-up resistors
Rp
Rp
SDA (Serial Data Line)
SCL (Serial Clock Line)
SCLK
SCLKN1 OUT
DATAN1 OUT
SCLK IN
DATA IN
DEVICE 1
SCLKN2 OUT
DATAN2 OUT
DEVICE 2

Write Sequence

1) Send the start condition
2) Send the slave address
3) Check for the acknowledge
4) Send the sub-address to be written to
5) Check for the acknowledge from
6) Send the data to write to specified sub address
7) Check for the acknowledge
8) If No-acknowledge send the stop condition
9) Send a stop condition

Read Sequence

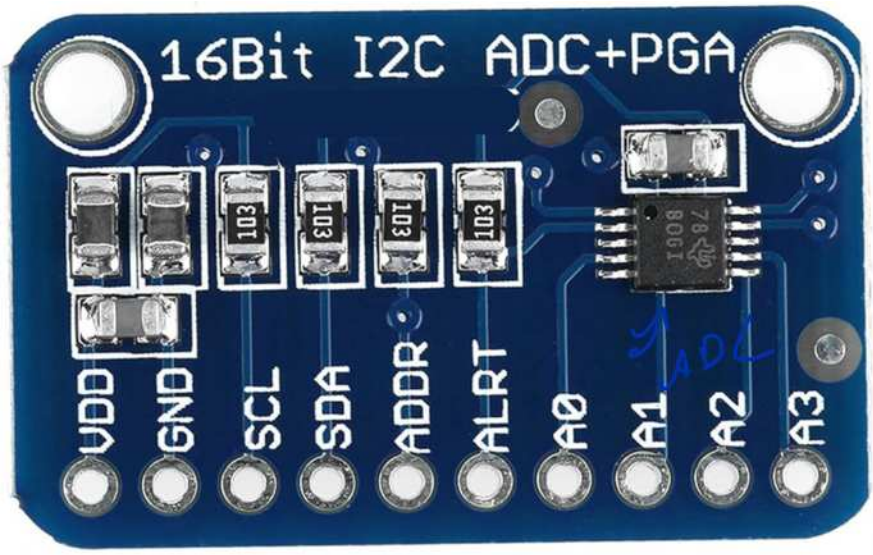
1) Send the start condition
2) Send the slave address + write
3) check for the acknowledge
4) Send the sub-address to be read from
5) check for the acknowledge
6) Send the start condition
7) Send the slave address + Read
8) check for the acknowledge
9) If No-acknowledge send the stop condition
10) If acknowledged read the data from specified sub-address
12) Send a No-Acknowledge
13) Send a stop condition



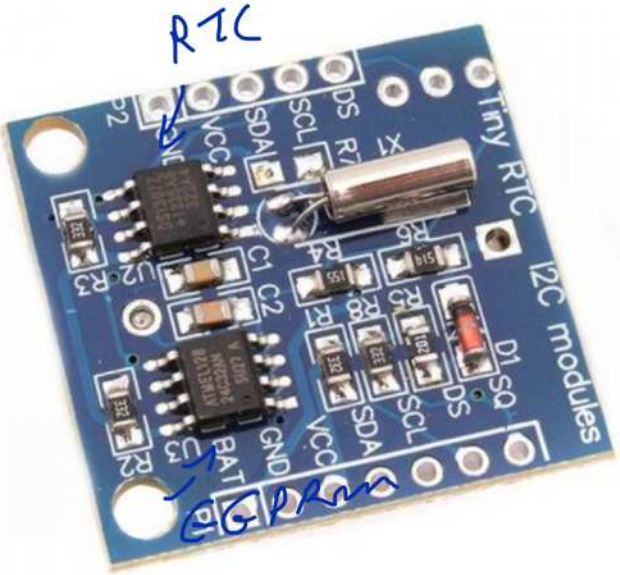
A NACK is generated when any of the following conditions occurs:

- No slave device is present on the bus that owns the transmitted address
- The receiver is busy and is not ready for communication
- The receiver gets data or commands that it cannot understand
- The receiver cannot receive any more data
- A master-receiver has received the requested data and is ready to terminate transmission
- An I²C Error condition has occurred

Slave Address	R/W Bit	Description
000 0000	0	General call address
000 0000	1	START byte[1]
000 0001	X	CBUS address[2]
000 0010	X	Reserved for different bus format[3]
000 0011	X	Reserved for future purposes
000 01XX	X	Hs-mode master code
111 10XX	X	10-bit slave addressing
111 11XX	X	Reserved for future purposes



RTC

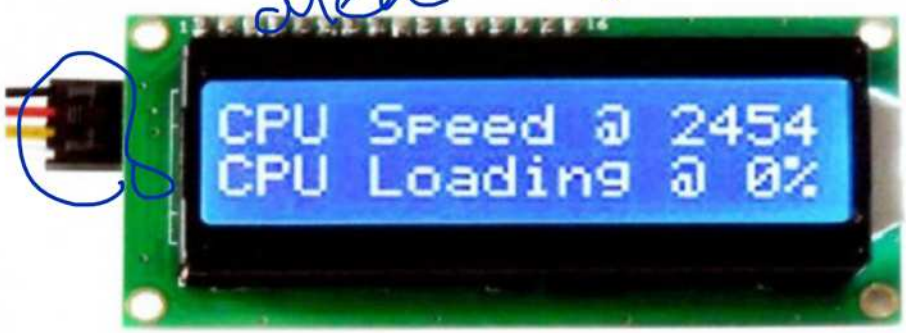


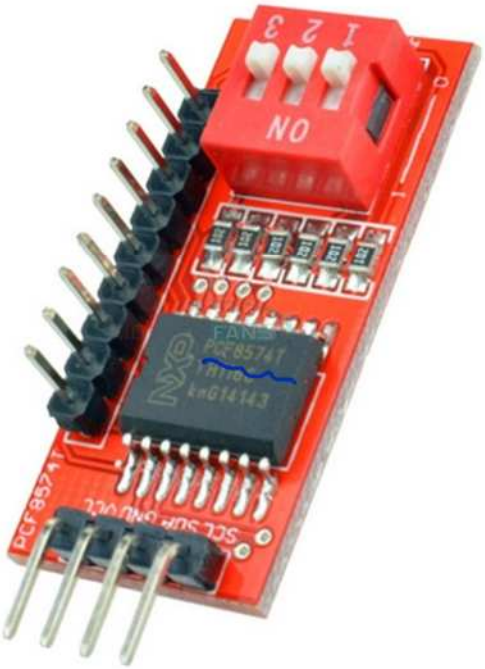
BMP280

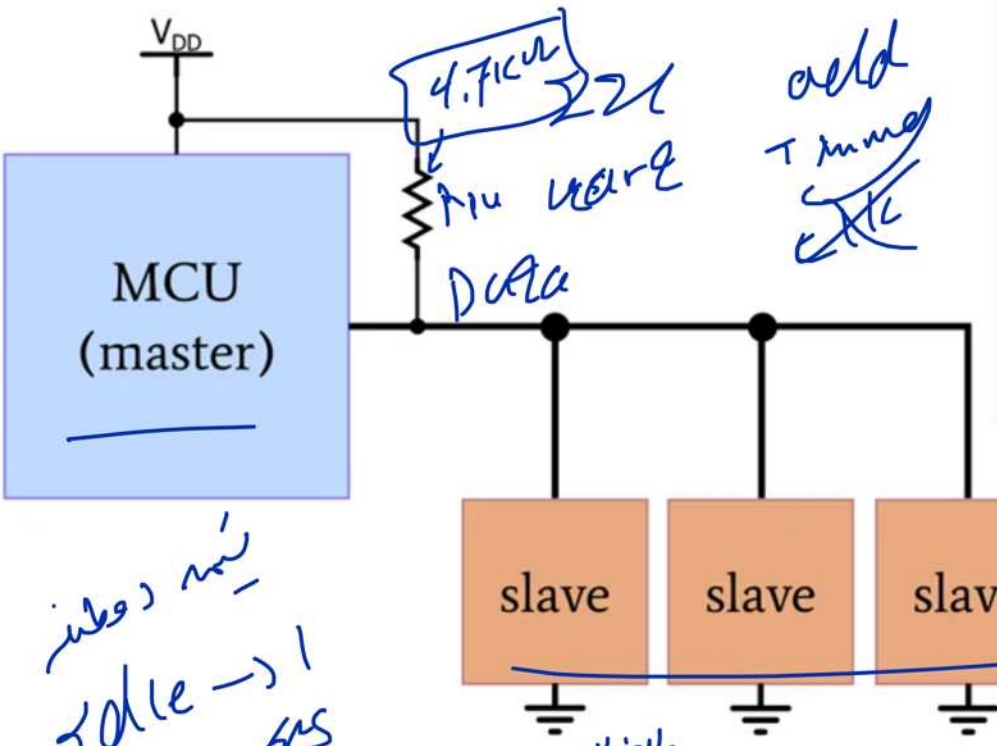
oled

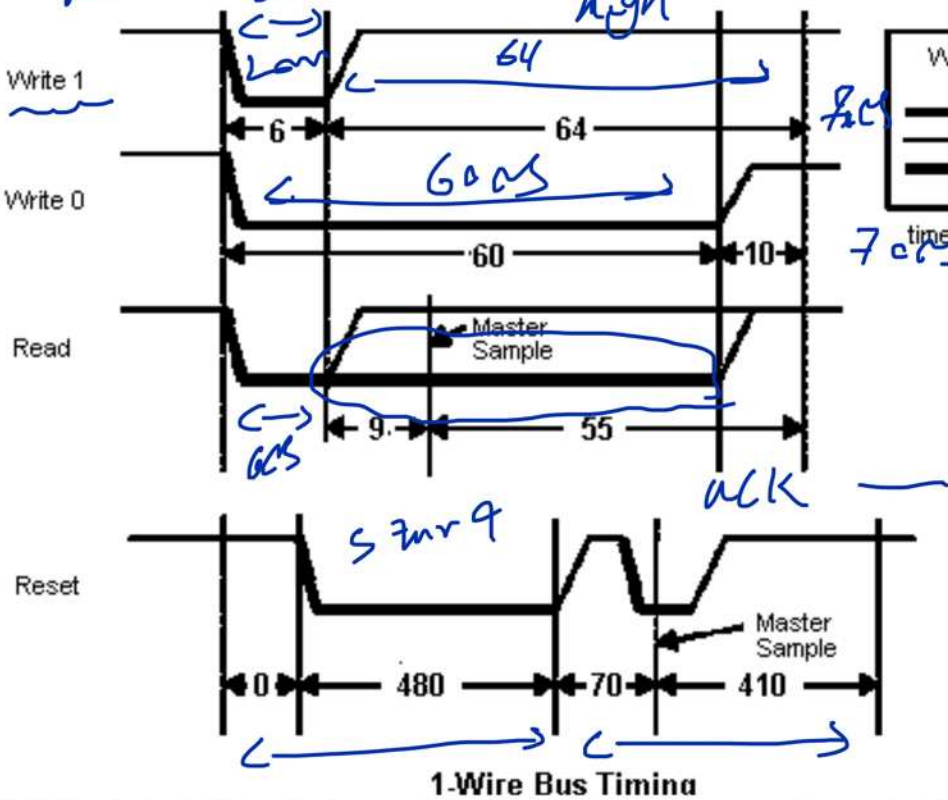
SR04

oled I2C





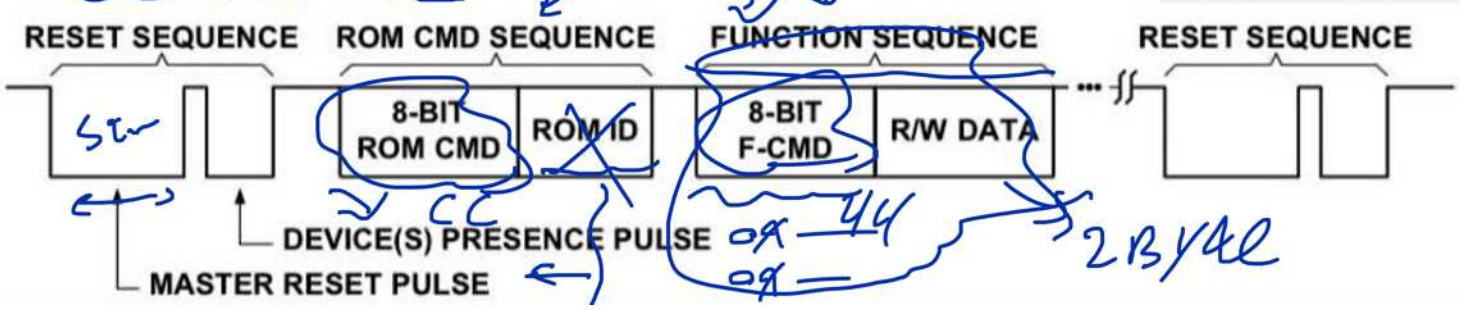


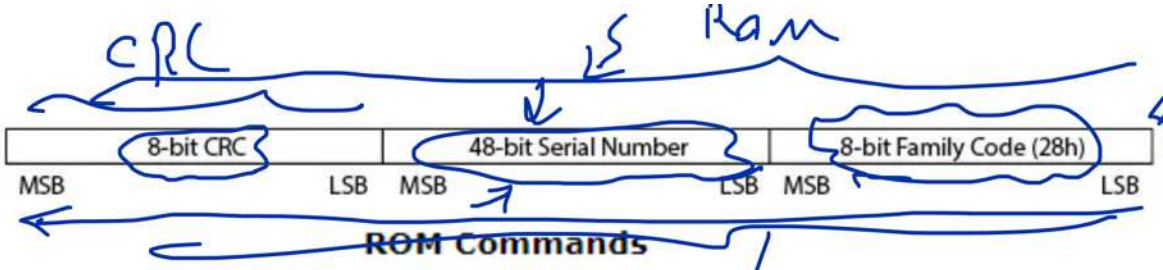


1-Wire Bus Timing

All 1-Wire devices follow a basic communication sequence:

1. The master sends the "Reset" pulse.
2. The slave(s) respond with a "Presence" pulse.
3. The master sends a ROM command. This effectively addresses one or several slave devices.
4. The master sends a Memory command.





ROM Commands

Command	Code	Usage
READ ROM	33H	Identification
SKIP ROM	CCH	Skip addressing
MATCH ROM	55H	Address specific device
SEARCH ROM	F0H	Obtain IDs of all devices on the bus
OVERDRIVE SKIP ROM	3CH	Overdrive version of SKIP ROM
OVERDRIVE MATCH ROM	69H	Overdrive version of MATCH ROM

Table 3. DS18B20 Function Command Set

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS ACTIVITY AFTER COMMAND IS ISSUED	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	DS18B20 transmits conversion status to master (not applicable for parasite-powered DS18B20s).	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	DS18B20 transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2, 3, and 4 (T_H, T_L, and configuration registers).	4Eh	Master transmits 3 data bytes to DS18B20.	3
Copy Scratchpad	Copies T_H, T_L, and configuration register data from the scratchpad to EEPROM.	48h	None	1
Recall E^2	Recalls T_H, T_L, and configuration register data from EEPROM to the scratchpad.	B8h	DS18B20 transmits recall status to master.	
Read Power Supply	Signals DS18B20 power supply mode to the master.	B4h	DS18B20 transmits supply status to master.	

RP 33 28 5A 2A FF 00 00 00 51

Serial number

Family ID

Read ROM

Presence pulse

Reset

CRC

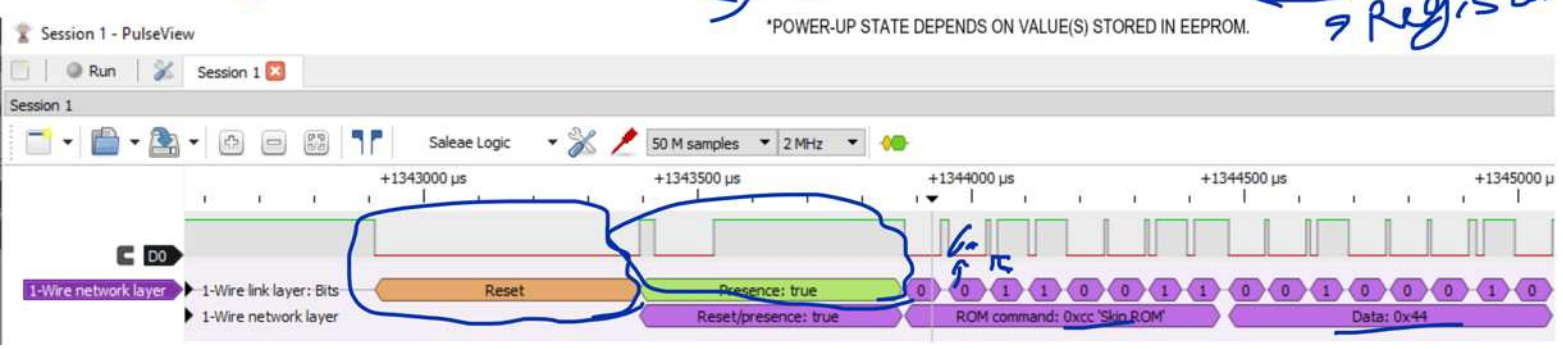
SCRATCHPAD (POWER-UP STATE)

BYTE 0	TEMPERATURE LSB (50h)	(85°C)
BYTE 1	TEMPERATURE MSB (05h)	
BYTE 2	T_H REGISTER OR USER BYTE 1*	
BYTE 3	T_L REGISTER OR USER BYTE 2*	
BYTE 4	CONFIGURATION REGISTER*	
BYTE 5	RESERVED (FFh)	
BYTE 6	RESERVED	
BYTE 7	RESERVED (10h)	
BYTE 8	CRC*	

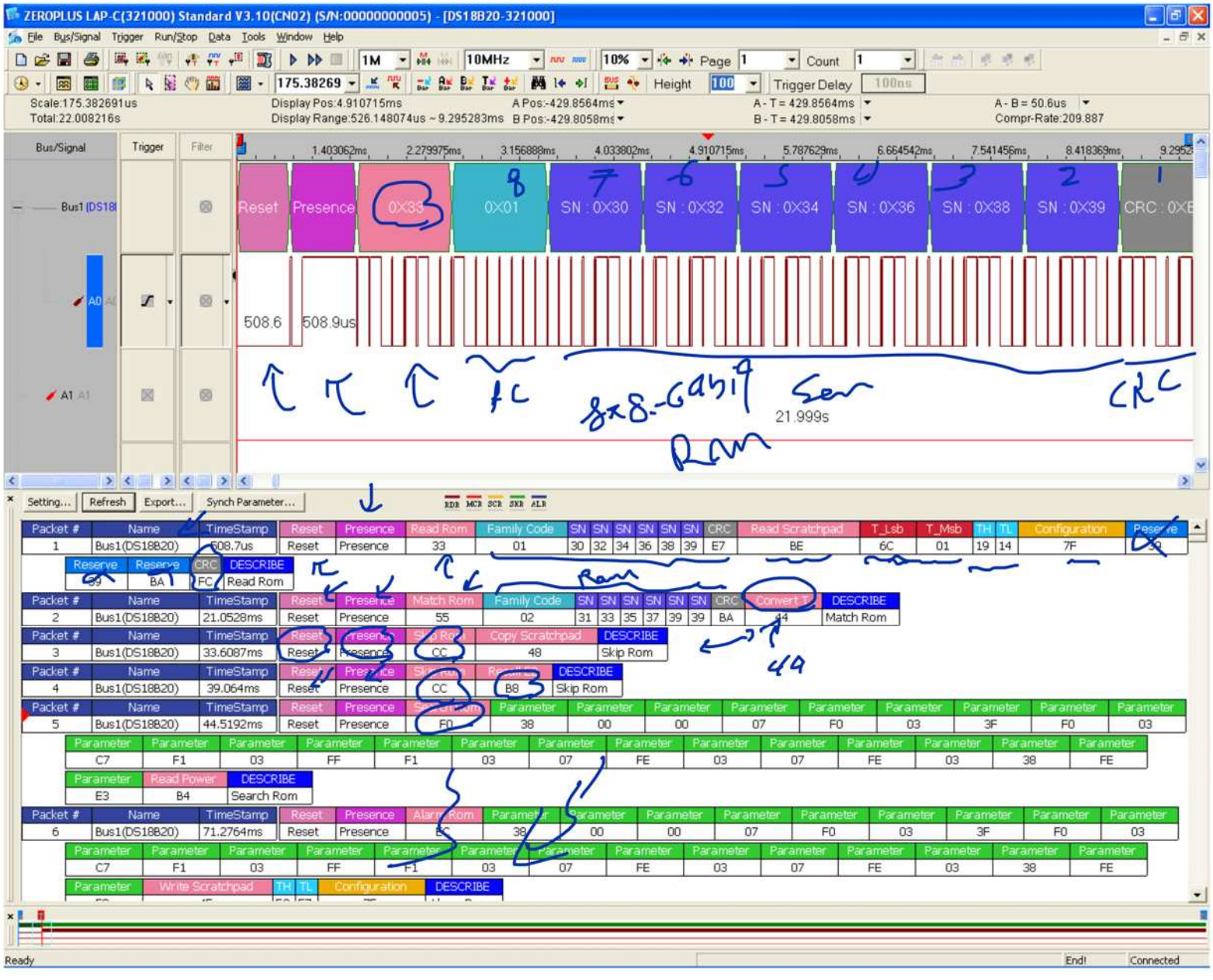
EEPROM

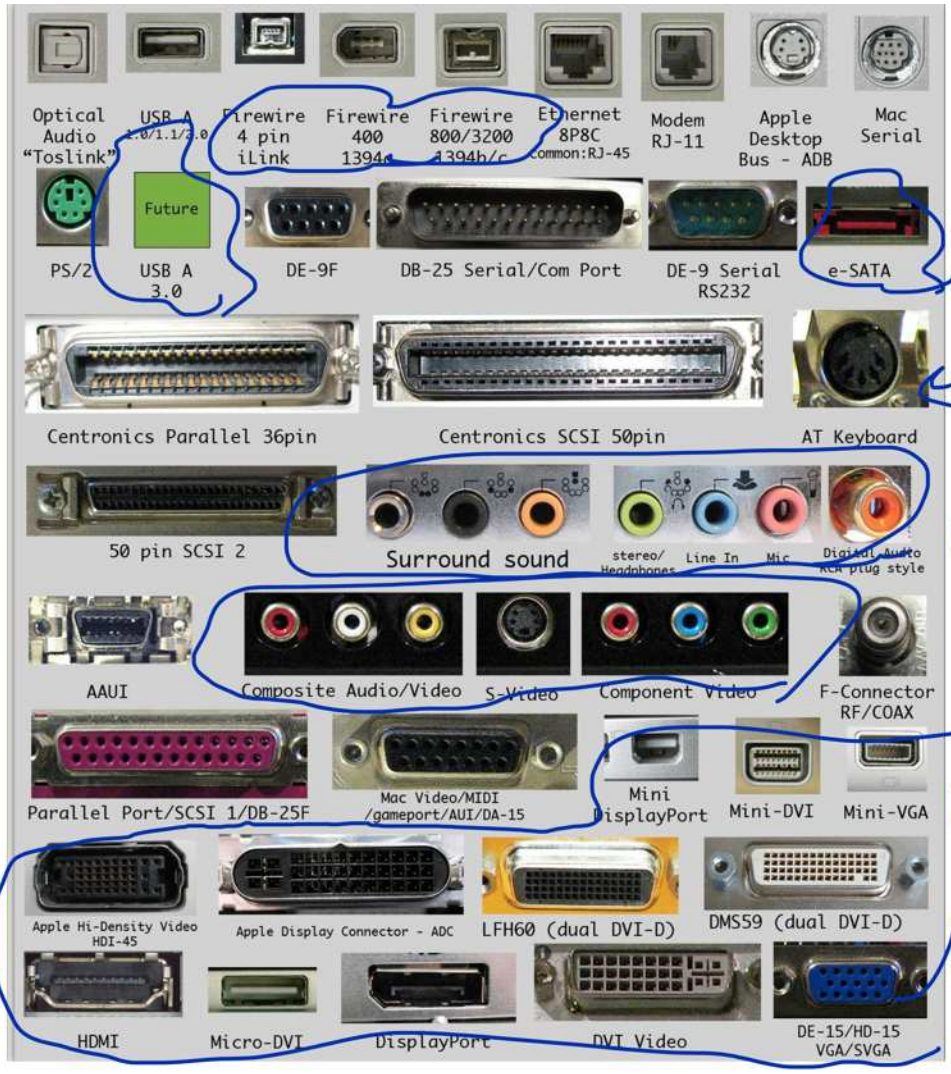
T_H REGISTER OR USER BYTE 1*
T_L REGISTER OR USER BYTE 2*
CONFIGURATION REGISTER*

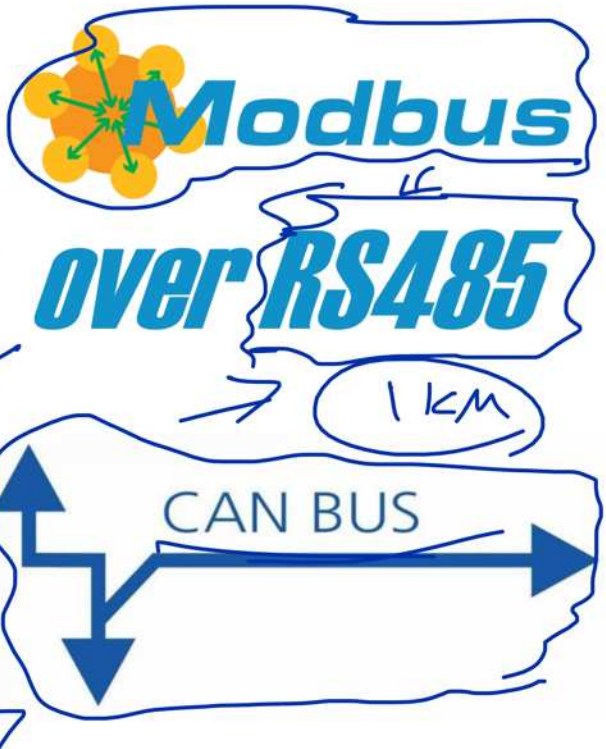
*POWER-UP STATE DEPENDS ON VALUE(S) STORED IN EEPROM.



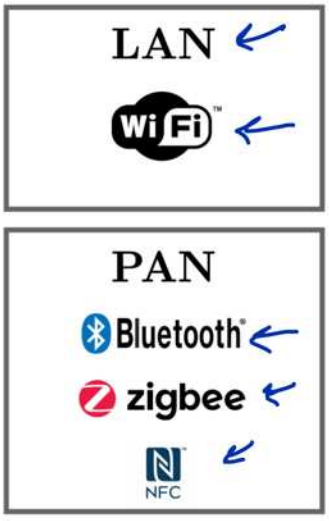
MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx →	Reset →	Master issues reset pulse.
Rx ←	Presence	DS18B20s respond with presence pulse.
Tx →	55h	Master issues Match ROM command.
Tx →	64-bit ROM code	Master sends DS18B20 ROM code.
Tx →	44h	Master issues Convert T command.
Tx →	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (t_{CONV}).
Tx →	Reset	Master issues reset pulse.
Rx ←	Presence	DS18B20s respond with presence pulse.
Tx →	55h	Master issues Match ROM command.
Tx →	64-bit ROM code	Master sends DS18B20 ROM code.
Tx →	BEh	Master issues Read Scratchpad command.
Rx ←	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.




Optical Audio "Toslink"
USB A 1.0/1.1/2.0
Firewire 4 pin iLink
Firewire 400 1394a
Firewire 800/3200 1394b/c
Ethernet 8P8C common:RJ-45
Modem RJ-11
Apple Desktop Bus - ADB
Mac Serial
PS/2
Future
USB A 3.0
DE-9F
DB-25 Serial/Com Port
DE-9 Serial RS232
e-SATA
Centronics Parallel 36pin
Centronics SCSI 50pin
AT Keyboard
50 pin SCSI 2
Surround sound
stereo/ Headphones
Line In
Mic
Digital Audio RCA plug style
AAUI
Composite Audio/Video
S-Video
Component Video
F-Connector RF/COAX
Parallel Port/SCSI 1/DB-25F
Mac Video/MIDI /gameport/AUI/DA-15
Mini DisplayPort
Mini-DVI
Mini-VGA
Apple Hi-Density Video HDI-45
Apple Display Connector - ADC
LFH60 (dual DVI-D)
DMS59 (dual DVI-D)
HDMI
Micro-DVI
DisplayPort
DVI Video
DE-15/HD-15 VGA/SVGA

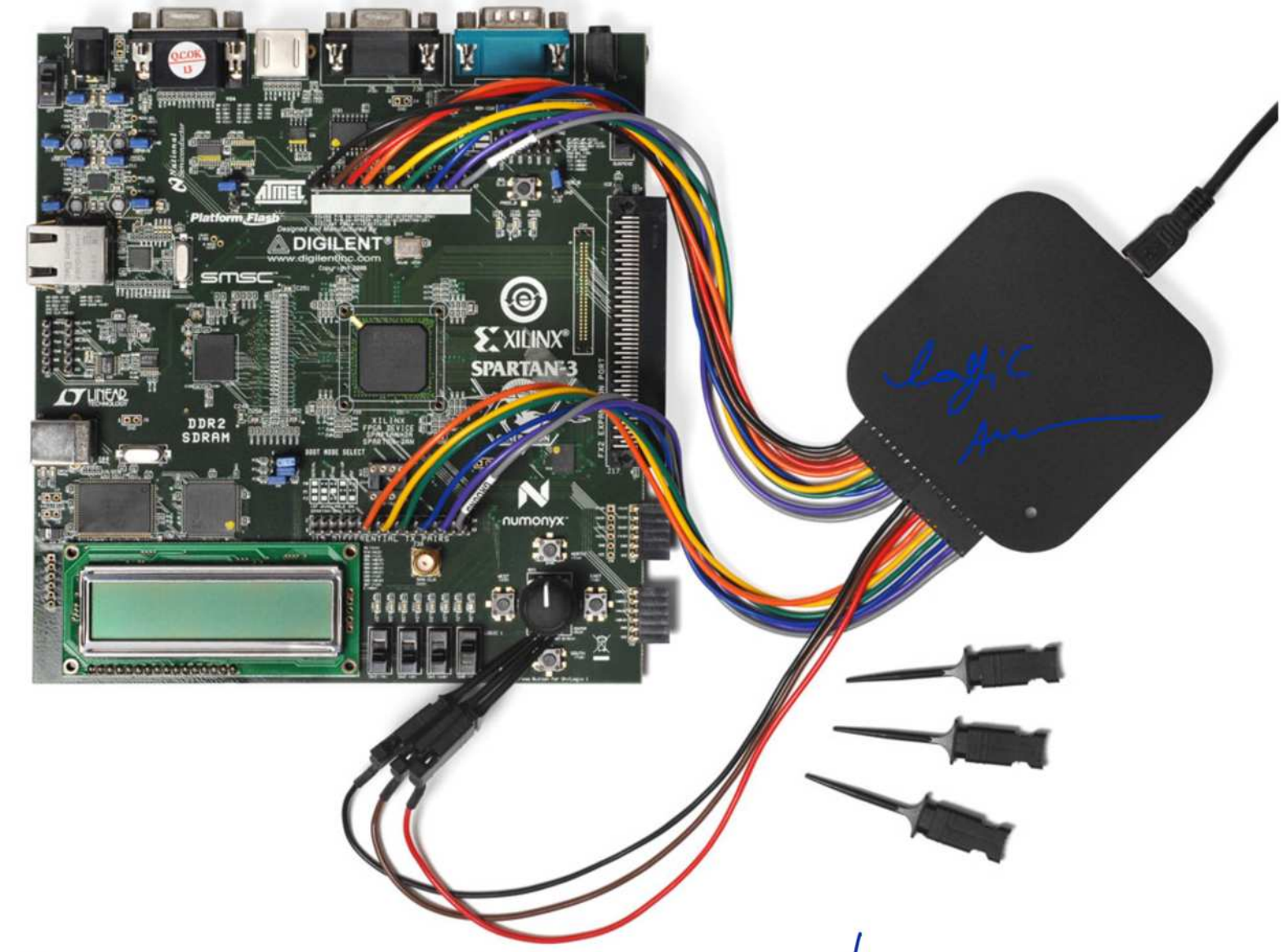

Modbus
over RS485
1 KM
CAN BUS


I2S


LAN
Wi Fi
PAN
Bluetooth
zigbee
NFC
WAN
Lte
GSM
3GPP
A GLOBAL INITIATIVE
LPWAN
LoRa
sigfox
LTE-M
NB-IoT
Satellite


RC5
DY-001


RGB


DIGILENT
www.digilentinc.com
XILINX
SPARTAN-3
DDR2
SDRAM
numonyx
smsc


sainsmart_dds120_powerup_scl_analog.sr - PulseView
Run
sainsmart_dds120_powerup_scl_analog.sr
sainsmart_dds120_powerup_scl_analog.sr
+178900 µs
+178920 µs
+178940 µs
+178960 µs
+178980 µs
+179000 µs
+179020 µs
SCL analog
SCL
SDA
I²C
I²C: Bits
1 0 1 0 0 0 1 0
I²C: Address/Data
Address write: 51
Write
ACK
24xx EEPROM: Bits/bytes
Control code bits: 1010
Addr bit 2
Addr bit 1
Addr bit 0
R/W bit: write
24xx EEPROM: Fields
Control word
24xx EEPROM: Operations
Sequential random read (addr=00, 4110 bytes)
24xx EEPROM: Warnings