15. 8-bit Timer/Counter0 with PWM

15.1 Features

- Two Independent Output Compare Units
- Double Buffered Output Compare Registers
- Clear Timer on Compare Match (Auto Reload)
- Glitch Free, Phase Correct Pulse Width Modulator (PWM)
- Variable PWM Period
- Frequency Generator
- Three Independent Interrupt Sources (TOV0, OCF0A, and OCF0B)

Figure 15-1. 8-bit Timer/Counter Block Diagram

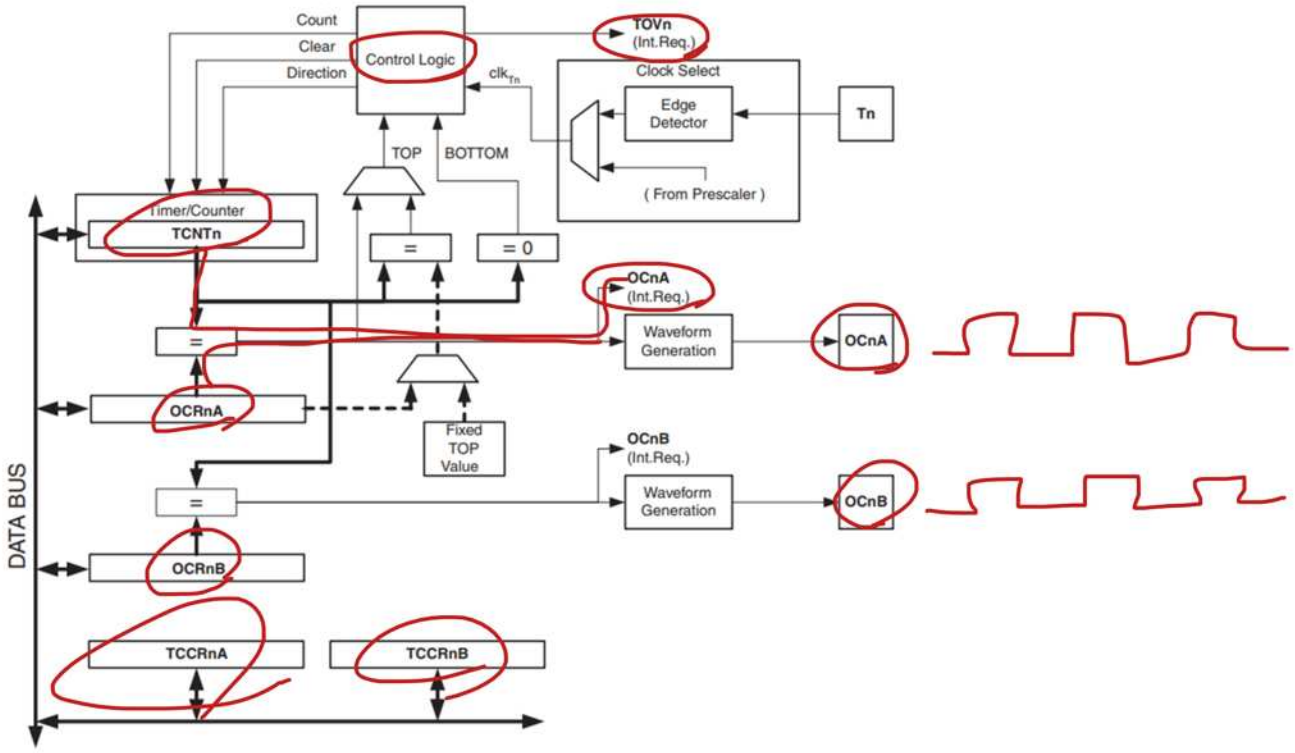
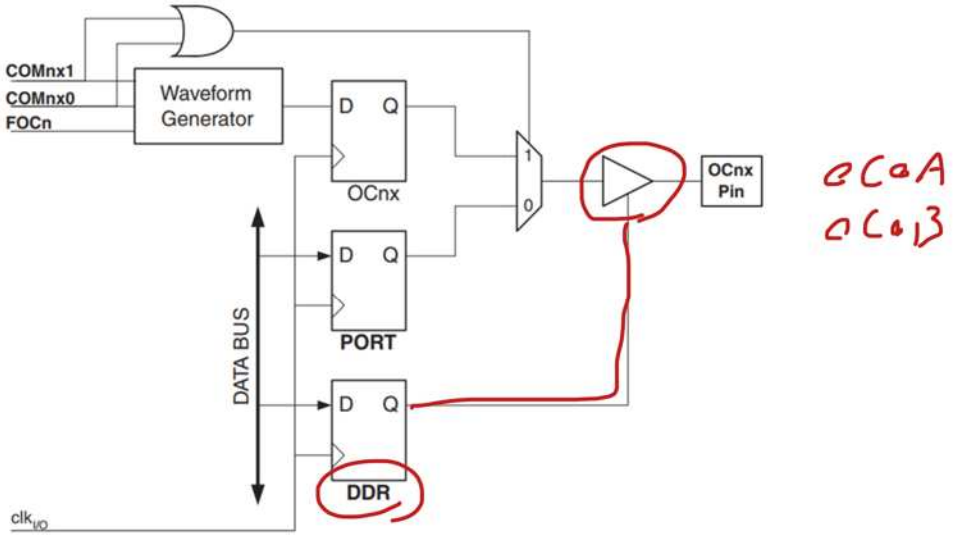
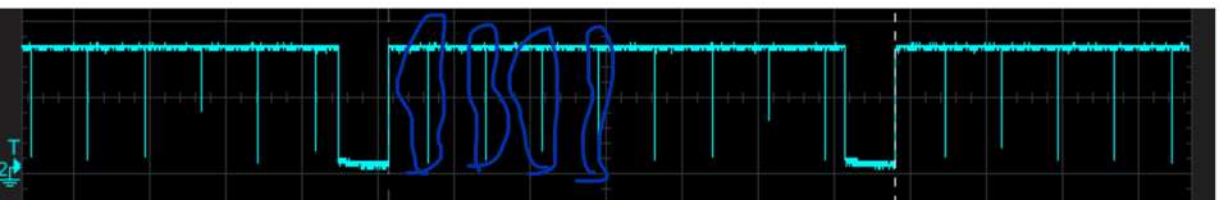


Figure 15-4. Compare Match Output Unit, Schematic





15.9.1 TCCR0A – Timer/Counter Control Register A

Bit	7	6	5	4	3	2	1	0	
0x24 (0x44)	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	TCCR0A
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

duty 25% → 50%

Table 15-8. Waveform Generation Mode Bit Description

Mode	WGM02	WGM01	WGM00	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on (1)(2)
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	BOTTOM	MAX
4	1	0	0	Reserved	–	–	–
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	–	–	–
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

Notes: 1. MAX = 0xFF
2. BOTTOM = 0x00

$f = \frac{f_{clk}}{N(1+OCR0A)}$

1 2

1000 Hz

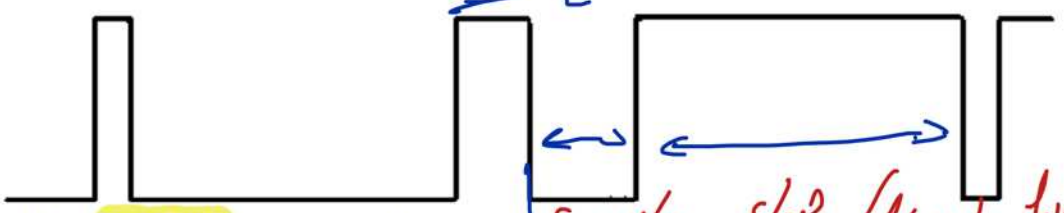
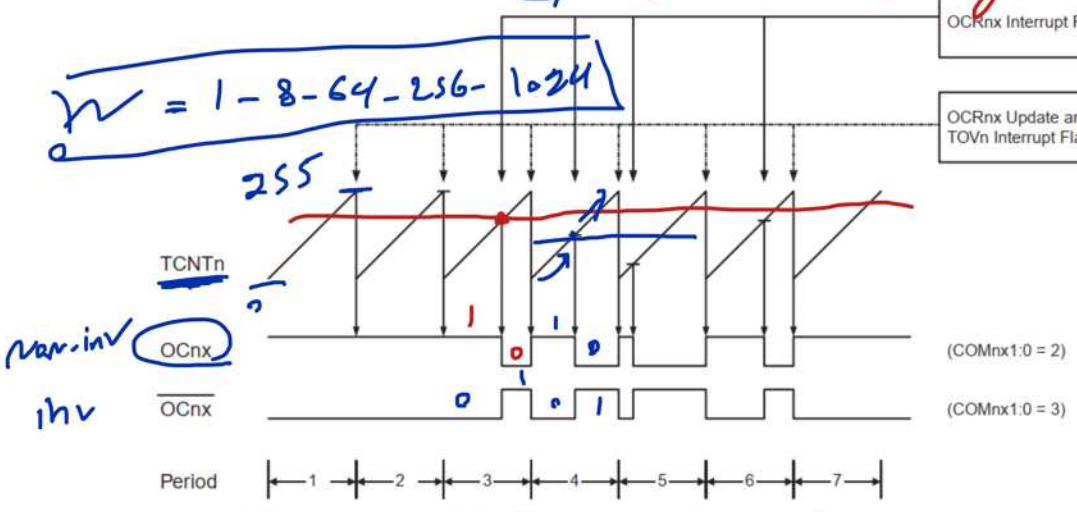


Figure 15-6. Fast PWM Mode, Timing Diagram

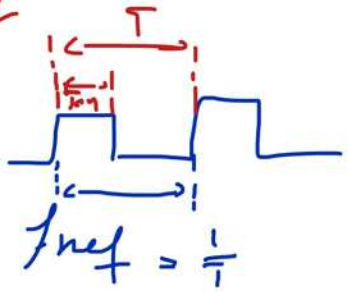
Single slop / high freq



N = 1 - 8 - 64 - 256 - 1024

non-inv

inv



$f_{ref} = \frac{1}{T}$

$duty = \frac{T_{on}}{T}$

$f = \frac{f_{clk}}{N \cdot 256}$

$f = \frac{16 \times 10^6}{N \times 256}$

N	f
1	62,500 Hz
8	7,812 Hz
64	976 Hz
256	244 Hz
1024	61 Hz

OCR0A ← OCR0A → 100 %

OCR0B 0 → 0 %

So y, x 255 = 128

Table 15-3. Compare Output Mode, Fast PWM Mode(1)

COM0A1	COM0A0	Description
0	0	Normal port operation, OC0A disconnected.
0	1	WGM02 = 0: Normal Port Operation, OC0A Disconnected. WGM02 = 1: Toggle OC0A on Compare Match.
1	0	Clear OC0A on Compare Match, set OC0A at BOTTOM, (non-inverting mode).
1	1	Set OC0A on Compare Match, clear OC0A at BOTTOM, (inverting mode).

Note: 1. A special case occurs when OCR0A equals TOP and COM0A1 is set. In this case, the Compare Match is ignored, but the set or clear is done at BOTTOM. See "Fast PWM Mode" on page 99 for more details.

Table 15-4 shows the COM0A1:0 bit functionality when the WGM02:0 bits are set to phase correct PWM mode.

OCoA

Table 15-6. Compare Output Mode, Fast PWM Mode(1)

COM0B1	COM0B0	Description
0	0	Normal port operation, OC0B disconnected.
0	1	Reserved
1	0	Clear OC0B on Compare Match, set OC0B at BOTTOM, (non-inverting mode)
1	1	Set OC0B on Compare Match, clear OC0B at BOTTOM, (inverting mode).

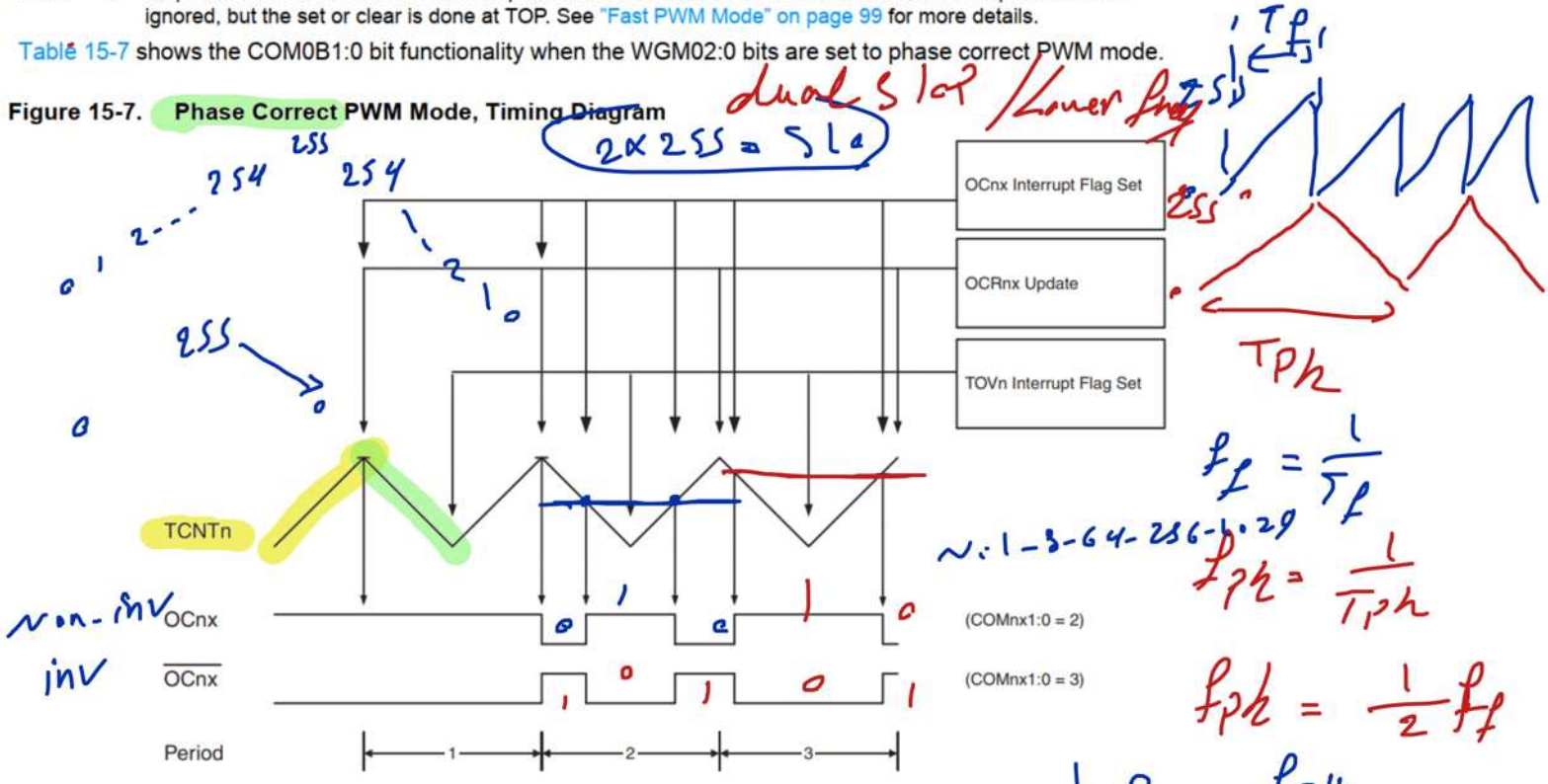
Note: 1. A special case occurs when OCR0B equals TOP and COM0B1 is set. In this case, the Compare Match is ignored, but the set or clear is done at TOP. See "Fast PWM Mode" on page 99 for more details.

Table 15-7 shows the COM0B1:0 bit functionality when the WGM02:0 bits are set to phase correct PWM mode.

Figure 15-7. Phase Correct PWM Mode, Timing Diagram

dual slop / Lower freq

2 × 255 = 510



$f_f = \frac{1}{T_f}$

$f_{ph} = \frac{1}{T_{ph}}$

$f_{ph} = \frac{1}{2} f_f$

$f = \frac{f_{clk}}{N(510)}$

N	f
1	31,372 Hz
8	3,921 Hz
64	490 Hz
256	112 Hz
1.024	30 Hz

Table 15-4. Compare Output Mode, Phase Correct PWM Mode(1)

COM0A1	COM0A0	Description
0	0	Normal port operation, OC0A disconnected.
0	1	WGM02 = 0: Normal Port Operation, OC0A Disconnected. WGM02 = 1: Toggle OC0A on Compare Match.
1	0	Clear OC0A on Compare Match when up-counting. Set OC0A on Compare Match when down-counting.
1	1	Set OC0A on Compare Match when up-counting. Clear OC0A on Compare Match when down-counting.

Note: 1. A special case occurs when OCR0A equals TOP and COM0A1 is set. In this case, the Compare Match is ignored, but the set or clear is done at TOP. See "Phase Correct PWM Mode" on page 125 for more details.

Table 15-7. Compare Output Mode, Phase Correct PWM Mode(1)

COM0B1	COM0B0	Description
0	0	Normal port operation, OC0B disconnected.
0	1	Reserved
1	0	Clear OC0B on Compare Match when up-counting. Set OC0B on Compare Match when down-counting.
1	1	Set OC0B on Compare Match when up-counting. Clear OC0B on Compare Match when down-counting.

Note: 1. A special case occurs when OCR0B equals TOP and COM0B1 is set. In this case, the Compare Match is ignored, but the set or clear is done at TOP. See "Phase Correct PWM Mode" on page 100 for more details.

15.9.2 TCCR0B – Timer/Counter Control Register B

Bit	7	6	5	4	3	2	1	0	
0x25 (0x45)	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	TCCR0B
Read/Write	W	W	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Table 15-9. Clock Select Bit Description

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/(No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

15.9.3 TCNT0 – Timer/Counter Register

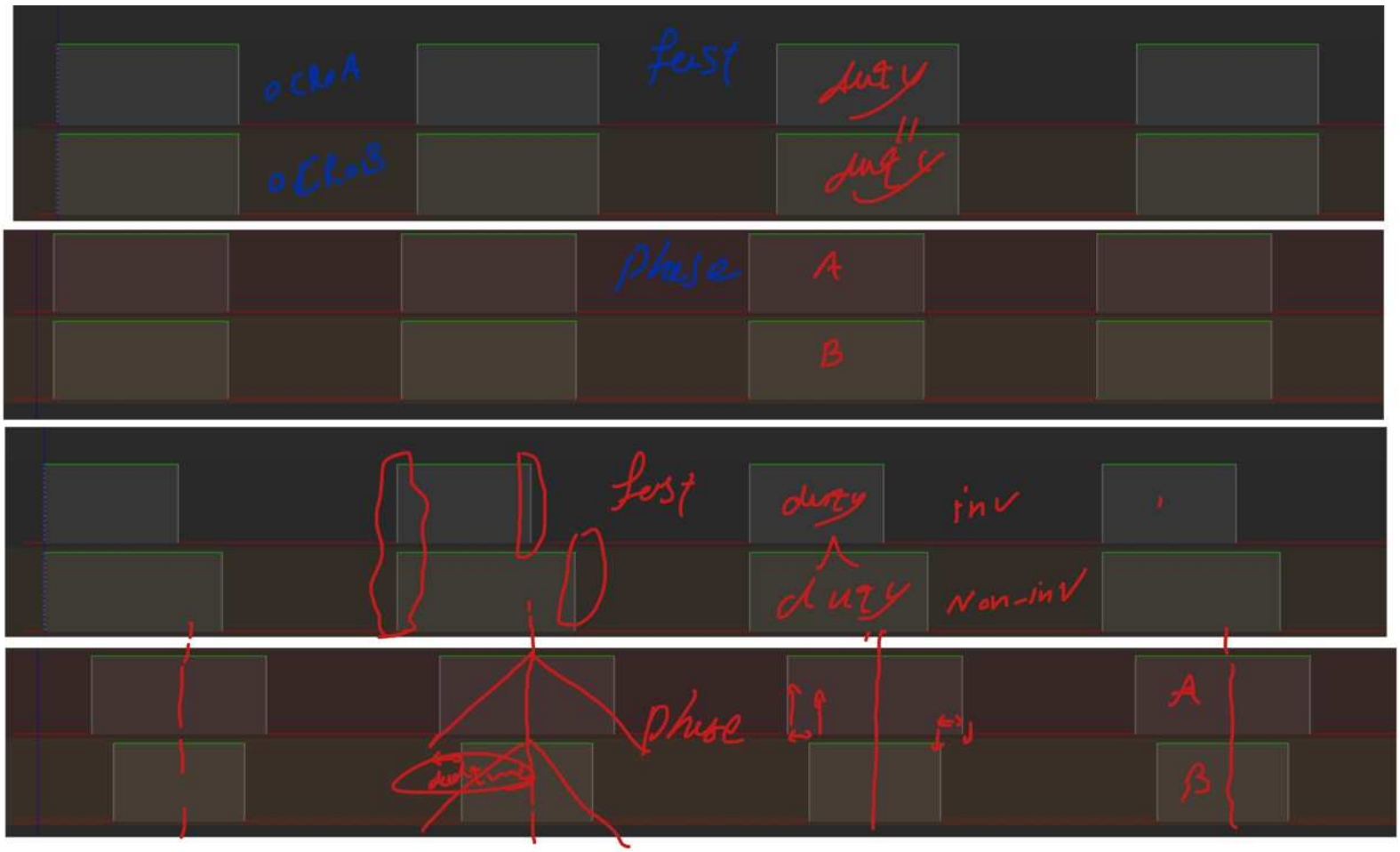
Bit	7	6	5	4	3	2	1	0	
0x26 (0x46)	TCNT0[7:0]								TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

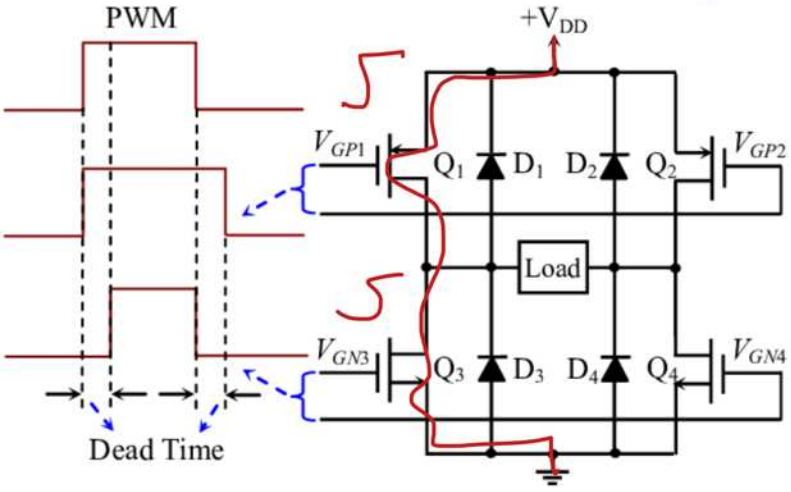
15.9.4 OCR0A – Output Compare Register A

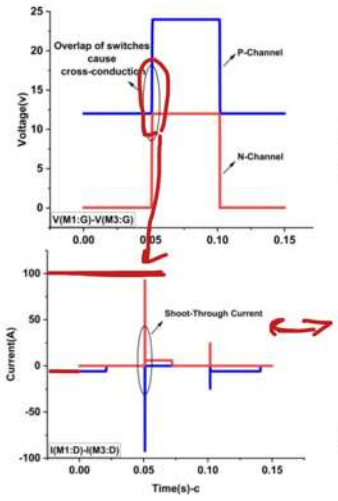
Bit	7	6	5	4	3	2	1	0	
0x27 (0x47)	OCR0A[7:0]								OCR0A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

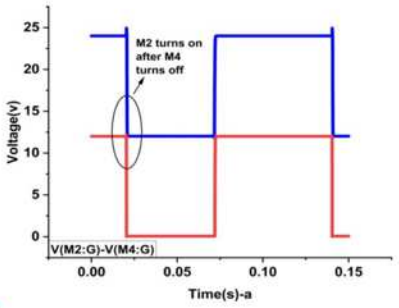
15.9.5 OCR0B – Output Compare Register B

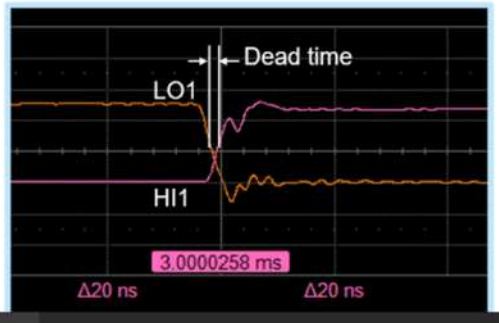
Bit	7	6	5	4	3	2	1	0	
0x28 (0x48)	OCR0B[7:0]								OCR0B
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	


OCR0A
OCR0B
Phase
A
B

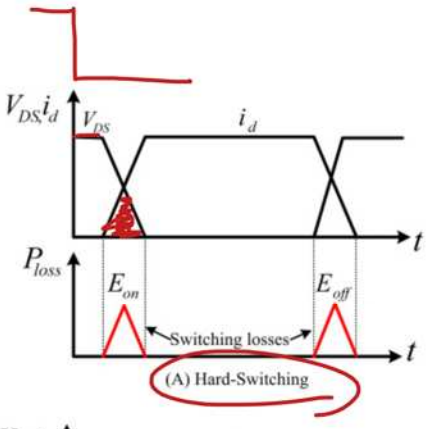

PWM
+V_DD
V_GP1
V_GP2
V_GN3
V_GN4
Q1
Q2
Q3
Q4
D1
D2
D3
D4
Load
Dead Time

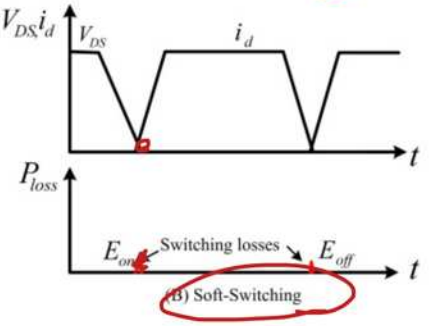

Overlap of switches cause cross-conduction
P-Channel
N-Channel
Voltage(v)
V(M1:G)-V(M3:G)
Shoot-Through Current
Current(A)
I(M1:D)-I(M3:D)
Time(s)-c

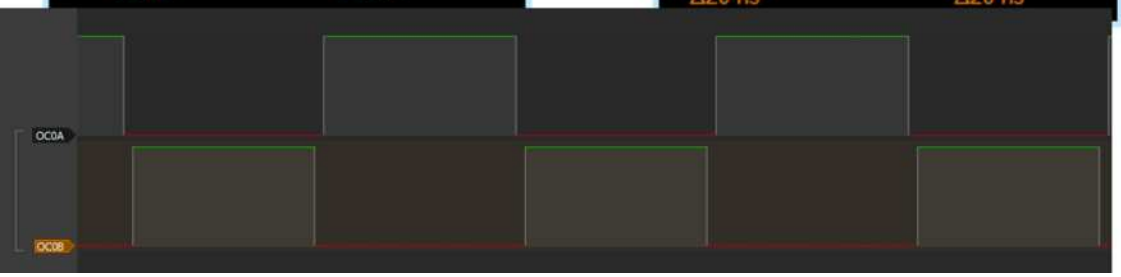

M2 turns on after M4 turns off
Voltage(v)
V(M2:G)-V(M4:G)
Time(s)-a


Dead time
LO1
HI1
3.0000258 ms
Δ20 ns
Δ20 ns


Dead time
LO1
HI1
3.0002118 ms
Δ20 ns
Δ20 ns


V_DS, i_d
V_DS
i_d
t
P_loss
E_on
E_off
Switching losses
(A) Hard-Switching


V_DS, i_d
V_DS
i_d
t
P_loss
E_on
Switching losses
E_off
(B) Soft-Switching


OC0A
OC0B