GPIO functional description

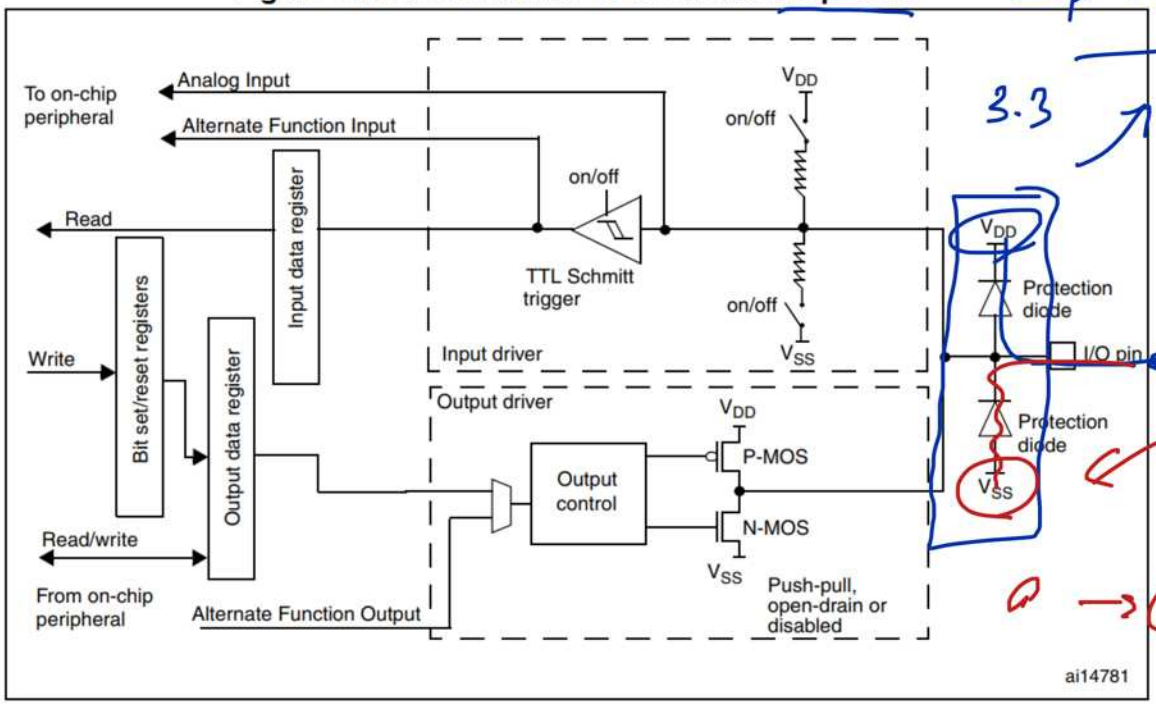
Each of the general-purpose I/O ports has two 32-bit configuration registers (GPIOx_CRL, GPIOx_CRH), two 32-bit data registers (GPIOx_IDR, GPIOx_ODR), a 32-bit set/reset register (GPIOx_BSRR), a 16-bit reset register (GPIOx_BRR) and a 32-bit locking register (GPIOx_LCKR).

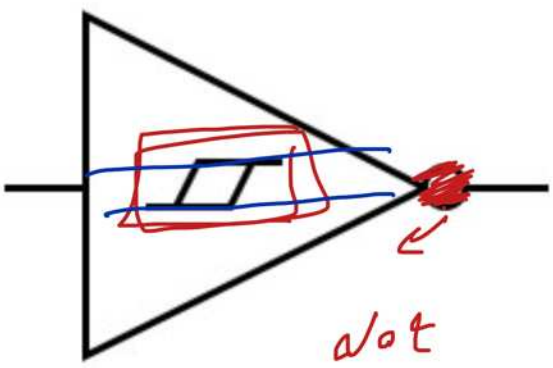
Subject to the specific hardware characteristics of each I/O port listed in the *datasheet*, each port bit of the General Purpose IO (GPIO) Ports, can be individually configured by software in several modes:

- Input floating
- Input pull-up
- Input-pull-down
- Analog
- Output open-drain
- Output push-pull
- Alternate function push-pull
- Alternate function open-drain

Each I/O port bit is freely programmable, however the I/O port registers have to be accessed as 32-bit words (half-word or byte accesses are not allowed). The purpose of the GPIOx_BSRR and GPIOx_BRR registers is to allow atomic read/modify accesses to any of the GPIO registers. This way, there is no risk that an IRQ occurs between the read and the modify access.

Figure 13. Basic structure of a standard I/O port bit





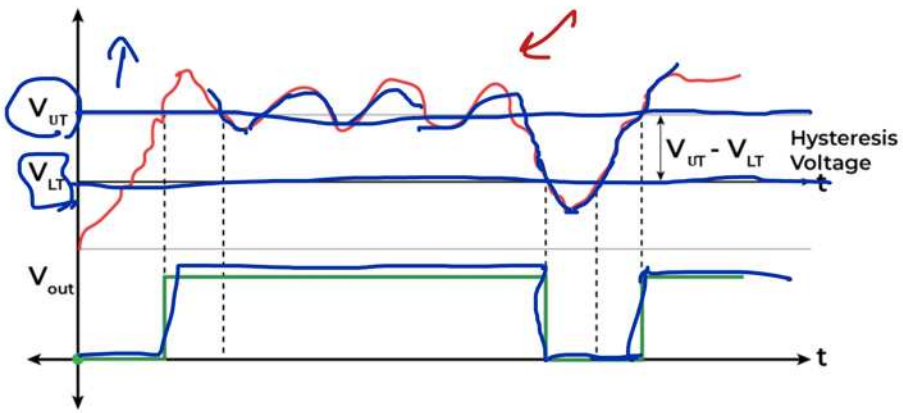
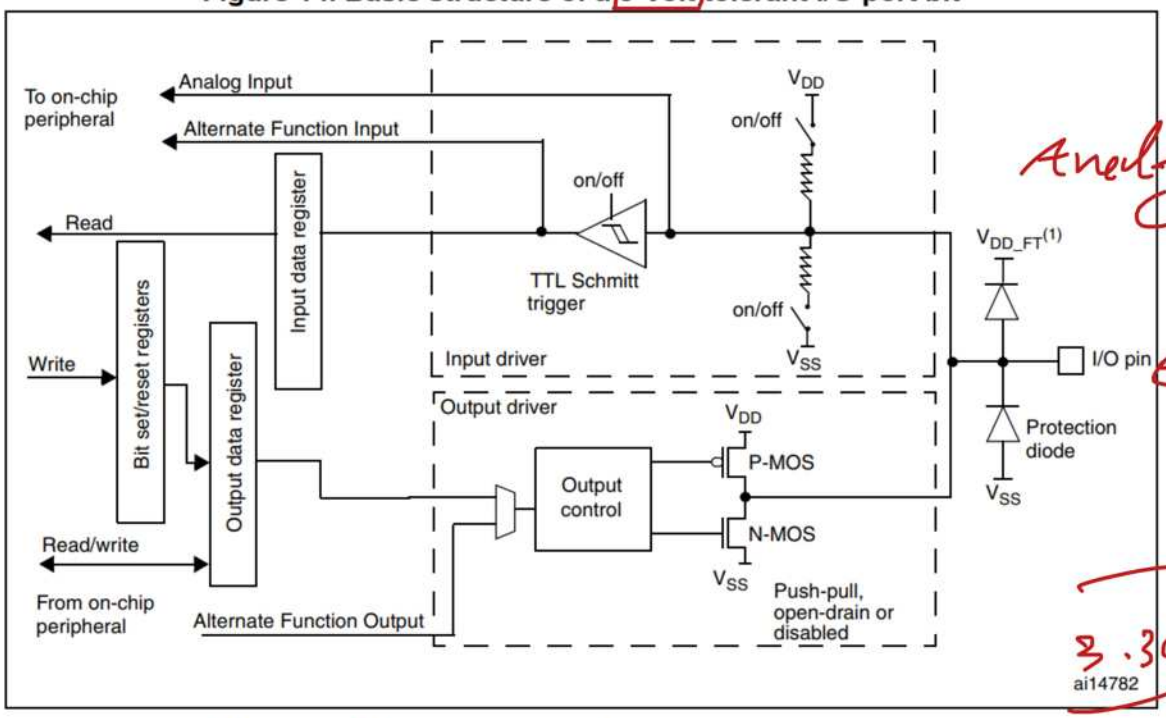


Figure 14. Basic structure of a 5-Volt tolerant I/O port bit



1. V_{DD_FT} is a potential specific to 5-Volt tolerant I/Os, and different from V_{DD}.

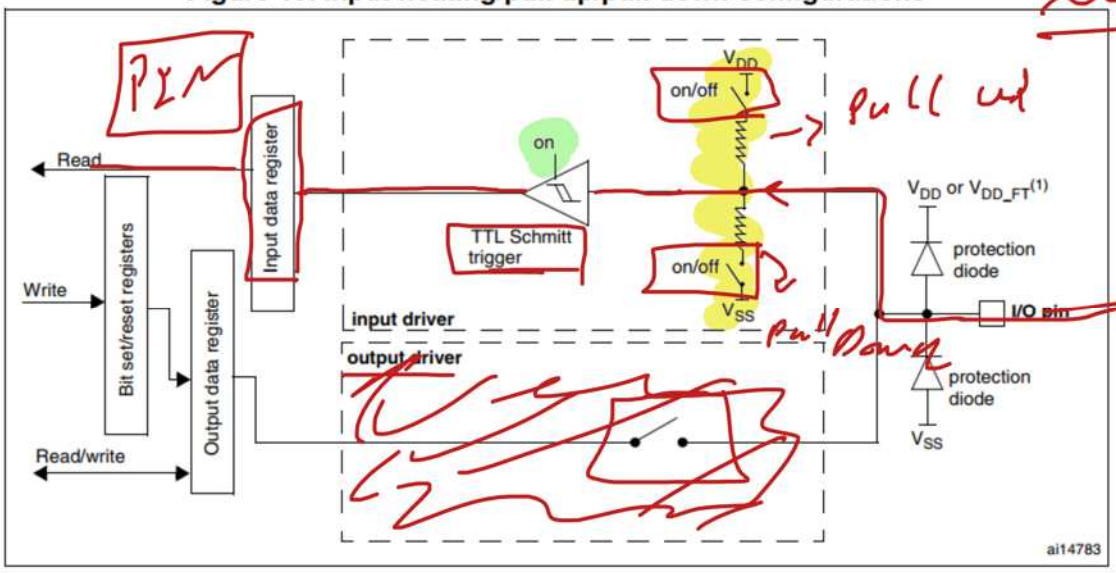
Input configuration

When the I/O Port is programmed as Input:

- The Output Buffer is disabled
- The Schmitt Trigger Input is activated
- The weak pull-up and pull-down resistors are activated or not depending on input configuration (pull-up, pull-down or floating):
- The data present on the I/O pin is sampled into the Input Data Register every APB2 clock cycle
- A read access to the Input Data Register obtains the I/O State.

Figure 15 shows the Input Configuration of the I/O Port bit.

Figure 15. Input floating/pull up/pull down configurations



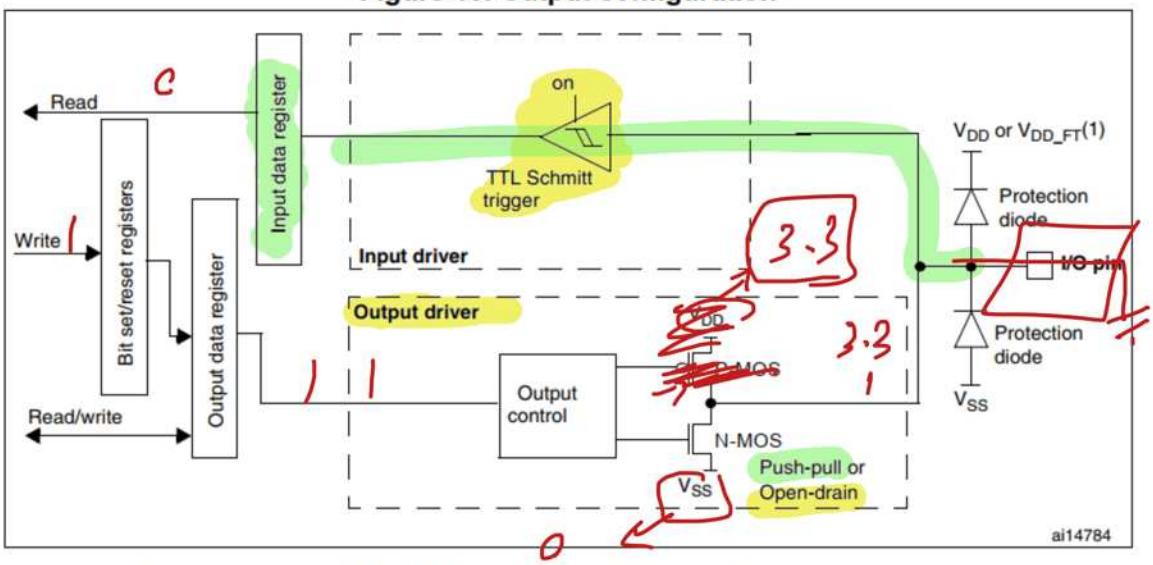
1. V_{DD_FT} is a potential specific to 5-Volt tolerant I/Os, and different from V_{DD}.

Output configuration

When the I/O Port is programmed as Output:

- The Output Buffer is enabled:
  - Open Drain Mode: A “0” in the Output register activates the N-MOS while a “1” in the Output register leaves the port in Hi-Z (the P-MOS is never activated)
  - Push-Pull Mode: A “0” in the Output register activates the N-MOS while a “1” in the Output register activates the P-MOS
- The Schmitt Trigger Input is activated.
- The weak pull-up and pull-down resistors are disabled.
- The data present on the I/O pin is sampled into the Input Data Register every APB2 clock cycle
- A read access to the Input Data Register gets the I/O state in open drain mode
- A read access to the Output Data register gets the last written value in Push-Pull mode

Figure 16. Output configuration



1. V_{DD_FT} is a potential specific to 5-Volt tolerant I/Os, and different from V_{DD}.

Alternate function configuration

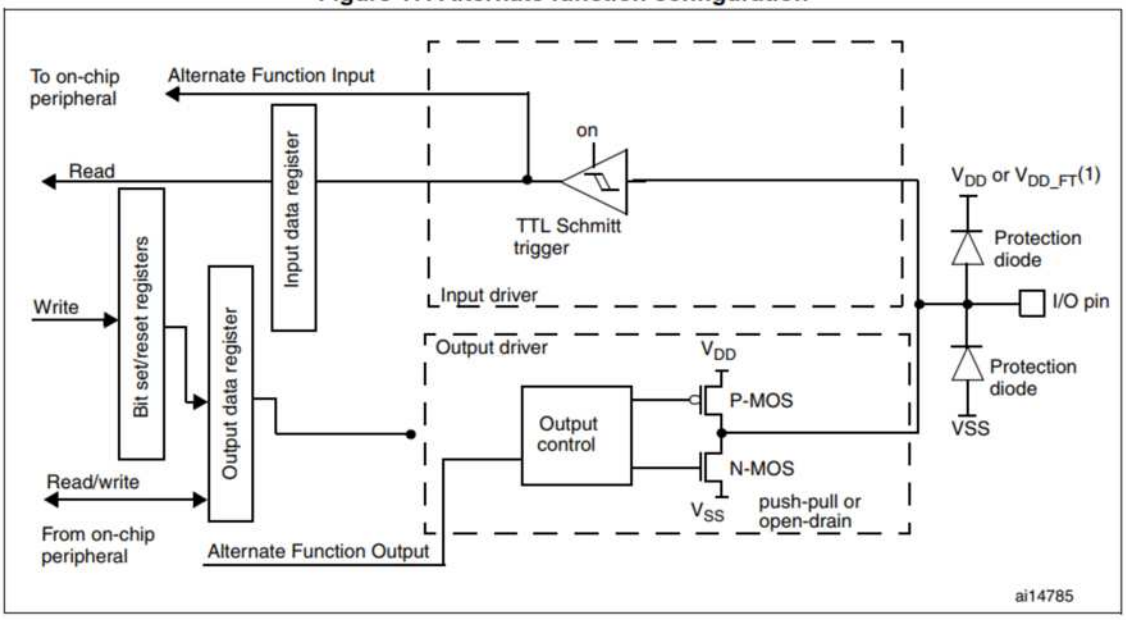
When the I/O Port is programmed as Alternate Function:

- The Output Buffer is turned on in Open Drain or Push-Pull configuration
- The Output Buffer is driven by the signal coming from the peripheral (alternate function out)
- The Schmitt Trigger Input is activated
- The weak pull-up and pull-down resistors are disabled.
- The data present on the I/O pin is sampled into the Input Data Register every APB2 clock cycle
- A read access to the Input Data Register gets the I/O state in open drain mode
- A read access to the Output Data register gets the last written value in Push-Pull mode

Figure 17 shows the Alternate Function Configuration of the I/O Port bit. Also, refer to *Section 9.4: AFIO registers* for further information.

A set of Alternate Function I/O registers allows the user to remap some alternate functions to different pins. Refer to *Section 9.3: Alternate function I/O and debug configuration (AFIO)*.

Figure 17. Alternate function configuration



1. V_{DD_FT} is a potential specific to 5-Volt tolerant I/Os, and different from V_{DD}.

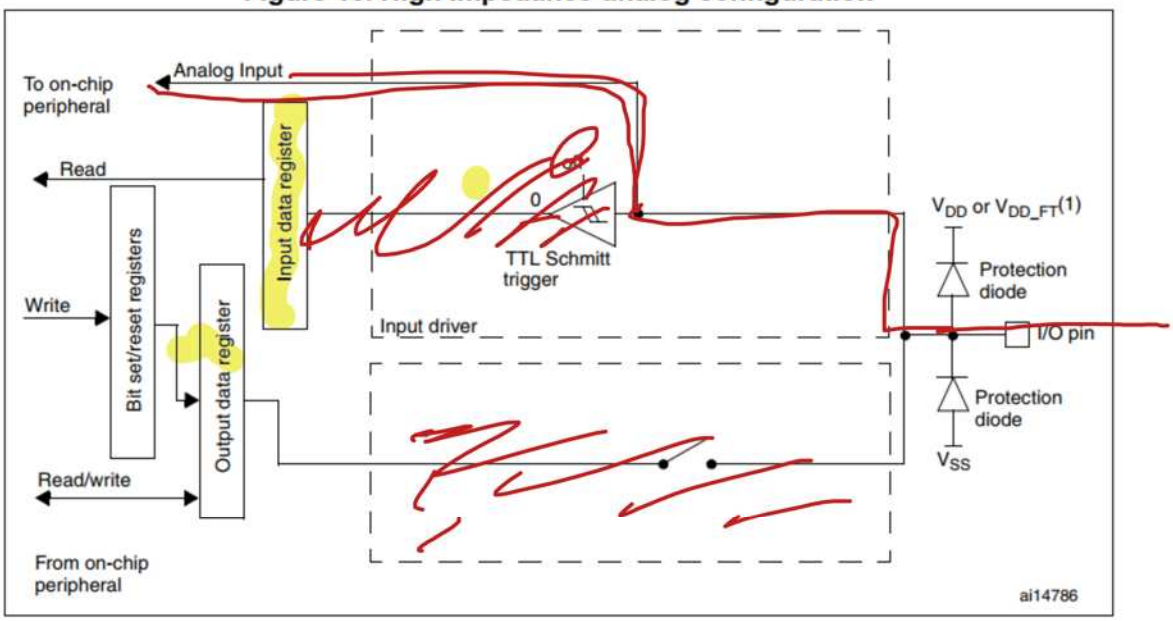
9.1.10 Analog configuration

When the I/O Port is programmed as Analog configuration:

- The Output Buffer is disabled.
- The Schmitt Trigger Input is de-activated providing zero consumption for every analog value of the I/O pin. The output of the Schmitt Trigger is forced to a constant value (0).
- The weak pull-up and pull-down resistors are disabled.
- Read access to the Input Data Register gets the value "0".

Figure 18 shows the high impedance-analog configuration of the I/O Port bit.

Figure 18. High impedance-analog configuration



Initialization and de-initialization functions

This section provides functions allowing to initialize and de-initialize the GPIOs to be ready for use.

This section contains the following APIs:

- *HAL_GPIO_Init*
- *HAL_GPIO_DeInit*

IO operation functions

This subsection provides a set of functions allowing to manage the GPIOs.

This section contains the following APIs:

- *HAL_GPIO_ReadPin*
- *HAL_GPIO_WritePin*
- *HAL_GPIO_TogglePin*
- *HAL_GPIO_LockPin*
- ~~*HAL_GPIO_EXTI_IRQHandler*~~
- ~~*HAL_GPIO_EXTI_Callback*~~

HAL_GPIO_Init

Function name

void HAL_GPIO_Init (GPIO_TypeDef * GPIOx, GPIO_InitTypeDef * GPIO_Init)

Function description

Initializes the GPIOx peripheral according to the specified parameters in the GPIO_Init.

Parameters

- **GPIOx:** where x can be (A..G depending on device used) to select the GPIO peripheral
- **GPIO_Init:** pointer to a GPIO_InitTypeDef structure that contains the configuration information for the specified GPIO peripheral.

Return values

- **None:**

GPIO_InitTypeDef

GPIO_InitTypeDef is defined in the stm32f1xx_hal_gpio.h

Data Fields

- *uint32_t Pin*
- *uint32_t Mode*
- *uint32_t Pull*
- *uint32_t Speed*

Field Documentation

- ***uint32_t GPIO_InitTypeDef::Pin***
  Specifies the GPIO pins to be configured. This parameter can be any value of *GPIO_pins_define*
- ***uint32_t GPIO_InitTypeDef::Mode***
  Specifies the operating mode for the selected pins. This parameter can be a value of *GPIO_mode_define*
- ***uint32_t GPIO_InitTypeDef::Pull***
  Specifies the Pull-up or Pull-Down activation for the selected pins. This parameter can be a value of *GPIO_pull_define*
- ***uint32_t GPIO_InitTypeDef::Speed***
  Specifies the speed for the selected pins. This parameter can be a value of *GPIO_speed_define*

HAL_GPIO_DeInit

Function name

void HAL_GPIO_DeInit (GPIO_TypeDef * GPIOx, uint32_t GPIO_Pin)

Function description

De-initializes the GPIOx peripheral registers to their default reset values.

Parameters

- **GPIOx:** where x can be (A..G depending on device used) to select the GPIO peripheral
- **GPIO_Pin:** specifies the port bit to be written. This parameter can be one of GPIO_PIN_x where x can be (0..15).

Return values

- **None:**

0 ~> 15

GPIO pins define

GPIO_PIN_0

GPIO_PIN_1

GPIO_PIN_2

GPIO mode define

GPIO_MODE_INPUT — Input Floating Mode

GPIO_MODE_OUTPUT_PP — Output Push Pull Mode

GPIO_MODE_OUTPUT_OD — Output Open Drain Mode

GPIO_MODE_AF_PP — Alternate Function Push Pull Mode

GPIO_MODE_AF_OD — Alternate Function Open Drain Mode

GPIO pull define

GPIO_NOPULL — No Pull-up or Pull-down activation

GPIO_PULLUP — Pull-up activation

GPIO_PULLDOWN — Pull-down activation

GPIO speed define

GPIO_SPEED_FREQ_LOW — Low speed

GPIO_SPEED_FREQ_MEDIUM — Medium speed

GPIO_SPEED_FREQ_HIGH — High speed

HAL_GPIO_WritePin

Function name

void HAL_GPIO_WritePin (GPIO_TypeDef * GPIOx, uint16_t GPIO_Pin, GPIO_PinState PinState)

Function description

Sets or clears the selected data port bit.

Parameters

- **GPIOx:** where x can be (A..G depending on device used) to select the GPIO peripheral
- **GPIO_Pin:** specifies the port bit to be written. This parameter can be one of GPIO_PIN_x where x can be (0..15).
- **PinState:** specifies the value to be written to the selected bit. This parameter can be one of the GPIO_PinState enum values:
  - GPIO_PIN_RESET: to clear the port pin
  - GPIO_PIN_SET: to set the port pin

Return values

- **None:**

Notes

- This function uses GPIOx_BSRR register to allow atomic read/modify accesses. In this way, there is no risk of an IRQ occurring between the read and the modify access.

HAL_GPIO_TogglePin

Function name

void HAL_GPIO_TogglePin (GPIO_TypeDef * GPIOx, uint16_t GPIO_Pin)

Function description

Toggles the specified GPIO pin.

Parameters

- **GPIOx:** where x can be (A..G depending on device used) to select the GPIO peripheral
- **GPIO_Pin:** Specifies the pins to be toggled.

Return values

- **None:**

HAL_GPIO_ReadPin

Function name

GPIO_PinState HAL_GPIO_ReadPin (GPIO_TypeDef * GPIOx, uint16_t GPIO_Pin)

Function description

Reads the specified input port pin.

Parameters

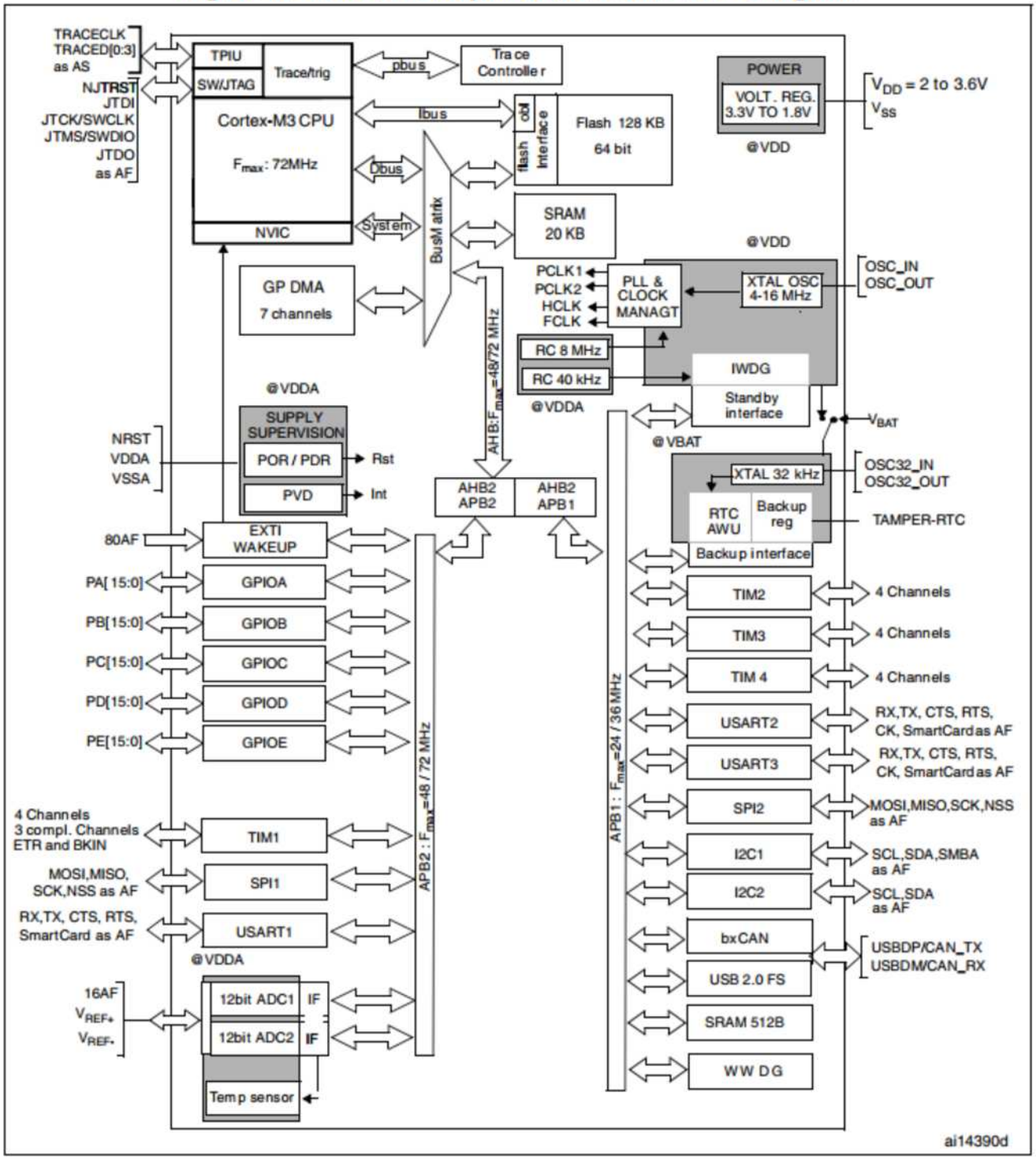
- **GPIOx:** where x can be (A..G depending on device used) to select the GPIO peripheral
- **GPIO_Pin:** specifies the port bit to read. This parameter can be GPIO_PIN_x where x can be (0..15).

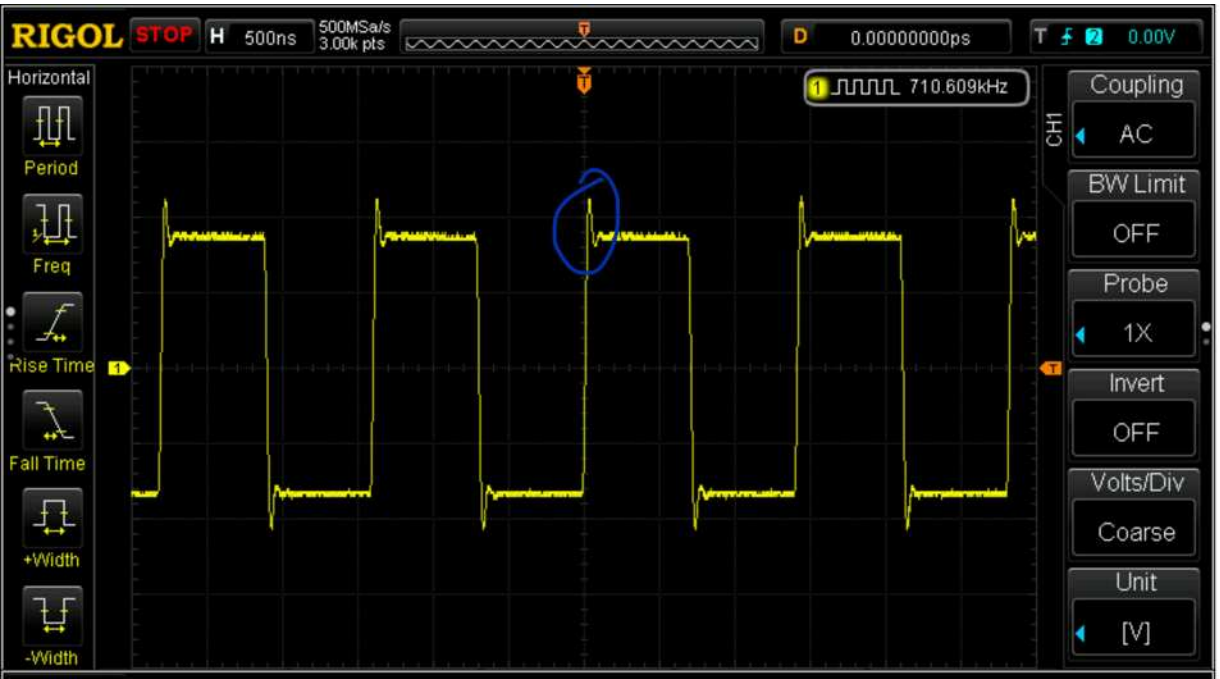
Return values

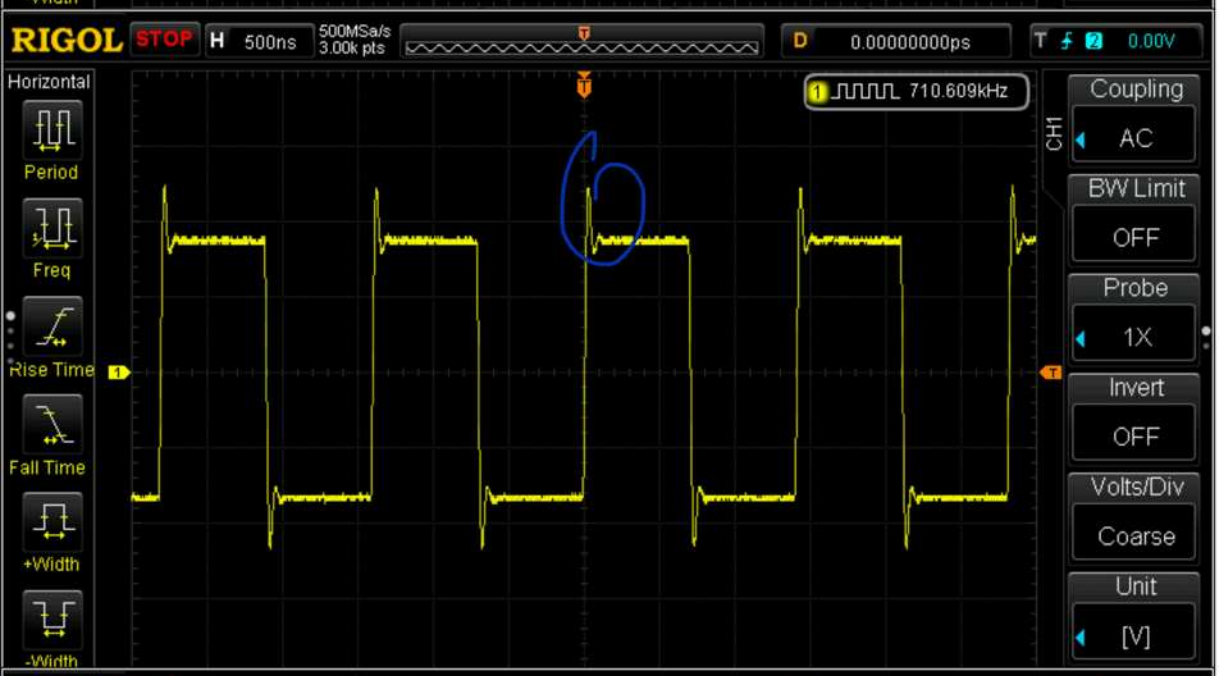
- **The:** input port pin value.

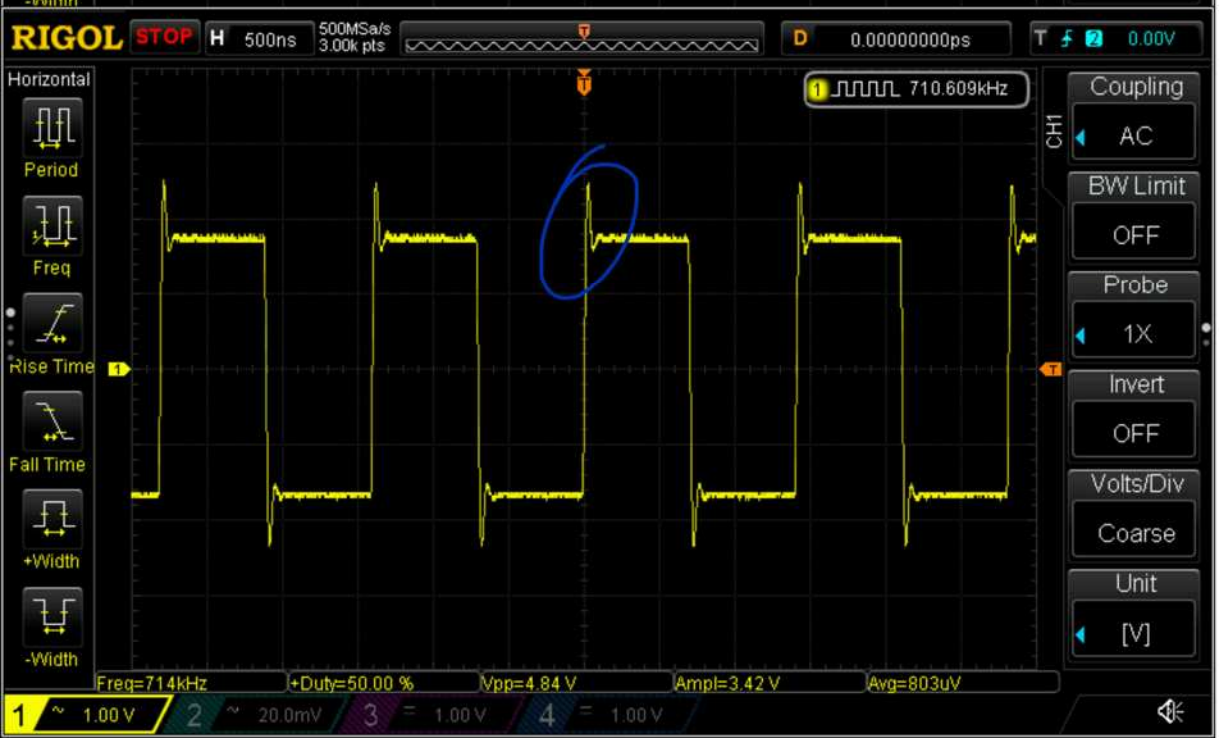
21 HAL GPIO Extension Driver

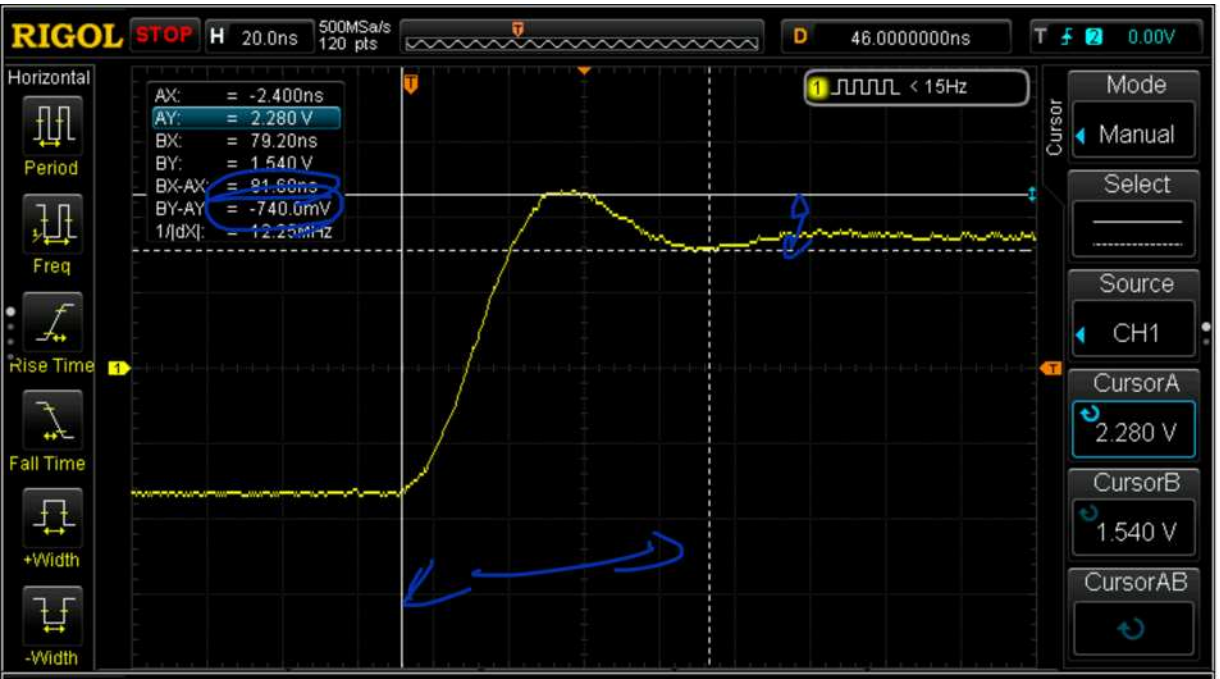
Figure 1. STM32F103xx performance line block diagram



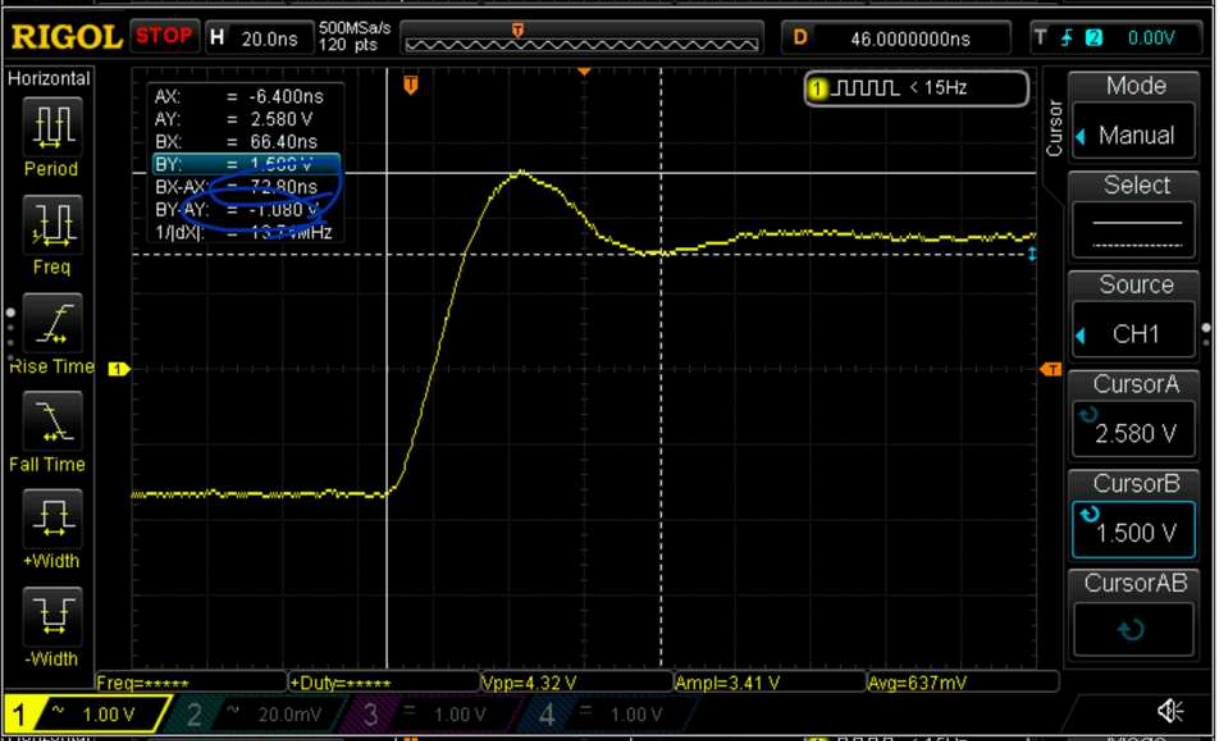

RIGOL
STOP
H 500ns
500MSa/s
3.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
710.609kHz
CH1
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]


RIGOL
STOP
H 500ns
500MSa/s
3.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
710.609kHz
CH1
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]

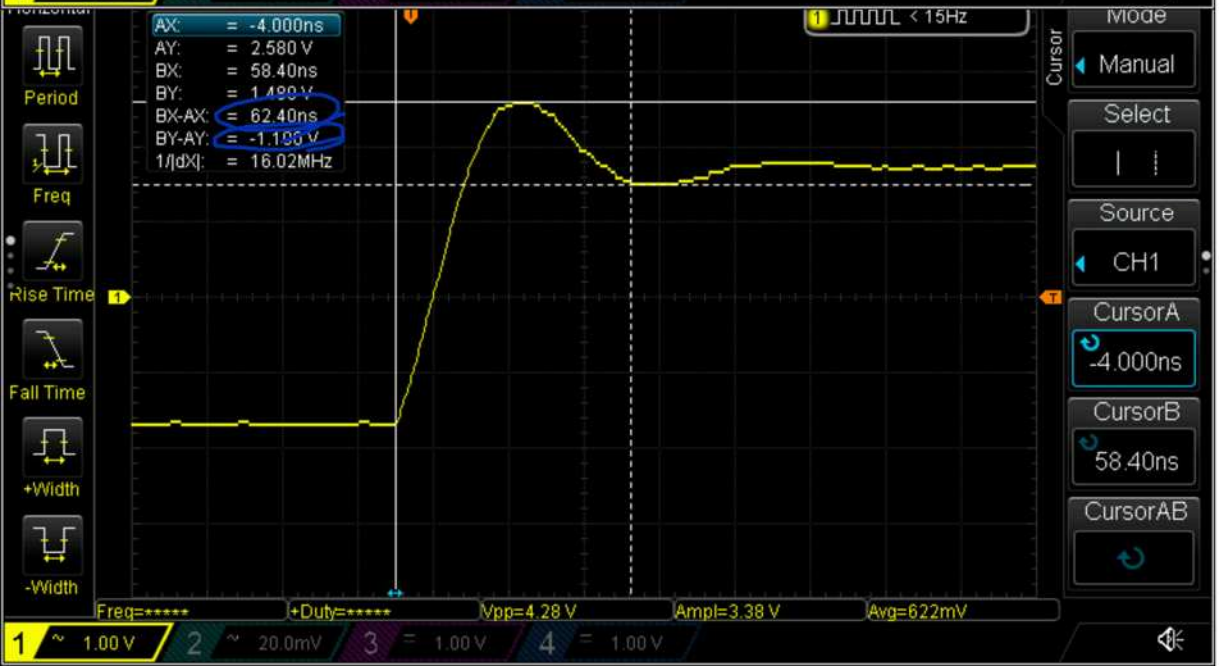

RIGOL
STOP
H 500ns
500MSa/s
3.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
710.609kHz
CH1
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Freq=714kHz
+Duty=50.00 %
Vpp=4.84 V
Ampl=3.42 V
Avg=803uV
1 ~ 1.00 V
2 ~ 20.0mV
3 = 1.00 V
4 = 1.00 V


RIGOL
STOP
H 20.0ns
500MSa/s
120 pts
D 46.0000000ns
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
AX: = -2.400ns
AY: = 2.280 V
BX: = 79.20ns
BY: = 1.540 V
BX-AX: = 81.60ns
BY-AY: = -740.0mV
1/|dX|: = 12.25MHz
< 15Hz
Cursor
Mode
Manual
Select
Source
CH1
CursorA
2.280 V
CursorB
1.540 V
CursorAB

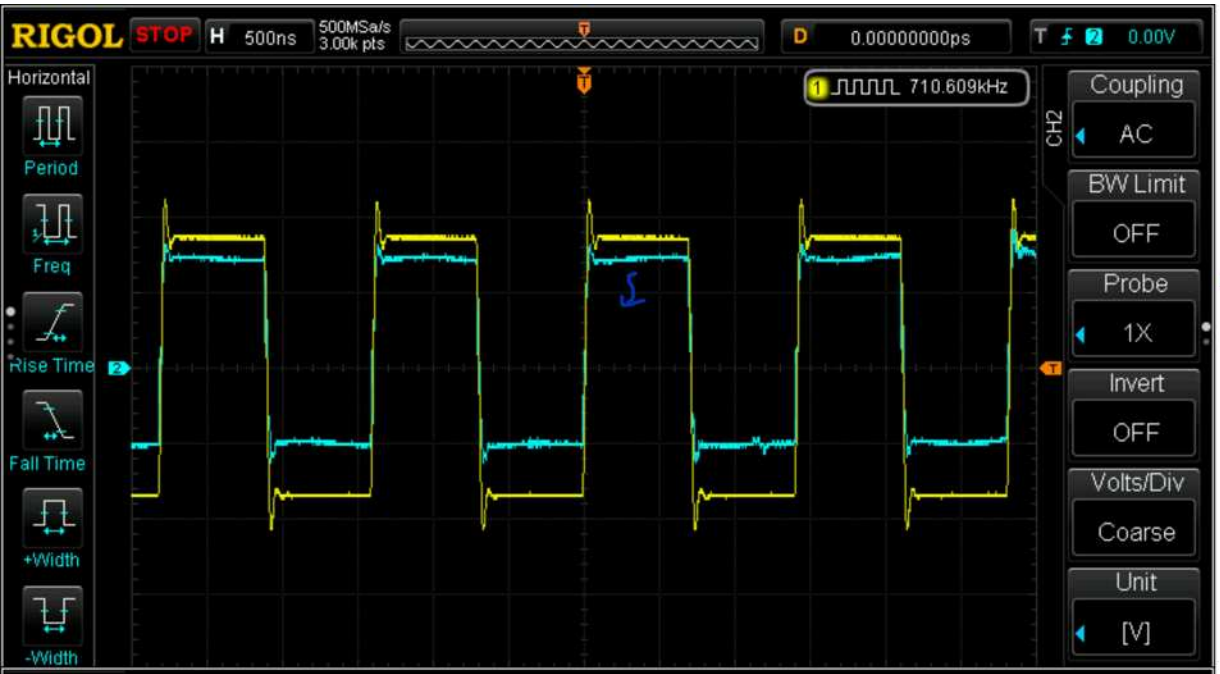
Low

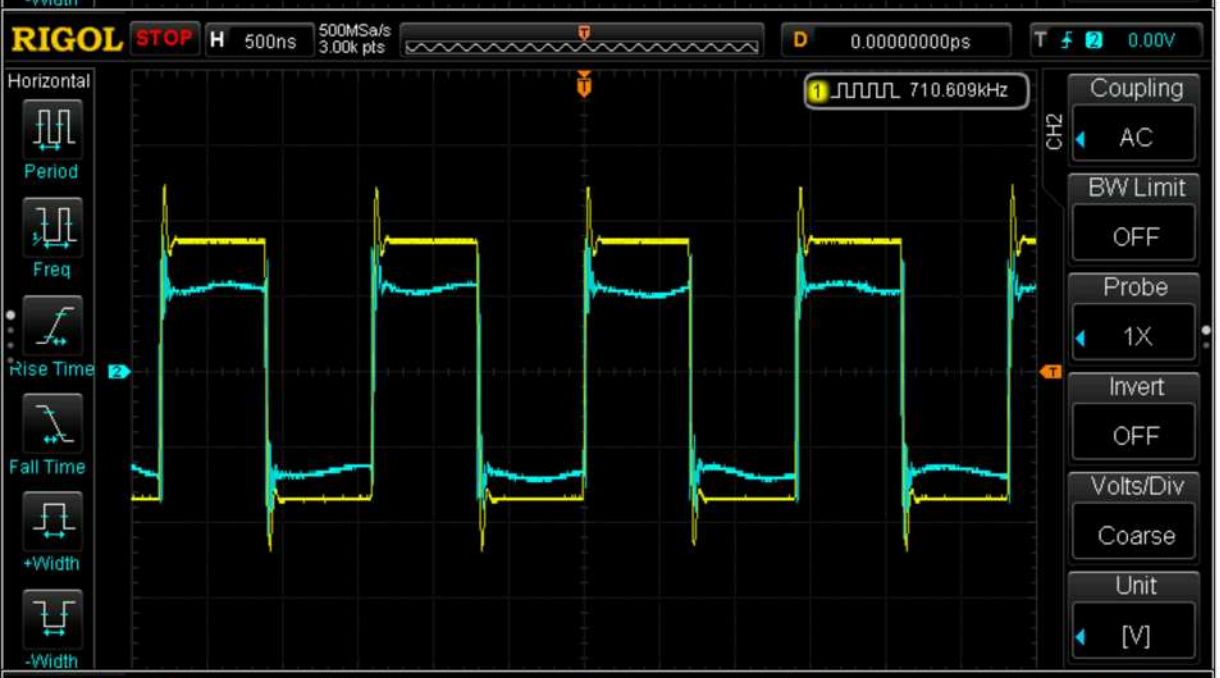

RIGOL
STOP
H 20.0ns
500MSa/s
120 pts
D 46.0000000ns
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
AX: = -6.400ns
AY: = 2.580 V
BX: = 66.40ns
BY: = 1.500 V
BX-AX: = 72.80ns
BY-AY: = -1.080 V
1/|dX|: = 13.74MHz
< 15Hz
Cursor
Mode
Manual
Select
Source
CH1
CursorA
2.580 V
CursorB
1.500 V
CursorAB
Freq=*****
+Duty=*****
Vpp=4.32 V
Ampl=3.41 V
Avg=637mV
1 ~ 1.00 V
2 ~ 20.0mV
3 = 1.00 V
4 = 1.00 V

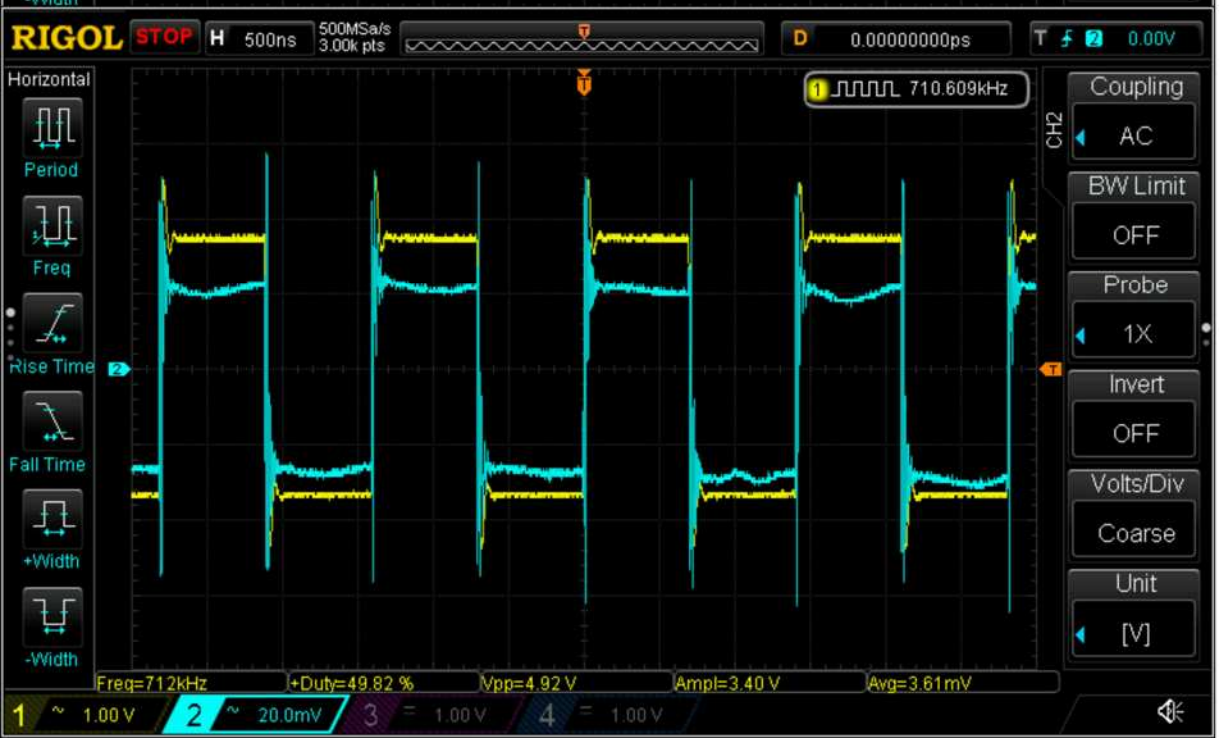
mid


Period
Freq
Rise Time
Fall Time
+Width
-Width
AX: = -4.000ns
AY: = 2.580 V
BX: = 58.40ns
BY: = 1.480 V
BX-AX: = 62.40ns
BY-AY: = -1.100 V
1/|dX|: = 16.02MHz
< 15Hz
Cursor
Mode
Manual
Select
Source
CH1
CursorA
-4.000ns
CursorB
58.40ns
CursorAB
Freq=*****
+Duty=*****
Vpp=4.28 V
Ampl=3.38 V
Avg=622mV
1 ~ 1.00 V
2 ~ 20.0mV
3 = 1.00 V
4 = 1.00 V

High

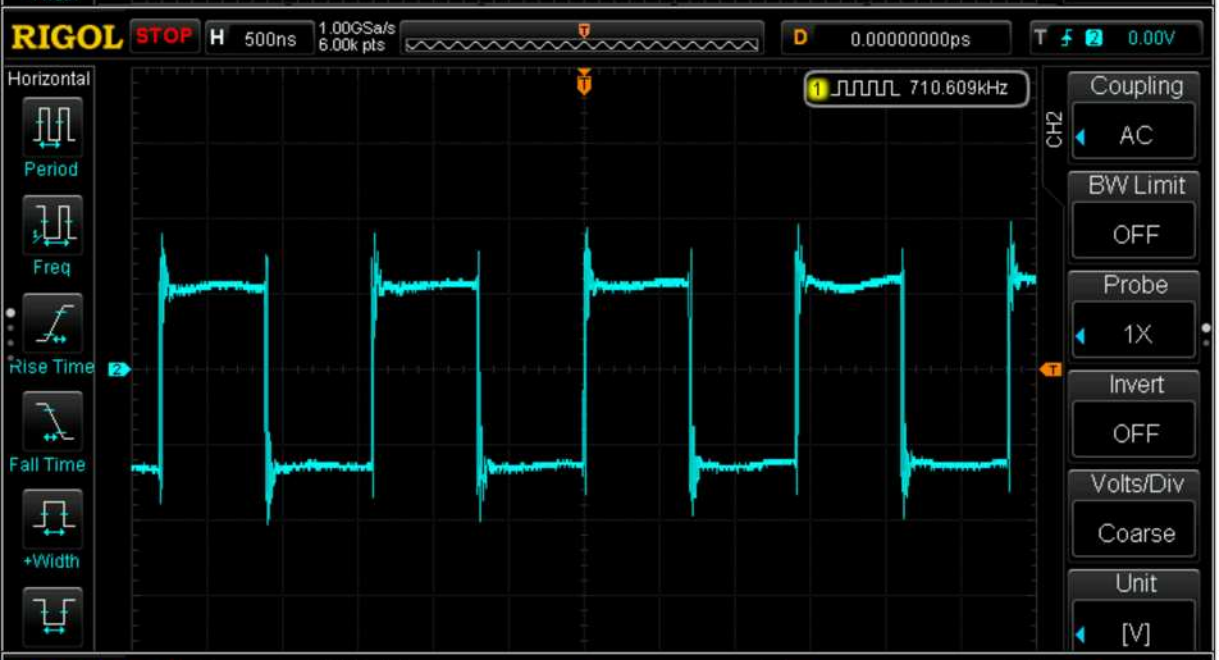

RIGOL
STOP
H 500ns
500MSa/s
3.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
710.609kHz
CH2
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]


RIGOL
STOP
H 500ns
500MSa/s
3.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
710.609kHz
CH2
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]


RIGOL
STOP
H 500ns
500MSa/s
3.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
710.609kHz
CH2
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Freq=712kHz
+Duty=49.82 %
Vpp=4.92 V
Ampl=3.40 V
Avg=3.61mV
1 ~ 1.00 V
2 ~ 20.0mV
3 = 1.00 V
4 = 1.00 V


RIGOL
STOP
H 500ns
1.00GSa/s
6.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
< 15Hz
Zone < 2.5
Zone
CH2
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]

Low


RIGOL
STOP
H 500ns
1.00GSa/s
6.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
710.609kHz
CH2
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]

med


RIGOL
STOP
H 500ns
500MSa/s
3.00k pts
D 0.00000000ps
T 0.00V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
710.609kHz
1 ms
CH2
Coupling
AC
BW Limit
OFF
Probe
1X
Invert
OFF
Volts/Div
Coarse
Unit
[V]
Freq=*****
+Duty=*****
Vpp=*****
Ampl=*****
Avg=*****
1 ~ 1.00 V
2 ~ 20.0mV
3 = 1.00 V
4 = 1.00 V

high