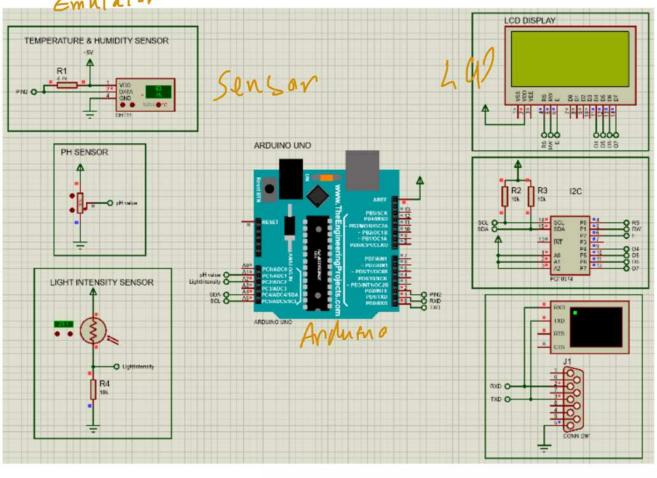
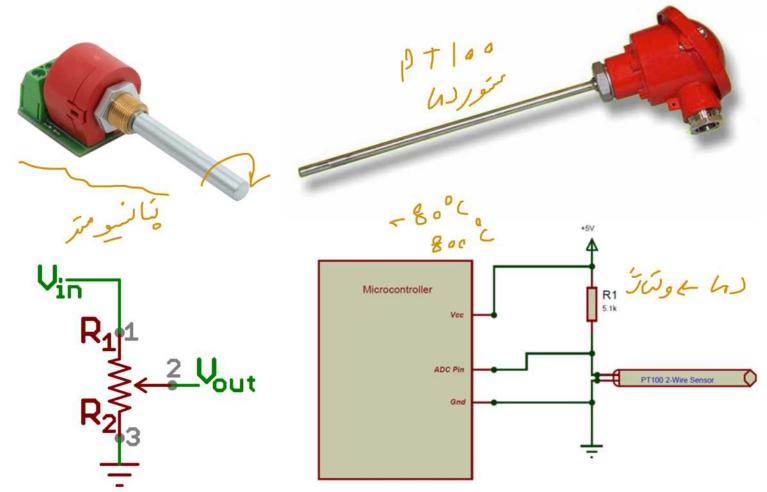


Simulator Emulator



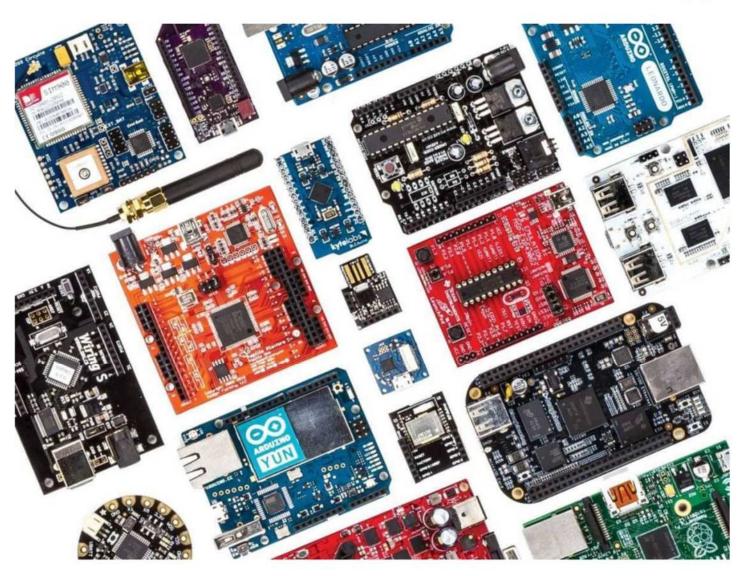




Reduced Instruction Set Computer

Complex Instruction Set Computer

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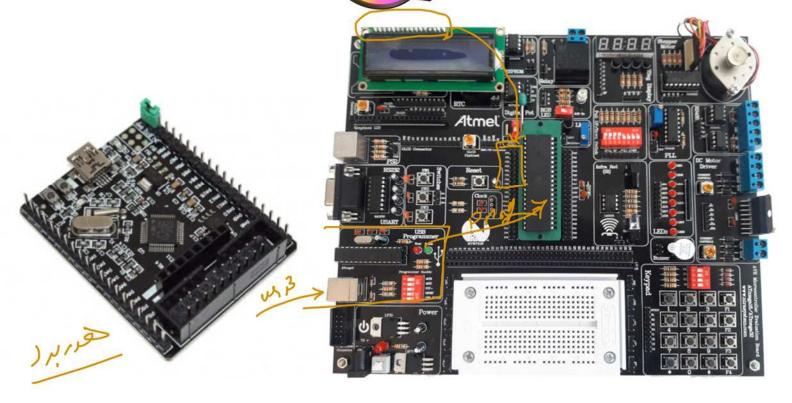


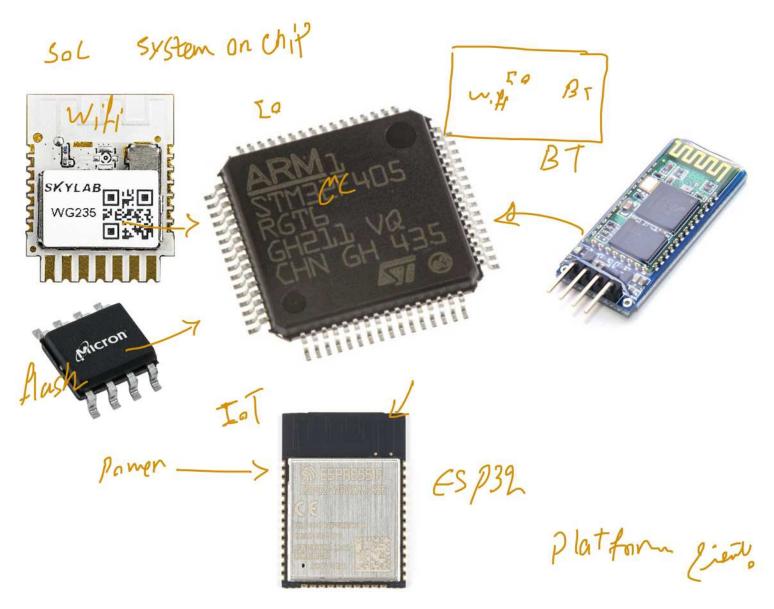






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- Table 1. Device summary
- 1 Introduction 1 Introduction

- □ □ 3 Pinouts and pin description
 □ □ 4 Memory mapping
- □ □ 5 Electrical characteristics
- ☐ 6 Package information
 ☐ 7 Ordering information 7 Ordering information schem
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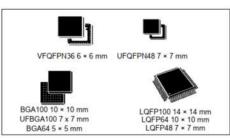
STM32F103x8 STM32F103xB

Medium-density performance line Arm®-based 32-bit MCU with 64 or 128 KB Flash, USB, CAN, 7 timers, 2 ADCs, 9 com. interfaces

Datasheet - production data

Features

- Arm® 32-bit Cortex®-M3 CPU core
 - -/72 MHz maximum frequency, 1.25 DMIPS / MHz (Dhrystone 2.1) performance at 0 wait state memory access
 - Single-cycle multiplication and hardware division
- Memories
 - 64 or 128 Kbytes of Flash memory
 - 20 Kbytes of SRAM



- Debug mode
 - Serial wire debug (SWD) and JTAG interfaces

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- ⊕ ☐ 7 Low-, medium-, high- and XL-density reset and clock control (RCC) ⊕ ☐ 8 Connectivity line devices: reset and clock control (RCC)
- ⊕ Q General-purpose and alternate-function I/Os (GPIOs and AFIOs)
- E-□ 10 Interrupts and events
 E-□ 11 Analog-to-digital converter (ADC)
- ⊕- □ 12 Digital-to-analog converter (DAC)
- B → 13 Direct memory access controller (DMA)
 D → 14 Advanced-control timers (TIM1 and TIM8)
 D → 15 General-purpose timers (TIM2 to TIM5)

- ⊞-□ 16 General-purpose timers (TIM9 to TIM14)
- B □ □ 17 Basic timers (TIM6 and TIM7)
 □ □ □ 18 Real-time clock (RTC)
- □ □ 19 Independent watchdog (IWDG)
- B-□ 20 Window watchdog (WWDG)
 D-□ 21 Flexible static memory controller (FSMC)
- ⊕ □ 22 Secure digital input/output interface (SDIO)
- ⊕ ☐ 23 Universal serial bus full-speed device interface (USB) ⊕ ☐ 24 Controller area network (bxCAN)
- □ □ 25 Serial perpheral interface (SPI)
 □ □ 26 Inter-integrated circuit (I2C) interface
 □ □ 27 Universal synchronous asynchronous receiver transmitter (USART)
- ⊕- ☐ 28 USB on-the-go full-speed (OTG_FS)
- \oplus \square 29 Ethernet (ETH): media access control (MAC) with DMA controlle \oplus \square 30 Device electronic signature
- 31 Debug support (DBG)
- ⊕ □ 32 Revision history



RM0008 Reference manual

STM32F101xx, STM32F102xx, STM32F103xx, STM32F105xx and STM32F107xx advanced Arm®-based 32-bit MCUs

Introduction

This reference manual is addressed to application developers.

It provides complete information on how to use the STM32F101xx, STM32F102xx, STM32F103xx and STM32F105xx/STM32F107xx microcontroller memory and peripherals. These devices, featuring different memory sizes, packages and peripherals, are referred to as STM32F10xxx throughout the document, unless otherwise specified.

For ordering information, mechanical and electrical device characteristics refer to the low-, medium-, high- and XL-density STM32F101xx and STM32F103xx datasheets, to the low-and medium-density STM32F102xx datasheets and to the STM32F105xx/STM32F107xx

For information on programming, erasing and protection of the internal Flash memory refer

- . PM0075 for low-, medium- high-density and connectivity line STM32F10xxx devices
- PM0068 for XL-density STM32F10xxx devices

For information on the Arm® Cortex®-M3 core, refer to PM0056, STM32F10xxx Cortex®-M3 programming manual













AN2834 Application note

How to optimize the ADC accuracy in the STM32 MCUs

Introduction

STM32 MCUs embed advanced 12-bit to 16-bit ADCs depending on the device. A selfcalibration feature is provided to enhance ADC accuracy versus environmental condition changes.

In applications involving analog-to-digital conversion, ADC accuracy has an impact on the overall system quality and efficiency. To improve this accuracy, the errors associated with the ADC and the parameters affecting them must be understood.

ADC accuracy does not only depend on ADC performance and features, but also on the overall application design around the ADC.

This application note aim is to help understand ADC errors and explain how to enhance ADC accuracy. It is divided into three main parts:

- A simplified description of ADC internal structure to help understand ADC operation and related ADC parameters.
- Explanations of the different types and sources of ADC errors, related to the ADC design and to external ADC parameters, such as the external hardware design.
- Recommendations on how to minimize these errors, focusing on hardware and software methods.

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Table 13-1. Device Clocking Options Select

Cuco Bit		7 113.07%
andister	1 number	

Device Clocking Option	25	CKSEL[3:0]
Low Power Crystal Oscillator	(INY)	1111 - 1000
Full Swing Crystal Oscillator	(1/1)	0111 - 0110
Low Frequency Crystal Oscillator		0101 - 0100
Internal 128kHz RC Oscillator		0011
Calibrated Internal RC Oscillator		0010
External Clock		0000
Reserved		0001

Note: For all fuses, '1' means unprogrammed while '0' means programmed.

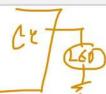


Table 14-1. Port Pin Configurations

DDxn	PORTxn	PUD (in MCUCR)	1/0	Pull-up	Comment
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)