14.4.3 DDRB – The Port B Data Direction Register

Bit	7	6	5	4	3	2	1	0	
0x04 (0x24)	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PB0 → کمترین

DDRB	The Port B Data Direction Register						
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1

DDRB = 0b00000001 → 76 ... 0 → Bin

4 bit → 2^3 2^2 2^1 2^0

DDRB	The Port B Data Direction Register							
8	4	2	1	8	4	2	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1

0 + 0 + 0 + 0 = 0 → بیشترین مقدار

DDRB = 0x01 → 16

8x0 + 4x0 + 2x0 + 1x1 = 1

DECIMAL	HEX	BINARY
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

$2^7 = 128$ → 2^1 → 2^0

DDRB	The Port B Data Direction Register						
128	64	32	16	8	4	2	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1

DDRB = 1

128x0 + 64x0 + 32x0 + 16x0 + 8x0 + 4x0 + 2x0 + 1x1 = 1

DDRB	The Port B Data Direction Register						
DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1

DDRB = 1<<0

DDRB = 1<<DDB0

DDRB	The Port B Data Direction Register						
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	0	0	1	0	1

DDRB = 0b00100101

DDRB	The Port B Data Direction Register						
8	4	2	1	8	4	2	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	0	0	1	0	1

DDRB = 0x25

DDRB	The Port B Data Direction Register						
DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	0	0	1	0	1

DDRB = 1<<0 | DDRB = 1<<DDB0

DDRB = 1<<2 | DDRB = 1<<DDB2

DDRB = 1<<5 | DDRB = 1<<DDB5

DDRB = 1<<5 | 1<<2 | 1<<0

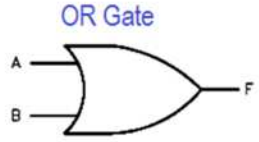
DDRB	The Port B Data Direction Register						
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	0	1	0	1	0	1
0	0	0	0	1	0	0	0

OR

1<<3

Or

0	1	0	1	1	1	0	1



INPUT		OUTPUT
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

```
#define setBit(Reg, Bit) (Reg |= (1<<Bit))
```

setBit(DDRB, 3)

DDRB	The Port B Data Direction Register						
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	0	1	0	1	0	1
0	0	0	1	0	0	0	0
1	1	1	0	1	1	1	1
0	1	0	0	0	1	0	1

1<<4

~(1<<4)

AND

AND Gate

INPUT		OUTPUT
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

```
#define clearBit(Reg, Bit) (Reg &= ~(1<<Bit))
```

```
clearBit(DDRB, 4)
```

DDRB	The Port B Data Direction Register						
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	0	1	0	1	0	1
0	0	1	0	0	0	0	0
0	1	1	0	0	1	0	1

1<<5

Exclusive OR Gate

INPUT		OUTPUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

I

II

```
#define toggleBit(Reg, Bit) (Reg ^= 1<<Bit)
```

```
toggleBit(DDRB, 5)
```

```
#define changeBit(Reg, Bit, Value) (Value == 1 ? setBit(Reg, Bit) : clearBit(Reg, Bit))
```

```
changeBit(DDRB, 2, 1)
```

```
setBit(DDRB, 2)
```

```
changeBit(DDRB, 5, 0)
```

```
clearBit(DDRB, 5)
```

PINB	The Port B Input Pins Address						
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	0	1	0	1	0	1

PB2 → input

0	0	0	1	0	1	0	1

PINB>>2

0	0	0	0	0	0	0	1

0x01

0	0	0	0	0	0	0	1

And

0x01 1 0b1

```
#define checkBit(Reg, Bit) ((Reg>>Bit) & 0x01)
```

checkBit(PINB, 2) = 1

PINB	The Port B Input Pins Address						
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	0	1	0	0	0	1

0	0	0	1	0	1	0	0

DDRB>>2

0	0	0	0	0	0	0	1

0x01

0	0	0	0	0	0	0	0

And

0x00 0 0b0

checkBit(PINB, 2) = 0

DDB2