For all fuses “1” means unprogrammed while “0” means programmed.

Table 28-6. Extended Fuse Byte for ATmega328/328P

Extended Fuse Byte	Bit No	Description	Default Value
–	7	–	1
–	6	–	1
–	5	–	1
–	4	–	1
–	3	–	1
BODLEVEL2[1]	2	Brown-out Detector trigger level	1 (unprogrammed)
BODLEVEL1[1]	1	Brown-out Detector trigger level	1 (unprogrammed)
BODLEVEL0[1]	0	Brown-out Detector trigger level	1 (unprogrammed)

ef = 0xff

Figure 29-1. Maximum Frequency vs. V_{CC}

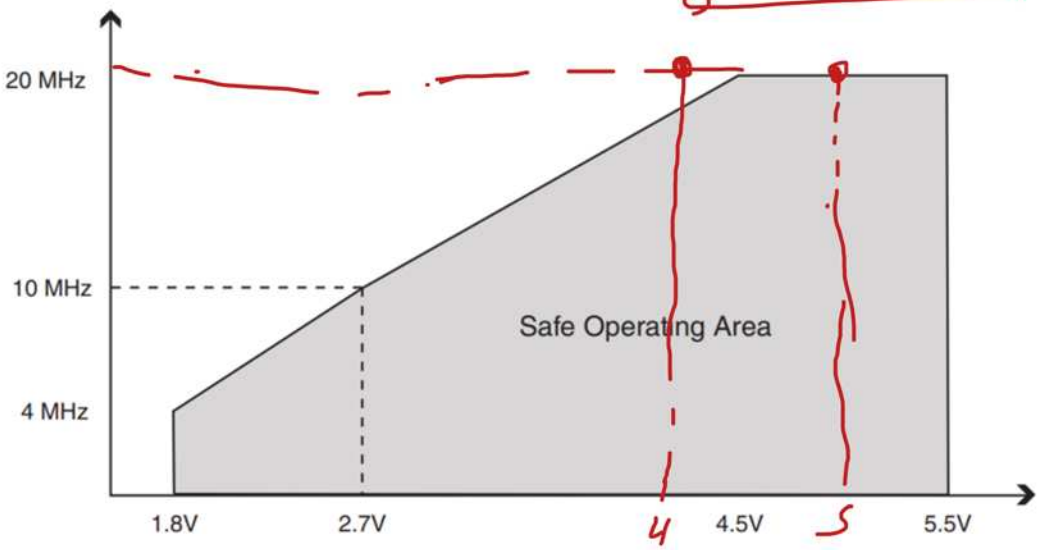

Figure 11-5. Brown-out Reset During Operation

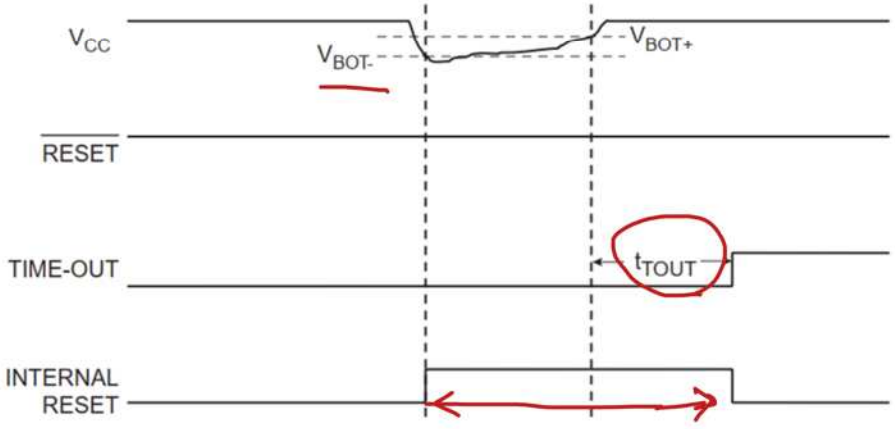

Table 29-12. BODLEVEL Fuse Coding[1][2]

BODLEVEL 2:0 Fuses	Min. V_{BOT}	Typ V_{BOT}	Max V_{BOT}	Units
111	BOD Disabled			
110	1.7	1.8	2.0	V
101	2.5	2.7	2.9	
100	4.1	4.3	4.5	
011	Reserved			
010				
001				
000				

Notes:
1. V_{BOT} may be below nominal minimum operating voltage for some devices. For devices where this is the case, the device is tested down to $V_{CC} = V_{BOT}$ during the production test. This guarantees that a Brown-Out Reset will occur before V_{CC} drops to a voltage where correct operation of the microcontroller is no longer guaranteed. The test is performed using BODLEVEL = 110, 101 and 100.
2. V_{BOT} tested at 25°C and 85°C in production

Table 28-8. Fuse High Byte for **ATmega328/328P**

High Fuse Byte	Bit No	Description	Default Value
RSTDISBL[1]	7	External Reset Disable	1 (unprogrammed)
DWEN	6	debugWIRE Enable	1 (unprogrammed)
SPIEN[2]	5	Enable Serial Program and Data Downloading	0 (programmed, SPI programming enabled)
WDTON[3]	4	Watchdog Timer Always On	1 (unprogrammed)
EESAVE	3	EEPROM memory is preserved through the Chip Erase	0 (unprogrammed), EEPROM not reserved
BOOTSZ1	2	Select Boot Size (see Table 27-7 on page 275, Table 27-10 on page 276 and Table 27-13 on page 277 for details)	0 (programmed)[4]
BOOTSZ0	1	Select Boot Size (see Table 27-7 on page 275, Table 27-10 on page 276 and Table 27-13 on page 277 for details)	0 (programmed)[4]
BOOTRST	0	Select Reset Vector	1 (unprogrammed)

Notes:
1. See "Alternate Functions of Port C" on page 85 for description of RSTDISBL Fuse.
2. The SPIEN Fuse is not accessible in serial programming mode.
3. See "WDTCSR – Watchdog Timer Control Register" on page 54 for details.
4. The default value of BOOTSZ[1:0] results in maximum Boot Size. See "Pin Name Mapping" on page 286.

Hf = 0x17

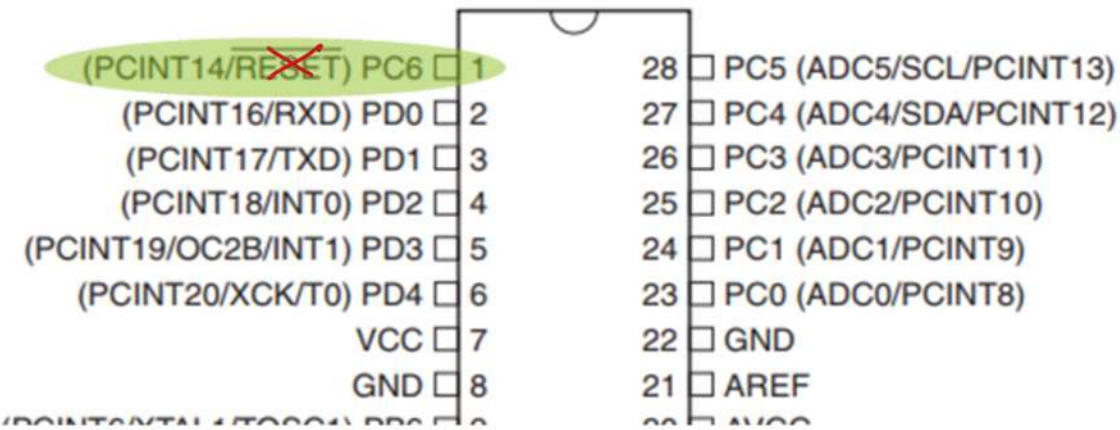

Table 27-7. Boot Size Configuration, ATmega88A/88PA

BOOTSZ1	BOOTSZ0	Boot Size	Pages	Application Flash Section	Boot Loader Flash Section	End Application Section	Boot Reset Address (Start Boot Loader Section)
1	1	128 words	4	0x000 - 0xF7F	0xF80 - 0xFFF	0xF7F	0xF80
1	0	256 words	8	0x000 - 0xEFF	0xF00 - 0xFFF	0xEFF	0xF00
0	1	512 words	16	0x000 - 0xDFF	0xE00 - 0xFFF	0xDFF	0xE00
0	0	1024 words	32	0x000 - 0xBFF	0xC00 - 0xFFF	0xBFF	0xC00

Note: The different BOOTSZ Fuse configurations are shown in Figure 27-2 on page 266.

2KB word = 2Byte

Table 28-9. Fuse Low Byte

Low Fuse Byte	Bit No	Description	Default Value
CKDIV8[4]	7	Divide clock by 8	0 (programmed)
CKOUT[3]	6	Clock output	1 (unprogrammed)
SUT1	5	Select start-up time	1 (unprogrammed)[1]
SUT0	4	Select start-up time	0 (programmed)[1]
CKSEL3	3	Select Clock source	0 (programmed)[2]
CKSEL2	2	Select Clock source	0 (programmed)[2]
CKSEL1	1	Select Clock source	1 (unprogrammed)[2]
CKSEL0	0	Select Clock source	0 (programmed)[2]

LF = 0xE2

Note: 1. The default value of SUT1...0 results in maximum start-up time for the default clock source. See Table 9-12 on page 34 for details.
2. The default setting of CKSEL3...0 results in internal RC Oscillator @ 8MHz. See Table 9-11 on page 34 for details.
3. The CKOUT Fuse allows the system clock to be output on PORTB0. See "Clock Output Buffer" on page 36 for details.
4. See "System Clock Prescaler" on page 36 for details.

The status of the Fuse bits is not affected by Chip Erase. Note that the Fuse bits are locked if Lock bit1 (LB1) is programmed. Program the Fuse bits before programming the Lock bits.

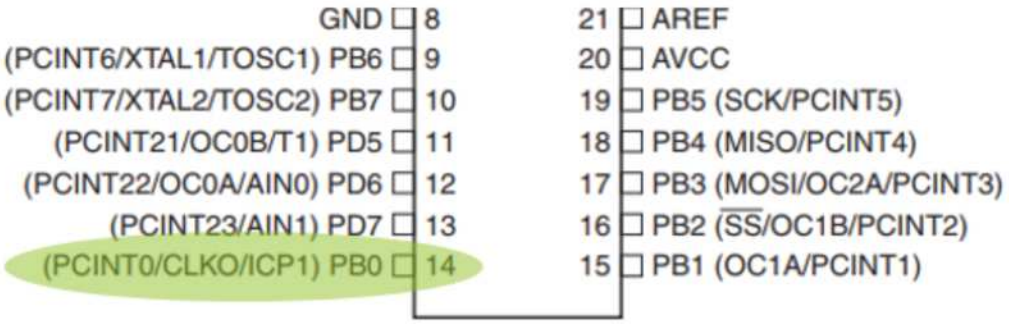

Table 9-1. Device Clocking Options Select[1]

Device Clocking Option	CKSEL3...0
Low Power Crystal Oscillator	< 16 → 1111 - 1000
Full Swing Crystal Oscillator	20 → 0111 - 0110
Low Frequency Crystal Oscillator	128k 0101 - 0100
Internal 128kHz RC Oscillator	128k 0011
Calibrated Internal RC Oscillator	8MHz 0010
External Clock	0000
Reserved	0001

Note: 1. For all fuses "1" means unprogrammed while "0" means programmed.

0.4MHZ ~ 16MHZ

Table 9-3. Low Power Crystal Oscillator Operating Modes[3]

Frequency Range (MHz)	Recommended Range for Capacitors C1 and C2 (pF)	CKSEL3...1[1]
0.4 - 0.9	–	100[2]
0.9 - 3.0	12 - 22	101
3.0 - 8.0	12 - 22	110
8.0 - 16.0	12 - 22 pF	111

Notes:
1. This is the recommended CKSEL settings for the difference frequency ranges.
2. This option should not be used with crystals, only with ceramic resonators.
3. If the crystal frequency exceeds the specification of the device (depends on V_{CC}), the CKDIV8 Fuse can be programmed in order to divide the internal frequency by 8. It must be ensured that the resulting divided clock meets the frequency specification of the device.

The CKSEL0 Fuse together with the SUT1...0 Fuses select the start-up times as shown in Table 9-4.

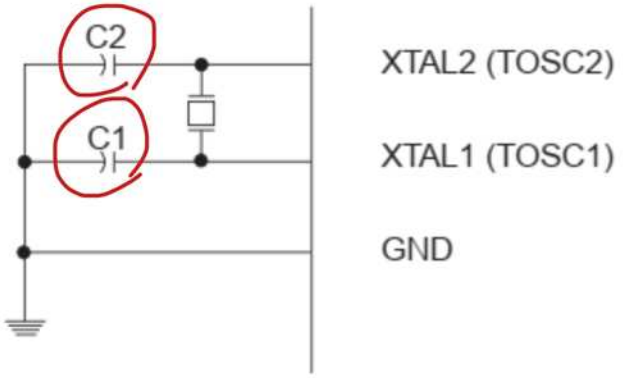

Table 9-4. Start-up Times for the Low Power Crystal Oscillator Clock Selection

Oscillator Source / Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	CKSEL0	SUT1...0
Ceramic resonator, fast rising power	258 CK	14CK + 4.1ms[1]	0	00
Ceramic resonator, slowly rising power	258 CK	14CK + 65ms[1]	0	01
Ceramic resonator, BOD enabled	1K CK	14CK[2]	0	10
Ceramic resonator, fast rising power	1K CK	14CK + 4.1ms[2]	0	11
Ceramic resonator, slowly rising power	1K CK	14CK + 65ms[2]	1	00
Crystal Oscillator, BOD enabled	16K CK	14CK	1	01
Crystal Oscillator, fast rising power	16K CK	14CK + 4.1ms	1	10
Crystal Oscillator, slowly rising power	16K CK	14CK + 65ms	1	11

Notes:
1. These options should only be used when not operating close to the maximum frequency of the device, and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum frequency of the device, and if frequency stability at start-up is not important for the application.

Table 9-5. Full Swing Crystal Oscillator operating modes

Frequency Range[1] (MHz)	Recommended Range for Capacitors C1 and C2 (pF)	CKSEL3...1
0.4 - 20	12 - 22	011

Notes: 1. If the cryatal frequency exceeds the specification of the device (depends on V_{CC}), the CKDIV8 Fuse can be programmed in order to divide the internal frequency by 8. It must be ensured that the resulting divided clock meets the frequency specification of the device.

Figure 9-3. Crystal Oscillator Connections

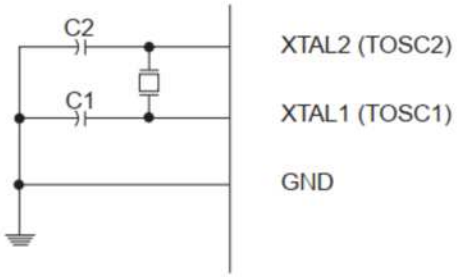

Table 9-6. Start-up Times for the Full Swing Crystal Oscillator Clock Selection

Oscillator Source / Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	CKSEL0	SUT1...0
Ceramic resonator, fast rising power	258 CK	14CK + 4.1ms[1]	0	00
Ceramic resonator, slowly rising power	258 CK	14CK + 65ms[1]	0	01
Ceramic resonator, BOD enabled	1K CK	14CK[2]	0	10
Ceramic resonator, fast rising power	1K CK	14CK + 4.1ms[2]	0	11
Ceramic resonator, slowly rising power	1K CK	14CK + 65ms[2]	1	00
Crystal Oscillator, BOD enabled	16K CK	14CK	1	01
Crystal Oscillator, fast rising power	16K CK	14CK + 4.1ms	1	10
Crystal Oscillator, slowly rising power	16K CK	14CK + 65ms	1	11

Notes: 1. These options should only be used when not operating close to the maximum frequency of the device, and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.

2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum frequency of the device, and if frequency stability at start-up is not important for the application.

9.5 Low Frequency Crystal Oscillator 128KHZ

The Low-frequency Crystal Oscillator must be selected by setting the CKSEL Fuses to “0110” or “0111”, as shown in Table 9-10 on page 33. Start-up times are determined by the SUT Fuses as shown in Table 9-9.

Table 9-9. Start-up Times for the Low-frequency Crystal Oscillator Clock Selection

SUT1...0	Additional Delay from Reset (V_{CC} = 5.0V)	Recommended Usage
00	4 CK	Fast rising power or BOD enabled
01	4 CK + 4.1ms	Slowly rising power
10	4 CK + 65ms	Stable frequency at start-up
11	Reserved	

Table 9-10. Start-up Times for the Low-frequency Crystal Oscillator Clock Selection

CKSEL3...0	Start-up Time from Power-down and Power-save	Recommended Usage
0100(1)	1K CK	
0101	32K CK	Stable frequency at start-up

9.7 128kHz Internal Oscillator

The 128kHz internal Oscillator is a low power Oscillator providing a clock of 128kHz. The frequency is nominal at 3V and 25°C. This clock may be select as the system clock by programming the CKSEL Fuses to “11” as shown in Table 9-13.

Table 9-13. 128kHz Internal Oscillator Operating Modes

Nominal Frequency(1)	CKSEL3...0
128kHz	0011

Note: 1. Note that the 128kHz oscillator is a very low power clock source, and is not designed for high accuracy.

Table 9-14. Start-up Times for the 128kHz Internal Oscillator

Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset	SUT1...0
BOD enabled	6 CK	14CK(1)	00
Fast rising power	6 CK	14CK + 4ms	01
Slowly rising power	6 CK	14CK + 64ms	10
Reserved			11

Note: 1. If the RSTDISBL fuse is programmed, this start-up time will be increased to 14CK + 4.1ms to ensure programming mode can be entered.

9.6 Calibrated Internal RC Oscillator 8MHZ

Table 9-11. Internal Calibrated RC Oscillator Operating Modes

Frequency Range[2] (MHz)	CKSEL3...0
7.3 - 8.1	0010[1]

Notes: 1. The device is shipped with this option selected.
2. If 8MHz frequency exceeds the specification of the device (depends on V_{CC}), the CKDIV8 Fuse can be programmed in order to divide the internal frequency by 8.

When this Oscillator is selected, start-up times are determined by the SUT Fuses as shown in Table 9-12.

Table 9-12. Start-up times for the internal calibrated RC Oscillator clock selection

Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	SUT1...0
BOD enabled	6 CK	14CK[1]	00
Fast rising power	6 CK	14CK + 4.1ms	01
Slowly rising power	6 CK	14CK + 65ms[2]	10
Reserved			11

Note: 1. If the RSTDISBL fuse is programmed, this start-up time will be increased to 14CK + 4.1ms to ensure programming mode can be entered.
2. The device is shipped with this option selected.

9.8 External Clock

Table 9-15. Crystal Oscillator Clock Frequency

Frequency	CKSEL3...0
0 - 20MHz	0000

Figure 9-4. External Clock Drive Configuration

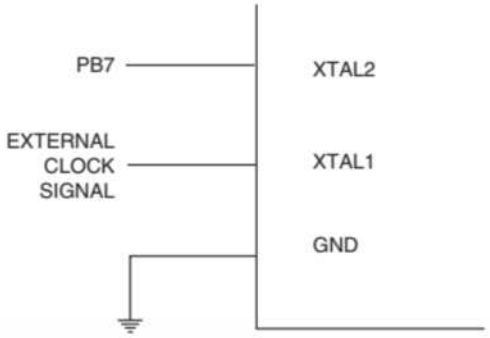

Table 9-16. Start-up Times for the External Clock Selection

Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	SUT1...0
BOD enabled	6 CK	14CK	00
Fast rising power	6 CK	14CK + 4.1ms	01
Slowly rising power	6 CK	14CK + 65ms	10
Reserved			11

When applying an external clock, it is required to avoid sudden changes in the applied clock frequency to ensure stable operation of the MCU. A variation in frequency of more than 2% from one clock cycle to the next can lead to unpredictable behavior. If changes of more than 2% is required, ensure that the MCU is kept in Reset during the changes.

hardWare	softWare	Delay 1'S
8'MHz	8'MHz	1sec
8/8 = 1'MHz	8'MHz	1×8 = 8Sec
1×8 = 8'MHz	1'MHz	1/8 = 125mS

Table 28-1. Lock Bit Byte[1]

Lock Bit Byte	Bit No	Description	Default Value
	7	–	1 (unprogrammed)
	6	–	1 (unprogrammed)
BLB12[2]	5	Boot Lock bit	1 (unprogrammed)
BLB11[2]	4	Boot Lock bit	1 (unprogrammed)
BLB02[2]	3	Boot Lock bit	1 (unprogrammed)
BLB01[2]	2	Boot Lock bit	1 (unprogrammed)
LB2	1	Lock bit	1 (unprogrammed)
LB1	0	Lock bit	1 (unprogrammed)

LB = 0xFF

Boot

APP

Notes: 1. "1" means unprogrammed, "0" means programmed.
2. Only on ATmega88A/88PA/168A/168PA/328/328P.

Table 28-2. Lock Bit Protection Modes[1][2]

Memory Lock Bits			Protection Type
LB Mode	LB2	LB1	
1	1	1	No memory lock features enabled.
2	1	0	Further programming of the Flash and EEPROM is disabled in Parallel and Serial Programming mode. The Fuse bits are locked in both Serial and Parallel Programming mode.[1]
3	0	0	Further programming and verification of the Flash and EEPROM is disabled in Parallel and Serial Programming mode. The Boot Lock bits and Fuse bits are locked in both Serial and Parallel Programming mode.[1]

Notes: 1. Program the Fuse bits and Boot Lock bits before programming the LB1 and LB2.
2. "1" means unprogrammed, "0" means programmed

SPM: Store Program memory
LPM: Load program memory

Table 28-3. Lock Bit Protection Modes[1][2]. Only ATmega88A/88PA/168A/168PA/328/328P.

BLB0 Mode	BLB02	BLB01	
1	1	1	No restrictions for SPM or LPM accessing the Application section.
2	1	0	SPM is not allowed to write to the Application section.
3	0	0	SPM is not allowed to write to the Application section, and LPM executing from the Boot Loader section is not allowed to read from the Application section. If Interrupt Vectors are placed in the Boot Loader section, interrupts are disabled while executing from the Application section.
4	0	1	LPM executing from the Boot Loader section is not allowed to read from the Application section. If Interrupt Vectors are placed in the Boot Loader section, interrupts are disabled while executing from the Application section.

SPM → write

LPM → Read

BLB1 Mode	BLB12	BLB11	
1	1	1	No restrictions for SPM or LPM accessing the Boot Loader section.
2	1	0	SPM is not allowed to write to the Boot Loader section.
3	0	0	SPM is not allowed to write to the Boot Loader section, and LPM executing from the Application section is not allowed to read from the Boot Loader section. If Interrupt Vectors are placed in the Application section, interrupts are disabled while executing from the Boot Loader section.
4	0	1	LPM executing from the Application section is not allowed to read from the Boot Loader section. If Interrupt Vectors are placed in the Application section, interrupts are disabled while executing from the Boot Loader section.

Notes: 1. Program the Fuse bits and Boot Lock bits before programming the LB1 and LB2.
2. "1" means unprogrammed, "0" means programmed