

mega 328

(PCINT14/RESET) PC6	1	28	PC5 (ADC5/SCL/PCINT13)
(PCINT16/RXD) PD0	2	27	PC4 (ADC4/SDA/PCINT12)
(PCINT17/TXD) PD1	3	26	PC3 (ADC3/PCINT11)
(PCINT18/INT0) PD2	4	25	PC2 (ADC2/PCINT10)
(PCINT19/OC2B/INT1) PD3	5	24	PC1 (ADC1/PCINT9)
(PCINT20/XCK/T0) PD4	6	23	PC0 (ADC0/PCINT8)
VCC	7	22	GND
GND	8	21	AREF
(PCINT6/XTAL1/TOSC1) PB6	9	20	AVCC
(PCINT7/XTAL2/TOSC2) PB7	10	19	PB5 (SCK/PCINT5)
(PCINT21/OC0B/T1) PD5	11	18	PB4 (MISO/PCINT4)
(PCINT22/OC0A/AIN0) PD6	12	17	PB3 (MOSI/OC2A/PCINT3)
(PCINT23/AIN1) PD7	13	16	PB2 (\overline{SS} /OC1B/PCINT2)
(PCINT0/CLKO/ICP1) PB0	14	15	PB1 (OC1A/PCINT1)

$\left\{ \begin{array}{l} \text{DDR}_X \\ \text{PORT}_X \\ \text{PIN}_X \end{array} \right\} \mid X = \{B, C, D\}$

$\left\{ \begin{array}{l} \text{DDRB} \\ \text{PORTB} \\ \text{PINB} \end{array} \right\}$

مجموع ریسٹر ها کنترلی
PORTB

$\left\{ \begin{array}{l} \text{DDRC} \\ \text{PORTC} \\ \text{PINC} \end{array} \right\}$

$\left\{ \begin{array}{l} \text{DDR}_D \\ \text{PORT}_D \\ \text{PIN}_D \end{array} \right\}$

مجموع ریسٹر ها کنترلی
PORTD

14.4.2 PORTB – The Port B Data Register

High یا سول کترین خروجی

Bit	7	6	5	4	3	2	1	0	
0x05 (0x25)	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

14.4.3 DDRB – The Port B Data Direction Register

تعیین ورودی/خروجی

Bit	7	6	5	4	3	2	1	0	
0x04 (0x24)	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

14.4.4 PINB – The Port B Input Pins Address⁽¹⁾

خواندن مقدار پین

Bit	7	6	5	4	3	2	1	0	
0x03 (0x23)	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

PB.0

14.4.3 DDRB – The Port B Data Direction Register

Bit	7	6	5	4	3	2	1	0	
0x04 (0x24)	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

DDRB	The Port B Data Direction Register						
DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1

setBit(DDRB, 0)

14.4.2 PORTB – The Port B Data Register

PB0

Bit	7	6	5	4	3	2	1	0	
0x05 (0x25)	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Table 14-1. Port Pin Configurations

DDxn	PORTxn	PUD (in MCUCR)	I/O	Pull-up	Comment
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

PORTB	The Port B Data Register						
PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1

setBit(PORTB, 0)

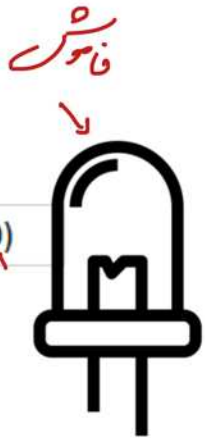


Table 14-1. Port Pin Configurations

DDxn	PORTxn	PUD (in MCUCR)	I/O	Pull-up	Comment
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

PORTB	The Port B Data Register						
PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0

clearBit(PORTB, 0)



setBit(DDRB, 0)

setBit(DDRB, 0)

setBit(PORTB, 0)

changeBit(PORTB, 0, 1)

changeBit(PORTB, PORTB0, 1)

clearBit(PORTB, 0)

changeBit(PORTB, 0, 0)

changeBit(PORTB, PORTB0, 0)

#define Led_ON setBit(PORTB, 0)

active High

#define Led_Off clearBit(PORTB, 0)

#define Led_ON clearBit(PORTB, 0)

→ active High

#define Led_toggle toggleBit(PORTB, 0)

setBit(DDRB, 0)

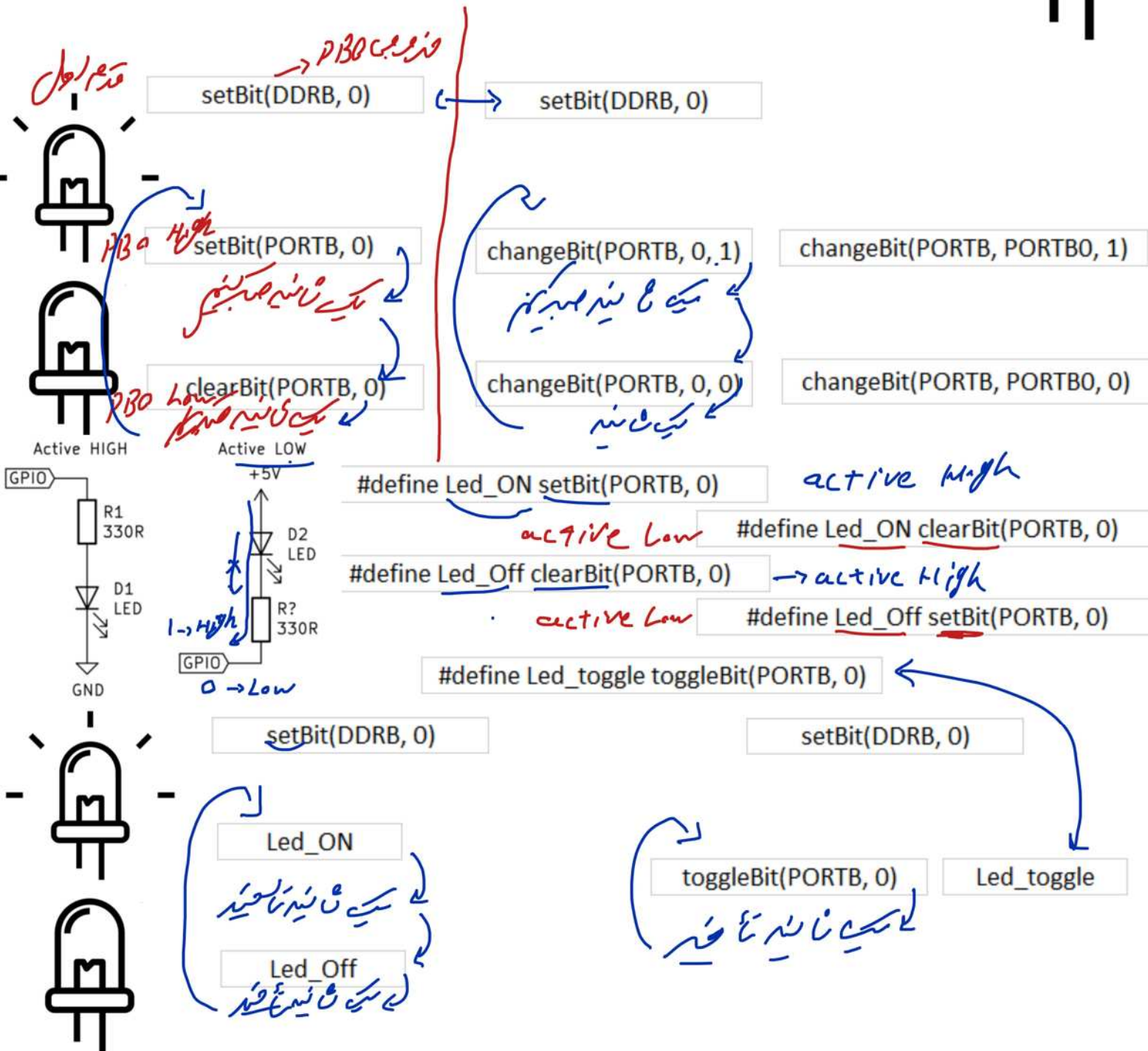
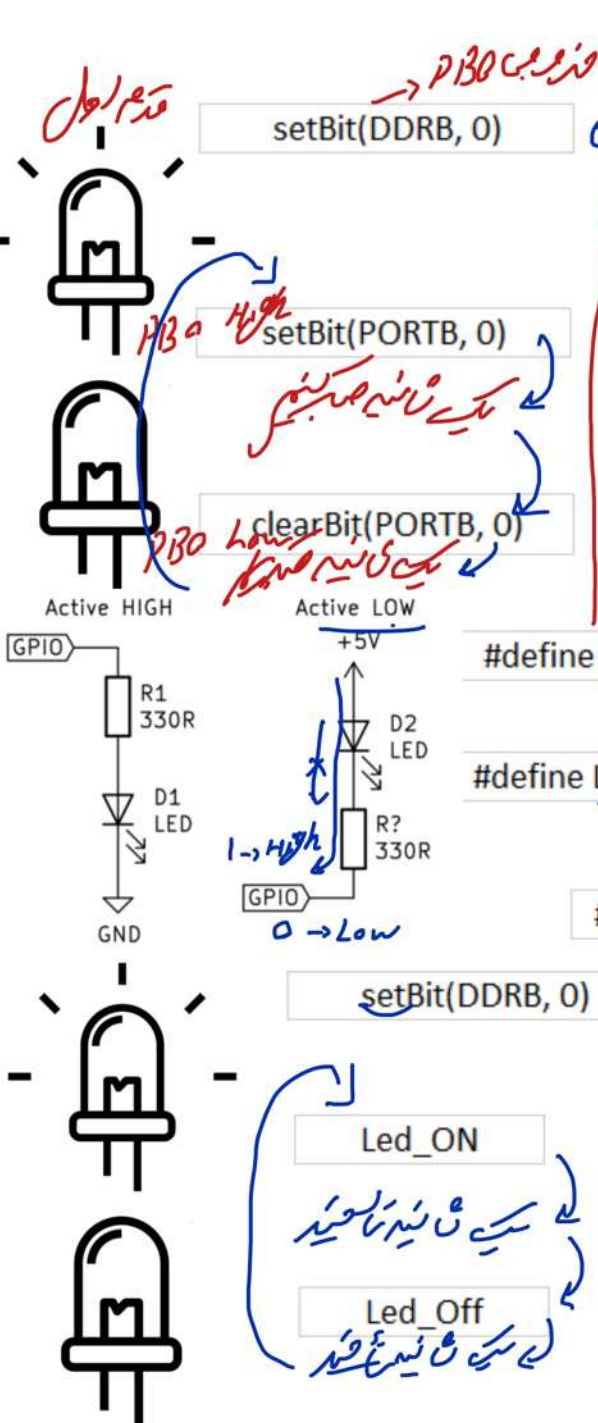
setBit(DDRB, 0)

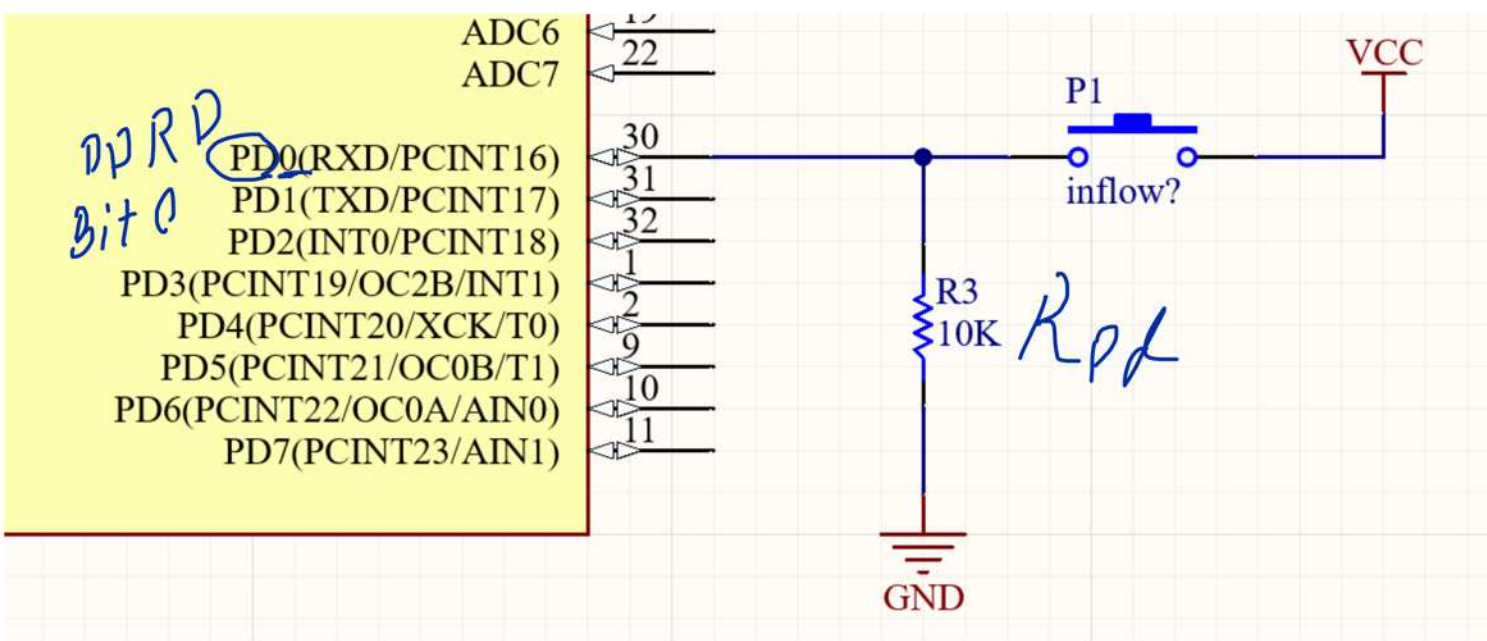
Led_ON

toggleBit(PORTB, 0)

Led_toggle

Led_Off





14.4.9 DDRD – The Port D Data Direction Register

Bit	7	6	5	4	3	2	1	0	
0x0A (0x2A)	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

DDRD	The Port D Data Direction Register						
DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0

clearBit(DDRD, 0)

Handwritten arrows pointing to Bit0 and Bit7, and the text 'PDD'.

14.4.10 PIND – The Port D Input Pins Address⁽¹⁾

Bit	7	6	5	4	3	2	1	0	
0x09 (0x29)	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

Note: 1. Writing to the pin register provides toggle functionality for IO (see "Toggling the Pin" on page 85)

PIND	The Port D Input Pins Address						
PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	0

checkBit(PIND, 0)

Handwritten checkmark and arrow pointing to Bit0.

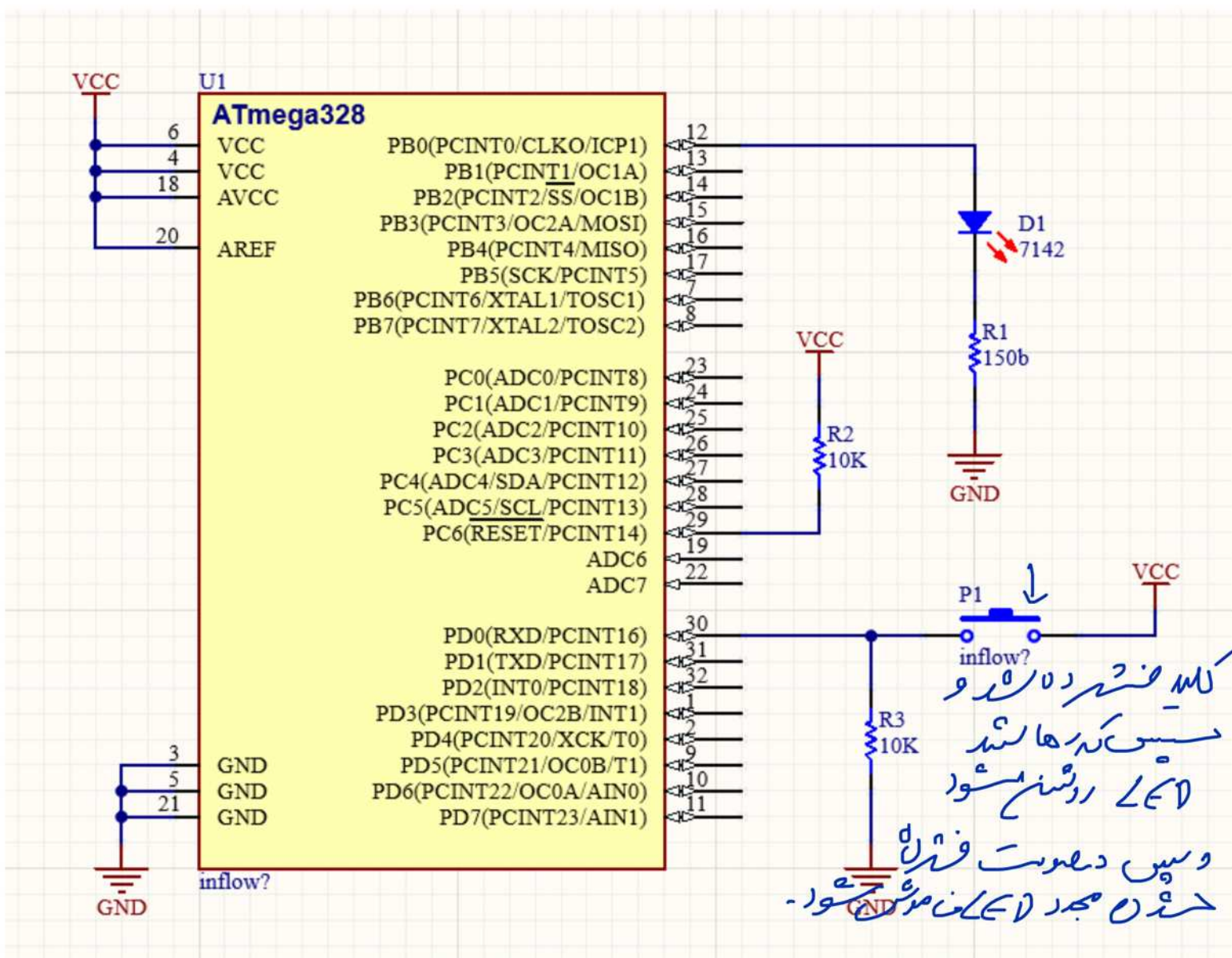


Table 14-1. Port Pin Configurations

DDxn	PORTxn	PUD (in MCUCR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low.
0	1	1	Input	No	Tri-state (Hi-Z)

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