Design Rules Verification Report

Filename : E:\aKaReZa\#gitHub\RCS_AVR\AVR RCS\PCB.PcbDoc

Warnings 0
Rule Violations 0
Waived Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Clearance Constraint (Gap=0.25mm) (All),(InPolygon)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=10mm) (Preferred=0.3mm) (All)	0
Routing Layers(All)	0
Routing Via (MinHoleWidth=0.4mm) (MaxHoleWidth=3mm) (PreferredHoleWidth=0.4mm) (MinWidth=0.7mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Acute Angle Constraint [Tracks Only] (Minimum=60.000) (All)	0
Hole Size Constraint (Min=0.4mm) (Max=10mm) (All)	0
Hole To Hole Clearance (Gap=0.3mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.01mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.01mm) (IsPad),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	0

Waived Violations	
Board Clearance Constraint (Gap=0mm) (All)	1
Total	1

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.029mm < 0.2mm) Between Board Edge And Pad MP1-1(11.049mm,148.844mm) on Multi-Layer Waived by

Micro-Segment: Board region P1(11.242mm,152.814mm) P2(11.242mm,152.814mm)

Reference point outside the component area: Small Component J1-Female (20.574mm,21.844mm) on Top Layer

Reference point outside the component area: Small Component F5-5A (59.69mm,50.8mm) on Top Layer