Design Rules Verification Report

Filename: E:\aKaReZa\#gitHub\eBoard_STM32F103C8\STM32F103C8\PCB.PcbDoc

Warnings 0 Rule Violations 0 Waived Violations 6

Warnings Total 0

Rule Violations Clearance Constraint (Gap=0.2mm) (All), (All) Clearance Constraint (Gap=0.25mm) (All), (InPolygon) Short-Circuit Constraint (Allowed=No) (All), (All) Un-Routed Net Constraint ((All)) Modified Polygon (Allow modified: No), (Allow shelved: No) Width Constraint (Min=0.2mm) (Max=10mm) (Preferred=0.2mm) (All) Routing Layers(All) Routing Via (MinHoleWidth=0.4mm) (MaxHoleWidth=3mm) (PreferredHoleWidth=0.4mm) (MinWidth=0.7mm)
Clearance Constraint (Gap=0.25mm) (All), (InPolygon) Short-Circuit Constraint (Allowed=No) (All), (All) Un-Routed Net Constraint ((All)) Modified Polygon (Allow modified: No), (Allow shelved: No) Width Constraint (Min=0.2mm) (Max=10mm) (Preferred=0.2mm) (All) Routing Layers(All)
Short-Circuit Constraint (Allowed=No) (All), (All) Un-Routed Net Constraint ((All)) Modified Polygon (Allow modified: No), (Allow shelved: No) Width Constraint (Min=0.2mm) (Max=10mm) (Preferred=0.2mm) (All) Routing Layers(All)
Un-Routed Net Constraint ((All)) Modified Polygon (Allow modified: No), (Allow shelved: No) Width Constraint (Min=0.2mm) (Max=10mm) (Preferred=0.2mm) (All) Routing Layers(All)
Modified Polygon (Allow modified: No), (Allow shelved: No) Width C onstraint (Min=0.2mm) (Max=10mm) (Preferred=0.2mm) (All) Routing Layers(All)
Width Constraint (Min=0.2mm) (Max=10mm) (Preferred=0.2mm) (All) Routing Layers(All)
Routing Layers(All)
0 3
Routing Via (MinHoleWidth=0.4mm) (MaxHoleWidth=3mm) (PreferredHoleWidth=0.4mm) (MinWidth=0.7mm)
1 3
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm)
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)
Minimum Annular Ring (Minimum=0.15mm) (All)
Acute Angle Constraint [Tracks Only] (Minimum=60.000) (All)
Hole Size Constraint (Min=0.4mm) (Max=10mm) (All)
Hole To Hole Clearance (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver (Gap=0.01mm) (All),(All)
Silk To Solder Mask (Clearance=0.01mm) (IsPad),(All)
Net Antennae (Tolerance=0mm) (All)
Board Clearance Constraint (Gap=0mm) (All)
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)
Total

Waived Violations	
Minimum Annular Ring (Minimum=0.15mm) (All)	6
Total	6

Minimum Annular Ring (Minimum=0.15mm) (All)

Minimum Annular Ring: (No Ring) Pad P2-H1(2.667mm,54.737mm) on Multi-Layer (Annular Ring missing on Top Layer)Waived by aKaReZa a Minimum Annular Ring: (No Ring) Pad P2-H2(7.747mm,2.667mm) on Multi-Layer (Annular Ring missing on Top Layer)Waived by aKaReZa a Minimum Annular Ring: (No Ring) Pad P2-H3(35.687mm,2.667mm) on Multi-Layer (Annular Ring missing on Top Layer)Waived by aKaReZa a Minimum Annular Ring: (No Ring) Pad P2-H4(50.927mm,53.467mm) on Multi-Layer (Annular Ring missing on Top Layer)Waived by aKaReZa a Minimum Annular Ring: (No Ring) Via (41.675mm,3.674mm) from Top Layer to Bottom Layer (Annular Ring missing on Top Layer)Waived by its ok a Minimum Annular Ring: (No Ring) Via (45.675mm,3.674mm) from Top Layer to Bottom Layer (Annular Ring missing on Top Layer)Waived by its ok a

Reference point outside the component area: Small Component J2-Female (14.224mm,72.771mm) on Top Layer

Micro-Segment: Region (0 hole(s)) Top Layer P1(16.51mm,51.689mm) P2(16.51mm,51.689mm)

Micro-Segment: Region (0 hole(s)) Top Layer P1(16.51mm,49.403mm) P2(16.51mm,49.403mm)

Self-intersection: Region (0 hole(s)) Top Layer (9.273mm,29.045mm)